PART -1 : NGSPICE (PRE-LAYOUT)

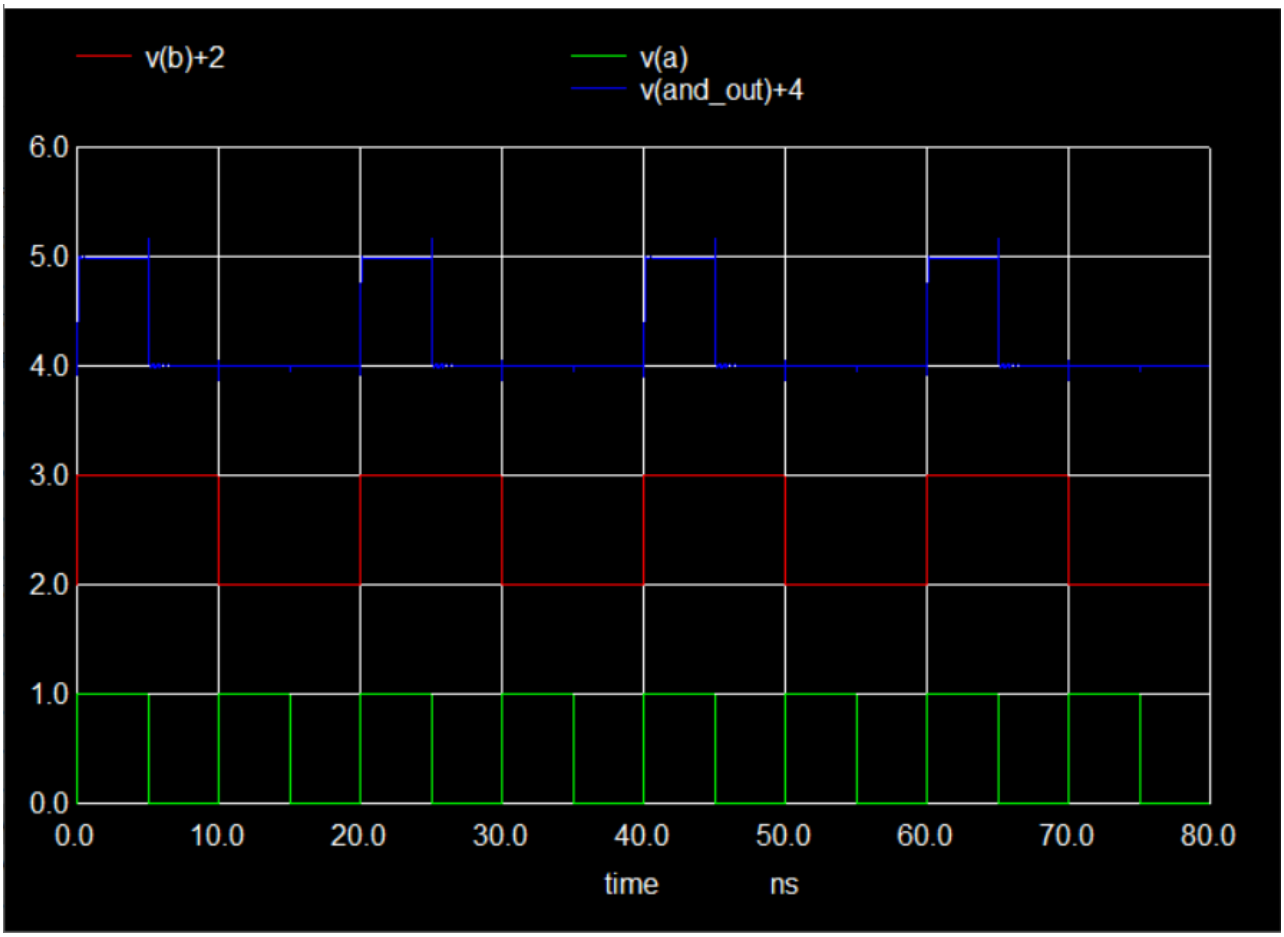
1.1 Subcircuits.

Given are the spice netlists written for the subcircuits used to build the multiplier.

a) AND GATE :

```
.SUBCKT AND out a b vdd gnd

MN1 node1 a node2 node2 nmos W={2*lamda}  L=lamda
MN2 node2 b gnd gnd nmos W={2*lamda}  L=lamda
MP1 node1 a vdd vdd pmos W={2*lamda}  L=lamda
MP2 node1 b vdd vdd pmos W={2*lamda}  L=lamda

MN3 out node1 gnd gnd nmos W={2*lamda}  L=lamda
MP3 out node1 vdd vdd pmos W={2*lamda}  L=lamda

.ENDS AND
```

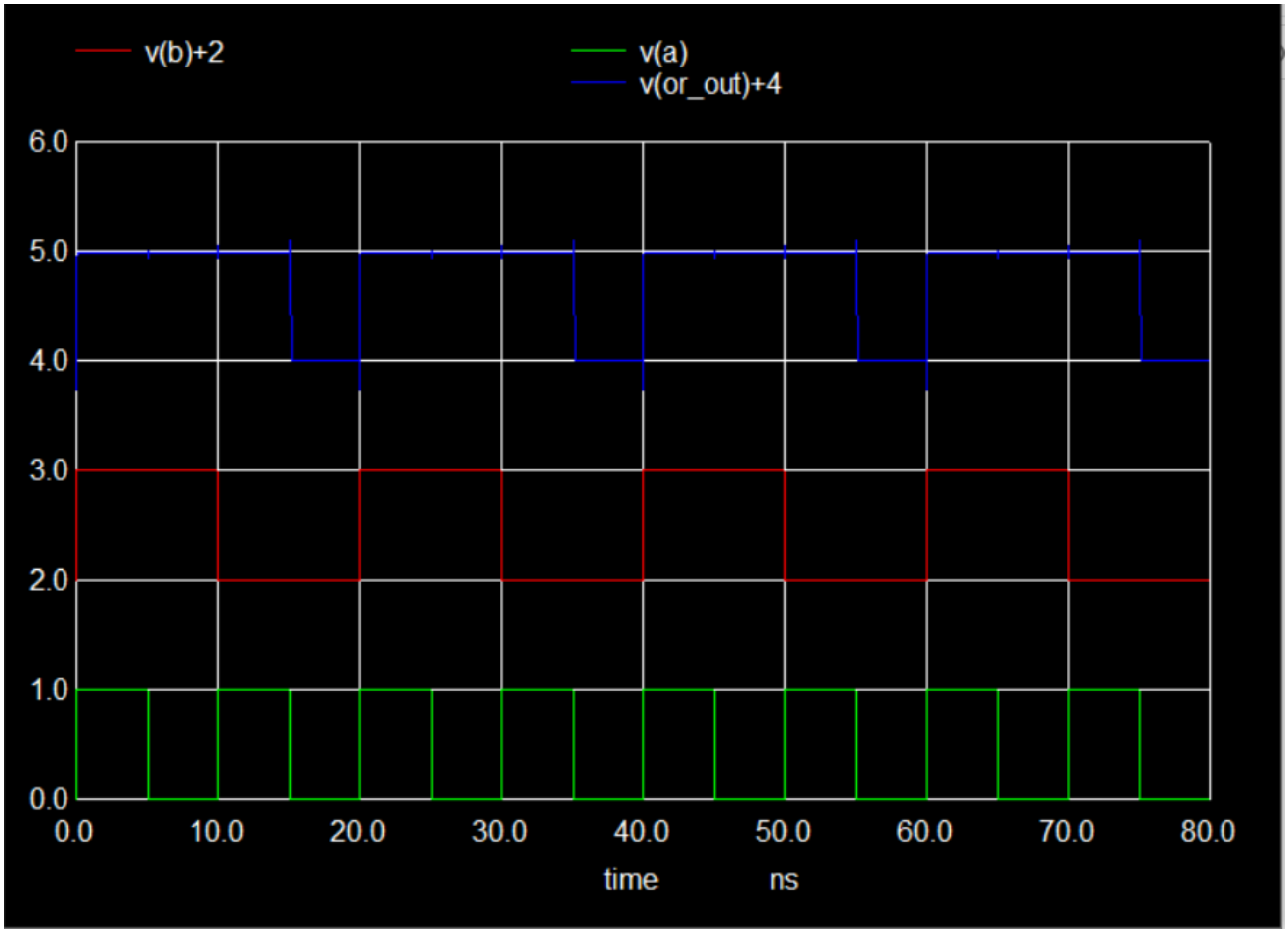
The simulation is as given :



b) OR GATE :

```
.SUBCKT OR out a b vdd gnd


MN1 node1 a gnd gnd nmos W={2*lamda}  L=lamda
MN2 node1 b gnd gnd nmos W={2*lamda}  L=lamda
MP1 node1 a node2 node2 pmos W={2*lamda}  L=lamda
MP2 node2 b vdd vdd pmos W={2*lamda}  L=lamda


MN3 out node1 gnd gnd nmos W={2*lamda}  L=lamda
MP3 out node1 vdd vdd pmos W={2*lamda}  L=lamda

.ends OR
```

The simulation is as given :



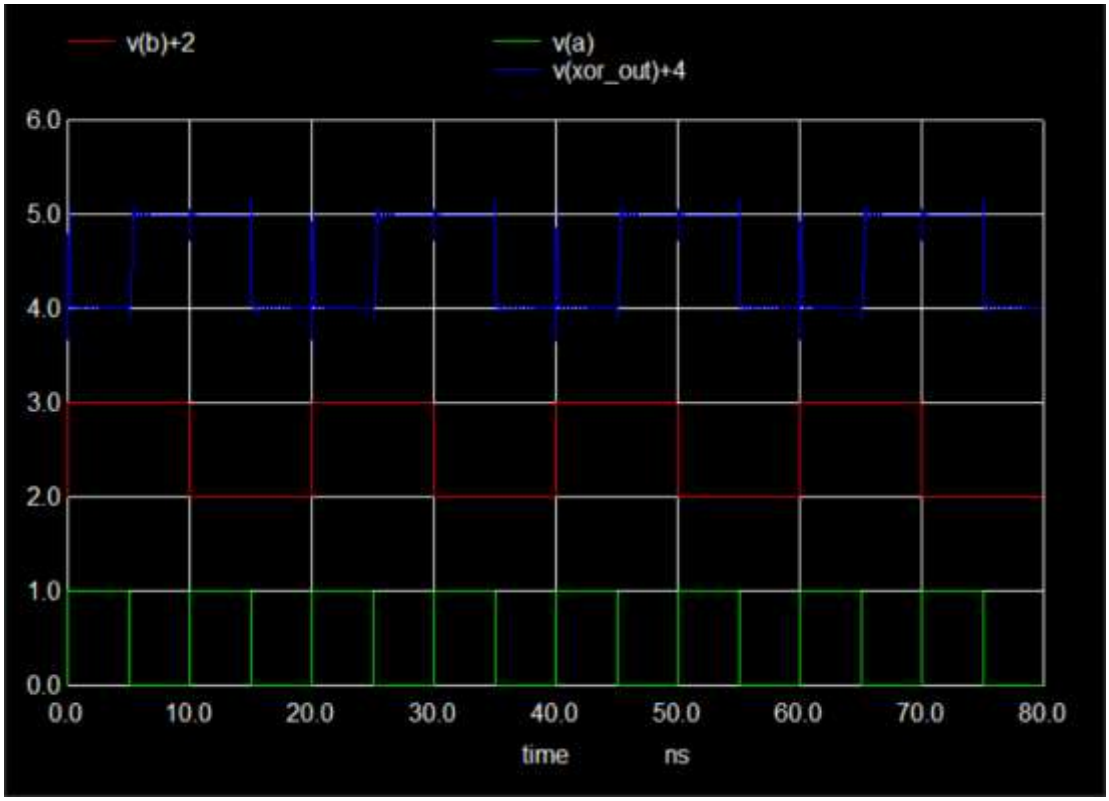
c) NAND GATE :

```
.SUBCKT NAND out a b vdd gnd

MN1 out a node2 node2 nmos W={2*lamda}  L=lamda
MN2 node2 b gnd gnd nmos W={2*lamda}  L=lamda
MP1 out a vdd vdd pmos W={2*lamda}  L=lamda
MP2 out b vdd vdd pmos W={2*lamda}  L=lamda

.ends NAND
```

d) XOR GATE :

```
.SUBCKT XOR out a b vdd gnd

.INCLUDE NAND.sub

x1 node1 a b vdd gnd NAND
x2 node2 a node1 vdd gnd NAND
x3 node3 b node1 vdd gnd NAND
x4 out node2 node3 vdd gnd NAND

.ends XOR
```

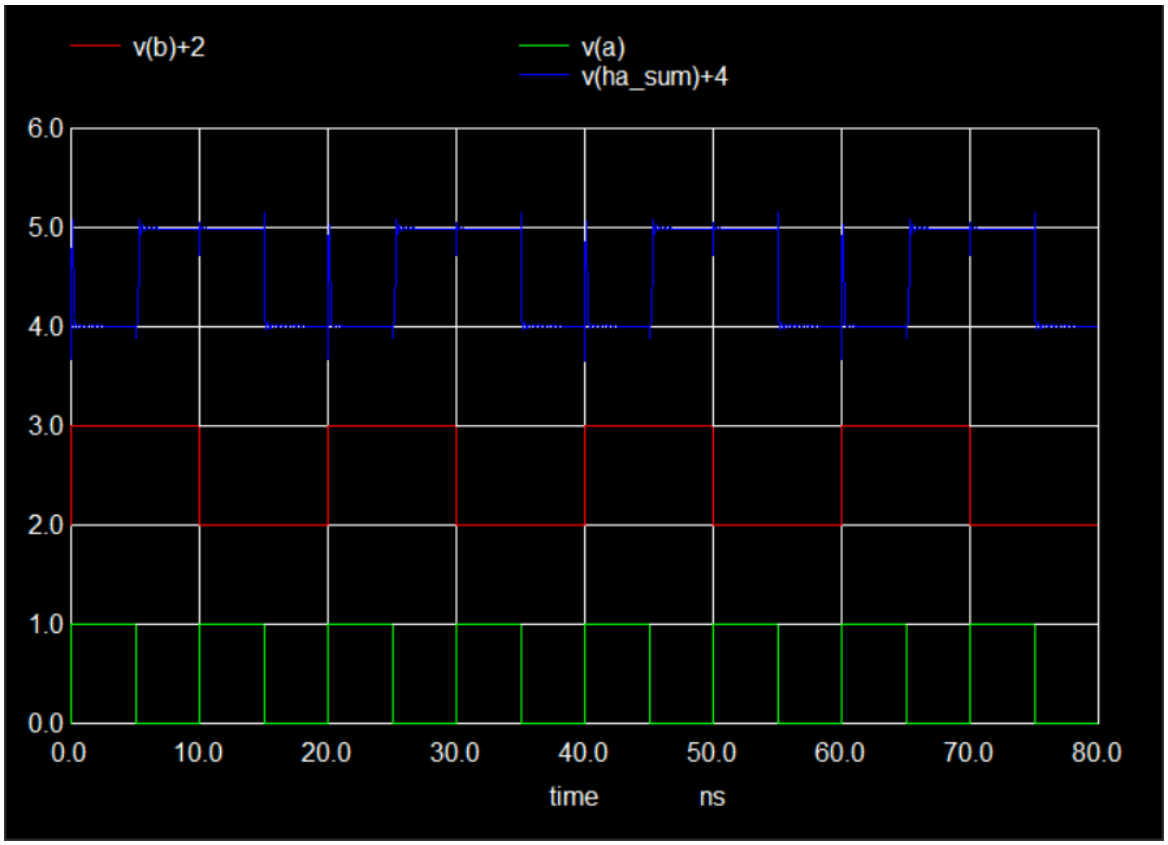
The simulation is as given :

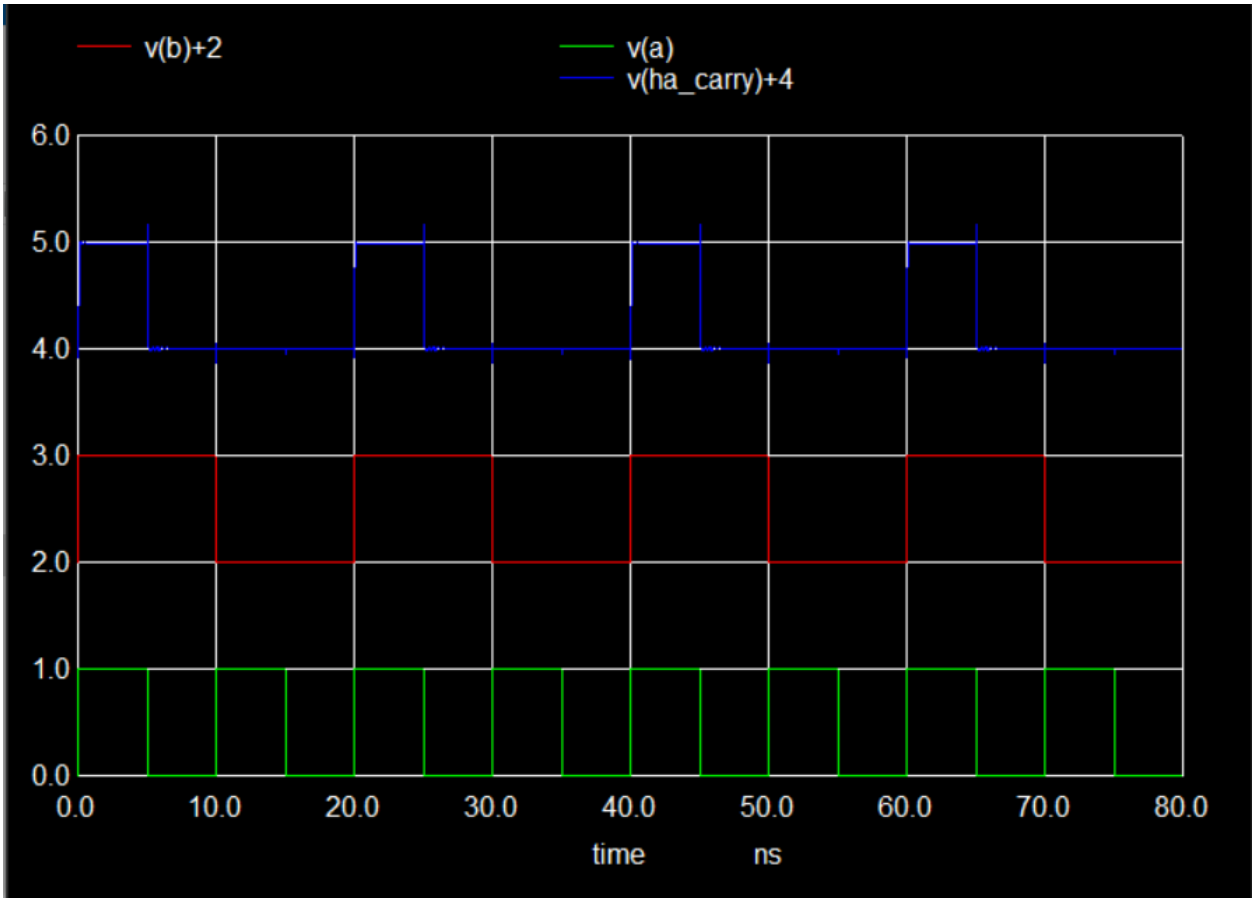


e) HALF ADDER :

```
.subckt HA a b sum carry vdd gnd

.INCLUDE AND.subs
.INCLUDE XOR.sp

x1 sum a b vdd gnd XOR
x2 carry a b vdd gnd AND


.ends HA
```

The simulation is as given :

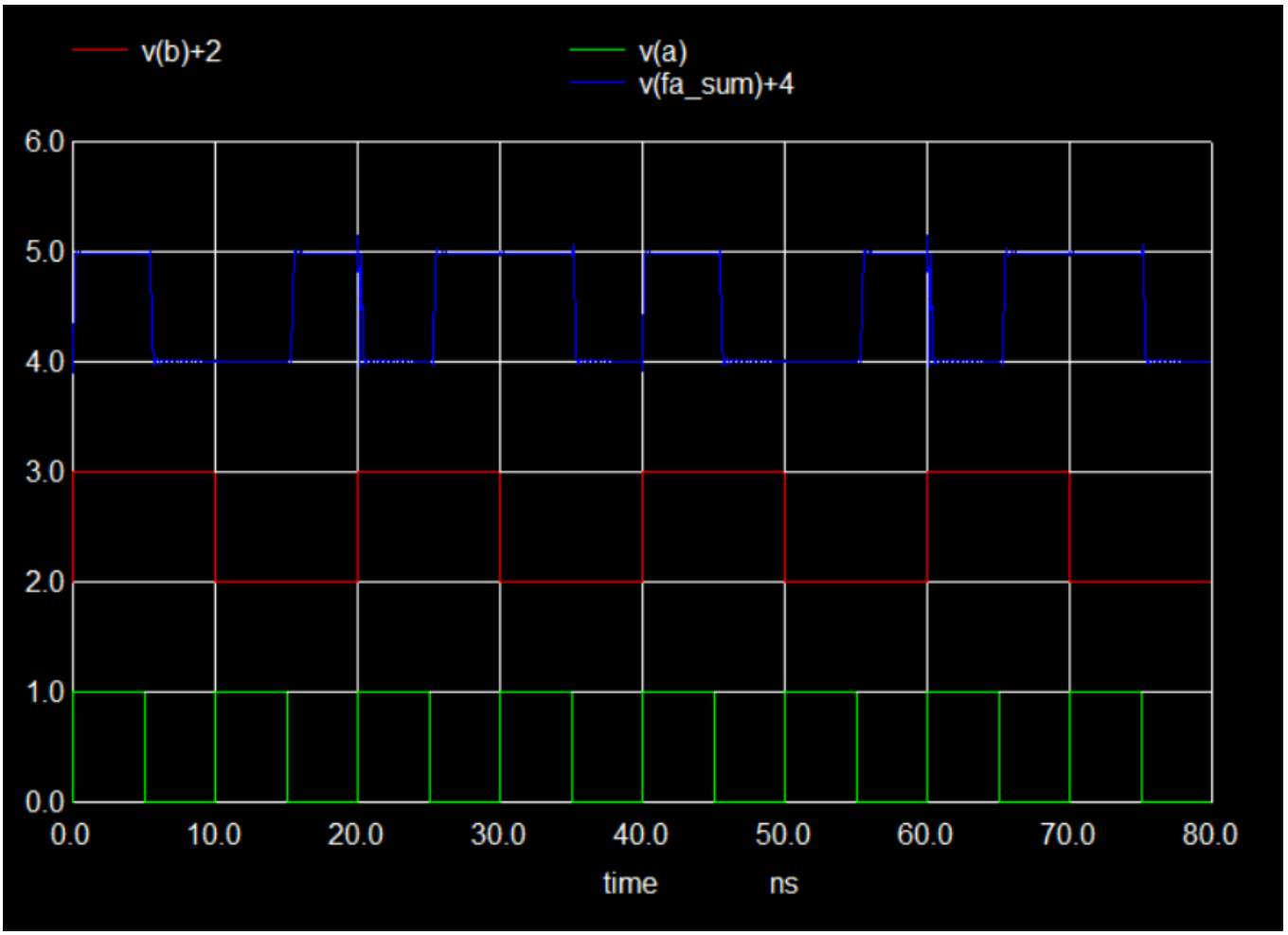


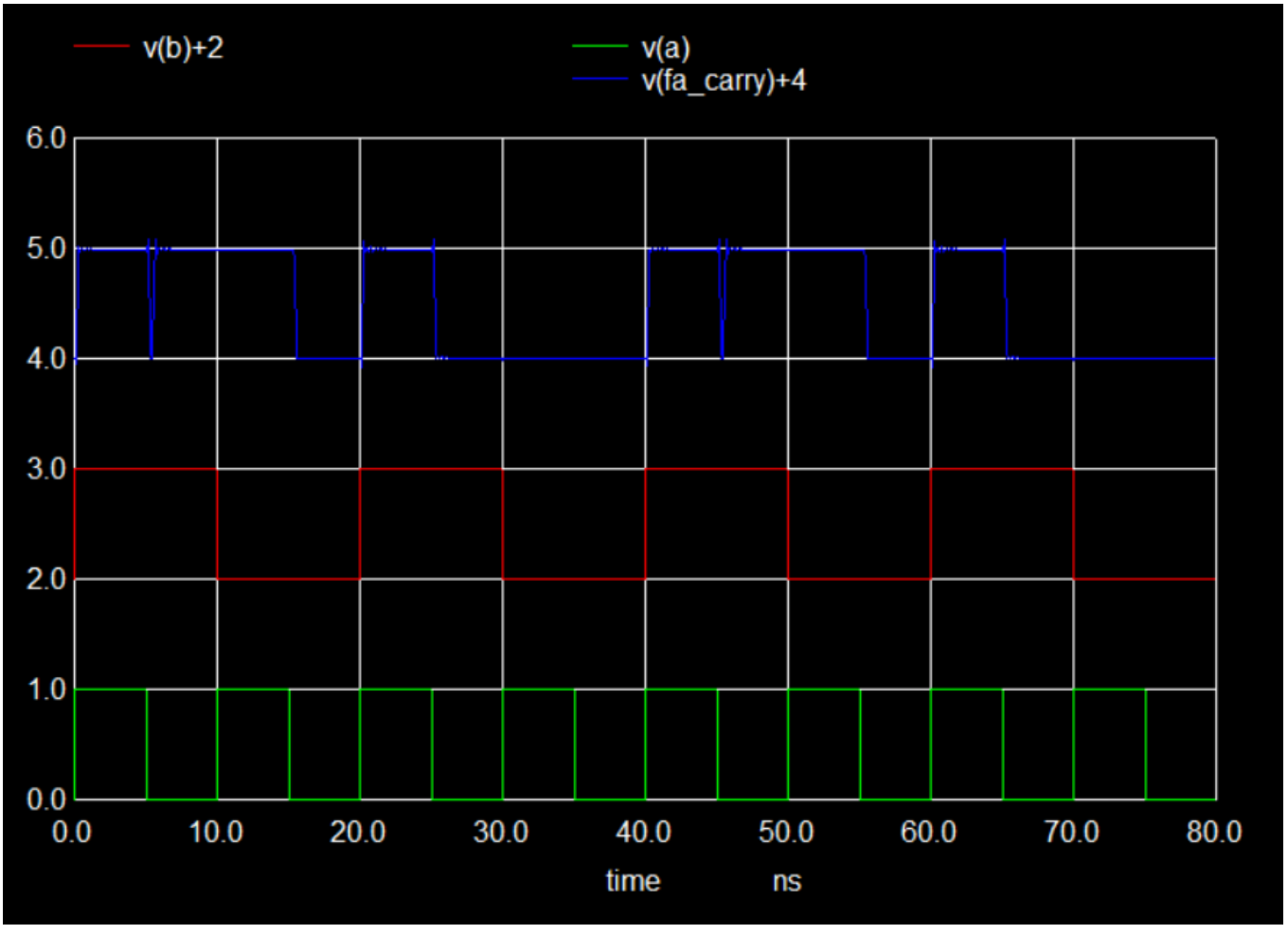


f) FULL ADDER :

```
.subckt FA a b c sum carry vdd gnd

.INCLUDE HA.sub
.INCLUDE OR.spice

x1 a b sum1 carry1 vdd gnd HA
x2 sum1 c sum carry2 vdd gnd HA
x3 carry carry1 carry2 vdd gnd OR

.ends FA
```

The simulation is as given :

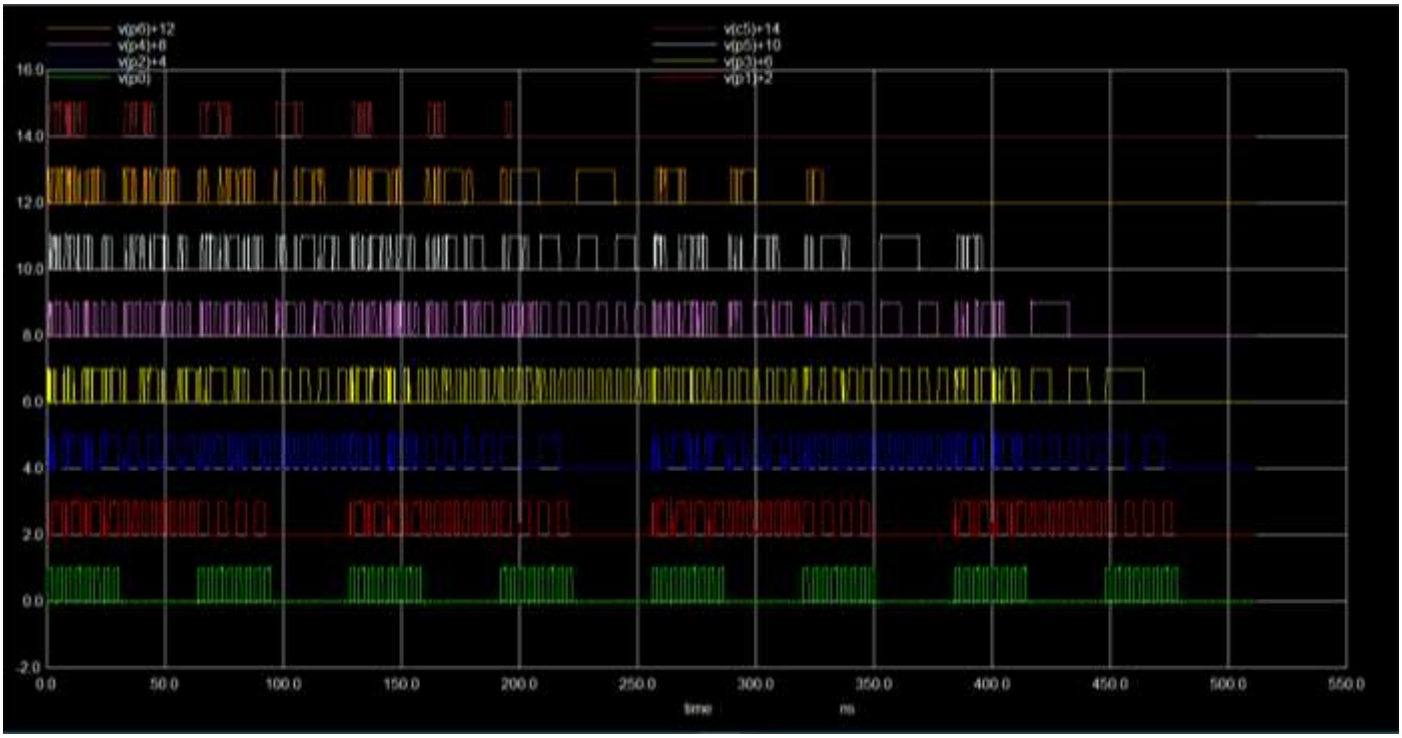




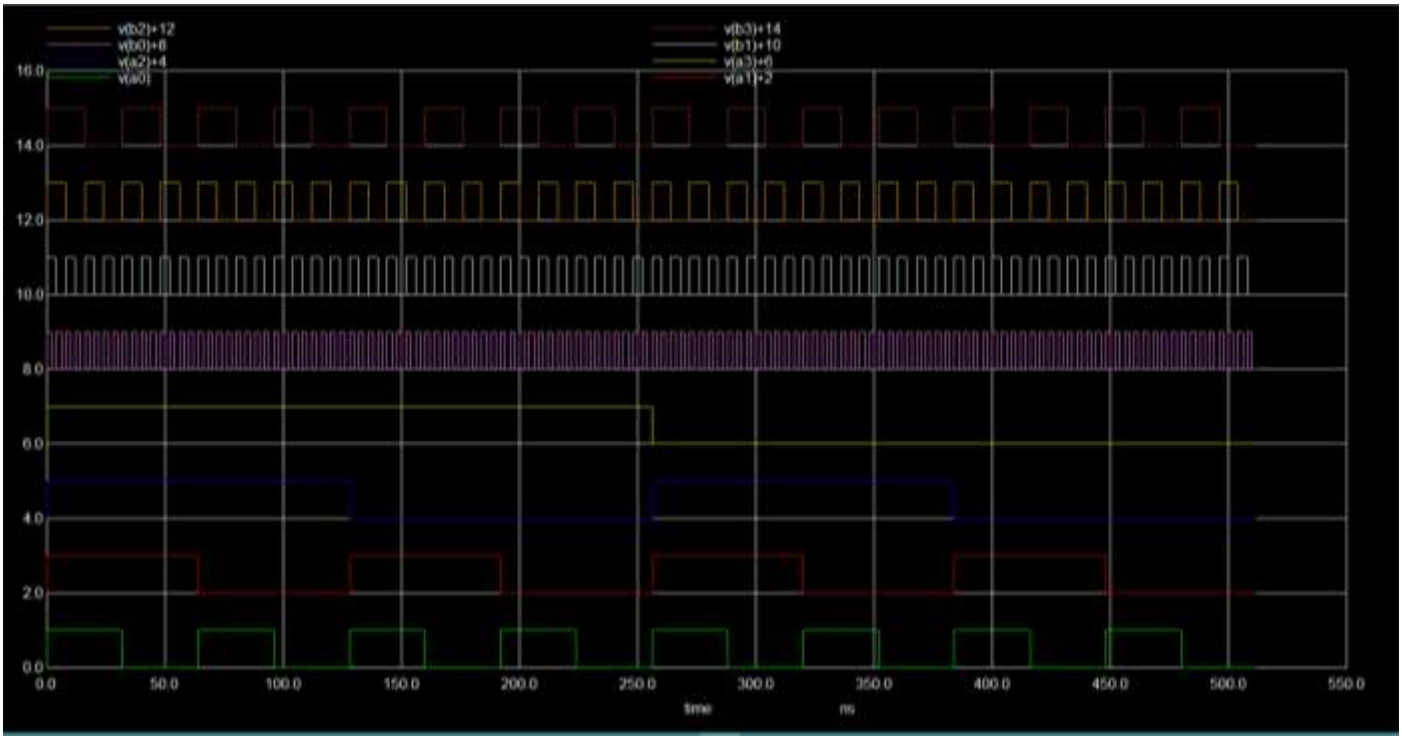
1.2 : 4 x 4MULTIPLIER NETLIST

```
.subckt multiplier p0 p1 p2 p3 p4 p5 p6 c5 a0 a1 a2 a3 b0 b1 b2 b3 vdd gnd

.INCLUDE HA.sub
.INCLUDE FA.sub
.INCLUDE AND.subs

x0 p0 a0 b0 vdd gnd AND
x1 x1 a0 b1 vdd gnd AND
x2 x2 a1 b0 vdd gnd AND
x3 x3 a0 b2 vdd gnd AND
x4 x4 a2 b0 vdd gnd AND
x5 x5 a1 b1 vdd gnd AND
x6 x6 a1 b2 vdd gnd AND
x7 x7 a0 b3 vdd gnd AND
x8 x8 b0 a3 vdd gnd AND
x9 x9 b1 a2 vdd gnd AND
x10 x10 a2 b2 vdd gnd AND
x11 x11 b1 a3 vdd gnd AND
x12 x12 b3 a1 vdd gnd AND
x13 x13 b3 a2 vdd gnd AND
x14 x14 b2 a3 vdd gnd AND
x15 x15 b3 a3 vdd gnd AND

// adders

xha1 x1 x2 p1 y1 vdd gnd HA
xha2 x4 x5 y2 y3 vdd gnd HA
xha3 x8 x9 y4 y5 vdd gnd HA
xfa1 x3 y1 y2 p2 z1 vdd gnd FA
xfa2 y3 y4 x6 z2 z3 vdd gnd FA
xfa3 y5 x10 x11 z4 z5 vdd gnd FA
xfa4 x13 x14 z5 z6 z7 vdd gnd FA
xfa5 z1 z2 x7 p3 v1 vdd gnd FA
xfa6 z3 z4 x12 v2 v3 vdd gnd FA
xha4 v1 v2 p4 v5 vdd gnd HA
xfa7 z6 v3 v5 p5 v4 vdd gnd FA
xfa8 v4 z7 x15 p6 c5 vdd gnd FA


.ends multiplier
```

Simulating with all 256 possible inputs :



Inputs given :



1.3 : Calculating delays.

We calculate for 64 delays between the 8 inputs (a0,a1,…,b3) and 8 outputs (p0,p1 …,c5).

These are outputted to a file and the file with the calculated delays is attached.

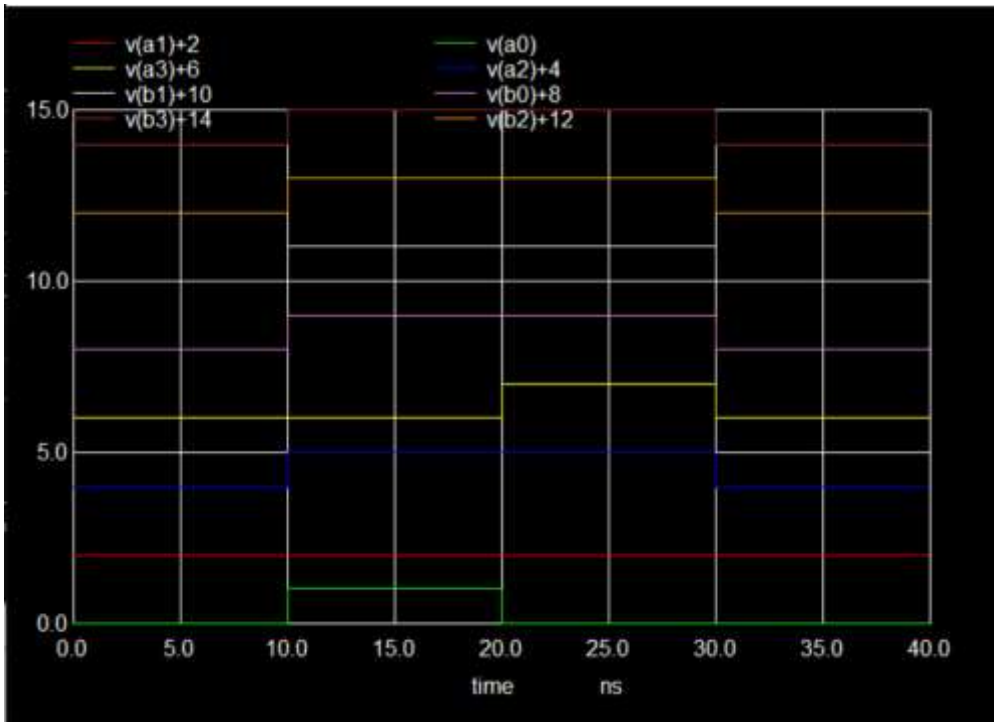
project - Notepad

File Edit Format View Help

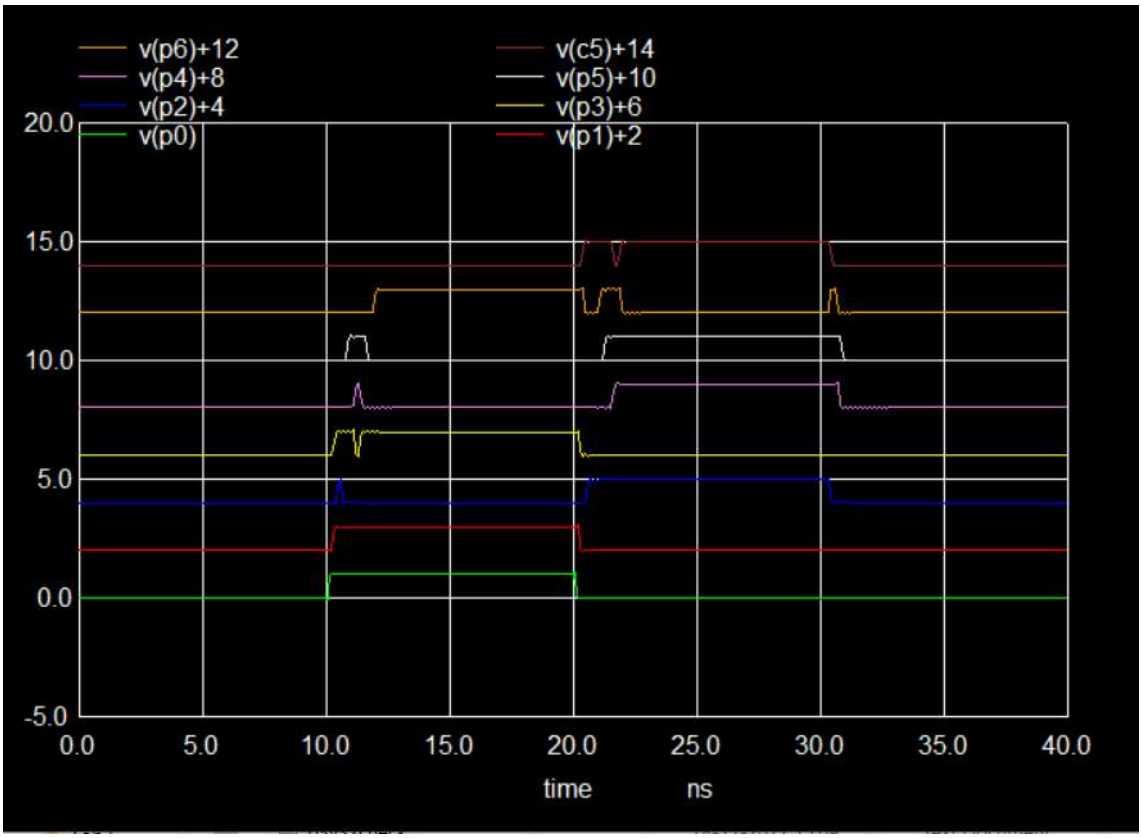
```
Delays with inputs and all outputs :
delay with p0 = 7.59974E-11
delay with p1 = 2.34295E-10
delay with p = 4.42208E-10
delay with p3 = 7.81061E-10
delay with p4 = 1.17089E-09
delay with p5 = 1.03624E-09
delay with p6 = 1.18272E-09
delay with c5 = 1.1311E-09
```

This amounts to 64 delays as the way that our inputs are given means that all inputs have the same delay with the outputs.

Our inputs given to test delays :



Output :



We can see that the worst-case delay is between input and output bit **p6.**

Delay = 1.183 x 10^{-9} .

1.4 : Calculating leakage power.

We use a python script to facilitate 256 input combinations.

PYTHON SCRIPT :

```
import os
# make sure value of starting in sp file is 0.
st = "Vina0 a0 0 0\nVina1 a1 0 0\nVina2 a2 0 0\nVina3 a3 0 0\nVinb0 b0 0 0\nVinb1 b1 0 0\nVinb2 b2 0 0\nVinb3 b3 0 0"

for i in range(255):

    number = format(i, '08b')
    # print(number)
    num = list(number)
    print(num)
    rt = f"Vina0 a0 0 {num[0]}\nVina1 a1 0 {num[1]}\nVina2 a2 0 {num[2]}\nVina3 a3 0 {num[3]}\nVinb0 b0 0 {num[4]}\nVinb1 b1 0 {num[5]}\nVinb2 b2 0 {num[6]}\nVinb3 b3 0 {num[7]}"  #go to sp file and reset value to 0

    with open("project.sp","r") as fp:
        data = fp.read()
        data = data.replace(st,rt)

    with open("project.sp", "w") as fp:
        fp.write(data)

    st = rt
    os.system("ngspice_con project.sp")
```

The output power values are outputted to a file which is attached.

Average Leakage Power = 1.1369 x 10^{-5} W.

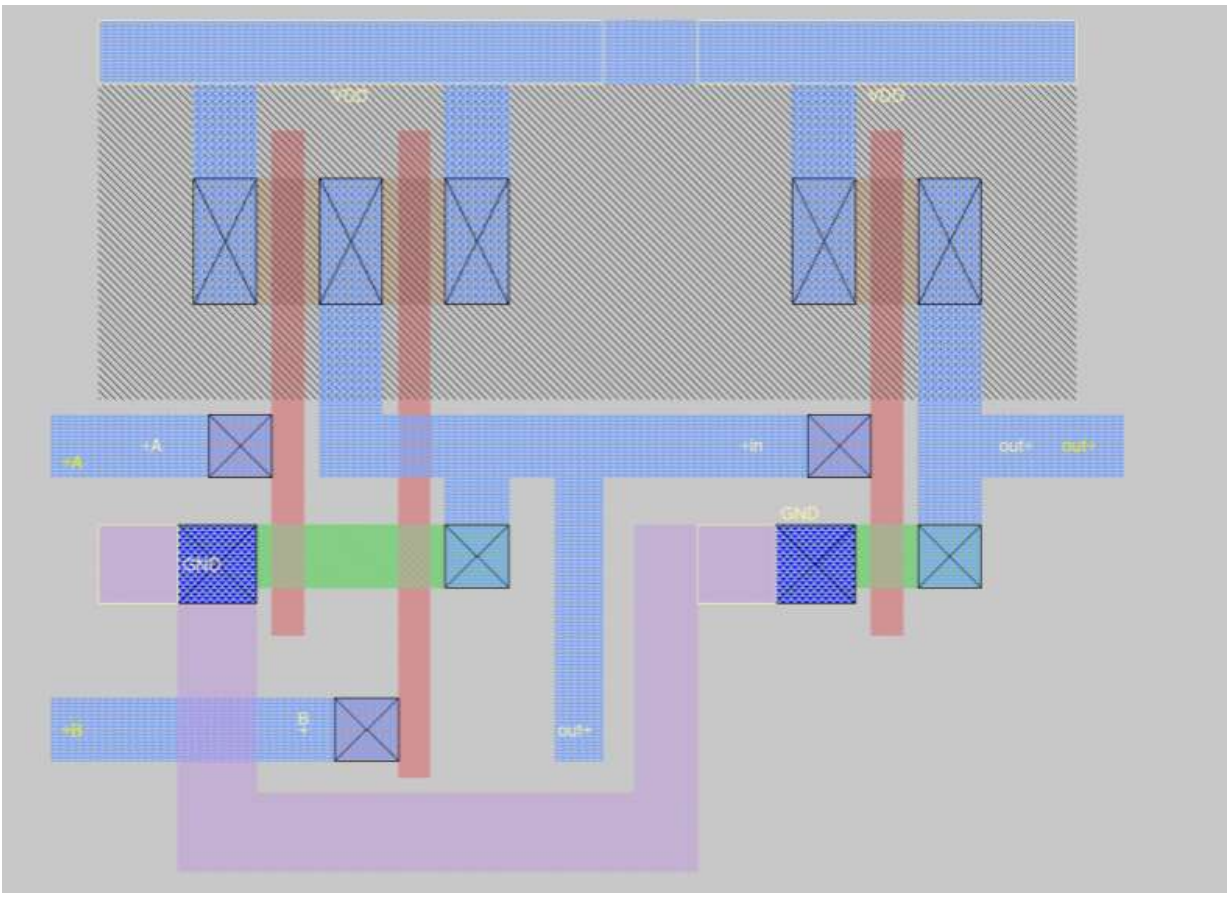
PART -2 : MAGIC (POST-LAYOUT)

1.1 : Subcircuits.

The following are the magic layouts of the gates and subcircuits used.

1.1.1 AND GATE

Magic Layout

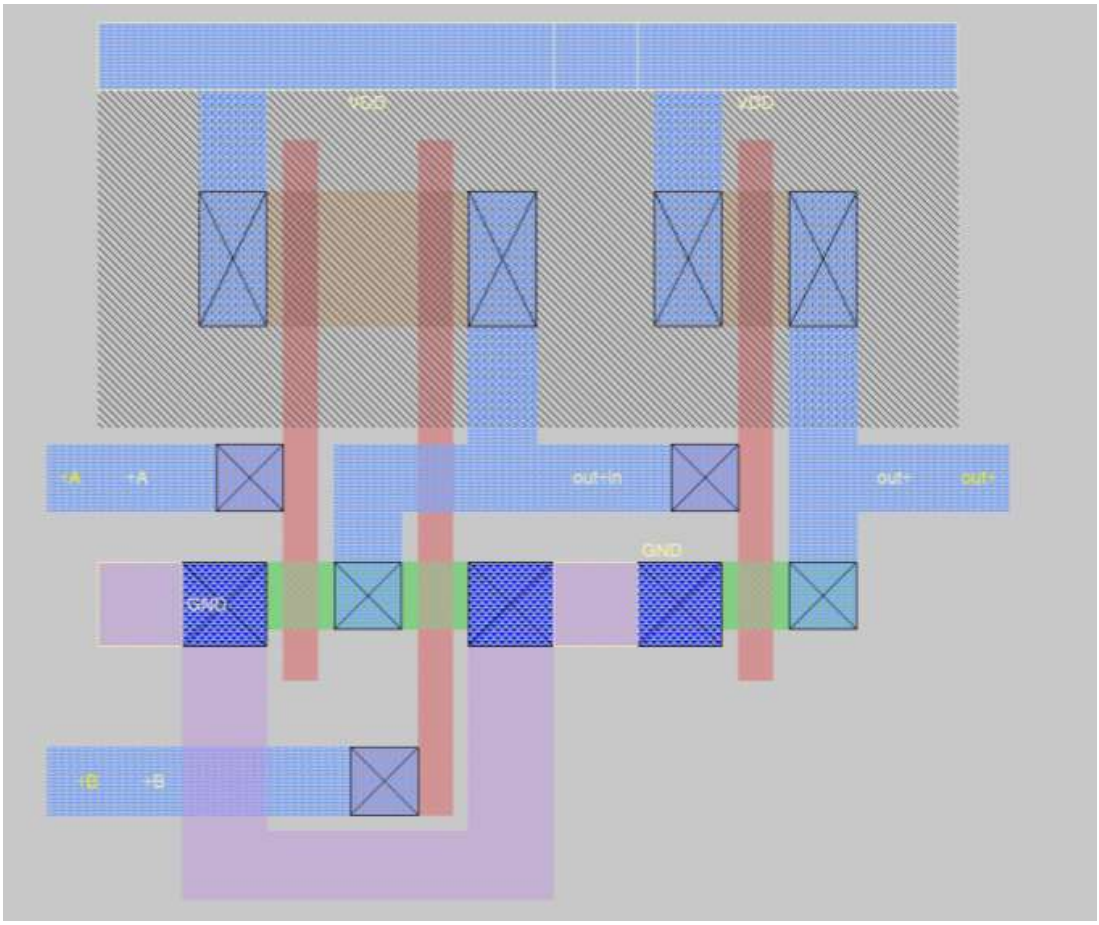


Netlist extracted :

```
* SPICE3 file created from and_magic.ext - technology: scmos

.option scale=0.09u

M1000 out NAND_magic_0/out VDD w_32_19# pfet w=8 l=2
+  ad=40 pd=26 as=120 ps=78
M1001 out NAND_magic_0/out GND Gnd nfet w=4 l=2
+  ad=20 pd=18 as=58 ps=44
M1002 VDD B NAND_magic_0/out w_32_19# pfet w=8 l=2
+  ad=0 pd=0 as=48 ps=28
M1003 NAND_magic_0/out A VDD w_32_19# pfet w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1004 NAND_magic_0/out B NAND_magic_0/a_13_n12# Gnd nfet w=4 l=2
+  ad=20 pd=18 as=24 ps=20
M1005 NAND_magic_0/a_13_n12# A GND Gnd nfet w=4 l=2
+  ad=0 pd=0 as=0 ps=0
C0 B A 0.08fF
C1 w_32_19# out 0.03fF
C2 NAND_magic_0/out out 0.05fF
C3 B GND 0.13fF
C4 out VDD 0.11fF
C5 w_32_19# NAND_magic_0/out 0.09fF
C6 A GND 0.07fF
C7 w_32_19# VDD 0.14fF
C8 NAND_magic_0/out VDD 0.24fF
C9 B w_32_19# 0.06fF
C10 B NAND_magic_0/out 0.08fF
C11 out GND 0.04fF
C12 w_32_19# A 0.06fF
C13 NAND_magic_0/out A 0.05fF
C14 NAND_magic_0/out GND 0.07fF
C15 A VDD 0.02fF
C16 GND Gnd 1.01fF
C17 NAND_magic_0/out Gnd 0.28fF
C18 VDD Gnd 0.16fF
C19 B Gnd 0.24fF
C20 A Gnd 0.16fF
C21 w_32_19# Gnd 1.25fF
C22 out Gnd 0.07fF
```

2.1.2 OR GATE

Magic Layout

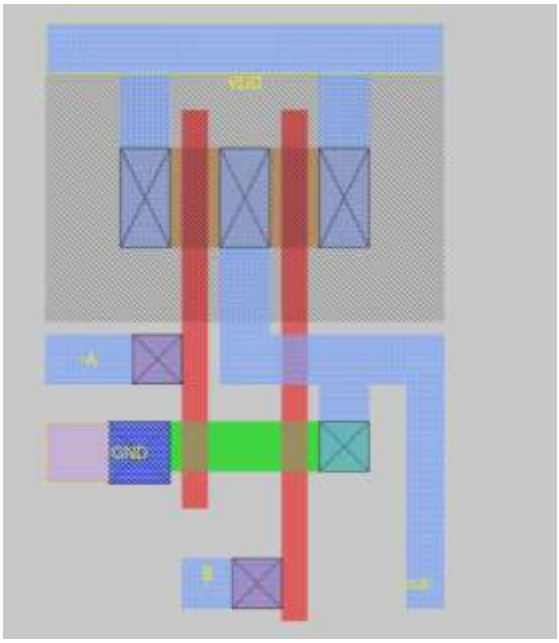


Netlist extracted :

```
* SPICE3 file created from or_magic.ext - technology: scmos

.option scale=0.09u

M1000 out NOR_magic_0/out VDD NOR_magic_0/w_0_0# pfet w=8 l=2
+  ad=40 pd=26 as=80 ps=52
M1001 out NOR_magic_0/out GND Gnd nfet w=4 l=2
+  ad=20 pd=18 as=87 ps=66
M1002 NOR_magic_0/out B NOR_magic_0/a_13_6# NOR_magic_0/w_0_0# pfet w=8 l=2
+  ad=40 pd=26 as=48 ps=28
M1003 NOR_magic_0/a_13_6# A VDD NOR_magic_0/w_0_0# pfet w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1004 GND B NOR_magic_0/out Gnd nfet w=4 l=2
+  ad=0 pd=0 as=24 ps=20
M1005 NOR_magic_0/out A GND Gnd nfet w=4 l=2
+  ad=0 pd=0 as=0 ps=0
C0 NOR_magic_0/out A 0.05fF
C1 GND B 0.13fF
C2 NOR_magic_0/w_0_0# B 0.06fF
C3 VDD NOR_magic_0/out 0.10fF
C4 VDD A 0.02fF
C5 out NOR_magic_0/out 0.05fF
C6 VDD out 0.11fF
C7 GND NOR_magic_0/out 0.22fF
C8 GND A 0.07fF
C9 NOR_magic_0/w_0_0# NOR_magic_0/out 0.10fF
C10 NOR_magic_0/w_0_0# A 0.06fF
C11 VDD NOR_magic_0/w_0_0# 0.11fF
C12 out GND 0.04fF
C13 B NOR_magic_0/out 0.10fF
C14 NOR_magic_0/w_0_0# out 0.03fF
C15 B A 0.08fF
C16 B Gnd 0.23fF
C17 A Gnd 0.16fF
C18 GND Gnd 0.38fF
C19 out Gnd 0.07fF
C20 VDD Gnd 0.14fF
C21 NOR_magic_0/out Gnd 0.20fF
C22 NOR_magic_0/w_0_0# Gnd 1.12fF
```

2.1.3 NAND GATE

Magic Layout :

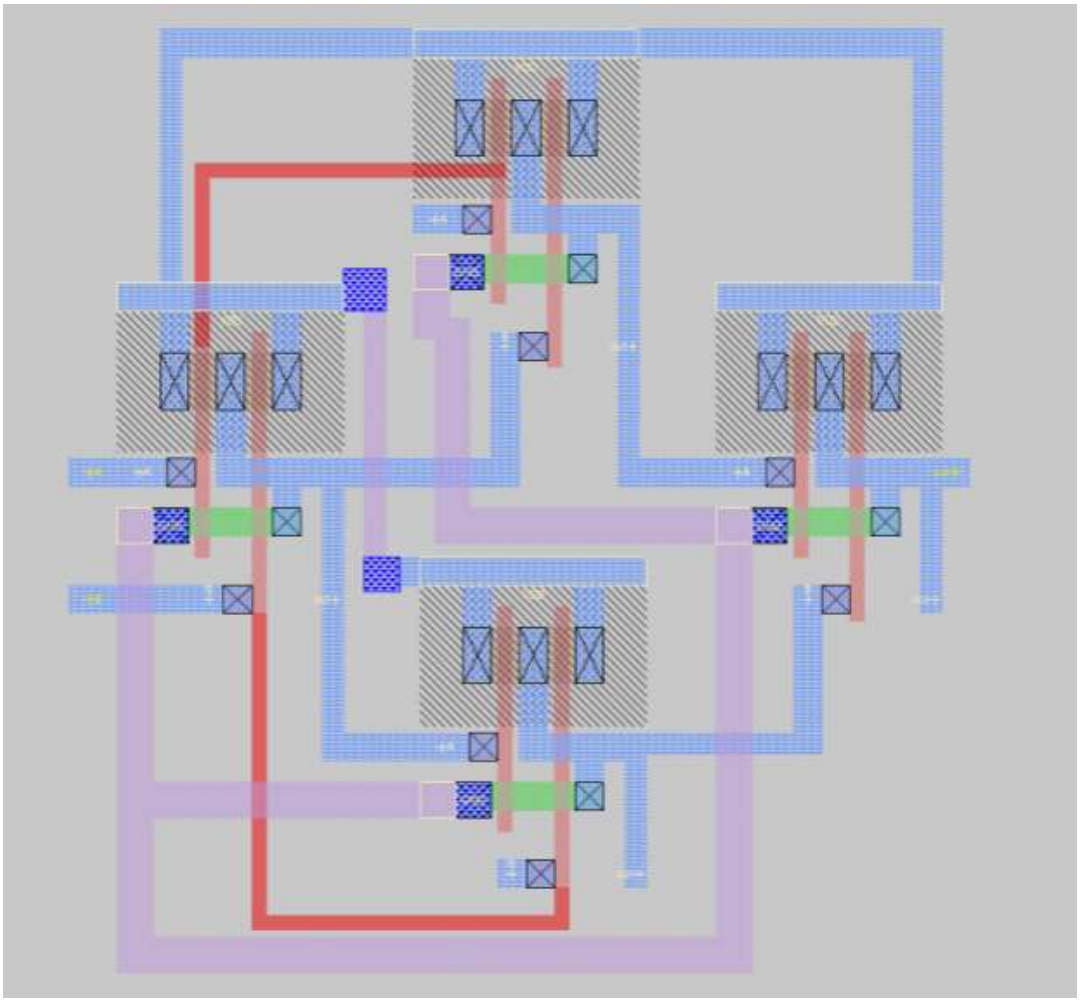


Netlist extracted :

```
* SPICE3 file created from NAND_magic.ext - technology: scmos

.option scale=0.09u

M1000 VDD B out w_0_0# pfet w=8 l=2
+  ad=80 pd=52 as=48 ps=28
M1001 out A VDD w_0_0# pfet w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1002 out B a_13_n12# Gnd nfet w=4 l=2
+  ad=20 pd=18 as=24 ps=20
M1003 a_13_n12# A GND Gnd nfet w=4 l=2
+  ad=0 pd=0 as=29 ps=22
C0 w_0_0# out 0.02fF
C1 B A 0.08fF
C2 A VDD 0.02fF
C3 B out 0.08fF
C4 w_0_0# B 0.06fF
C5 VDD out 0.22fF
C6 w_0_0# VDD 0.09fF
C7 A out 0.05fF
C8 w_0_0# A 0.06fF
C9 A GND 0.07fF
```

2.1.4 XOR GATE

Magic Layout :



Netlist Extracted :

```
* SPICE3 file created from XOR_magic.ext - technology: scmos

.option scale=0.09u

M1000 VDD NAND_magic_3/B out NAND_magic_3/w_0_0# pfet w=8 l=2
+  ad=320 pd=208 as=48 ps=28
M1001 out NAND_magic_3/A VDD NAND_magic_3/w_0_0# pfet w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1002 out NAND_magic_3/B NAND_magic_3/a_13_n12# Gnd nfet w=4 l=2
+  ad=20 pd=18 as=24 ps=20
M1003 NAND_magic_3/a_13_n12# NAND_magic_3/A GND Gnd nfet w=4 l=2
+  ad=0 pd=0 as=116 ps=88
M1004 VDD B NAND_magic_2/A NAND_magic_0/w_0_0# pfet w=8 l=2
+  ad=0 pd=0 as=48 ps=28
M1005 NAND_magic_2/A A VDD NAND_magic_0/w_0_0# pfet w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1006 NAND_magic_2/A B NAND_magic_0/a_13_n12# Gnd nfet w=4 l=2
+  ad=20 pd=18 as=24 ps=20
M1007 NAND_magic_0/a_13_n12# A GND Gnd nfet w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1008 VDD NAND_magic_2/A NAND_magic_3/A NAND_magic_1/w_0_0# pfet w=8 l=2
+  ad=0 pd=0 as=48 ps=28
M1009 NAND_magic_3/A A VDD NAND_magic_1/w_0_0# pfet w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1010 NAND_magic_3/A NAND_magic_2/A NAND_magic_1/a_13_n12# Gnd nfet w=4 l=2
+  ad=20 pd=18 as=24 ps=20
M1011 NAND_magic_1/a_13_n12# A GND Gnd nfet w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1012 VDD B NAND_magic_3/B NAND_magic_2/w_0_0# pfet w=8 l=2
+  ad=0 pd=0 as=48 ps=28
M1013 NAND_magic_3/B NAND_magic_2/A VDD NAND_magic_2/w_0_0# pfet w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1014 NAND_magic_3/B B NAND_magic_2/a_13_n12# Gnd nfet w=4 l=2
+  ad=20 pd=18 as=24 ps=20
```

M1015 NAND_magic_2/a_13_n12# NAND_magic_2/A GND Gnd nfet w=4 l=2

+ ad=0 pd=0 as=0 ps=0

C0 NAND_magic_3/B NAND_magic_2/A 0.05fF

C1 VDD NAND_magic_2/w_0_0# 0.09fF

C2 NAND_magic_3/B out 0.08fF

C3 NAND_magic_3/A NAND_magic_3/B 0.08fF

C4 VDD GND 0.07fF

C5 NAND_magic_3/w_0_0# out 0.02fF

C6 NAND_magic_3/w_0_0# NAND_magic_3/A 0.06fF

C7 NAND_magic_2/w_0_0# B 0.06fF

C8 NAND_magic_2/A A 0.13fF

C9 VDD NAND_magic_1/w_0_0# 0.09fF

C10 NAND_magic_3/A A 0.05fF

C11 B GND 0.14fF

C12 VDD NAND_magic_0/w_0_0# 0.09fF

C13 NAND_magic_3/B NAND_magic_2/w_0_0# 0.02fF

C14 NAND_magic_3/A NAND_magic_2/A 0.08fF

C15 NAND_magic_3/B VDD 0.22fF

C16 NAND_magic_3/A out 0.05fF

C17 NAND_magic_3/B GND 0.09fF

C18 NAND_magic_3/w_0_0# VDD 0.09fF

C19 B NAND_magic_0/w_0_0# 0.06fF

C20 NAND_magic_3/B B 0.08fF

C21 VDD A 0.12fF

C22 NAND_magic_2/w_0_0# NAND_magic_2/A 0.06fF

C23 VDD NAND_magic_2/A 0.38fF

C24 A GND 0.14fF

C25 VDD out 0.22fF

C26 NAND_magic_3/A VDD 0.24fF

C27 NAND_magic_2/A GND 0.17fF

C28 NAND_magic_3/A GND 0.07fF

C29 A B 0.08fF

C30 A NAND_magic_1/w_0_0# 0.12fF

C31 NAND_magic_3/w_0_0# NAND_magic_3/B 0.06fF

C32 NAND_magic_2/A B 0.15fF

C33 NAND_magic_2/A NAND_magic_1/w_0_0# 0.06fF

C34 A NAND_magic_0/w_0_0# 0.08fF

C35 NAND_magic_3/A NAND_magic_1/w_0_0# 0.02fF

C36 NAND_magic_2/A NAND_magic_0/w_0_0# 0.02fF

C37 GND Gnd 4.10fF

C38 B Gnd 0.98fF

C39 A Gnd 0.51fF

C40 NAND_magic_2/A Gnd 0.69fF

C41 NAND_magic_2/w_0_0# Gnd 0.64fF

C42 NAND_magic_1/w_0_0# Gnd 0.64fF

C43 NAND_magic_0/w_0_0# Gnd 0.64fF

C44 out Gnd 0.14fF

C45 VDD Gnd 1.11fF

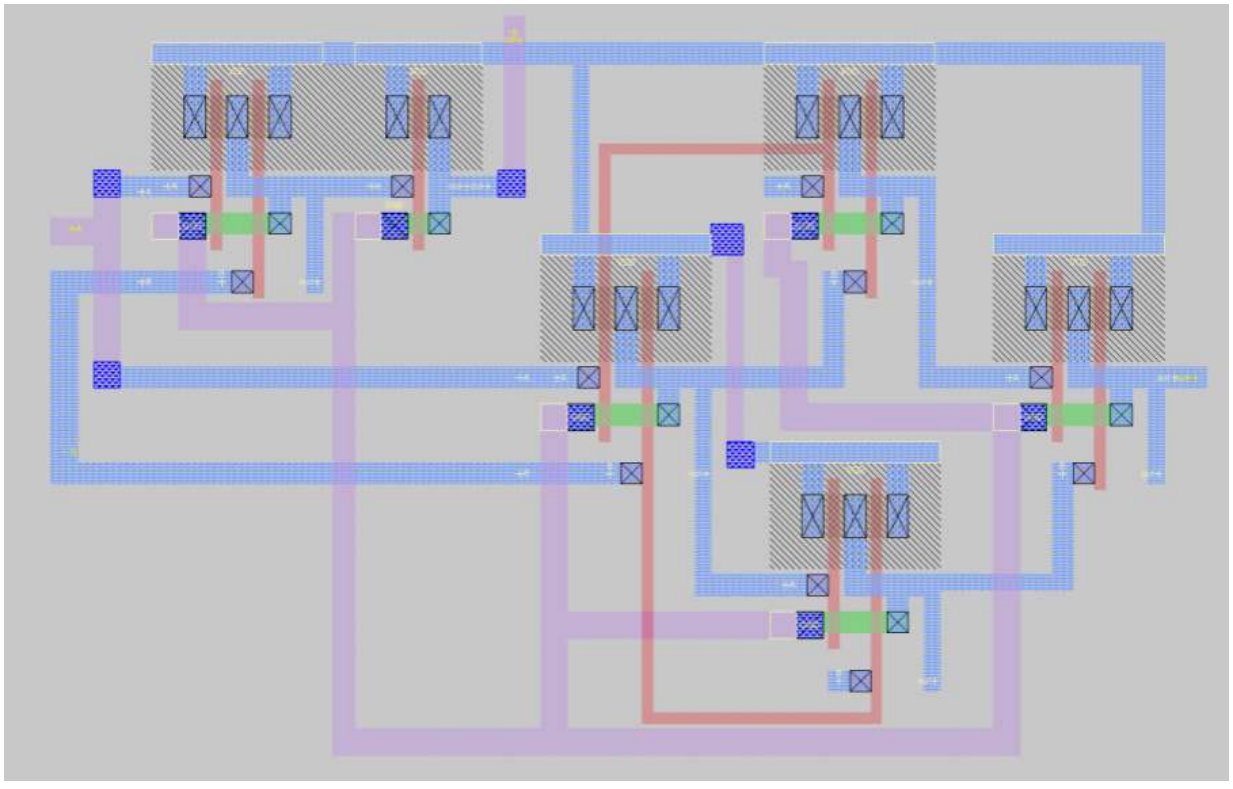
C46 NAND_magic_3/B Gnd 0.43fF

C47 NAND_magic_3/A Gnd 0.36fF

C48 NAND_magic_3/w_0_0# Gnd 0.64fF

2.1.5 HALF ADDER

Magic Layout :



Netlist extracted :

```
* SPICE3 file created from HA_magic.ext - technology: scmos


.option scale=0.09u


M1000 VDD XOR_magic_0/NAND_magic_3/B sum XOR_magic_0/NAND_magic_3/w_0_0# pfet w=8 l=2
+  ad=440 pd=286 as=48 ps=28
M1001 sum XOR_magic_0/NAND_magic_3/A VDD XOR_magic_0/NAND_magic_3/w_0_0# pfet w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1002 sum XOR_magic_0/NAND_magic_3/B XOR_magic_0/NAND_magic_3/a_13_n12# Gnd nfet w=4 l=2
+  ad=20 pd=18 as=24 ps=20
M1003 XOR_magic_0/NAND_magic_3/a_13_n12# XOR_magic_0/NAND_magic_3/A GND Gnd nfet w=4 l=2
+  ad=0 pd=0 as=174 ps=132
M1004 VDD B XOR_magic_0/NAND_magic_2/A XOR_magic_0/NAND_magic_0/w_0_0# pfet w=8 l=2
+  ad=0 pd=0 as=48 ps=28
M1005 XOR_magic_0/NAND_magic_2/A A VDD XOR_magic_0/NAND_magic_0/w_0_0# pfet w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1006 XOR_magic_0/NAND_magic_2/A B XOR_magic_0/NAND_magic_0/a_13_n12# Gnd nfet w=4 l=2
+  ad=20 pd=18 as=24 ps=20
M1007 XOR_magic_0/NAND_magic_0/a_13_n12# A GND Gnd nfet w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1008 VDD XOR_magic_0/NAND_magic_2/A XOR_magic_0/NAND_magic_3/A XOR_magic_0/NAND_magic_1/w_0_0# pfet w=8 l=2
+  ad=0 pd=0 as=48 ps=28
M1009 XOR_magic_0/NAND_magic_3/A A VDD XOR_magic_0/NAND_magic_1/w_0_0# pfet w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1010 XOR_magic_0/NAND_magic_3/A XOR_magic_0/NAND_magic_2/A XOR_magic_0/NAND_magic_1/a_13_n12# Gnd nfet w=4 l=2
+  ad=20 pd=18 as=24 ps=20
M1011 XOR_magic_0/NAND_magic_1/a_13_n12# A GND Gnd nfet w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1012 VDD B XOR_magic_0/NAND_magic_3/B XOR_magic_0/NAND_magic_2/w_0_0# pfet w=8 l=2
+  ad=0 pd=0 as=48 ps=28
M1013 XOR_magic_0/NAND_magic_3/B XOR_magic_0/NAND_magic_2/A VDD XOR_magic_0/NAND_magic_2/w_0_0# pfet w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1014 XOR_magic_0/NAND_magic_3/B B XOR_magic_0/NAND_magic_2/a_13_n12# Gnd nfet w=4 l=2
+  ad=20 pd=18 as=24 ps=20
M1015 XOR_magic_0/NAND_magic_2/a_13_n12# XOR_magic_0/NAND_magic_2/A GND Gnd nfet w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1016 carry and_magic_0/NAND_magic_0/out VDD and_magic_0/w_32_19# pfet w=8 l=2
+  ad=40 pd=26 as=0 ps=0
M1017 carry and_magic_0/NAND_magic_0/out GND Gnd nfet w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1018 VDD B and_magic_0/NAND_magic_0/out and_magic_0/w_32_19# pfet w=8 l=2
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+  ad=0 pd=0 as=48 ps=28
M1019 and_magic_0/NAND_magic_0/out A VDD and_magic_0/w_32_19# pfet w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1020 and_magic_0/NAND_magic_0/out B and_magic_0/NAND_magic_0/a_13_n12# Gnd nfet w=4 l=2
+  ad=20 pd=18 as=24 ps=20
M1021 and_magic_0/NAND_magic_0/a_13_n12# A GND Gnd nfet w=4 l=2
+  ad=0 pd=0 as=0 ps=0
C0 A GND 0.30fF
C1 XOR_magic_0/NAND_magic_2/w_0_0# XOR_magic_0/NAND_magic_2/A 0.06fF
C2 XOR_magic_0/NAND_magic_1/w_0_0# A 0.12fF
C3 XOR_magic_0/NAND_magic_2/A GND 0.17fF
C4 XOR_magic_0/NAND_magic_1/w_0_0# XOR_magic_0/NAND_magic_2/A 0.06fF
C5 XOR_magic_0/NAND_magic_3/B XOR_magic_0/NAND_magic_2/A 0.05fF
C6 VDD XOR_magic_0/NAND_magic_2/w_0_0# 0.09fF
C7 A B 0.32fF
C8 and_magic_0/NAND_magic_0/out carry 0.05fF
C9 VDD GND 0.07fF
C10 VDD XOR_magic_0/NAND_magic_1/w_0_0# 0.09fF
C11 and_magic_0/w_32_19# B 0.06fF
C12 XOR_magic_0/NAND_magic_3/B VDD 0.22fF
C13 XOR_magic_0/NAND_magic_3/A sum 0.05fF
C14 XOR_magic_0/NAND_magic_2/A B 0.15fF
C15 XOR_magic_0/NAND_magic_3/w_0_0# XOR_magic_0/NAND_magic_3/B 0.06fF
C16 and_magic_0/NAND_magic_0/out A 0.05fF
C17 and_magic_0/NAND_magic_0/out and_magic_0/w_32_19# 0.09fF
C18 XOR_magic_0/NAND_magic_0/w_0_0# B 0.06fF
C19 XOR_magic_0/NAND_magic_3/A A 0.05fF
C20 VDD and_magic_0/NAND_magic_0/out 0.24fF
C21 and_magic_0/w_32_19# carry 0.03fF
C22 XOR_magic_0/NAND_magic_3/B XOR_magic_0/NAND_magic_2/w_0_0# 0.02fF
C23 XOR_magic_0/NAND_magic_3/A XOR_magic_0/NAND_magic_2/A 0.08fF
C24 XOR_magic_0/NAND_magic_3/B GND 0.09fF
C25 VDD sum 0.22fF
C26 and_magic_0/w_32_19# A 0.06fF
C27 XOR_magic_0/NAND_magic_3/A VDD 0.24fF
C28 XOR_magic_0/NAND_magic_3/w_0_0# sum 0.02fF
C29 XOR_magic_0/NAND_magic_2/w_0_0# B 0.06fF
C30 XOR_magic_0/NAND_magic_2/A A 0.13fF
C31 VDD carry 0.20fF
C32 XOR_magic_0/NAND_magic_3/w_0_0# XOR_magic_0/NAND_magic_3/A 0.06fF
C33 XOR_magic_0/NAND_magic_0/w_0_0# A 0.08fF
C34 B GND 0.35fF
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C35 XOR_magic_0/NAND_magic_3/B B 0.08fF

C36 VDD A 0.15fF

C37 XOR_magic_0/NAND_magic_0/w_0_0# XOR_magic_0/NAND_magic_2/A 0.02fF

C38 VDD and_magic_0/w_32_19# 0.14fF

C39 and_magic_0/NAND_magic_0/out GND 0.07fF

C40 VDD XOR_magic_0/NAND_magic_2/A 0.38fF

C41 VDD XOR_magic_0/NAND_magic_0/w_0_0# 0.09fF

C42 XOR_magic_0/NAND_magic_3/A GND 0.07fF

C43 XOR_magic_0/NAND_magic_3/B sum 0.08fF

C44 XOR_magic_0/NAND_magic_3/A XOR_magic_0/NAND_magic_1/w_0_0# 0.02fF

C45 carry GND 0.04fF

C46 XOR_magic_0/NAND_magic_3/w_0_0# VDD 0.09fF

C47 XOR_magic_0/NAND_magic_3/A XOR_magic_0/NAND_magic_3/B 0.08fF

C48 and_magic_0/NAND_magic_0/out B 0.08fF

C49 and_magic_0/NAND_magic_0/out Gnd 0.28fF

C50 and_magic_0/w_32_19# Gnd 1.25fF

C51 carry Gnd 0.04fF

C52 GND Gnd 6.41fF

C53 B Gnd 1.66fF

C54 A Gnd 1.23fF

C55 XOR_magic_0/NAND_magic_2/A Gnd 0.69fF

C56 XOR_magic_0/NAND_magic_2/w_0_0# Gnd 0.64fF

C57 XOR_magic_0/NAND_magic_1/w_0_0# Gnd 0.64fF

C58 XOR_magic_0/NAND_magic_0/w_0_0# Gnd 0.64fF

C59 sum Gnd 0.16fF

C60 VDD Gnd 1.34fF

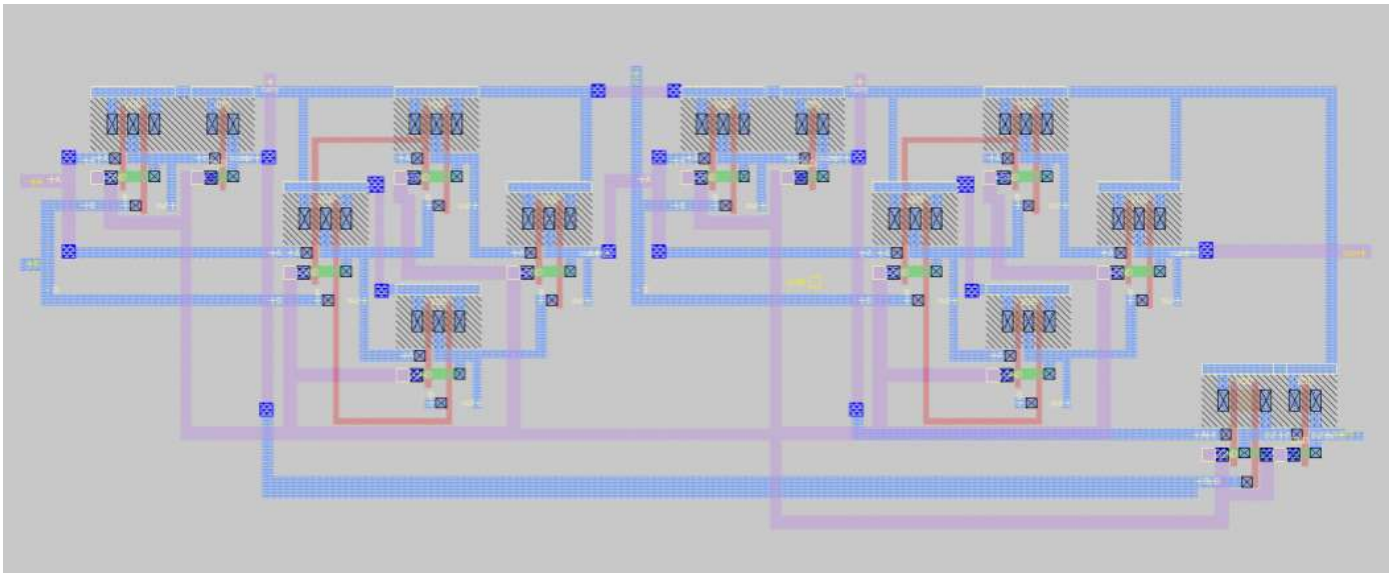
C61 XOR_magic_0/NAND_magic_3/B Gnd 0.43fF

C62 XOR_magic_0/NAND_magic_3/A Gnd 0.36fF

C63 XOR_magic_0/NAND_magic_3/w_0_0# Gnd 0.64fF

2.1.6 FULL ADDER

Magic Layout :



Netlist extracted :

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* SPICE3 file created from FA_magic.ext - technology: scmos

.SUBCKT fulladd A B C sum carry VDD GND

.option scale=0.09u


M1000 VDD HA_magic_0/XOR_magic_0/NAND_magic_3/B HA_magic_1/A HA_magic_0/XOR_magic_0/NAND_magic_3/w_0_0# CMOSP w=8 l=2

+  ad=960 pd=624 as=48 ps=28

M1001 HA_magic_1/A HA_magic_0/XOR_magic_0/NAND_magic_3/A VDD HA_magic_0/XOR_magic_0/NAND_magic_3/w_0_0# CMOSP w=8 l=2

+  ad=0 pd=0 as=0 ps=0

M1002 HA_magic_1/A HA_magic_0/XOR_magic_0/NAND_magic_3/B HA_magic_0/XOR_magic_0/NAND_magic_3/a_13_n12# Gnd CMOSN w=4
l=2

+  ad=20 pd=18 as=24 ps=20

M1003 HA_magic_0/XOR_magic_0/NAND_magic_3/a_13_n12# HA_magic_0/XOR_magic_0/NAND_magic_3/A GND Gnd CMOSN w=4 l=2

+  ad=0 pd=0 as=435 ps=330

M1004 VDD B HA_magic_0/XOR_magic_0/NAND_magic_2/A HA_magic_0/XOR_magic_0/NAND_magic_0/w_0_0# CMOSP w=8 l=2

+  ad=0 pd=0 as=48 ps=28

M1005 HA_magic_0/XOR_magic_0/NAND_magic_2/A A VDD HA_magic_0/XOR_magic_0/NAND_magic_0/w_0_0# CMOSP w=8 l=2

+  ad=0 pd=0 as=0 ps=0

M1006 HA_magic_0/XOR_magic_0/NAND_magic_2/A B HA_magic_0/XOR_magic_0/NAND_magic_0/a_13_n12# Gnd CMOSN w=4 l=2

+  ad=20 pd=18 as=24 ps=20

M1007 HA_magic_0/XOR_magic_0/NAND_magic_0/a_13_n12# A GND Gnd CMOSN w=4 l=2

+  ad=0 pd=0 as=0 ps=0

M1008 VDD HA_magic_0/XOR_magic_0/NAND_magic_2/A HA_magic_0/XOR_magic_0/NAND_magic_3/A
HA_magic_0/XOR_magic_0/NAND_magic_1/w_0_0# CMOSP w=8 l=2

+  ad=0 pd=0 as=48 ps=28

M1009 HA_magic_0/XOR_magic_0/NAND_magic_3/A A VDD HA_magic_0/XOR_magic_0/NAND_magic_1/w_0_0# CMOSP w=8 l=2
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+  ad=0 pd=0 as=0 ps=0

M1010 HA_magic_0/XOR_magic_0/NAND_magic_3/A HA_magic_0/XOR_magic_0/NAND_magic_2/A
HA_magic_0/XOR_magic_0/NAND_magic_1/a_13_n12# Gnd CMOSN w=4 l=2

+  ad=20 pd=18 as=24 ps=20

M1011 HA_magic_0/XOR_magic_0/NAND_magic_1/a_13_n12# A GND Gnd CMOSN w=4 l=2

+  ad=0 pd=0 as=0 ps=0

M1012 VDD B HA_magic_0/XOR_magic_0/NAND_magic_3/B HA_magic_0/XOR_magic_0/NAND_magic_2/w_0_0# CMOSP w=8 l=2

+  ad=0 pd=0 as=48 ps=28

M1013 HA_magic_0/XOR_magic_0/NAND_magic_3/B HA_magic_0/XOR_magic_0/NAND_magic_2/A VDD
HA_magic_0/XOR_magic_0/NAND_magic_2/w_0_0# CMOSP w=8 l=2

+  ad=0 pd=0 as=0 ps=0

M1014 HA_magic_0/XOR_magic_0/NAND_magic_3/B B HA_magic_0/XOR_magic_0/NAND_magic_2/a_13_n12# Gnd CMOSN w=4 l=2

+  ad=20 pd=18 as=24 ps=20

M1015 HA_magic_0/XOR_magic_0/NAND_magic_2/a_13_n12# HA_magic_0/XOR_magic_0/NAND_magic_2/A GND Gnd CMOSN w=4 l=2

+  ad=0 pd=0 as=0 ps=0

M1016 or_magic_0/B HA_magic_0/and_magic_0/NAND_magic_0/out VDD HA_magic_0/and_magic_0/w_32_19# CMOSP w=8 l=2

+  ad=40 pd=26 as=0 ps=0

M1017 or_magic_0/B HA_magic_0/and_magic_0/NAND_magic_0/out GND Gnd CMOSN w=4 l=2

+  ad=20 pd=18 as=0 ps=0

M1018 VDD B HA_magic_0/and_magic_0/NAND_magic_0/out HA_magic_0/and_magic_0/w_32_19# CMOSP w=8 l=2

+  ad=0 pd=0 as=48 ps=28

M1019 HA_magic_0/and_magic_0/NAND_magic_0/out A VDD HA_magic_0/and_magic_0/w_32_19# CMOSP w=8 l=2

+  ad=0 pd=0 as=0 ps=0

M1020 HA_magic_0/and_magic_0/NAND_magic_0/out B HA_magic_0/and_magic_0/NAND_magic_0/a_13_n12# Gnd CMOSN w=4 l=2

+  ad=20 pd=18 as=24 ps=20

M1021 HA_magic_0/and_magic_0/NAND_magic_0/a_13_n12# A GND Gnd CMOSN w=4 l=2

+  ad=0 pd=0 as=0 ps=0

M1022 VDD HA_magic_1/XOR_magic_0/NAND_magic_3/B sum HA_magic_1/XOR_magic_0/NAND_magic_3/w_0_0# CMOSP w=8 l=2

+  ad=0 pd=0 as=48 ps=28

M1023 sum HA_magic_1/XOR_magic_0/NAND_magic_3/A VDD HA_magic_1/XOR_magic_0/NAND_magic_3/w_0_0# CMOSP w=8 l=2

+  ad=0 pd=0 as=0 ps=0

M1024 sum HA_magic_1/XOR_magic_0/NAND_magic_3/B HA_magic_1/XOR_magic_0/NAND_magic_3/a_13_n12# Gnd CMOSN w=4 l=2

+  ad=20 pd=18 as=24 ps=20

M1025 HA_magic_1/XOR_magic_0/NAND_magic_3/a_13_n12# HA_magic_1/XOR_magic_0/NAND_magic_3/A GND Gnd CMOSN w=4 l=2

+  ad=0 pd=0 as=0 ps=0

M1026 VDD C HA_magic_1/XOR_magic_0/NAND_magic_2/A HA_magic_1/XOR_magic_0/NAND_magic_0/w_0_0# CMOSP w=8 l=2

+  ad=0 pd=0 as=48 ps=28

M1027 HA_magic_1/XOR_magic_0/NAND_magic_2/A HA_magic_1/A VDD HA_magic_1/XOR_magic_0/NAND_magic_0/w_0_0# CMOSP w=8 l=2

+  ad=0 pd=0 as=0 ps=0

M1028 HA_magic_1/XOR_magic_0/NAND_magic_2/A C HA_magic_1/XOR_magic_0/NAND_magic_0/a_13_n12# Gnd CMOSN w=4 l=2

+  ad=20 pd=18 as=24 ps=20

M1029 HA_magic_1/XOR_magic_0/NAND_magic_0/a_13_n12# HA_magic_1/A GND Gnd CMOSN w=4 l=2

+  ad=0 pd=0 as=0 ps=0
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M1030 VDD HA_magic_1/XOR_magic_0/NAND_magic_2/A HA_magic_1/XOR_magic_0/NAND_magic_3/A
HA_magic_1/XOR_magic_0/NAND_magic_1/w_0_0# CMOSP w=8 l=2

+  ad=0 pd=0 as=48 ps=28

M1031 HA_magic_1/XOR_magic_0/NAND_magic_3/A HA_magic_1/A VDD HA_magic_1/XOR_magic_0/NAND_magic_1/w_0_0# CMOSP w=8 l=2

+  ad=0 pd=0 as=0 ps=0

M1032 HA_magic_1/XOR_magic_0/NAND_magic_3/A HA_magic_1/XOR_magic_0/NAND_magic_2/A
HA_magic_1/XOR_magic_0/NAND_magic_1/a_13_n12# Gnd CMOSN w=4 l=2

+  ad=20 pd=18 as=24 ps=20

M1033 HA_magic_1/XOR_magic_0/NAND_magic_1/a_13_n12# HA_magic_1/A GND Gnd CMOSN w=4 l=2

+  ad=0 pd=0 as=0 ps=0

M1034 VDD C HA_magic_1/XOR_magic_0/NAND_magic_3/B HA_magic_1/XOR_magic_0/NAND_magic_2/w_0_0# CMOSP w=8 l=2

+  ad=0 pd=0 as=48 ps=28

M1035 HA_magic_1/XOR_magic_0/NAND_magic_3/B HA_magic_1/XOR_magic_0/NAND_magic_2/A VDD
HA_magic_1/XOR_magic_0/NAND_magic_2/w_0_0# CMOSP w=8 l=2

+  ad=0 pd=0 as=0 ps=0

M1036 HA_magic_1/XOR_magic_0/NAND_magic_3/B C HA_magic_1/XOR_magic_0/NAND_magic_2/a_13_n12# Gnd CMOSN w=4 l=2

+  ad=20 pd=18 as=24 ps=20

M1037 HA_magic_1/XOR_magic_0/NAND_magic_2/a_13_n12# HA_magic_1/XOR_magic_0/NAND_magic_2/A GND Gnd CMOSN w=4 l=2

+  ad=0 pd=0 as=0 ps=0

M1038 or_magic_0/A HA_magic_1/and_magic_0/NAND_magic_0/out VDD HA_magic_1/and_magic_0/w_32_19# CMOSP w=8 l=2

+  ad=40 pd=26 as=0 ps=0

M1039 or_magic_0/A HA_magic_1/and_magic_0/NAND_magic_0/out GND Gnd CMOSN w=4 l=2

+  ad=20 pd=18 as=0 ps=0

M1040 VDD C HA_magic_1/and_magic_0/NAND_magic_0/out HA_magic_1/and_magic_0/w_32_19# CMOSP w=8 l=2

+  ad=0 pd=0 as=48 ps=28

M1041 HA_magic_1/and_magic_0/NAND_magic_0/out HA_magic_1/A VDD HA_magic_1/and_magic_0/w_32_19# CMOSP w=8 l=2

+  ad=0 pd=0 as=0 ps=0

M1042 HA_magic_1/and_magic_0/NAND_magic_0/out C HA_magic_1/and_magic_0/NAND_magic_0/a_13_n12# Gnd CMOSN w=4 l=2

+  ad=20 pd=18 as=24 ps=20

M1043 HA_magic_1/and_magic_0/NAND_magic_0/a_13_n12# HA_magic_1/A GND Gnd CMOSN w=4 l=2

+  ad=0 pd=0 as=0 ps=0

M1044 carry or_magic_0/NOR_magic_0/out VDD or_magic_0/NOR_magic_0/w_0_0# CMOSP w=8 l=2

+  ad=40 pd=26 as=0 ps=0

M1045 carry or_magic_0/NOR_magic_0/out GND Gnd CMOSN w=4 l=2

+  ad=20 pd=18 as=0 ps=0

M1046 or_magic_0/NOR_magic_0/out or_magic_0/B or_magic_0/NOR_magic_0/a_13_6# or_magic_0/NOR_magic_0/w_0_0# CMOSP w=8
l=2

+  ad=40 pd=26 as=48 ps=28

M1047 or_magic_0/NOR_magic_0/a_13_6# or_magic_0/A VDD or_magic_0/NOR_magic_0/w_0_0# CMOSP w=8 l=2

+  ad=0 pd=0 as=0 ps=0

M1048 GND or_magic_0/B or_magic_0/NOR_magic_0/out Gnd CMOSN w=4 l=2

+  ad=0 pd=0 as=24 ps=20

M1049 or_magic_0/NOR_magic_0/out or_magic_0/A GND Gnd CMOSN w=4 l=2

+  ad=0 pd=0 as=0 ps=0
```

C0 sum VDD 0.31fF

C1 VDD HA_magic_1/XOR_magic_0/NAND_magic_0/w_0_0# 0.09fF

C2 HA_magic_1/XOR_magic_0/NAND_magic_3/A HA_magic_1/XOR_magic_0/NAND_magic_1/w_0_0# 0.02fF

C3 HA_magic_0/XOR_magic_0/NAND_magic_3/w_0_0# HA_magic_0/XOR_magic_0/NAND_magic_3/A 0.06fF

C4 GND C 0.35fF

C5 VDD HA_magic_0/and_magic_0/w_32_19# 0.14fF

C6 GND A 0.30fF

C7 VDD HA_magic_0/and_magic_0/NAND_magic_0/out 0.24fF

C8 HA_magic_0/and_magic_0/w_32_19# HA_magic_0/and_magic_0/NAND_magic_0/out 0.09fF

C9 GND or_magic_0/B 0.56fF

C10 HA_magic_0/XOR_magic_0/NAND_magic_2/w_0_0# B 0.06fF

C11 GND HA_magic_1/XOR_magic_0/NAND_magic_2/A 0.17fF

C12 VDD HA_magic_1/XOR_magic_0/NAND_magic_1/w_0_0# 0.09fF

C13 or_magic_0/NOR_magic_0/out or_magic_0/B 0.10fF

C14 VDD or_magic_0/A 0.22fF

C15 or_magic_0/NOR_magic_0/w_0_0# or_magic_0/B 0.06fF

C16 HA_magic_1/XOR_magic_0/NAND_magic_3/A HA_magic_1/XOR_magic_0/NAND_magic_3/w_0_0# 0.06fF

C17 GND HA_magic_1/XOR_magic_0/NAND_magic_3/A 0.07fF

C18 HA_magic_0/XOR_magic_0/NAND_magic_3/A HA_magic_0/XOR_magic_0/NAND_magic_1/w_0_0# 0.02fF

C19 GND carry 0.04fF

C20 HA_magic_1/XOR_magic_0/NAND_magic_3/w_0_0# HA_magic_1/XOR_magic_0/NAND_magic_3/B 0.06fF

C21 GND HA_magic_1/XOR_magic_0/NAND_magic_3/B 0.09fF

C22 A HA_magic_0/XOR_magic_0/NAND_magic_1/w_0_0# 0.12fF

C23 or_magic_0/NOR_magic_0/out carry 0.05fF

C24 GND HA_magic_0/XOR_magic_0/NAND_magic_2/A 0.17fF

C25 or_magic_0/NOR_magic_0/w_0_0# carry 0.03fF

C26 sum HA_magic_1/XOR_magic_0/NAND_magic_3/w_0_0# 0.02fF

C27 GND HA_magic_0/XOR_magic_0/NAND_magic_3/B 0.09fF

C28 VDD HA_magic_1/XOR_magic_0/NAND_magic_3/w_0_0# 0.09fF

C29 GND VDD 0.14fF

C30 HA_magic_1/A HA_magic_1/and_magic_0/NAND_magic_0/out 0.05fF

C31 HA_magic_1/A HA_magic_0/XOR_magic_0/NAND_magic_3/A 0.05fF

C32 HA_magic_1/and_magic_0/w_32_19# HA_magic_1/A 0.06fF

C33 HA_magic_0/XOR_magic_0/NAND_magic_0/w_0_0# B 0.06fF

C34 C HA_magic_1/XOR_magic_0/NAND_magic_2/w_0_0# 0.06fF

C35 HA_magic_0/XOR_magic_0/NAND_magic_3/w_0_0# HA_magic_0/XOR_magic_0/NAND_magic_3/B 0.06fF

C36 B A 0.32fF

C37 HA_magic_0/XOR_magic_0/NAND_magic_3/w_0_0# VDD 0.09fF

C38 VDD or_magic_0/NOR_magic_0/out 0.10fF

C39 HA_magic_1/A C 0.50fF

C40 GND HA_magic_0/and_magic_0/NAND_magic_0/out 0.07fF

C41 VDD or_magic_0/NOR_magic_0/w_0_0# 0.11fF

C42 HA_magic_1/and_magic_0/w_32_19# HA_magic_1/and_magic_0/NAND_magic_0/out 0.09fF

C43 or_magic_0/B B 0.09fF

C44 C HA_magic_1/and_magic_0/NAND_magic_0/out 0.08fF

C45 HA_magic_1/XOR_magic_0/NAND_magic_2/A HA_magic_1/XOR_magic_0/NAND_magic_2/w_0_0# 0.06fF

C46 HA_magic_1/and_magic_0/w_32_19# C 0.06fF

C47 A HA_magic_0/XOR_magic_0/NAND_magic_3/A 0.05fF

C48 HA_magic_1/XOR_magic_0/NAND_magic_2/A HA_magic_1/A 0.13fF

C49 GND or_magic_0/A 0.93fF

C50 HA_magic_0/XOR_magic_0/NAND_magic_2/A HA_magic_0/XOR_magic_0/NAND_magic_1/w_0_0# 0.06fF

C51 HA_magic_0/XOR_magic_0/NAND_magic_0/w_0_0# A 0.08fF

C52 HA_magic_0/XOR_magic_0/NAND_magic_2/w_0_0# HA_magic_0/XOR_magic_0/NAND_magic_2/A 0.06fF

C53 or_magic_0/NOR_magic_0/out or_magic_0/A 0.05fF

C54 HA_magic_0/XOR_magic_0/NAND_magic_2/w_0_0# HA_magic_0/XOR_magic_0/NAND_magic_3/B 0.02fF

C55 VDD HA_magic_0/XOR_magic_0/NAND_magic_1/w_0_0# 0.09fF

C56 or_magic_0/NOR_magic_0/w_0_0# or_magic_0/A 0.06fF

C57 HA_magic_1/A HA_magic_1/XOR_magic_0/NAND_magic_3/A 0.05fF

C58 VDD HA_magic_0/XOR_magic_0/NAND_magic_2/w_0_0# 0.09fF

C59 HA_magic_1/XOR_magic_0/NAND_magic_2/w_0_0# HA_magic_1/XOR_magic_0/NAND_magic_3/B 0.02fF

C60 HA_magic_1/XOR_magic_0/NAND_magic_2/A C 0.15fF

C61 HA_magic_0/XOR_magic_0/NAND_magic_2/A B 0.15fF

C62 or_magic_0/B A 0.09fF

C63 B HA_magic_0/XOR_magic_0/NAND_magic_3/B 0.08fF

C64 VDD HA_magic_1/XOR_magic_0/NAND_magic_2/w_0_0# 0.09fF

C65 HA_magic_1/A HA_magic_0/XOR_magic_0/NAND_magic_3/B 0.08fF

C66 B HA_magic_0/and_magic_0/w_32_19# 0.06fF

C67 HA_magic_0/XOR_magic_0/NAND_magic_2/A HA_magic_0/XOR_magic_0/NAND_magic_3/A 0.08fF

C68 VDD HA_magic_1/A 0.36fF

C69 HA_magic_1/A HA_magic_1/XOR_magic_0/NAND_magic_0/w_0_0# 0.08fF

C70 GND or_magic_0/NOR_magic_0/out 0.22fF

C71 C HA_magic_1/XOR_magic_0/NAND_magic_3/B 0.08fF

C72 B HA_magic_0/and_magic_0/NAND_magic_0/out 0.08fF

C73 HA_magic_0/XOR_magic_0/NAND_magic_0/w_0_0# HA_magic_0/XOR_magic_0/NAND_magic_2/A 0.02fF

C74 HA_magic_0/XOR_magic_0/NAND_magic_3/A HA_magic_0/XOR_magic_0/NAND_magic_3/B 0.08fF

C75 VDD HA_magic_1/and_magic_0/NAND_magic_0/out 0.24fF

C76 VDD HA_magic_0/XOR_magic_0/NAND_magic_3/A 0.24fF

C77 HA_magic_0/XOR_magic_0/NAND_magic_2/A A 0.13fF

C78 VDD HA_magic_1/and_magic_0/w_32_19# 0.14fF

C79 HA_magic_1/XOR_magic_0/NAND_magic_2/A HA_magic_1/XOR_magic_0/NAND_magic_3/A 0.08fF

C80 or_magic_0/NOR_magic_0/out or_magic_0/NOR_magic_0/w_0_0# 0.10fF

C81 VDD HA_magic_0/XOR_magic_0/NAND_magic_0/w_0_0# 0.09fF

C82 VDD C 0.09fF

C83 C HA_magic_1/XOR_magic_0/NAND_magic_0/w_0_0# 0.06fF

C84 HA_magic_1/XOR_magic_0/NAND_magic_2/A HA_magic_1/XOR_magic_0/NAND_magic_3/B 0.05fF

C85 VDD A 0.15fF

C86 HA_magic_1/A HA_magic_1/XOR_magic_0/NAND_magic_1/w_0_0# 0.12fF

C87 or_magic_0/A HA_magic_1/A 0.09fF

C88 A HA_magic_0/and_magic_0/w_32_19# 0.06fF

C89 A HA_magic_0/and_magic_0/NAND_magic_0/out 0.05fF

C90 VDD or_magic_0/B 0.20fF

C91 HA_magic_1/XOR_magic_0/NAND_magic_3/A HA_magic_1/XOR_magic_0/NAND_magic_3/B 0.08fF

C92 VDD HA_magic_1/XOR_magic_0/NAND_magic_2/A 0.38fF

C93 or_magic_0/A HA_magic_1/and_magic_0/NAND_magic_0/out 0.05fF

C94 HA_magic_1/XOR_magic_0/NAND_magic_2/A HA_magic_1/XOR_magic_0/NAND_magic_0/w_0_0# 0.02fF

C95 or_magic_0/A HA_magic_1/and_magic_0/w_32_19# 0.03fF

C96 or_magic_0/B HA_magic_0/and_magic_0/w_32_19# 0.03fF

C97 or_magic_0/A C 0.09fF

C98 or_magic_0/B HA_magic_0/and_magic_0/NAND_magic_0/out 0.05fF

C99 sum HA_magic_1/XOR_magic_0/NAND_magic_3/A 0.05fF

C100 VDD HA_magic_1/XOR_magic_0/NAND_magic_3/A 0.24fF

C101 GND B 0.35fF

C102 VDD carry 0.11fF

C103 sum HA_magic_1/XOR_magic_0/NAND_magic_3/B 0.08fF

C104 GND HA_magic_1/A 0.30fF

C105 HA_magic_0/XOR_magic_0/NAND_magic_2/A HA_magic_0/XOR_magic_0/NAND_magic_3/B 0.05fF

C106 VDD HA_magic_1/XOR_magic_0/NAND_magic_3/B 0.22fF

C107 or_magic_0/A or_magic_0/B 0.08fF

C108 VDD HA_magic_0/XOR_magic_0/NAND_magic_2/A 0.38fF

C109 HA_magic_1/XOR_magic_0/NAND_magic_2/A HA_magic_1/XOR_magic_0/NAND_magic_1/w_0_0# 0.06fF

C110 HA_magic_0/XOR_magic_0/NAND_magic_3/w_0_0# HA_magic_1/A 0.02fF

C111 GND HA_magic_1/and_magic_0/NAND_magic_0/out 0.07fF

C112 GND HA_magic_0/XOR_magic_0/NAND_magic_3/A 0.07fF

C113 VDD HA_magic_0/XOR_magic_0/NAND_magic_3/B 0.22fF

C114 carry Gnd 0.06fF

C115 or_magic_0/NOR_magic_0/out Gnd 0.20fF

C116 or_magic_0/NOR_magic_0/w_0_0# Gnd 1.12fF

C117 HA_magic_1/and_magic_0/NAND_magic_0/out Gnd 0.28fF

C118 HA_magic_1/and_magic_0/w_32_19# Gnd 1.25fF

C119 or_magic_0/A Gnd 1.11fF

C120 GND Gnd 17.19fF

C121 C Gnd 1.85fF

C122 HA_magic_1/A Gnd 1.41fF

C123 HA_magic_1/XOR_magic_0/NAND_magic_2/A Gnd 0.69fF

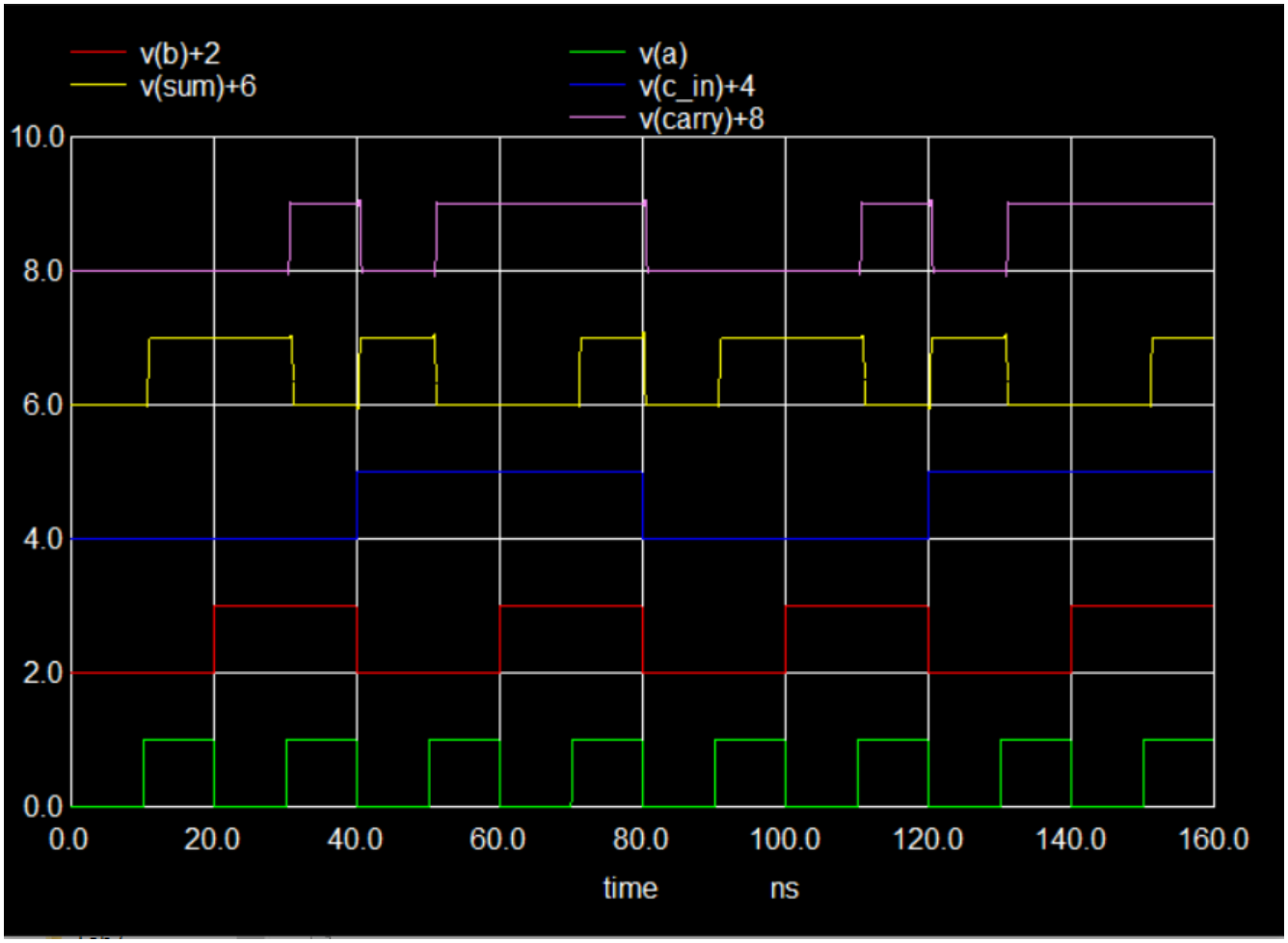
C124 HA_magic_1/XOR_magic_0/NAND_magic_2/w_0_0# Gnd 0.64fF

C125 HA_magic_1/XOR_magic_0/NAND_magic_1/w_0_0# Gnd 0.64fF

```
C126 HA_magic_1/XOR_magic_0/NAND_magic_0/w_0_0# Gnd 0.64fF
C127 VDD Gnd 3.49fF
C128 HA_magic_1/XOR_magic_0/NAND_magic_3/B Gnd 0.43fF
C129 HA_magic_1/XOR_magic_0/NAND_magic_3/A Gnd 0.36fF
C130 HA_magic_1/XOR_magic_0/NAND_magic_3/w_0_0# Gnd 0.64fF
C131 HA_magic_0/and_magic_0/NAND_magic_0/out Gnd 0.28fF
C132 HA_magic_0/and_magic_0/w_32_19# Gnd 1.25fF
C133 B Gnd 1.70fF
C134 A Gnd 1.37fF
C135 HA_magic_0/XOR_magic_0/NAND_magic_2/A Gnd 0.69fF
C136 HA_magic_0/XOR_magic_0/NAND_magic_2/w_0_0# Gnd 0.64fF
C137 HA_magic_0/XOR_magic_0/NAND_magic_1/w_0_0# Gnd 0.64fF
C138 HA_magic_0/XOR_magic_0/NAND_magic_0/w_0_0# Gnd 0.64fF
C139 HA_magic_0/XOR_magic_0/NAND_magic_3/B Gnd 0.43fF
C140 HA_magic_0/XOR_magic_0/NAND_magic_3/A Gnd 0.36fF
C141 HA_magic_0/XOR_magic_0/NAND_magic_3/w_0_0# Gnd 0.64fF

.ENDS fulladd
```

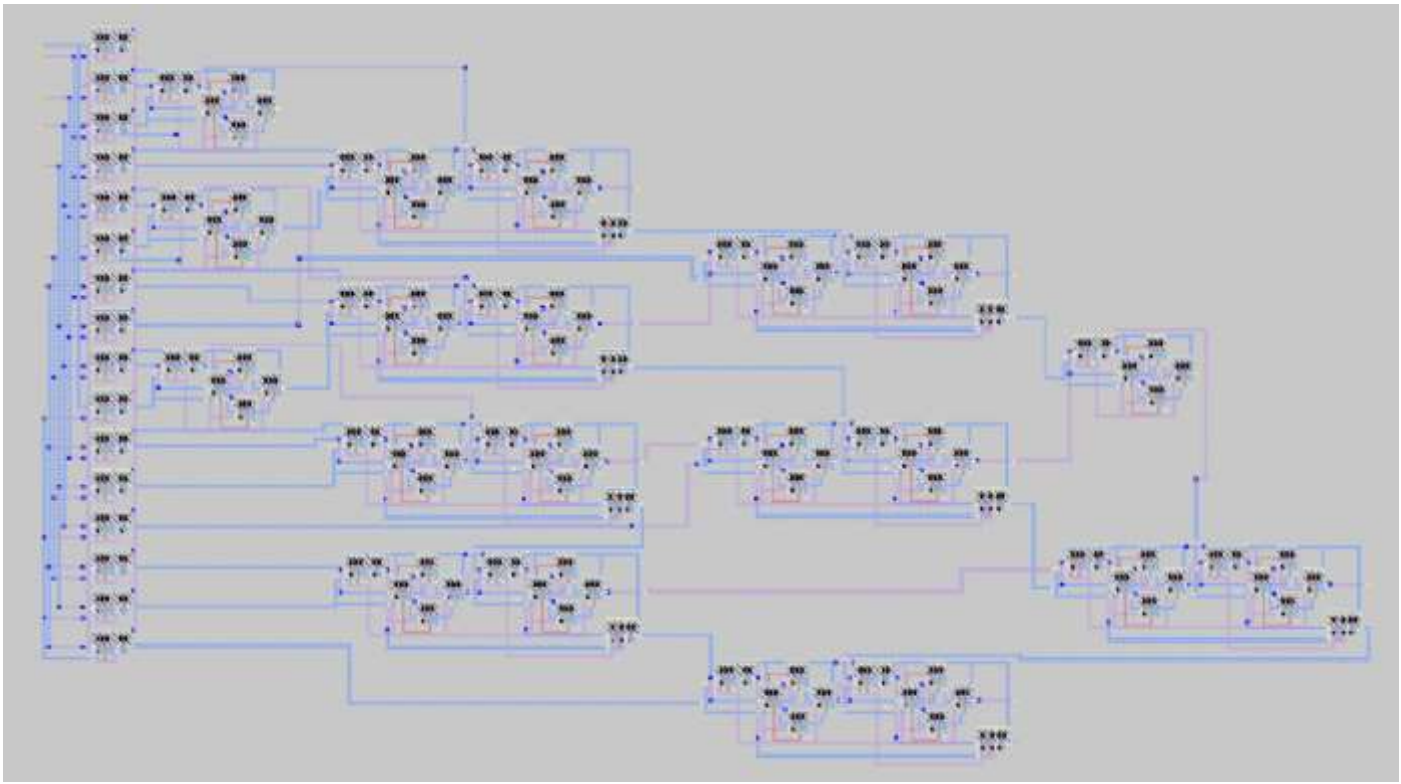
SIMULATION OF THE FULL ADDER :



The working of the full adder shows us that all the subcircuits included are working as expected.

2.2 Multiplier.

Given is the Magic layout of the final multiplier.



2.3 Calculating delays.

The calculated delays are shown below :

File Edit Format View Help

```
Delays with inputs and all outputs :
delay with p0 = 5.7552E-11
delay with p1 = 4.6681E-09
delay with p = 1.05254E-08
delay with p3 = 5.52132E-09
delay with p4 = 1.05655E-08
delay with p5 = 1.36607E-09
delay with p6 = 4.38025E-09
delay with c5 = 1.44134E-08
```

We can observe that the post layout delays are higher than that of pre-layout.

MAX delay = 1.44 x 10^{-8}.

2.4 Calculating Leakage power

The same script used pre-layout is used to calculate the leakage power. The output is outputted in a file that is attached.

- IT can be observed that the leakage powers increase pre-layout to post-layout.

PART – 3 : VERILOG

3.1 : Multiplier Module.

The given Verilog script is the module for the 4 x 4 binary multiplier.

```
`timescale 1ns/10ps
module HA(a,b,sum,carry);

input a,b;
output sum,carry;

 xor(sum,a,b);
 and(carry,a,b);

endmodule

module FA(a,b,c,sum,carry);

input a,b,c;
output sum,carry;

assign sum = a^b^c;
assign carry = (a&b) |(b&c)| (c&a);

endmodule

module project(a0,a1,a2,a3,b0,b1,b2,b3,p0,p1,p2,p3,p4,p5,p6,c5);

input a0,a1,a2,a3,b0,b1,b2,b3;
output p0,p1,p2,p3,p4,p5,p6,c5;

and(p0,a0,b0);
and(x1,a0,b1);
and(x2,a1,b0);
and(x3,a0,b2);
and(x4,a2,b0);
and(x5,a1,b1);
and(x6,a1,b2);
and(x7,a0,b3);
and(x8,b0,a3);
and(x9,b1,a2);
and(x10,a2,b2);
and(x11,b1,a3);
and(x12,b3,a1);
and(x13,b3,a2);
and(x14,b2,a3);
and(x15,b3,a3);

// adders

HA ha1 (x1,x2,p1,y1);
HA ha2 (x4,x5,y2,y3);
HA ha3 (x8,x9,y4,y5);
FA fa1 (x3,y1,y2,p2,z1);
FA fa2 (y3,y4,x6,z2,z3);
FA fa3 (y5,x10,x11,z4,z5);
FA fa4 (x13,x14,z5,z6,z7);
```

```
FA fa5 (z1,z2,x7,p3,v1);
FA fa6 (z3,z4,x12,v2,v3);
HA ha4 (v1,v2,p4,v5);
FA fa7 (z6,v3,v5,p5,v4);
FA fa8 (v4,z7,x15,p6,c5);

endmodule
```

3.2 : Multiplier Testbench.

The following Verilog testbench module gives 10 random input combinations to the multiplier.

```
`timescale 1ns/10ps

module project_tb;

reg a0,a1,a2,a3,b0,b1,b2,b3;
wire p0,p1,p2,p3,p4,p5,p6,c5;

project UUT (a0,a1,a2,a3,b0,b1,b2,b3,p0,p1,p2,p3,p4,p5,p6,c5);

initial

    begin
        $dumpfile("project_tb.vcd");
        $dumpvars(0,project_tb);

        a0=0;
        a1=0;
        a2=0;
        a3=0;
        b0=0;
        b1=0;
        b2=0;
        b3=0;

    end


initial
    begin

       $monitor ("time=%0t a= %d%d%d%d b = %d%d%d%d, Output = %d%d%d%d%d%d%d%d", $time,
a3,a2,a1,a0,b3,b2,b1,b0,c5,p6,p5,p4,p3,p2,p1,p0);

        #5
        a0=1;
        a1=0;
        a2=0;
        a3=0;
        b0=0;
        b1=1;
        b2=0;
        b3=0;

        #5
        a0=1;
        a1=1;
        a2=1;
        a3=1;
        b0=0;
        b1=0;
        b2=1;
        b3=0;
```

```
#5
 a0=1;
 a1=0;
 a2=1;
 a3=0;
 b0=1;
 b1=1;
 b2=0;
 b3=0;

 #5
 a0=0;
 a1=1;
 a2=0;
 a3=0;
 b0=1;
 b1=1;
 b2=0;
 b3=0;

 #5
 a0=1;
 a1=0;
 a2=0;
 a3=1;
 b0=1;
 b1=0;
 b2=0;
 b3=1;

 #5
 a0=1;
 a1=0;
 a2=1;
 a3=1;
 b0=1;
 b1=0;
 b2=0;
 b3=1;

 #5
 a0=1;
 a1=0;
 a2=1;
 a3=1;
 b0=0;
 b1=0;
 b2=0;
 b3=0;
```

```
        #5
        a0=1;
        a1=0;
        a2=0;
        a3=0;
        b0=1;
        b1=0;
        b2=0;
        b3=1;

        #5
        a0=1;
        a1=1;
        a2=1;
        a3=1;
        b0=1;
        b1=1;
        b2=1;
        b3=1;

        #5
        a0=1;
        a1=1;
        a2=0;
        a3=1;
        b0=1;
        b1=0;
        b2=1;
        b3=1;

        #5
        a0=0;
        a1=0;
        a2=0;
        a3=0;
        b0=0;
        b1=0;
        b2=0;
        b3=0;


    end


endmodule
```

3.3 : Output.

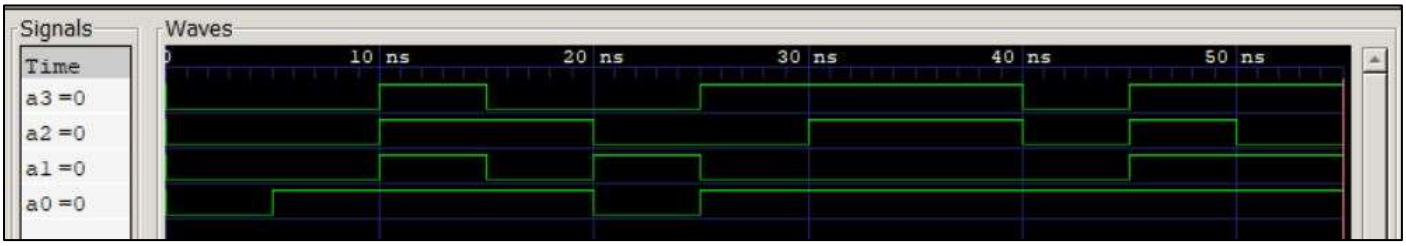
The following is the output obtained and printed in the terminal.

```
time=0 a= 0000 b = 0000, Output = 00000000
time=500 a= 0001 b = 0010, Output = 00000010
time=1000 a= 1111 b = 0100, Output = 00111100
time=1500 a= 0101 b = 0011, Output = 00001111
time=2000 a= 0010 b = 0011, Output = 00000110
time=2500 a= 1001 b = 1001, Output = 01010001
time=3000 a= 1101 b = 1001, Output = 01110101
time=3500 a= 1101 b = 0000, Output = 00000000
time=4000 a= 0001 b = 1001, Output = 00001001
time=4500 a= 1111 b = 1111, Output = 11100001
time=5000 a= 1011 b = 1101, Output = 10001111
time=5500 a= 0000 b = 0000, Output = 00000000
```

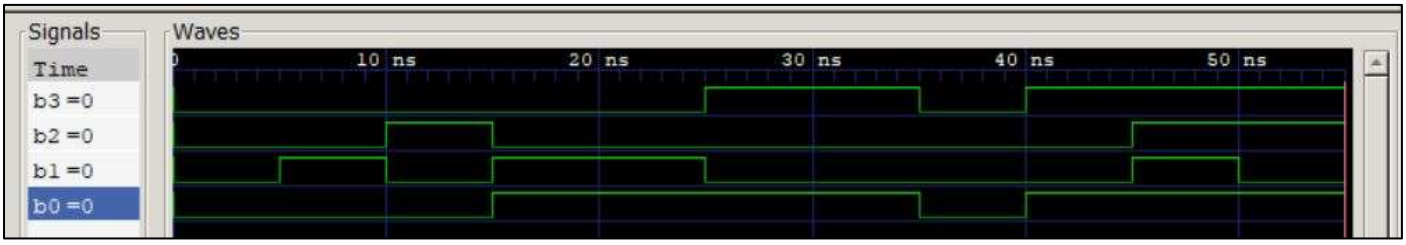
3.4 : GTKwave Output.

The following are the plots of the inputs followed by plots of the output on GTKwave.

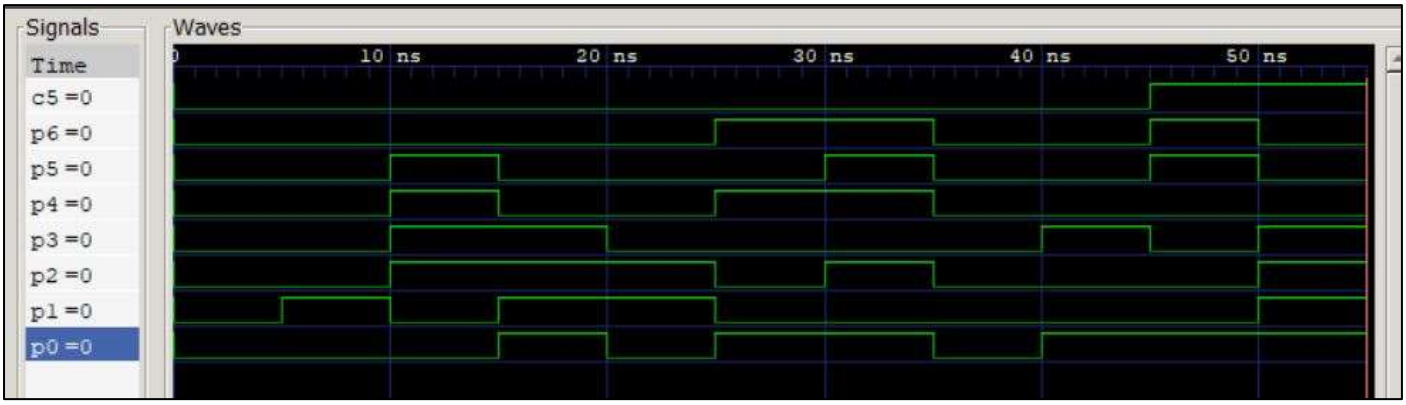
Input A :



Input B :



Output :


Signals
Waves
Time
c5 =0
p6 =0
p5 =0
p4 =0
p3 =0
p2 =0
p1 =0
p0 =0
10 ns
20 ns
30 ns
40 ns
50 ns