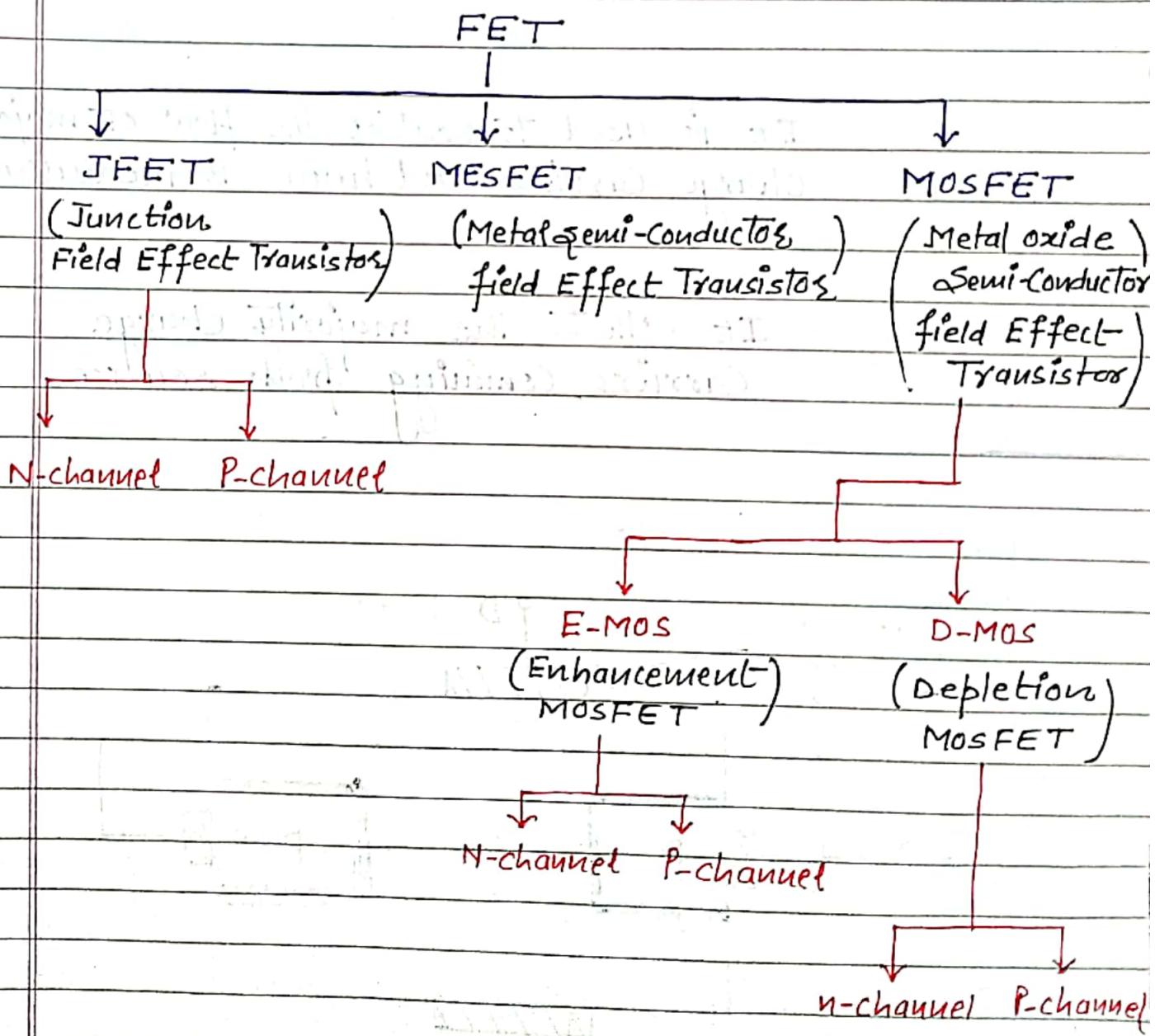


FIELD EFFECT TRANSISTOR

- * FET is a Voltage Controlled device. It is a uni-polar device.
- * It is called as FET b'coz Electric field controls the working.

Classification of FET :-



Terminals of FET :- It is a 3 terminals device.

(1) Source :- source provides majority charge carriers.

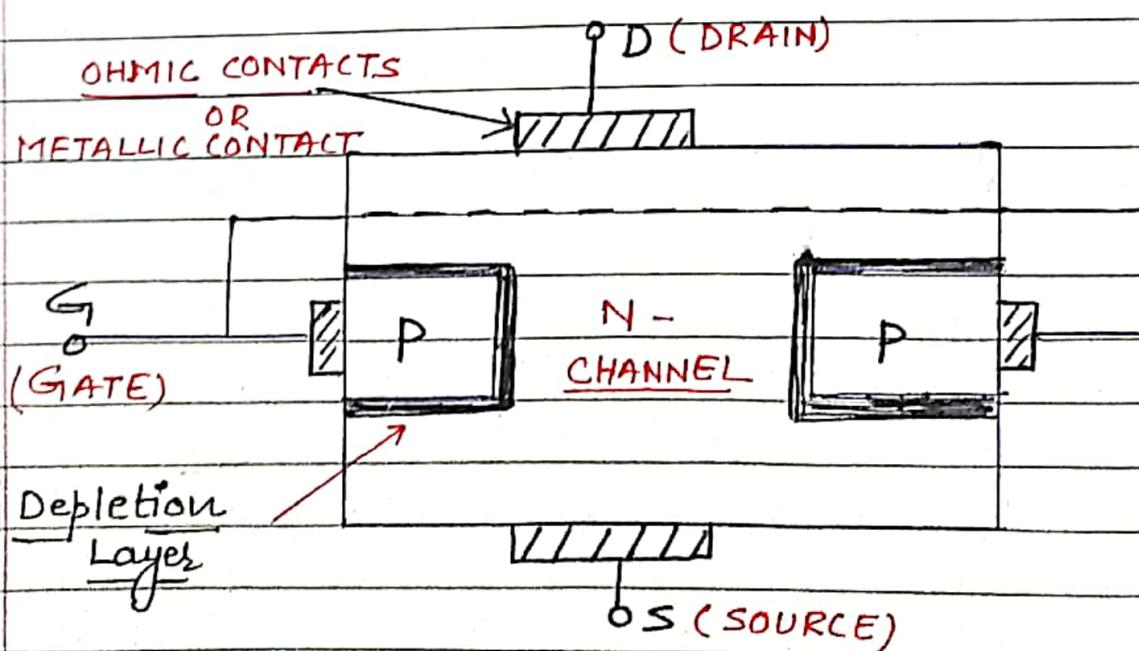
In N-channel → Majority charge carriers are electrons.

In P-channel → Holes are the majority charge carriers.

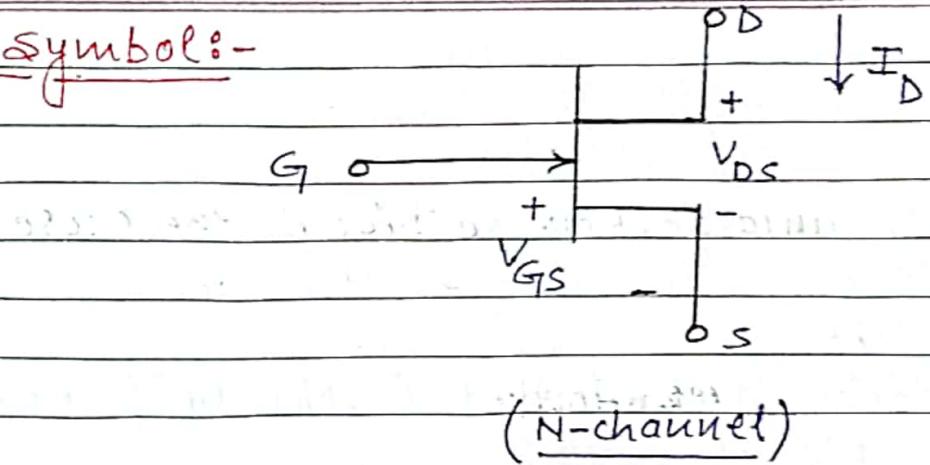
(2) Gate :- It is used to control the flow of majority charge carriers and hence the current.

(3) Drain :- It collects the majority charge carriers, coming from source.

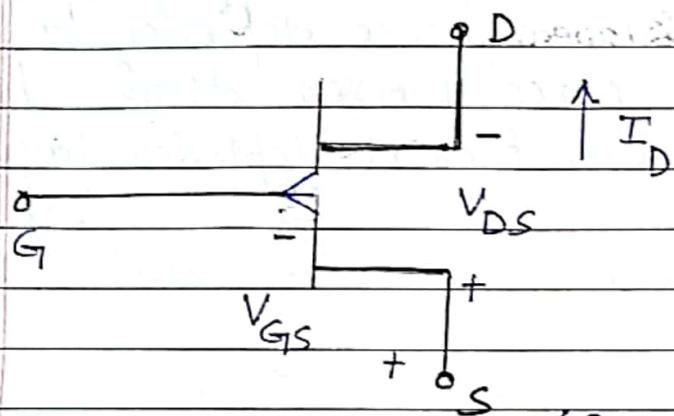
Construction of JFET (n-channel) :-



Symbol :-

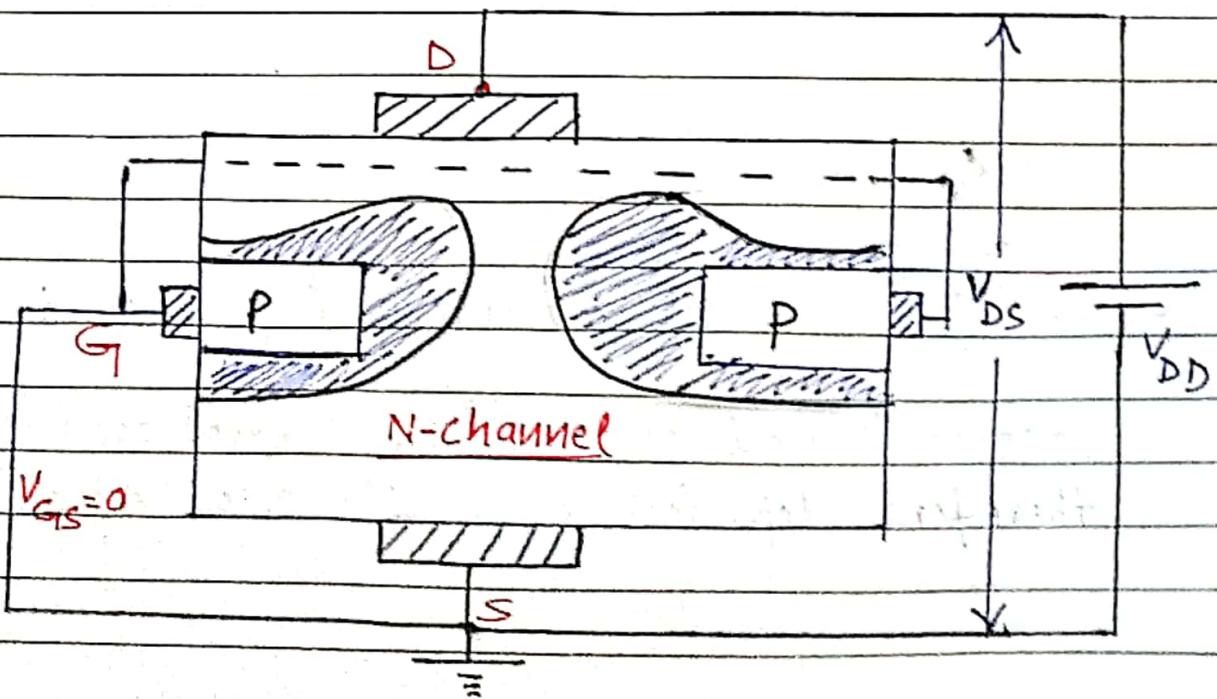


(N-channel)



(P-channel)

WORKING :- CASE 1 :- When $V_{DS} \rightarrow +ve$, $V_{GS} = 0V$



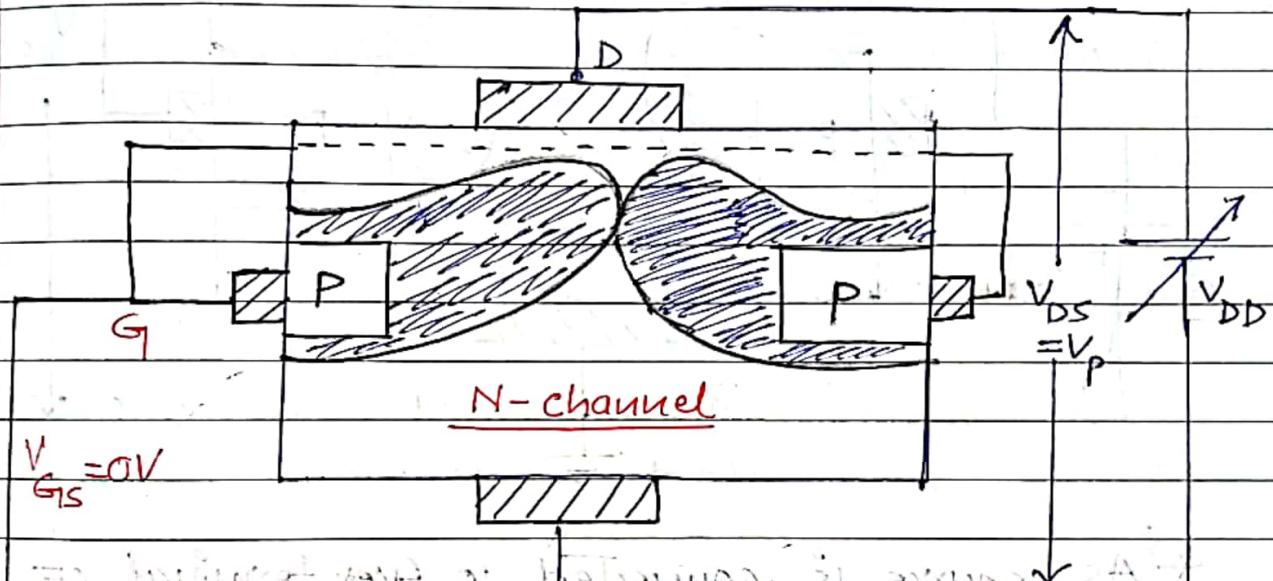


- * source is always Forward biased therefore it is connected to (+ve) terminal of V_{DD} .
- * Drain is always Reverse biased, therefore it is always connected to (-ve) terminal of V_{DD} .
- * The depletion layer formed is Non-uniform, which is kidney shaped. This is because, source is Forward Biased, hence depletion layer is narrow towards source whereas drain being Reverse biased has broader depletion layer.
- * Drain being connected to the terminal of V_{DD} , Exerts Force of attraction on electrons, which are repelled by source.
- * Thus all the electrons from source reach drain and hence

$$I_S = I_D$$
- ② CASE 2 :- When $V_D = V_P$ and $V_{GS} = 0V$
- * As V_D is kept on increasing then the reverse bias at drain also keeps on increasing, therefore depletion layer will also keep on increasing.



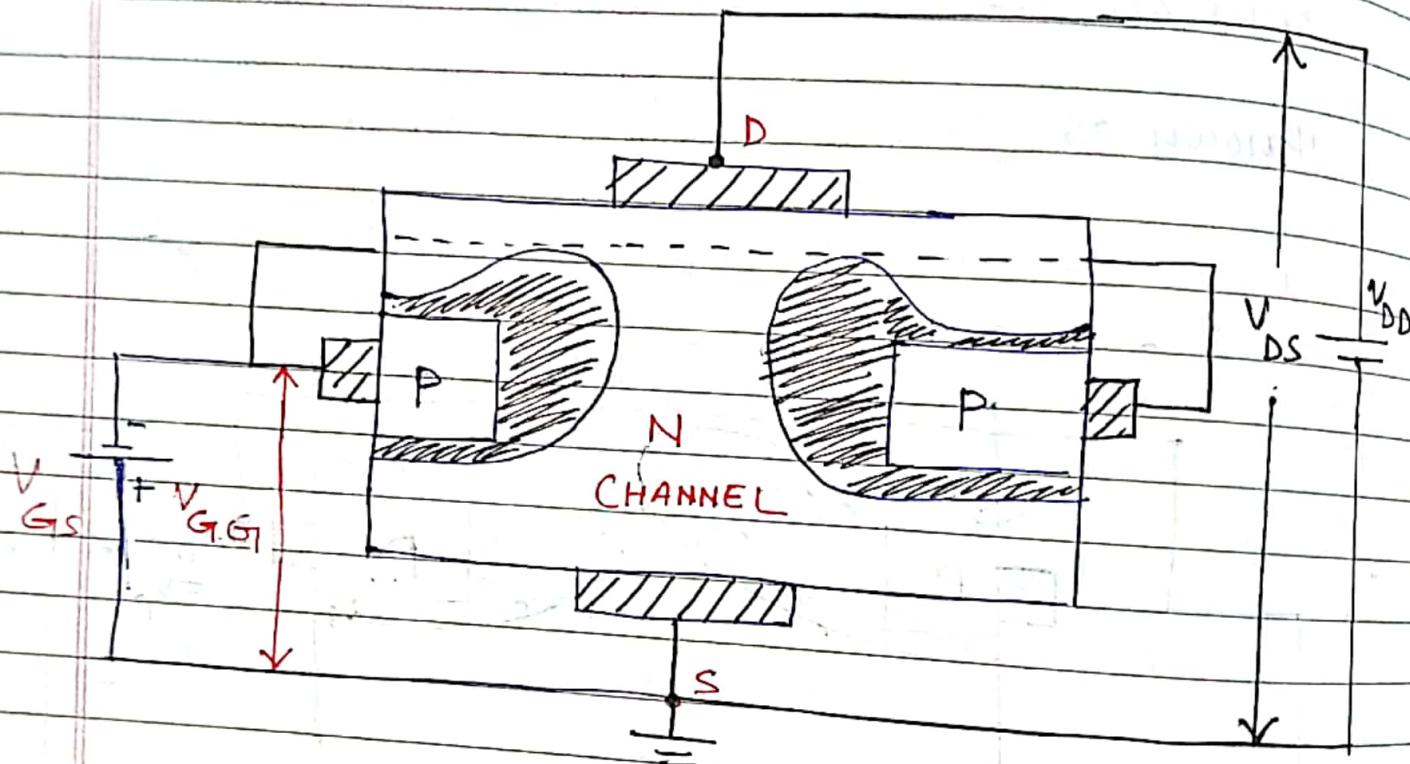
* But at a critical value of V_{DS} , both the depletion layers touch each other. This condition is known as 'PINCH OFF CONDITION' and that value of V_{DS} is known as Pinch off Voltage (V_p).



* As Forward bias on source increases, Force of repulsion on electrons in n-channel also increases therefore electrons in the channel with greater momentum puncture the depletion layer. Hence a very narrow channel with high density and high energy electrons exist and therefore $I_D = I_{DSS}$ flow.

I_{DSS} \rightarrow Drain to source saturation current.

3. Case-III: - When V_{DS} is (+ve) and V_{GS} is < 0 volt



* As source is connected to (+ve) terminal of V_{DD} , therefore it exerts a Force of repulsion on electrons whereas source is also connected to (+ve) terminal of battery V_{GS} , it exerts a Force of attraction on electrons. Due to this phenomenon, no. of electrons flowing in the channel decreases and therefore the current I_D also decreases.

As we keep on increasing the voltage V_{GS} ,

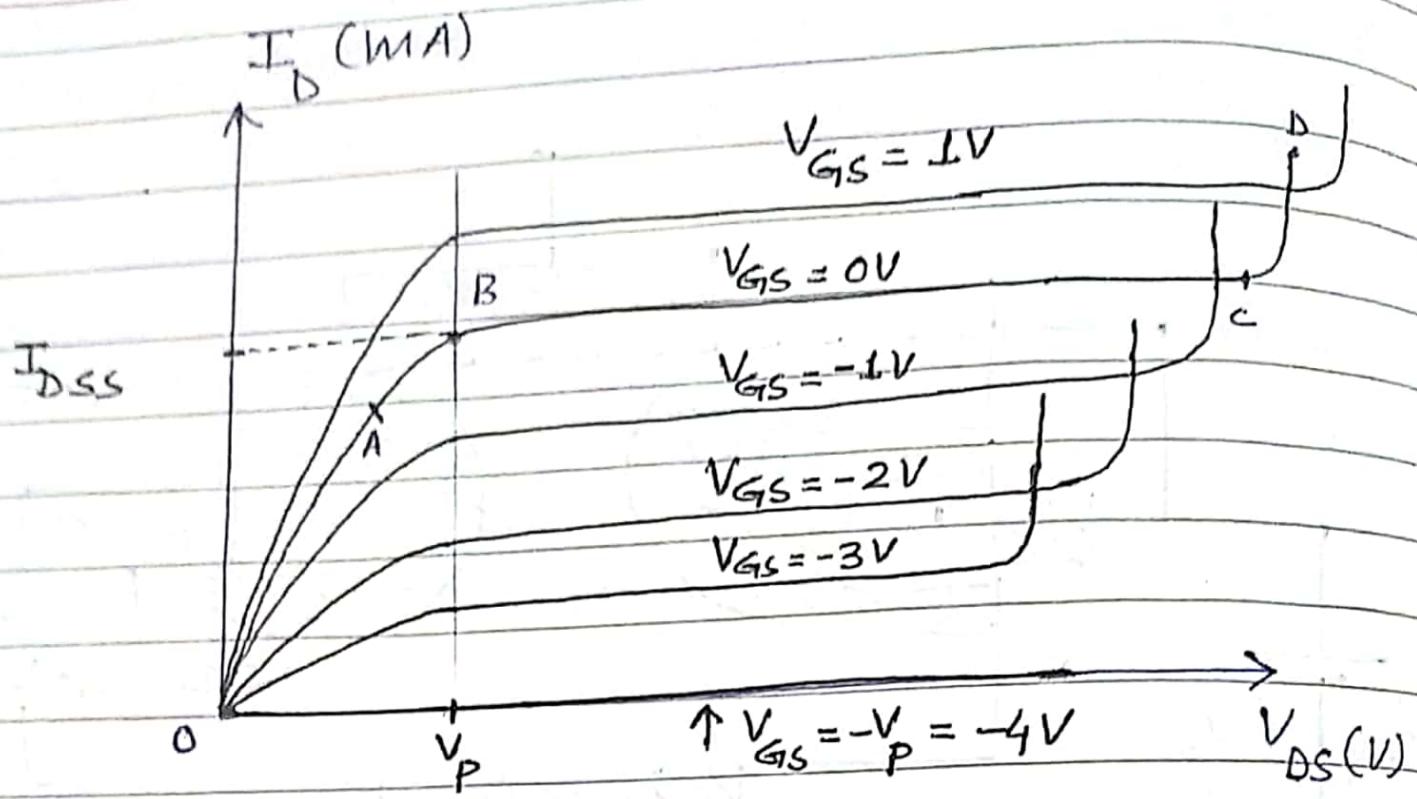
a point will come where at $V_{GS} = -V_P$,

Force of Attraction = Force of Repulsion on electrons

At this stage, No electrons flow in the channel

and Hence $I_D = 0$.

DRAIN CHARACTERISTICS OF JFET :-



Drain characteristics are drawn between o/p voltage V_{DS} and o/p current I_D , keeping input voltage V_{GS} constant.



(1) $V_{GS} = 0$:- At $V_{GS} = 0$ volt, maximum current I_{DSS} flows.

(2) $V_{GS} < 0$:- When $V_{GS} < 0$ volt, there will be

simultaneously Force of attraction and Force of repulsion on electrons therefore no. of electrons in the channel decreases and hence I_D also decreases.

(3) $V_{GS} > 0$ volt :- When $V_{GS} > 0$ volt, Force of

Repulsion on electrons increases and hence more no. of electrons with higher momentum flow in the channel, therefore I_D increases.

* Each Curve can be divided into 3 Regions:-

(1) Region OA :- In this region, as voltage varies, current also varies and hence JFET follows ohm's law, and this region is known as ohmic Region.

As the resistance of JFET varies with the applied voltage, therefore in ohmic region JFET behaves like a VVR (Voltage Variable Resistance).

② Region AB :- In this region, Current I_D increases at the reverse square law rate with respect to V_{DS} .

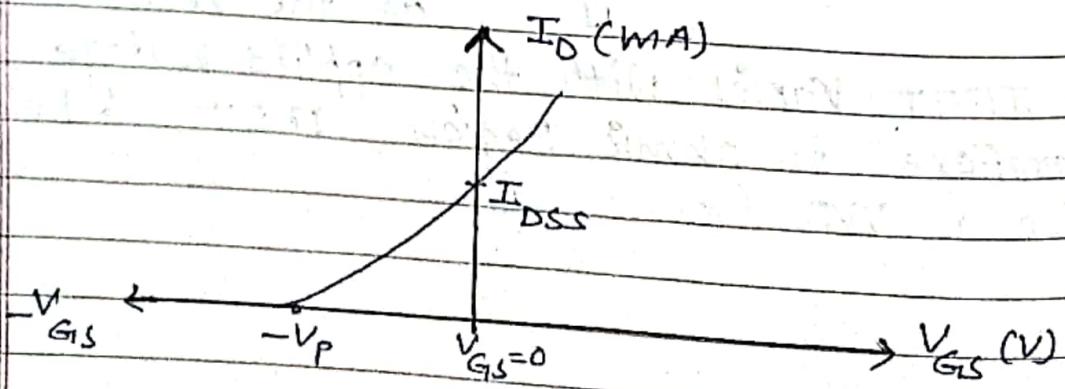
③ Region BC :- After V_P , Even when V_{DS} keeps on increasing, then also I_D remains constant. Hence this region is known as Saturation Region.

* In this region, JFET behaves like a constant current source.

④ Region CD :- In this region, I_D increases exponentially w.r.t V_{DS} and may lead to breakdown of JFET.

This region is known as Breakdown Region.

Transfer characteristics :-



① This Curve is plotted between I_D and V_{GS} , keeping $V_{DS} \rightarrow 0$ constant.

② At $V_{GS} = 0$:- At $V_{GS} = 0$ volt, current I_{DSS} flows at $V_{DS} = V_P$.

then

③ $V_{GS} < 0$ volt :- When $V_{GS} < 0$ volt, there will be

simultaneous Force of attraction and Force of repulsion on electrons, therefore current I_{DSS}

decreases.

When $V_{GS} = -V_P$, current $I_D = 0$

b'coz at $V_{GS} = -V_P$, Force of Attraction = Force of Repulsion

④ $V_{GS} > 0$ volt :- When $V_{GS} > 0$, the no. of electrons in the channel increases, therefore current I_D also increases.

JFET Parameters :-

JFET Follows Shockley's

Equation.

$$I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_P} \right]^2$$

Where

I_D = Drain Current in mA

I_{DSS} = Drain to source saturation current

V_{GS} = Gate to source Voltage

V_P = Pinch off Voltage

① Transconductance (g_m) :- It is defined as the ratio of

Change in drain current I_D to the change in V_{GS} , keeping $V_{DS} \rightarrow$ constant.

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} \quad \boxed{V_{DS} \rightarrow \text{constant}}$$

It is also known as Mutual Conductance.

Unit: mA/V or mili siemens

Q) Prove

$$g_m = g_{m0} \left[1 - \frac{V_{GS}}{V_{GS(\text{off})}} \right]$$

Where

g_{m0} \rightarrow Value of Transconductance for $V_{GS} = 0V$

$$g_{m0} = -2 \frac{I_{DSS}}{V_P}$$

$\rightarrow V_{GS(\text{off})}$ is the value of V_{GS} for which drain current $I_D = 0\text{mA}$ and is usually greater than and equal to pinch off voltage V_P .

Proof:- We know $I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_P} \right]^2 \rightarrow ①$

Differentiating Eqⁿ ① w.r.t V_{GS} .

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} = -2 \frac{I_{DSS}}{V_P} \left[1 - \frac{V_{GS}}{V_P} \right] \rightarrow ②$$

\rightarrow putting $V_{GS} = 0$ in above eqⁿ; g_m becomes g_{m0}

$$\text{Hence } g_{mo} = -\frac{2I_{DSS}}{V_P}$$

∴ Therefore Eqⁿ ② becomes:-

$$g_m = g_{mo} \left[1 - \frac{V_{GS}}{V_P} \right]$$

→ At the place of V_P , $V_{GS(\text{OFF})}$ is placed,

Assuming JFET current is zero.

$$g_m = g_{mo} \left[1 - \frac{V_{GS}}{V_{GS(\text{OFF})}} \right]$$

② Ac Drain Resistance :- (r_d)

* It is defined as the ratio of change in V_{DS} to change in I_D , keeping $V_{GS} \rightarrow \text{constant}$.

$$r_d = \frac{\Delta V_{DS}}{\Delta I_D} \quad \left| V_{GS} \rightarrow \text{constant} \right.$$

It is also known as Dynamic Drain Resistance.



③ Amplification Factor (μ) :-

$$\mu = \frac{\Delta V_{DS} \text{ (output)}}{\Delta V_{GS} \text{ (Input)}}$$

④ Input Resistance (r_i) :-

$$r_i = \frac{V_{GS}}{I_{GSS}}$$

Where

$I_{GSS} \rightarrow$ Gate reverse current in nano ampere.

? $r_i \approx 10^9$ Since r_i is very high :-

JFET is preferred as amplifiers.

⑤ DC Drain Resistance :-

$$R_D = \frac{V_{DS}}{I_D}$$

Relation Between μ , r_d and g_m :-

We know

$$\mu = \frac{\Delta V_{DS}}{\Delta I_D}$$

$$\Delta V_{GS}$$

Multiply & divide by ΔI_D :-

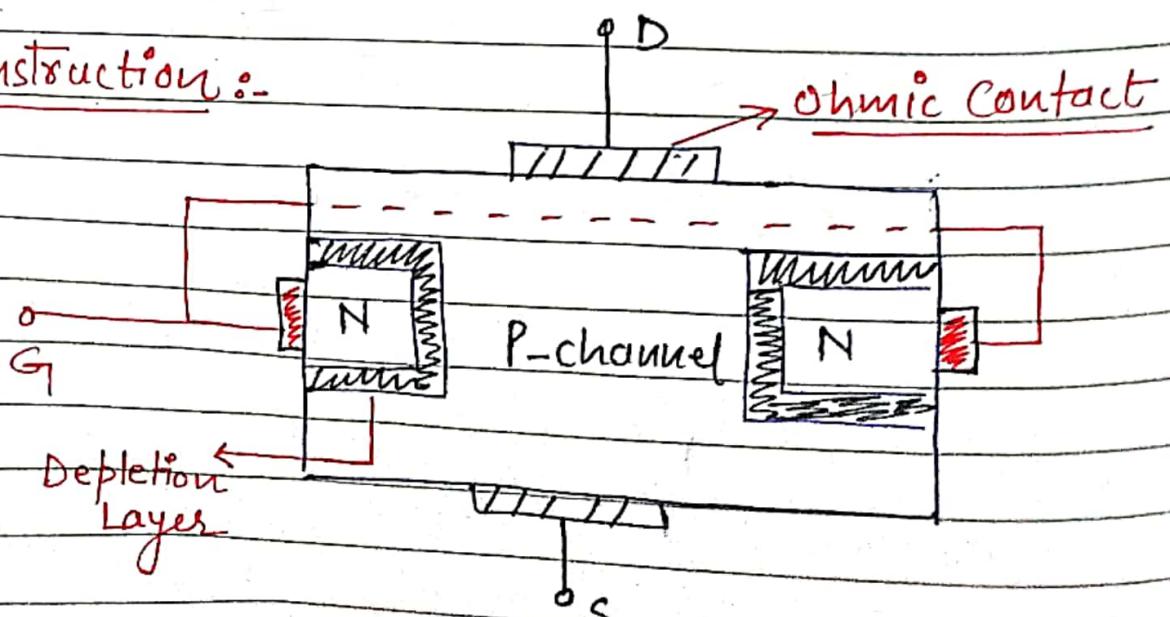
$$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}} \times \frac{\Delta I_D}{\Delta I_D}$$

$$= \frac{\Delta V_{DS}}{\Delta I_D} \times \frac{\Delta I_D}{\Delta V_{GS}}$$

$$\boxed{\mu = r_d \times g_m}$$

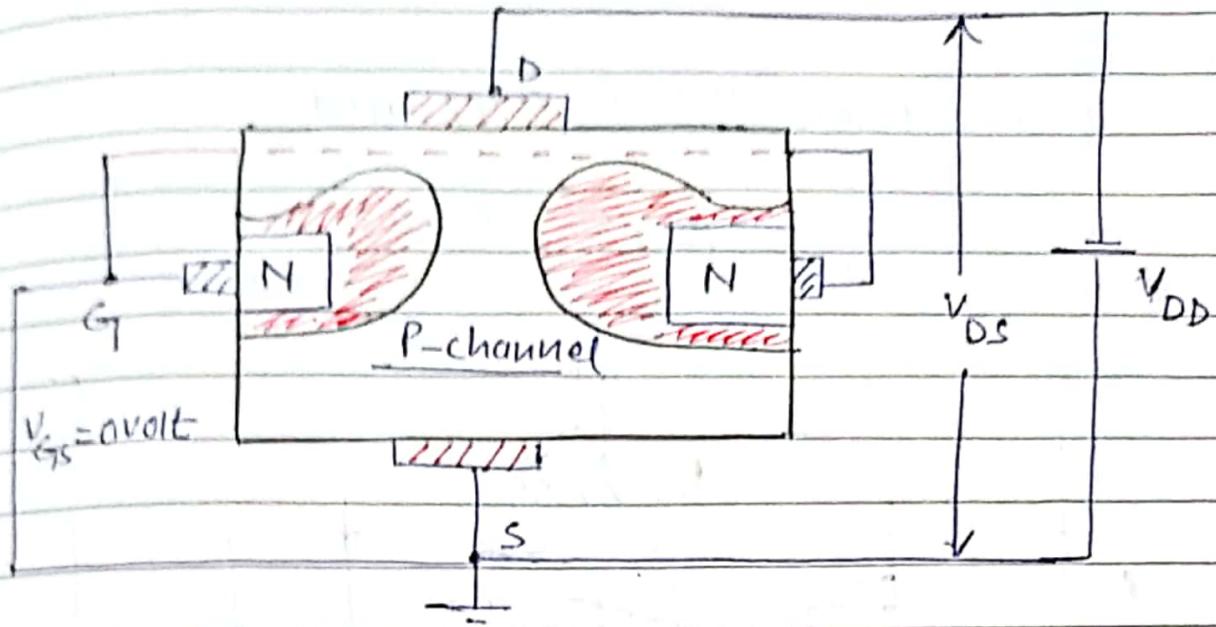
P-channel JFET :-

Construction :-



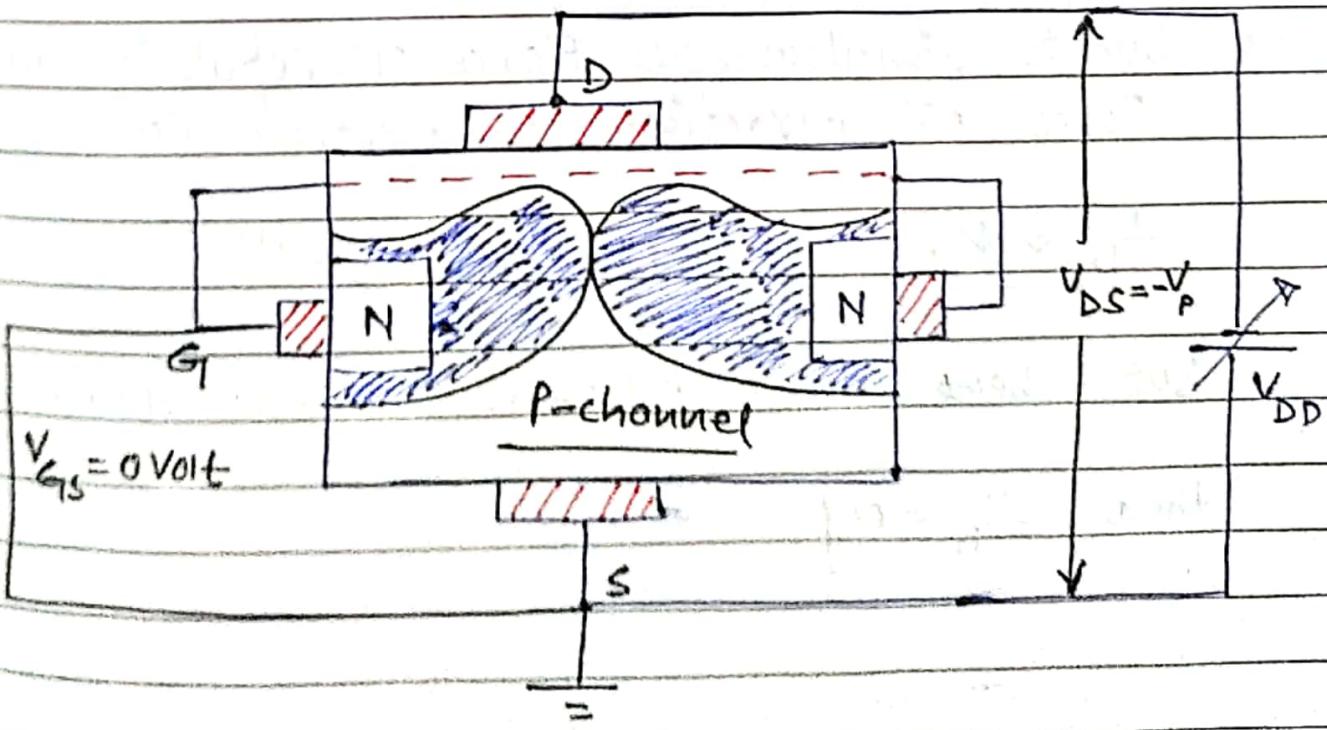
WORKING :-

① Case 1: When $V_{DS} = 0$ (-ve) and $V_{GS} = 0$ Volt.



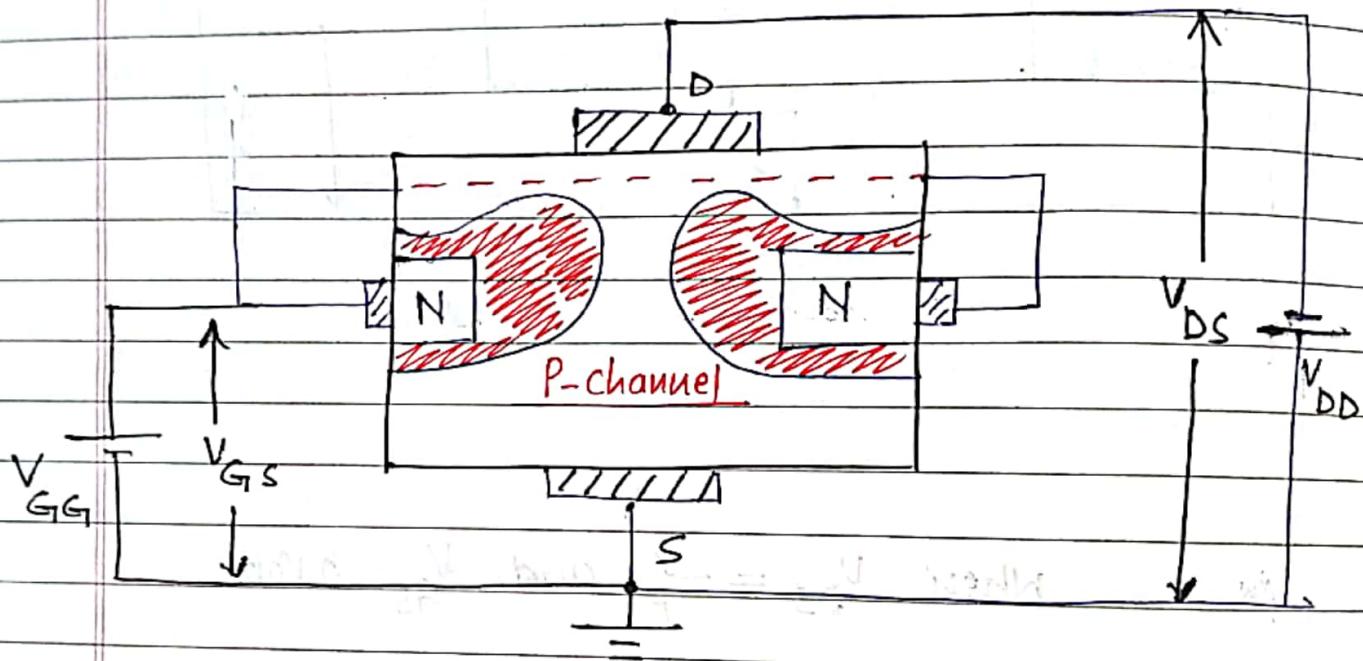
$$I_S = I_D$$

② Case 2: When $V_{DS} = -V_p$ and $V_{GS} = 0$ Volt



$$I_D = I_{DSS}$$

③ Case 3 :- When V_{DS} is (ve) and V_{GS} is > 0 volt.



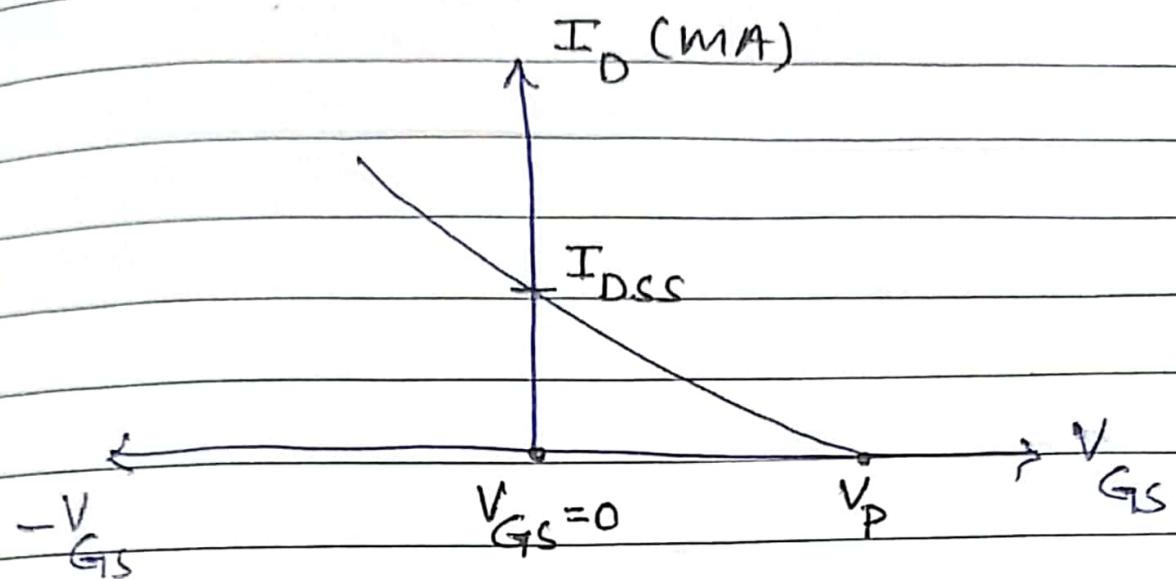
→ Due to simultaneous Force of repulsion and Force of attraction on electrons current

I_D ↓ ↓. But when $V_{GS} = +V_P$

Force of Repulsion = Force of attraction

then $I_D = 0$

Transfer characteristics :- (p -channel)

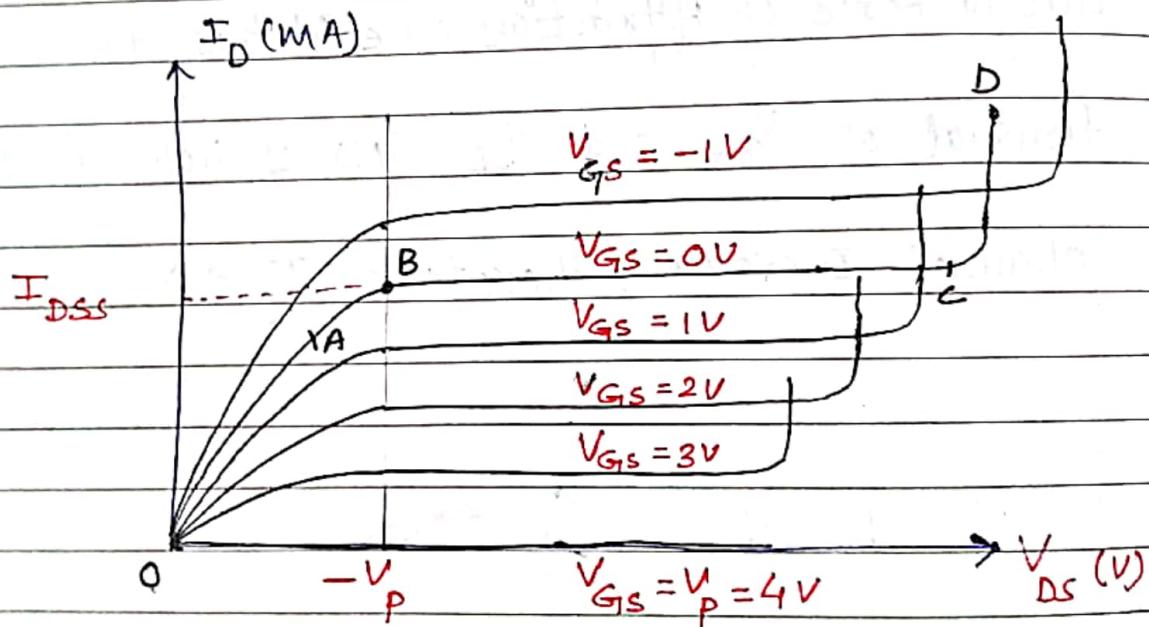


① When $V_{GS} = 0$:- When $V_{GS} = 0$, $I_D = I_{DSS}$

② When $V_{GS} > 0$:- As V_{GS} keep on increasing,
 $I_D \downarrow \downarrow$ but when $V_{GS} = V_P$, $I_D = 0$

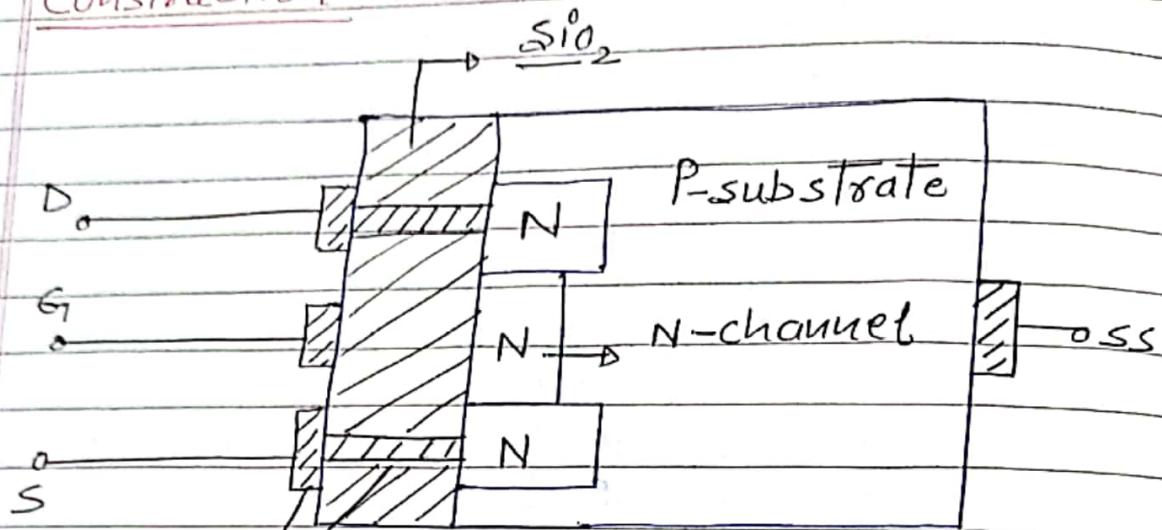
③ When $V_{GS} < 0$:- When $V_{GS} < 0$, $I_D \uparrow \uparrow$.

DRAIN Characteristics :-

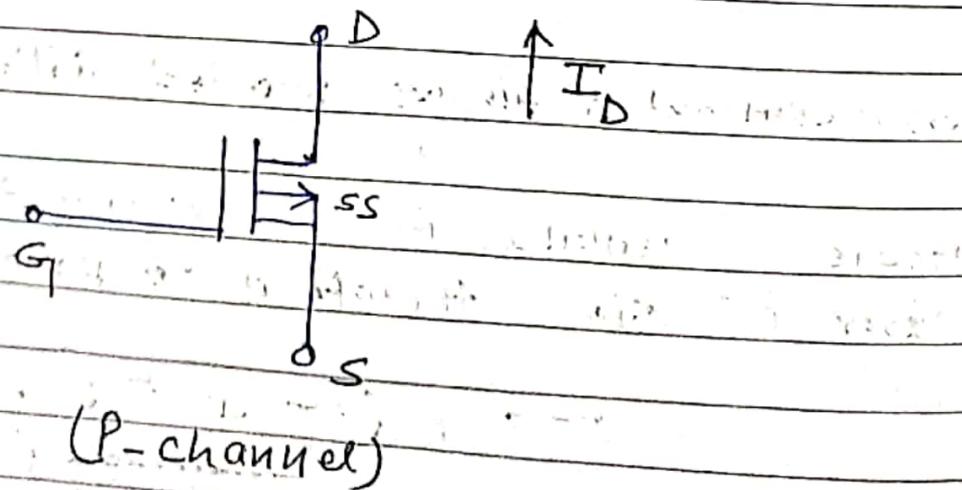
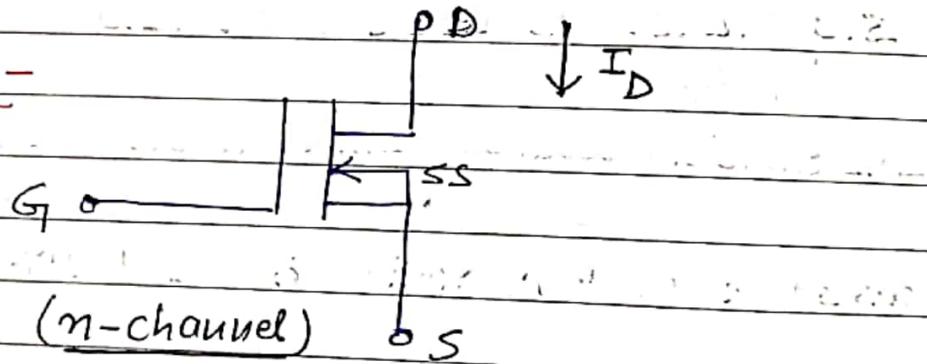


Depletion - MOSFET (D-MOS) :-

Construction :-



Symbol :-





Notes:- (1) Source is always Forward biased.

(2) Drain is always Reverse biased.

(3) In N-channel D-MOS, majority charge carriers are electrons.

(4) In P-channel, Holes are the majority charge carriers.

(5) In N-channel D-MOS, source and drain both are N-type whereas in P-channel, both are p-type.

* SiO_2 layer is used b'coz SiO_2 is a very good

Insulator which gives a very high input

Resistance of MOSFET, hence MOSFET can be used

as an Amplifier.

* SS terminal is always shorted with Source.

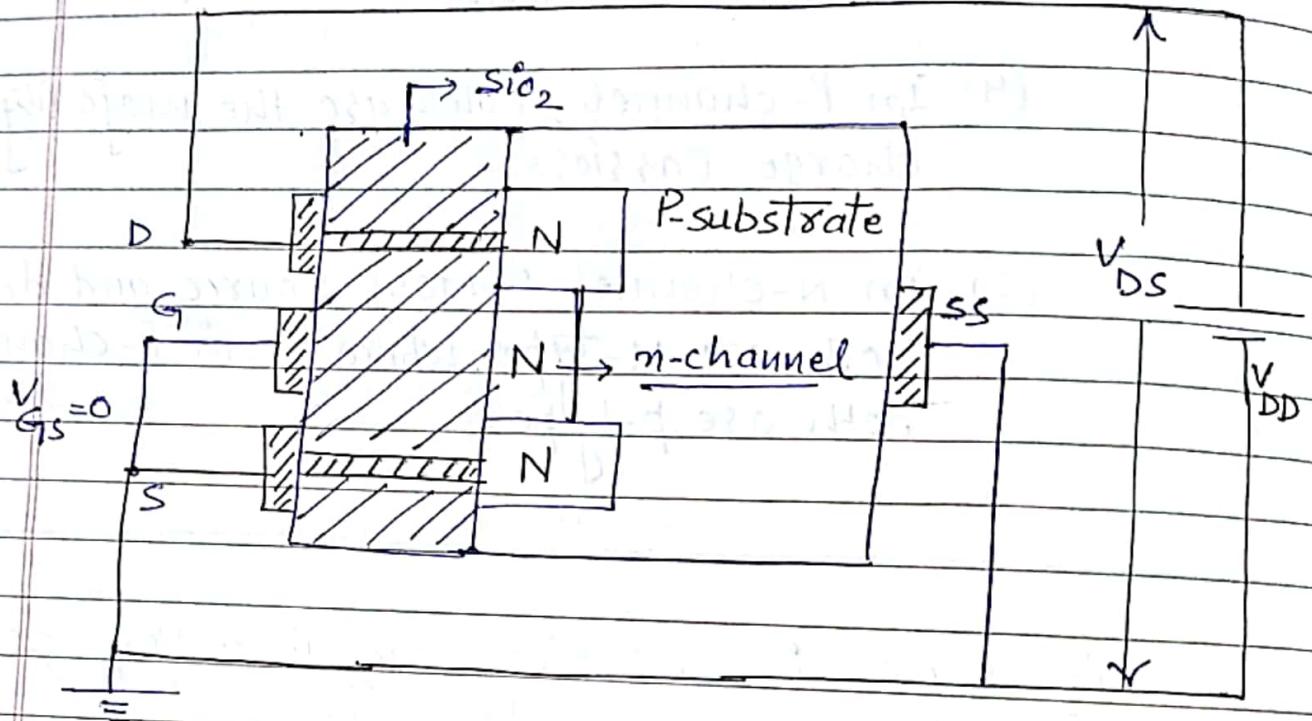
* Gate is isolated from N-channel by a very thin layer of SiO_2 , therefore MOSFET is also

known as IGFET (Insulated Gate Field Effect Transistor).

WORKING :-

CASE 1 :-

When $V_{DS} \rightarrow +ve$ and $V_{GS} = 0$ Volt



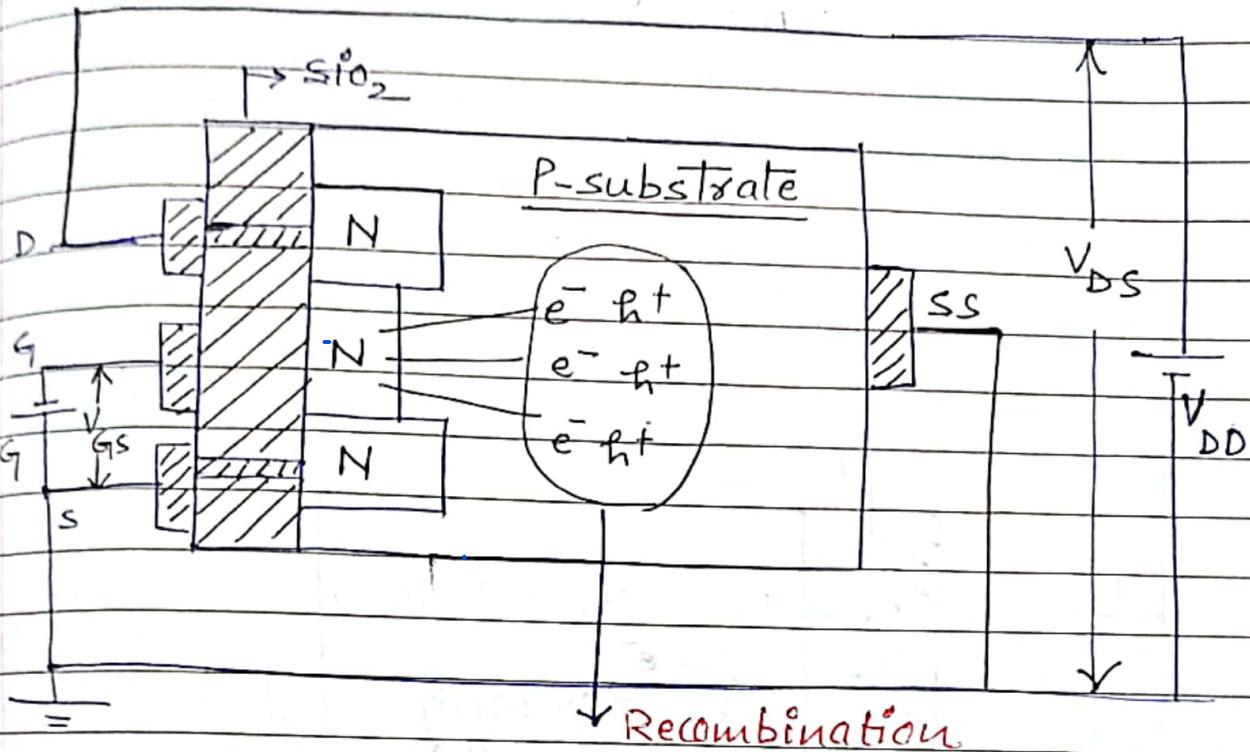
* As source is connected to the (-ve) terminal of battery V_{DD} , so there will be a Force of

Repulsion on electrons in N-tub and drain is connected to the (+ve) terminal of V_{DD} , so there will be a Force of attraction on electrons therefore all the electrons from

source reach drain via N-channel Hence -

$$I_S = I_D = I_{DSS}$$

Case-II :-

When $V_{DS} = +ve$ and $V_{GS} < 0$ volt

* As Gate is connected to (+ve) terminal of battery V_{GG} , therefore (-ve) potential at gate will repel the electrons from N-channel and will attract the holes from p-substrate.

* This will lead to recombination and no. of electrons in channel will also get reduced, Hence I_d decreases.

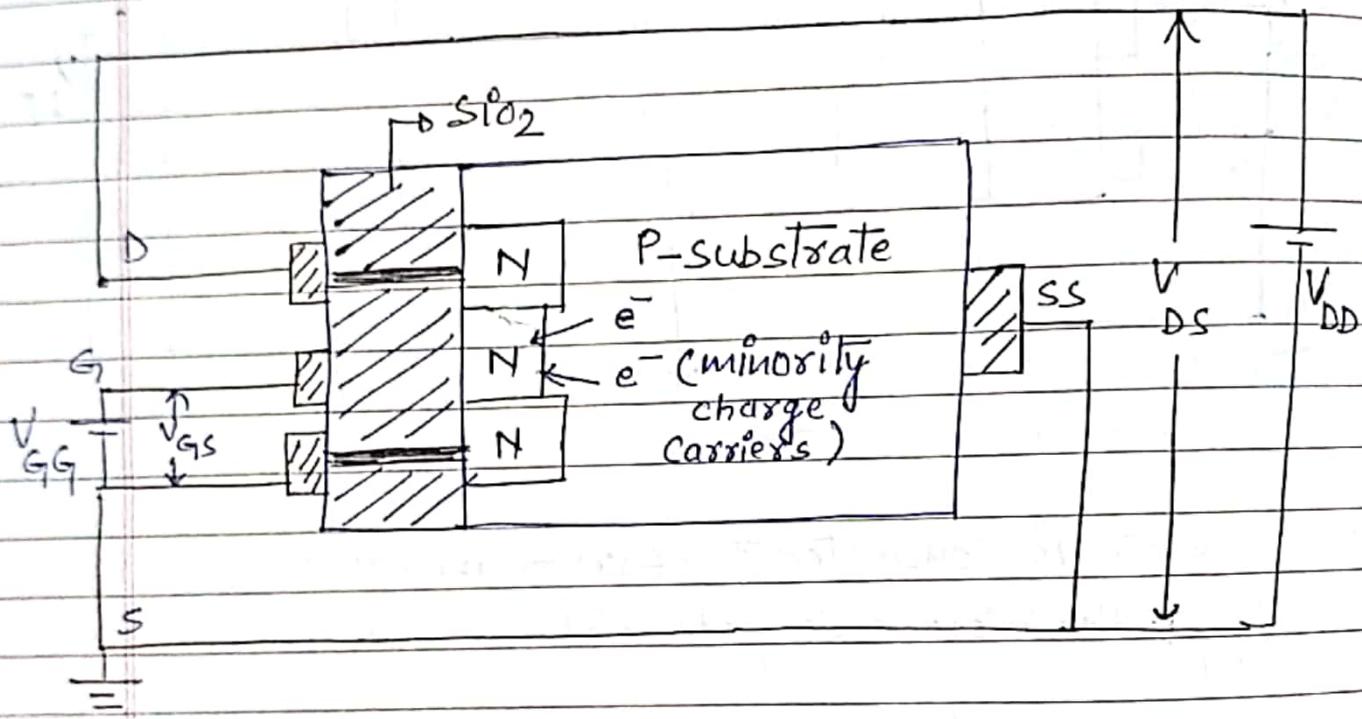
* But when $V_{GS} = -V_p$, all the electrons will be repelled from channel and there will be no electron

present in the channel therefore -

$$I_D = 0$$

CASE-III :-

When $V_{DS} = +Ve$ and $V_{GS} > 0$



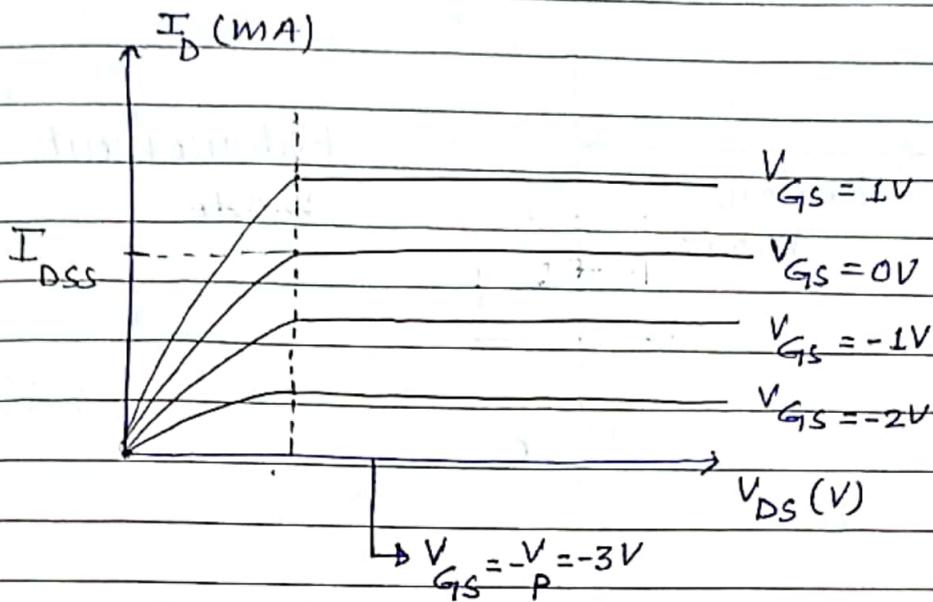
* As Gate is connected to (+ve) terminal of V_{GS} ,

a (+ve) potential at gate will attract the

minority electrons from p-substrate. Therefore
the no. of electrons in the channel increases

Hence Current I_D also increases -

Drain characteristics :- (n -channel D-MOS)



(1) These curves are drawn between V_{DS} and I_D , keeping V_{GS} constant

(2) $V_{GS} = 0V$:- When $V_{GS} = 0$ volt, we get $I_D = I_{DSS}$

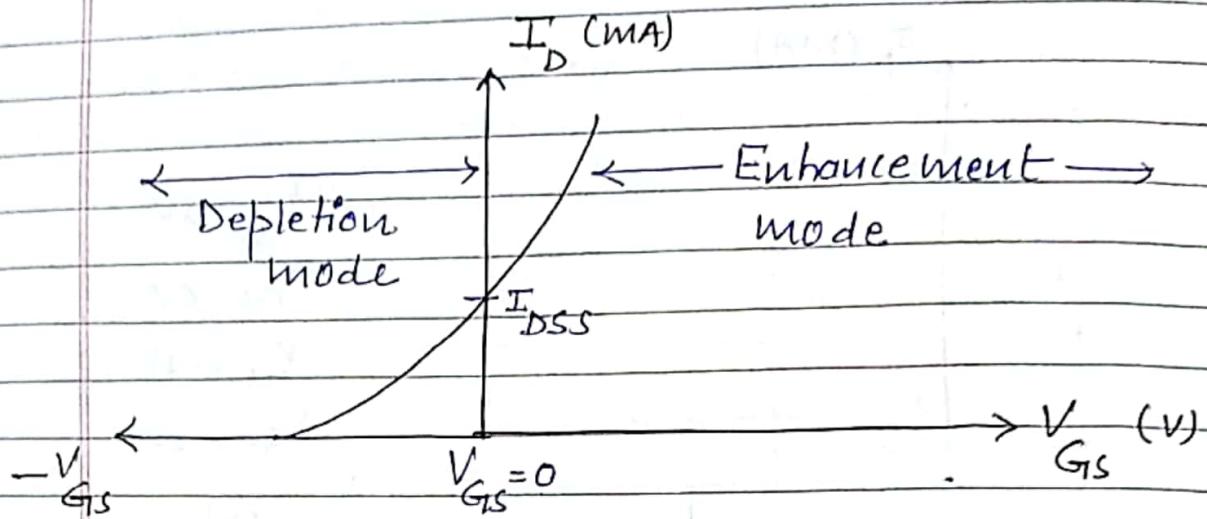
(3) $V_{GS} < 0V$:- As $V_{GS} < 0$, no of electrons in the channel reduces therefore I_D decreases, but when

(4) $V_{GS} > 0$ volt :- $V_{GS} = -\frac{V}{P}$, Current $I_D = 0$ mA

When $V_{GS} > 0$, a (+ve) potential V_G at gate attracts the minority electrons from p-substrate into the channel.

Therefore the no. of electrons in the channel increases, hence I_D increases.

Transfer characteristics :-



* These characteristics are plotted between drain current I_D and V_{GS} , keeping V_{DS} constant.

1. $V_{GS} = 0 \text{ V}$:- When $V_{GS} = 0 \text{ V}$, all the electrons

from source reach drain, therefore we get

$$I_D = I_{DSS}$$

2. $V_{GS} < 0 \text{ V}$:- When $V_{GS} < 0$, no of electrons in

the channel reduces, therefore I_D reduces and
MOSFET is said to be operated in Depletion Mode.

but when $V_{GS} = -V_F$, no free electron is present
in the channel and therefore $I_D = 0$.

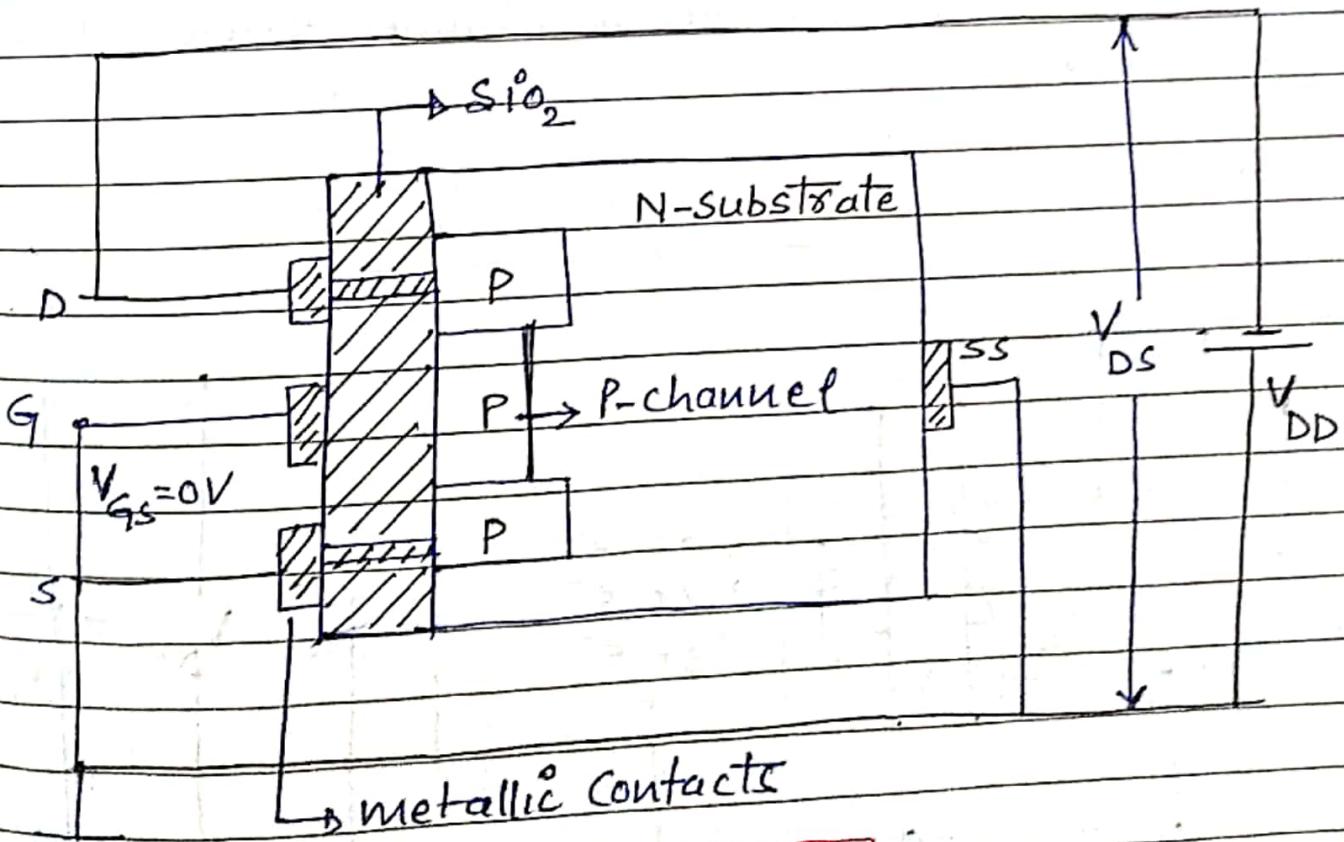
3. $V_{GS} > 0$:- When $V_{GS} > 0$, no. of electrons in the channel increases b'coz a (+ve) potential at gate attracts the minority electrons from p-Substrate into the channel, therefore current I_D increases and D-MOS is said to be operated in Enhancement Mode.

P-Channel D-MOS

Working :-

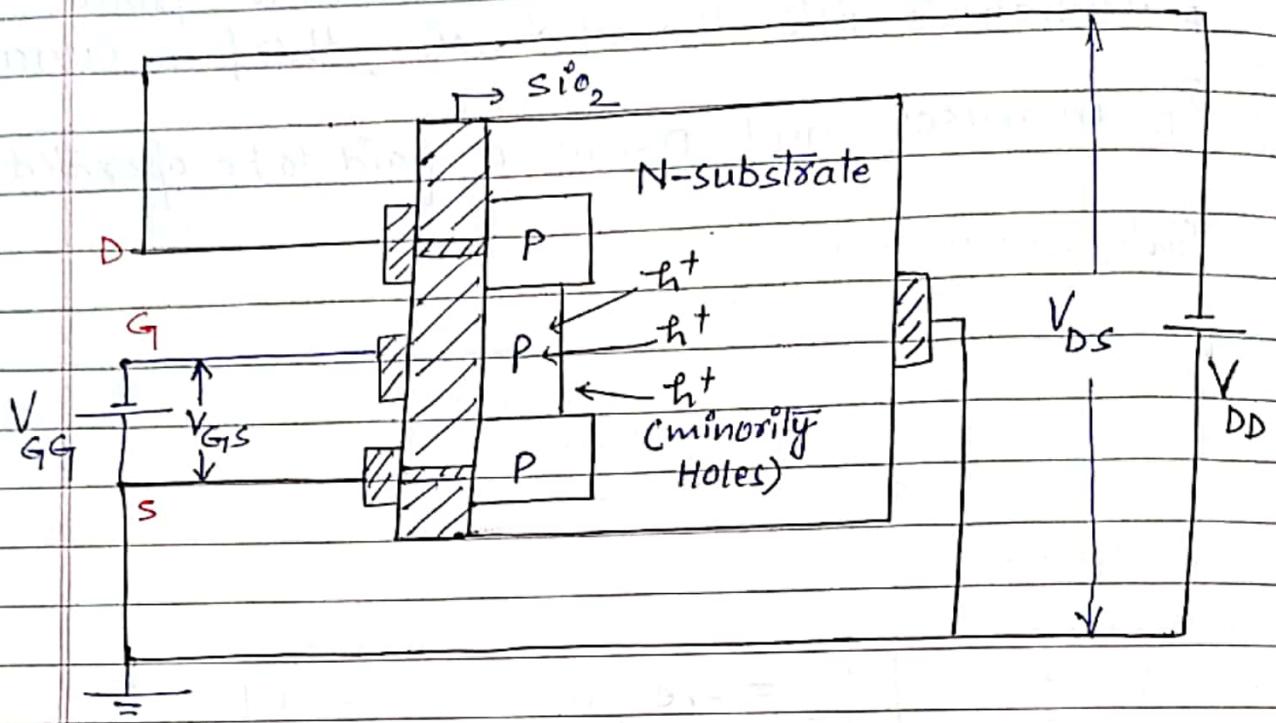
1. CASE 1 :-

$$V_{DS} = -\text{ve} \text{ and } V_{GS} = 0V$$



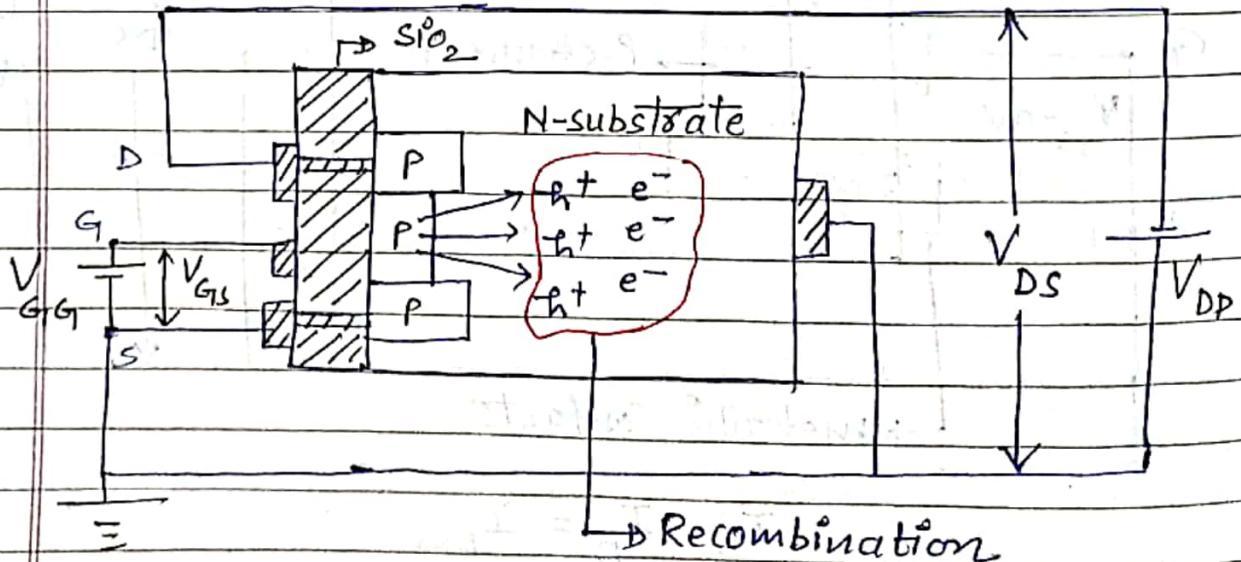
$$I_S = I_D = I_{DSS}$$

2. CASE 2 :- $V_{DS} = -V_e$ and $V_{GS} < 0V$



* NO. OF Holes $\uparrow\uparrow$ in the channel, therefore $I_D \uparrow\uparrow$.

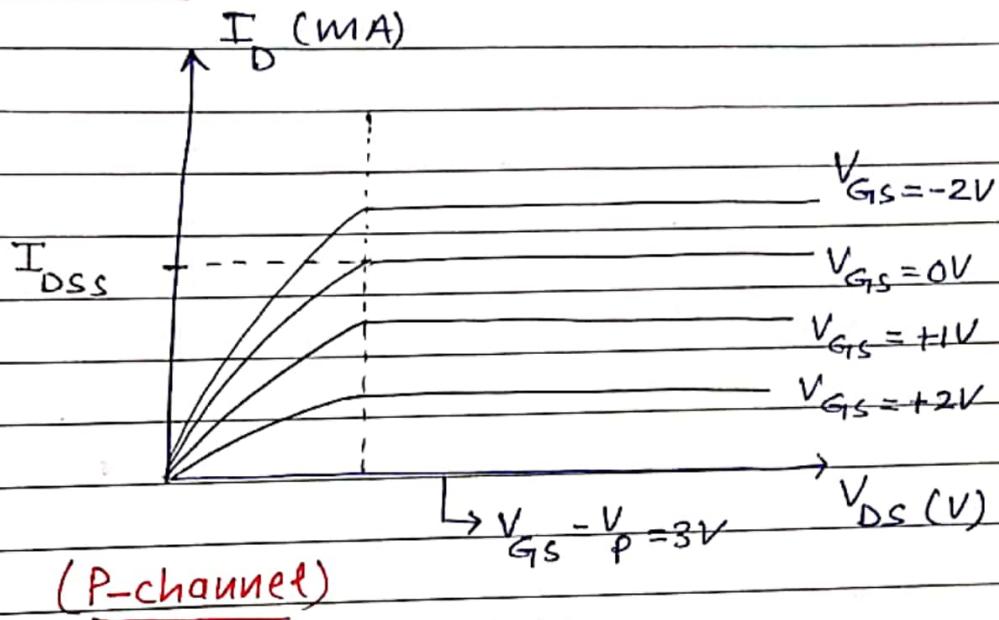
3. CASE-III :- $V_{DS} = -V_e$ and $V_{GS} > 0V$



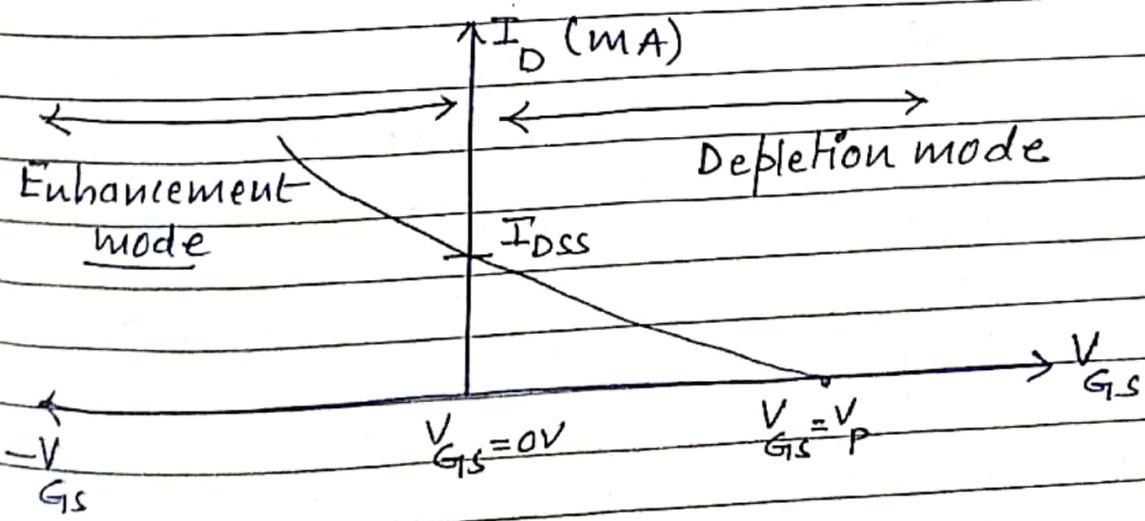
* NO. OF holes in the channel $\downarrow \downarrow$, therefore $I_D \downarrow \downarrow$

but when $V_{GS} = V_P$, no holes is present in the channel,
hence $I_D = 0 \text{ mA}$.

Drain characteristics :-



Transfer characteristics :-



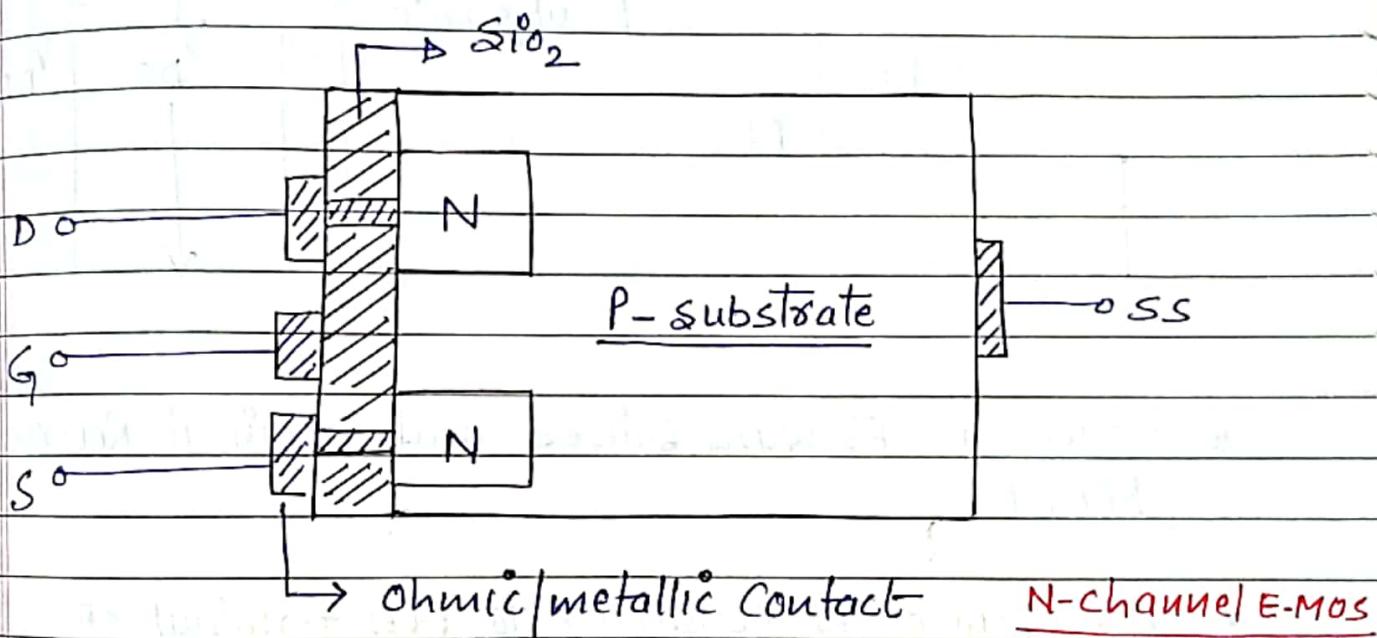


E-MOS (Enhancement MOSFET)

Construction :- The basic constructional difference between D-Mos and E-Mos is that there is the absence of conducting channel between drain and source in E-Mos.

In E-Mos, channel is

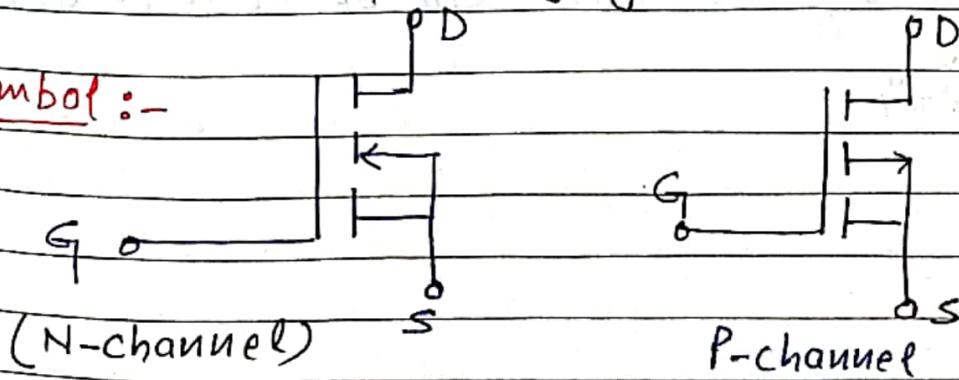
induced.



* There is no channel between drain and source.

* SiO_2 is used to provide very high input resistance to MOSFET, as it is a very good insulator.

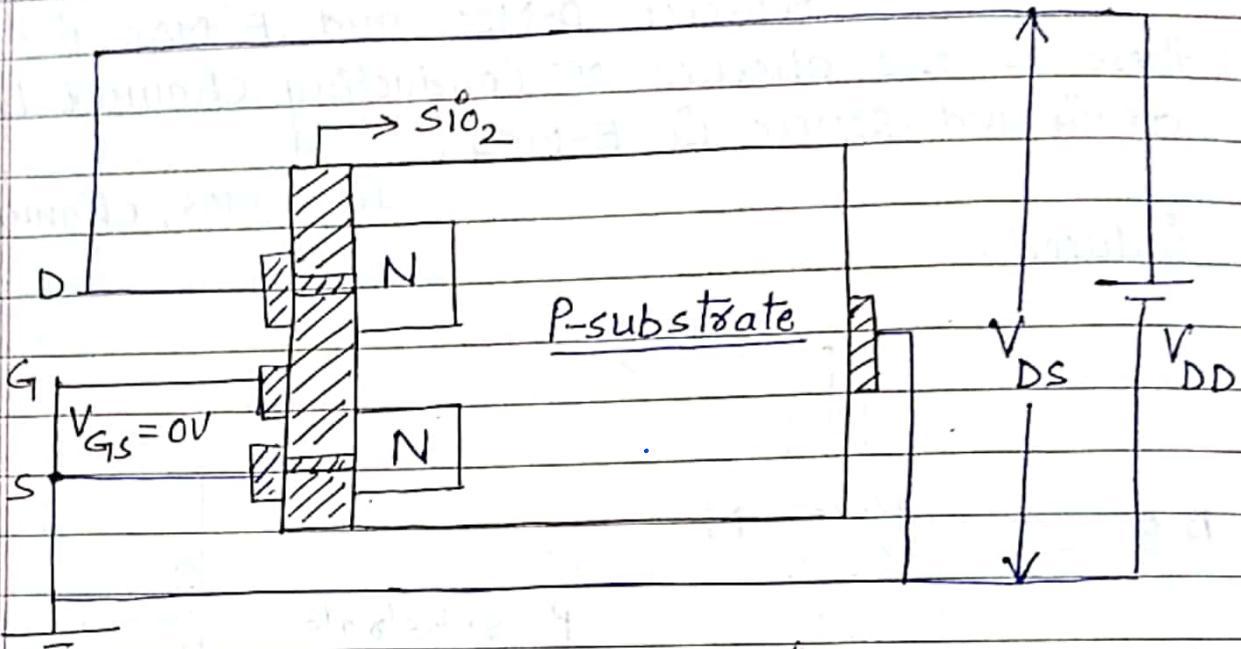
Symbol :-



WORKING :-

1. CASE-I

$$V_{DS} = +Ve \text{ and } V_{GS} = 0V$$

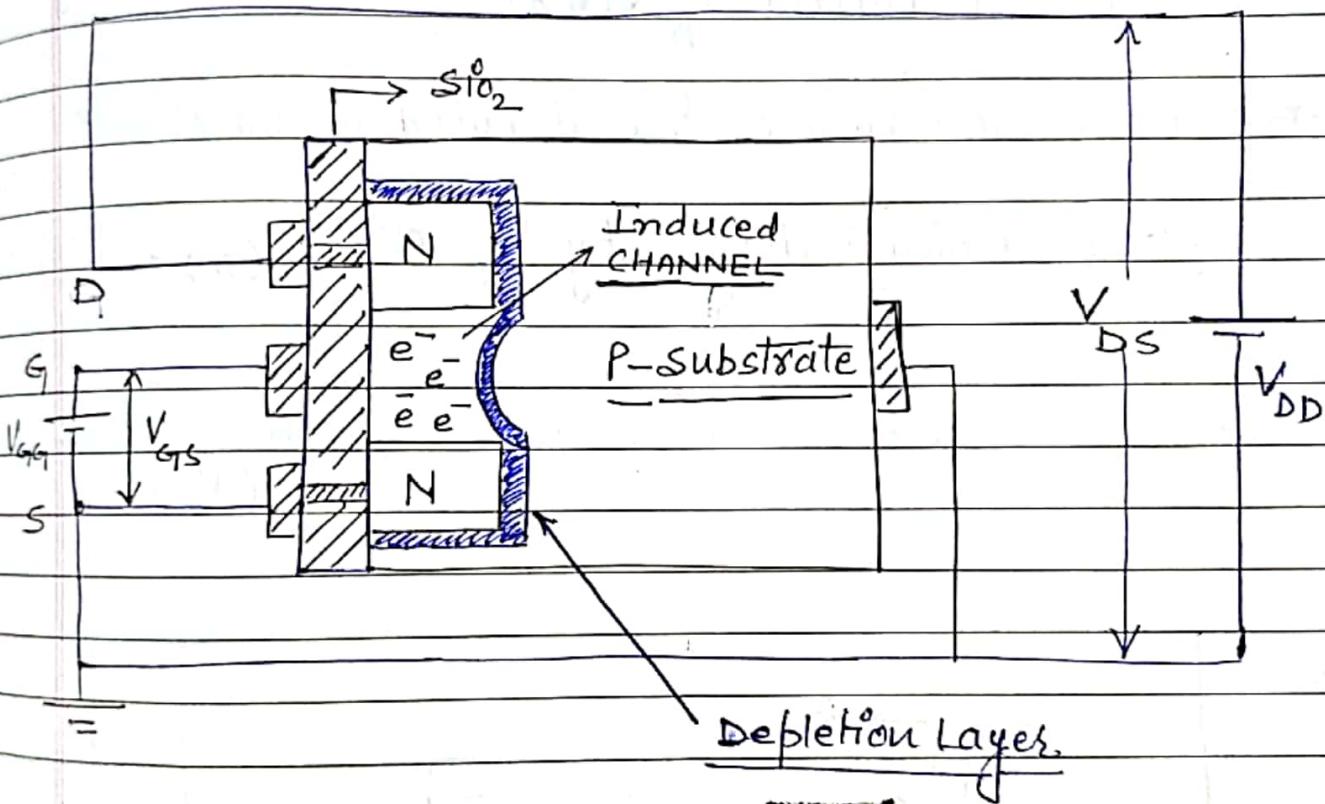


- * Source is Forward Biased and Drain is Reverse biased.
- * As source is Connected to (Eve) terminal of battery V_{DD} , so there will be Force of repulsion on electrons of source.
- * As Drain is Connected to (+ve) terminal of battery V_{DD} , so there will be Force of attraction at drain



* But there is no conducting channel present between source and drain, therefore current $I_D = 0$

2) CASE-II When $V_{DS} = +ve$ and $V_{GS} > 0V$



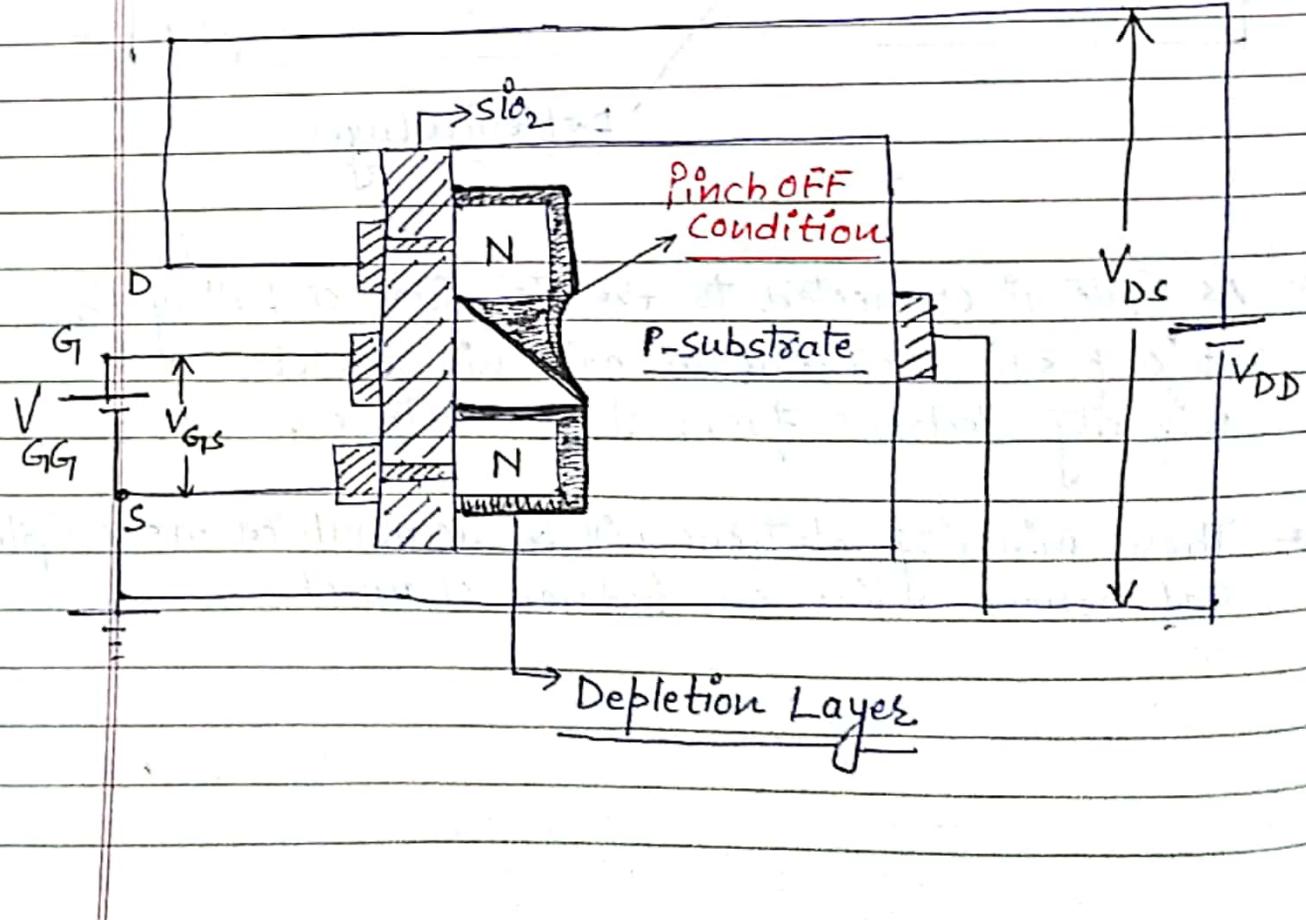
* As Gate is connected to +ve terminal of battery V_{GS} , so a positive potential at gate will attract minority electrons from P-substrate.

* These minority electrons will be accumulated near Gate, and behave like an induced channel.

- * These accumulated electrons are not sufficient to support heavy flow of current.
- * At a critical value of V_{GS} , sufficient electrons get accumulated near gate and support heavy flow of current I_D (mA).
- * This critical value of V_{GS} is called as threshold voltage which is denoted by V_T or $V_{GS}(m)$.

3. CASE 3:

When $V_{DS} = +V_e$ and $V_{GS} \rightarrow \text{Constant}$ (V_T).



* As V_{DS} is increased, the reverse bias at drain also increases, therefore width of depletion layer at drain also increases.

* After some time, a critical value of V_{DS} is reached where depletion layer touches SiO_2 layer.

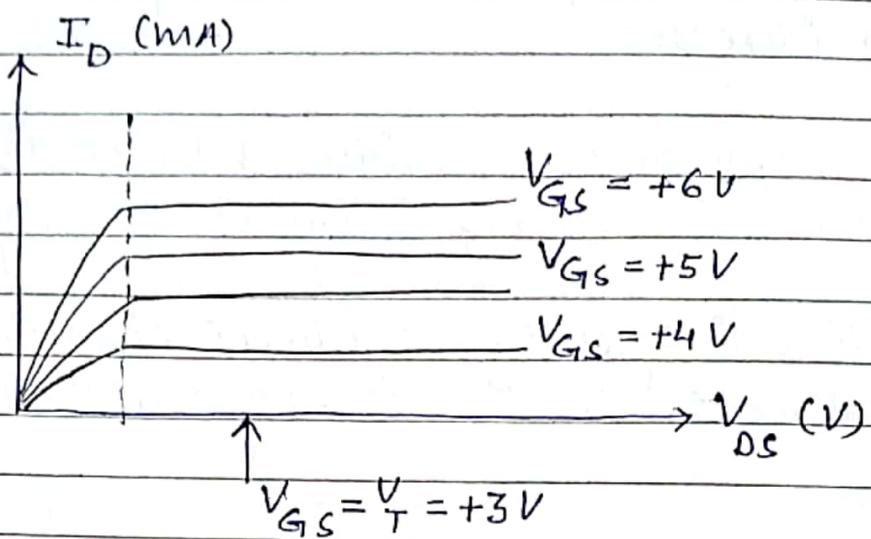
This condition is known as pinch-off condition and this critical value of V_{DS} is known as 'Pinch OFF Voltage' (V_p).

* But at the same time, Forward bias at source also increases, therefore force of repulsion at source will also be increased.

* Therefore electrons in the induced channel puncture the depletion layer, hence a very narrow channel with high density of electrons exists and

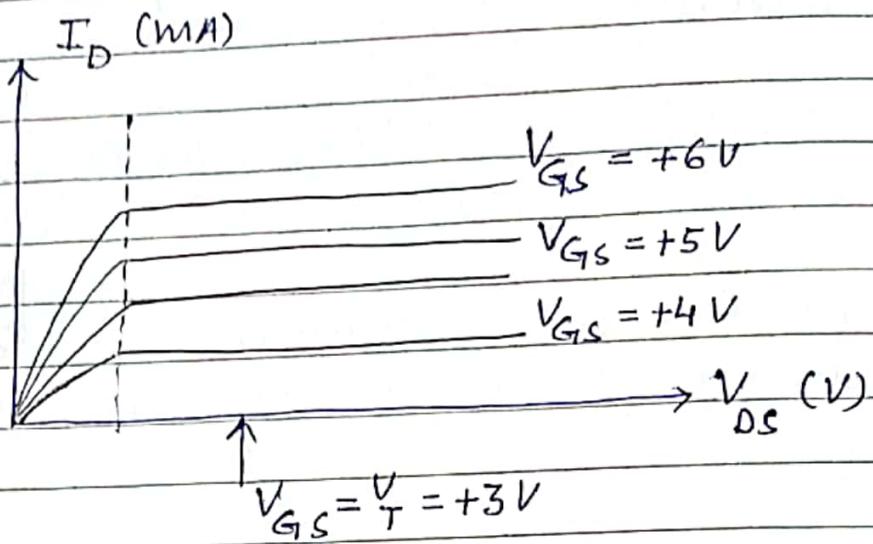
I_D current will flow to a saturation level.

Drain characteristics :- (E-Mos n-channel)



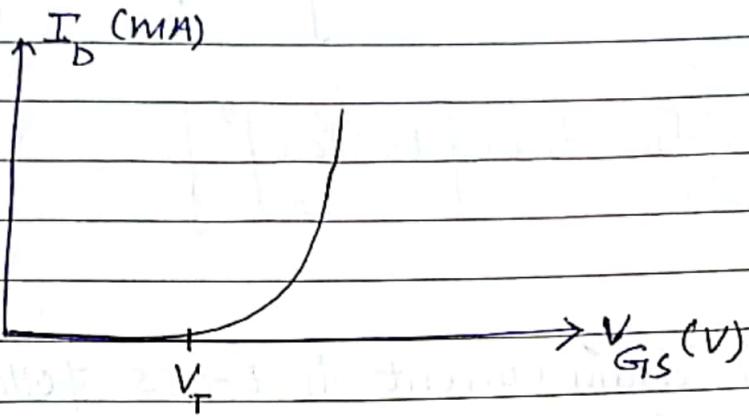
1. These Curves are plotted between I_D and V_{DS} keeping V_{GS} constant.
2. At $V_{GS} \leq V_T$:- When $V_{GS} \leq V_T$, channel between source and drain is induced but there are insufficient no. of electrons to support flow of current hence $I_D = 0 \text{ mA}$ (channel is not strong)
3. As V_{GS} is increased beyond V_T , channel becomes sufficiently strong to support I_D in mA, therefore current I_D increases.

Drain characteristics :- (E-MOS n-channel)



1. These curves are plotted between I_D and V_{DS} keeping V_{GS} constant.
2. At $V_{GS} \leq V_T$:- When $V_{GS} \leq V_T$, channel between source and drain is induced but there are insufficient no. of electrons to support flow of current hence $I_D = 0$ mA (channel is not strong)
3. As V_{GS} is increased beyond V_T , channel becomes sufficiently strong to support I_D in mA, therefore current I_D increases.

Transfer Characteristics (n-channel):



1. This curve is plotted between drain current I_D and V_{GS} keeping V_{DS} constant.

2. At $V_{GS} \leq V_T$:- When $V_{GS} \leq V_T$, current $I_D = 0 \text{ mA}$

because channel is not strong to support flow of current in mA.

3. As V_{GS} is increased beyond V_T , more and more no. of electrons get accumulated near SiO_2 layer, therefore channel becomes sufficiently strong to support I_D in mA, hence current I_D increases.

Note:- 1) D-MOS and JFET Follows
Shockley's Equation given by -

$$I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_P} \right]^2$$

2) The drain Current in E-MOS follows the following equation -

$$I_D = K \left[\frac{V_{GS} - V_T}{T} \right]^2$$

Where

$$K = \frac{I_{D(ON)}}{\left(\frac{V_{GS(ON)}}{T} \right)^2}$$

* $I_{D(ON)}$ and $V_{GS(ON)}$ are the points on the characteristics of E-MOS and is provided by manufacturers.