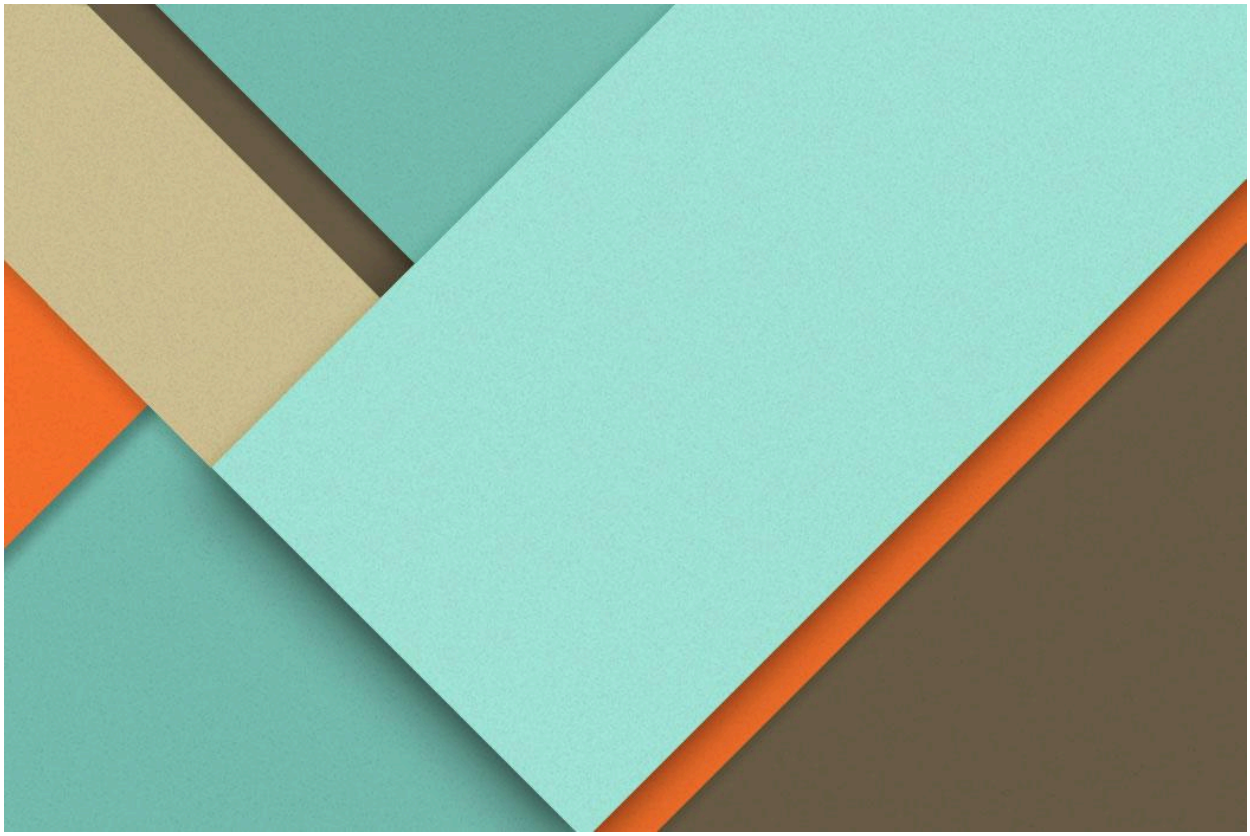


VLSI Architecture Design

Assignment - 3

26.03.2025

Submitted by:

Niranjan Gopal IMT2022543

Bijeet Basak IMT2022510

Abhinav Deshpande IMT2022580

Yash Sengupta IMT2022532

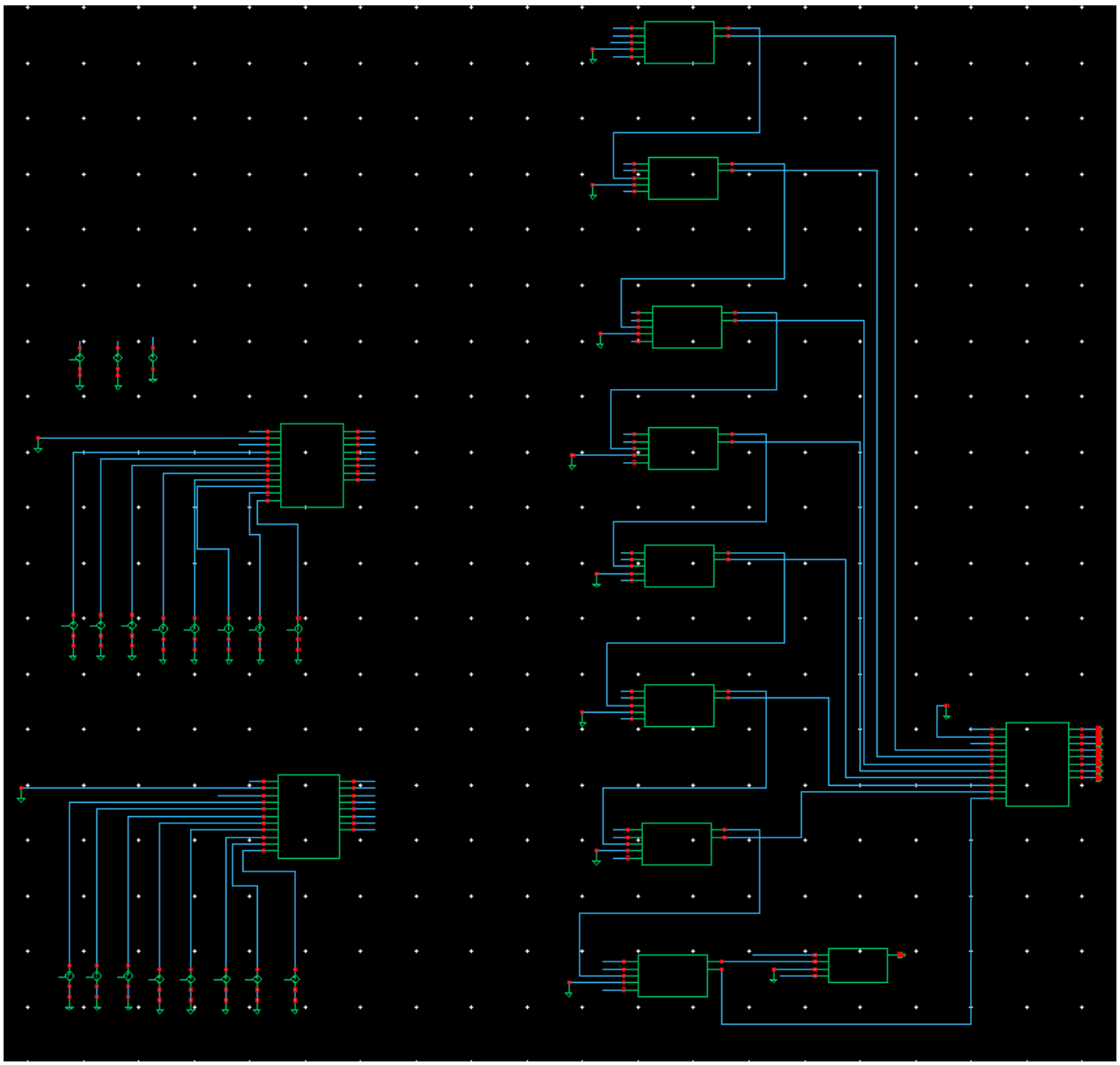
Dikshant Mahawar IMT2022549

Teerth Bhagat IMT2022586

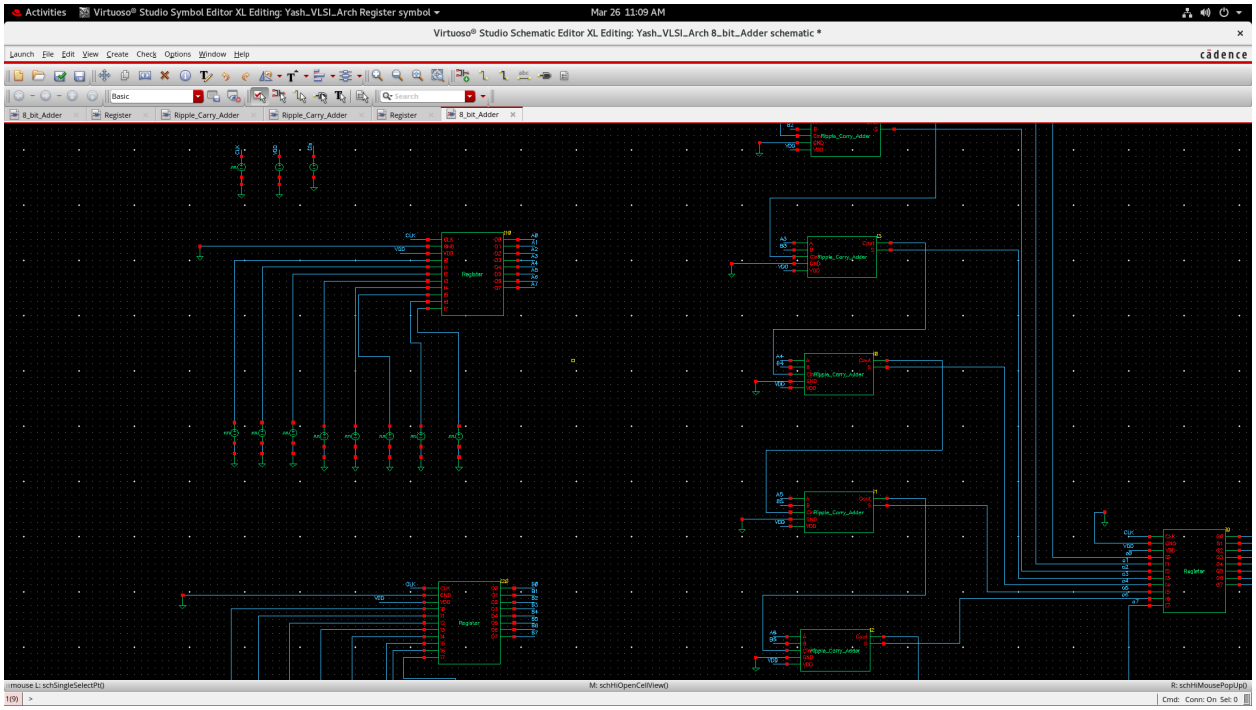
Source code and reports: Click here

Schematic from Virtuoso:

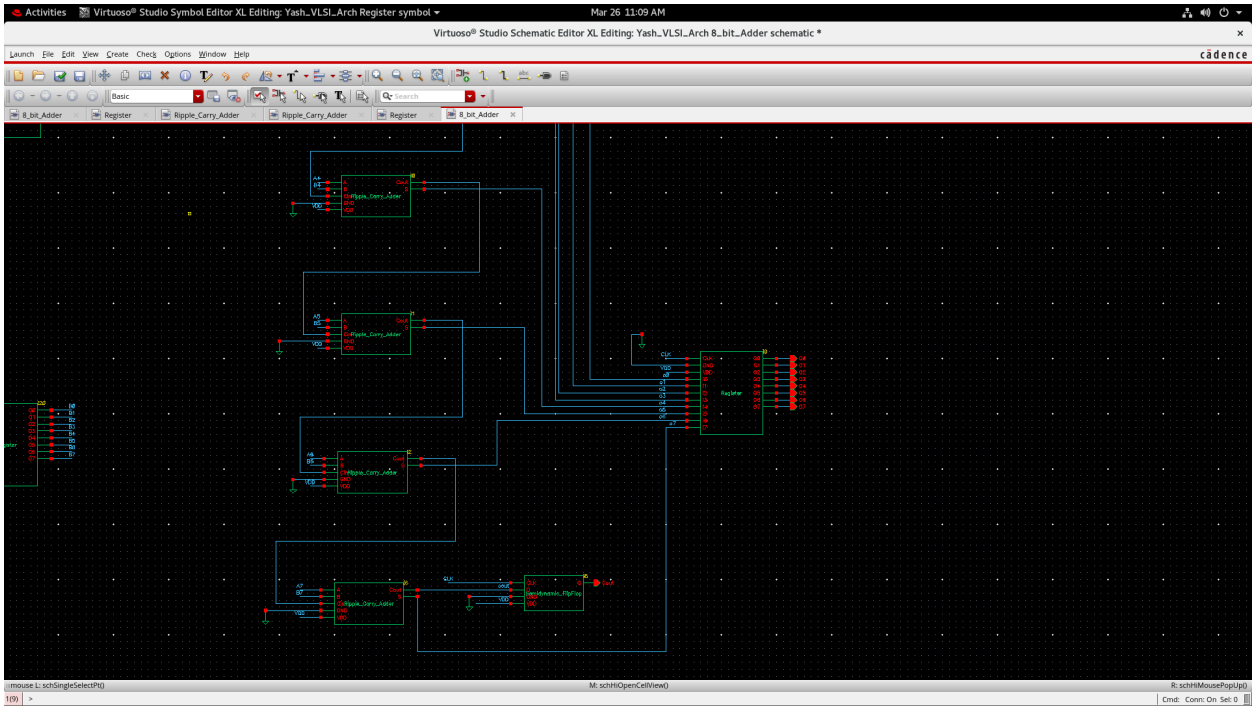
8 bit adder (Full circuit)



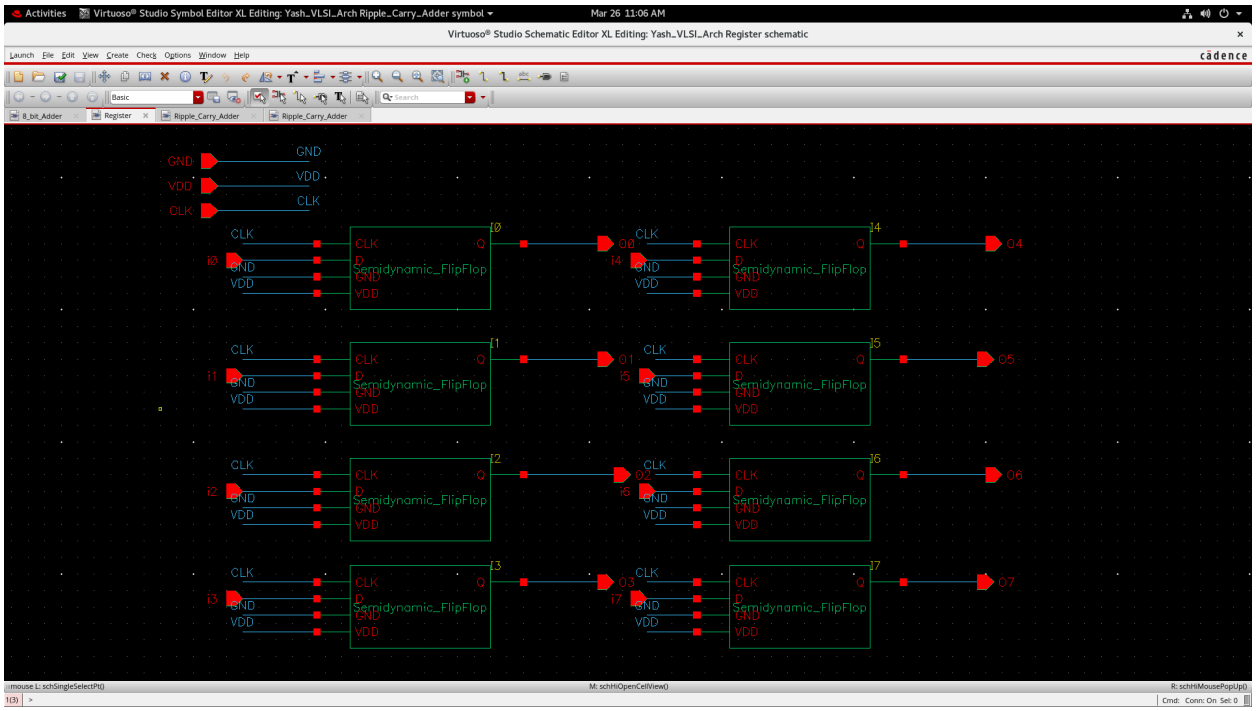
8 bit adder (Zoomed) (Part 1)



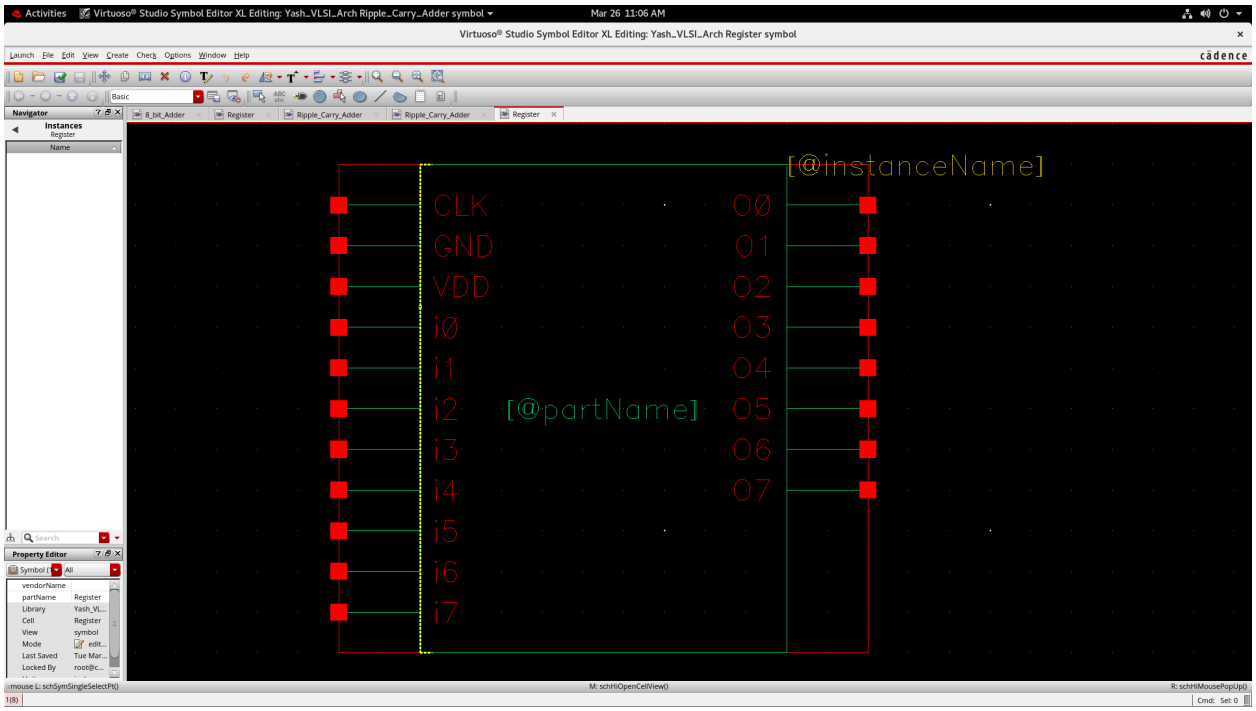
8 bit adder (Zoomed) (Part 2)



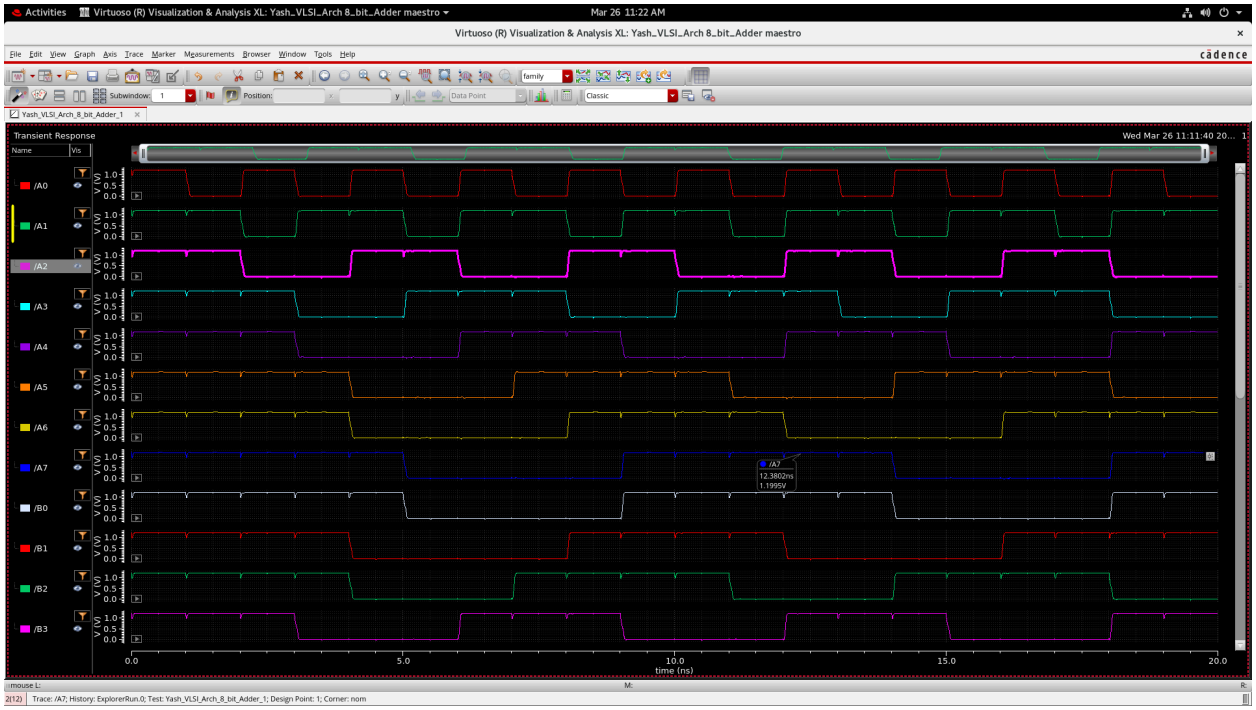
Register:


Activities
Virtuoso® Studio Symbol Editor XL Editing: Yash_VLSI_Arch Ripple_Carry_Adder symbol
Mar 26 11:06 AM
Virtuoso® Studio Schematic Editor XL Editing: Yash_VLSI_Arch Register schematic
cadence
GND
VDD
CLK
Semidynamic_FlipFlop
i0
i1
i2
i3
i4
i5
i6
i7
O0
O1
O2
O3
O4
O5
O6
O7

Register Symbol:

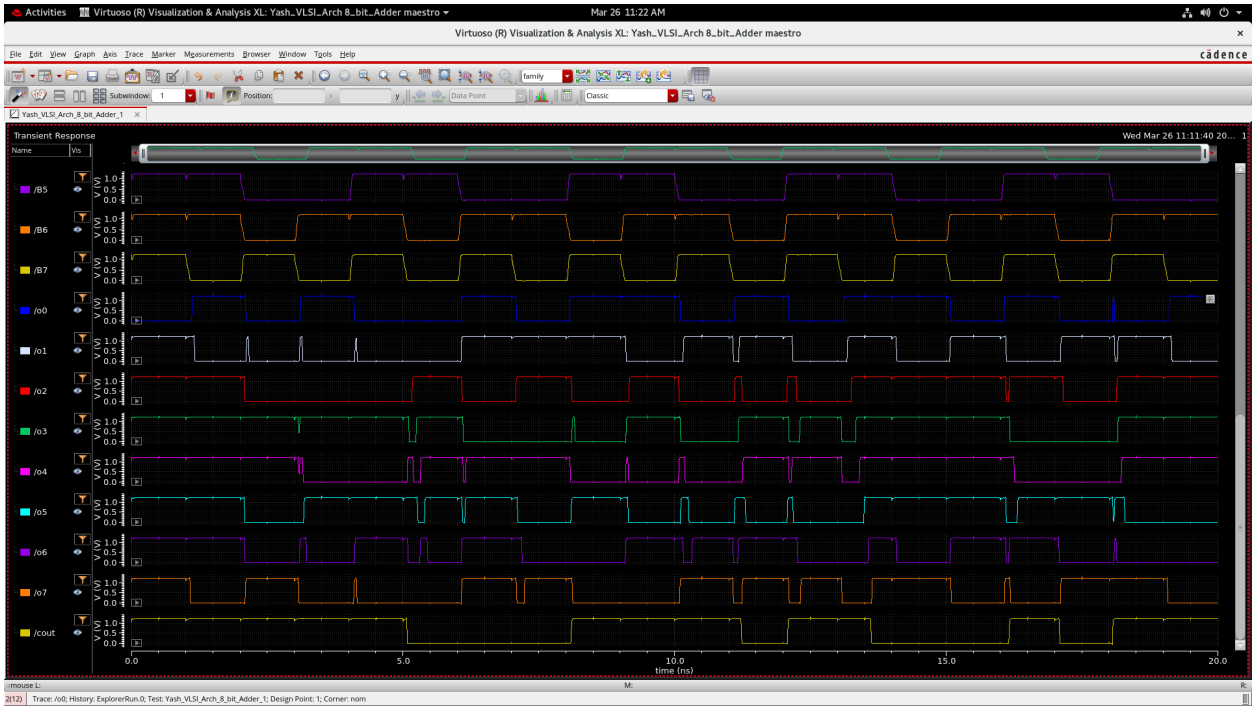


Results (A0 - A7 ; B0 - B3)

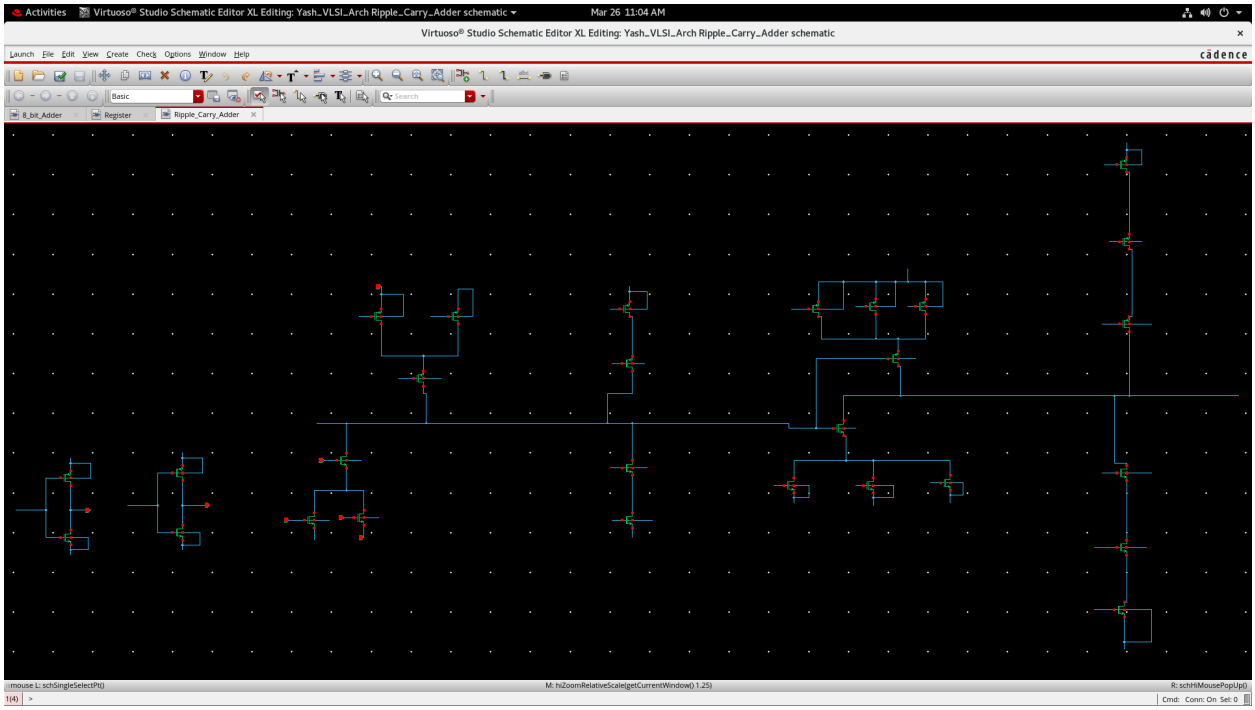


Results (B2 - B7 ; O0 - O5)

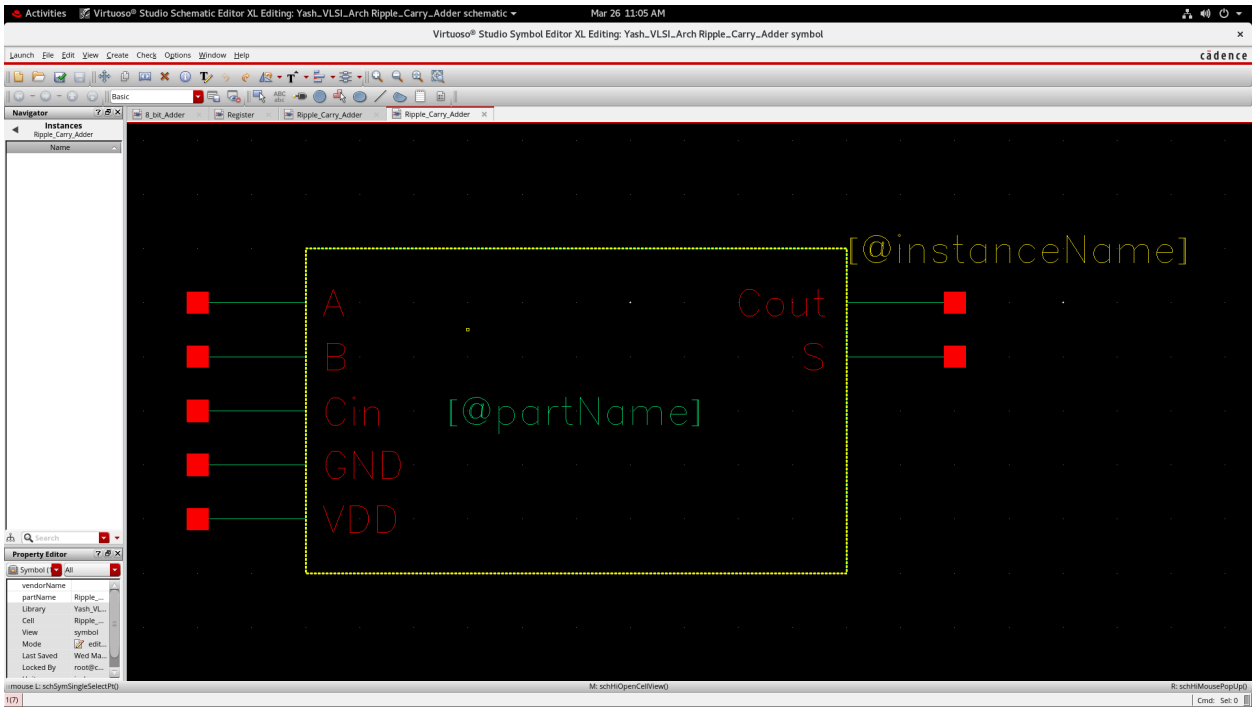
Results (B5 - B7 ; O1 - O7 ; Cout)



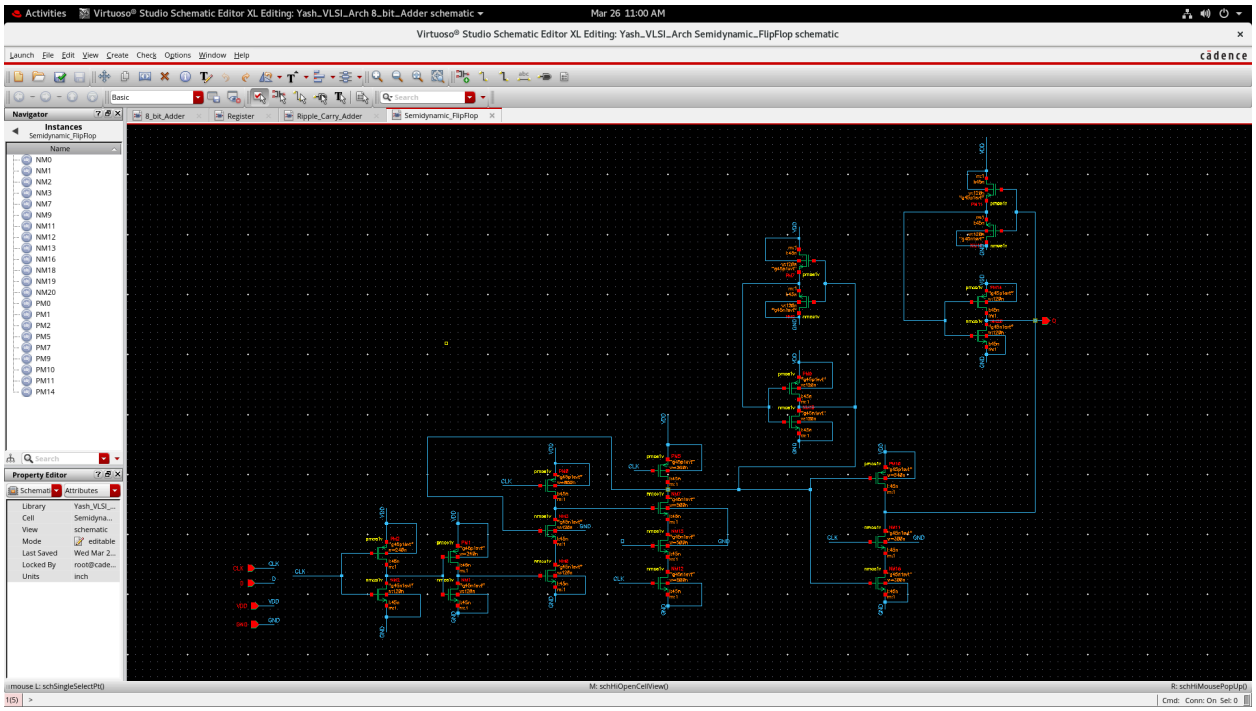
Ripple Adder



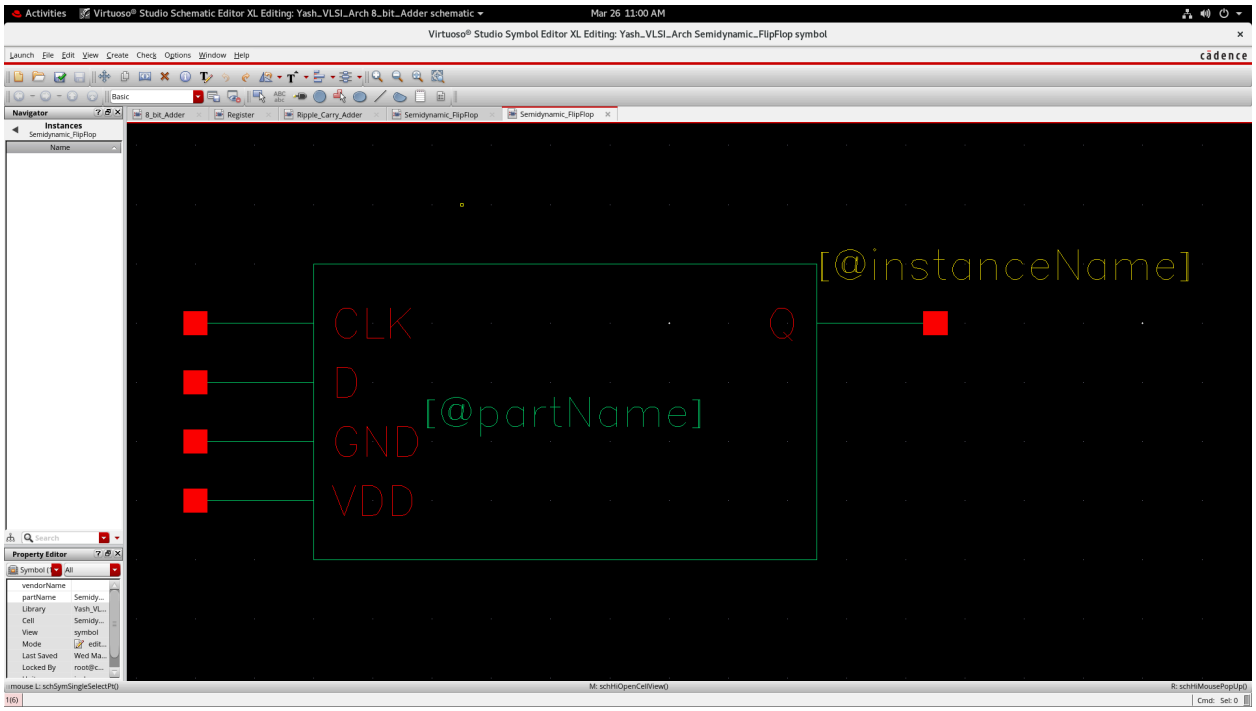
Ripple Adder symbol:



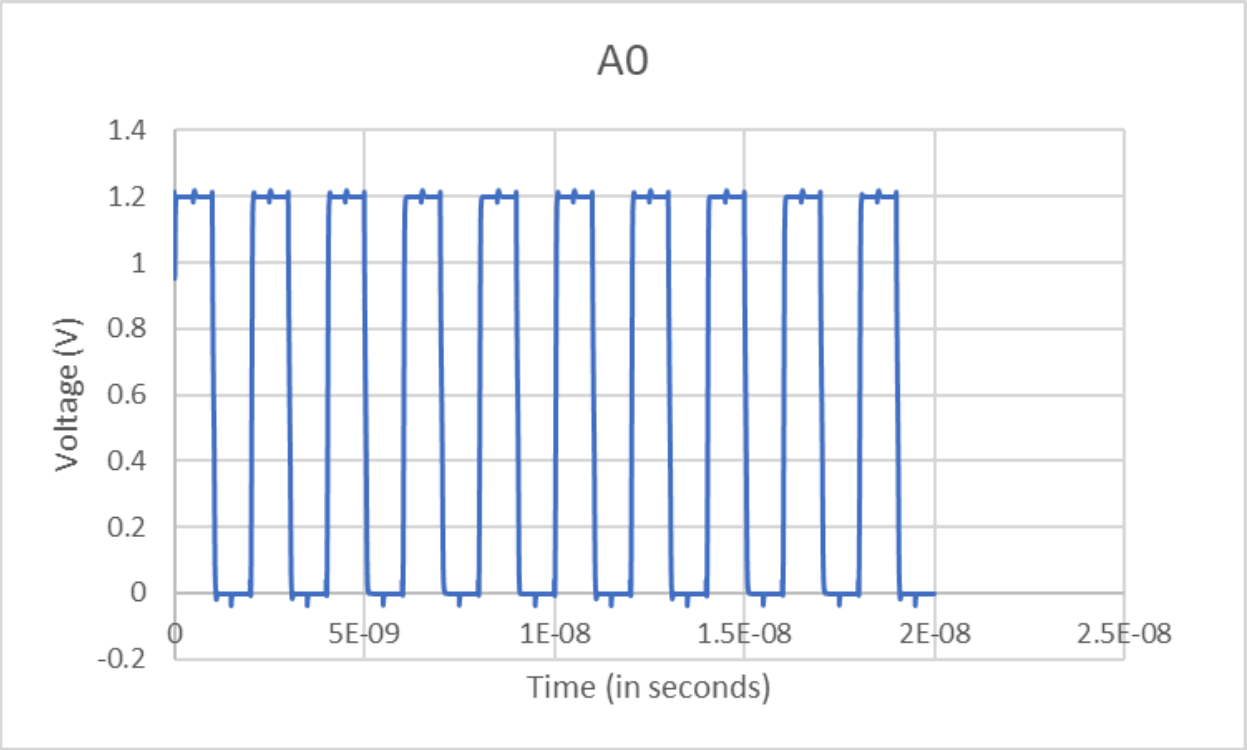
Semi Dynamic Flip Flop

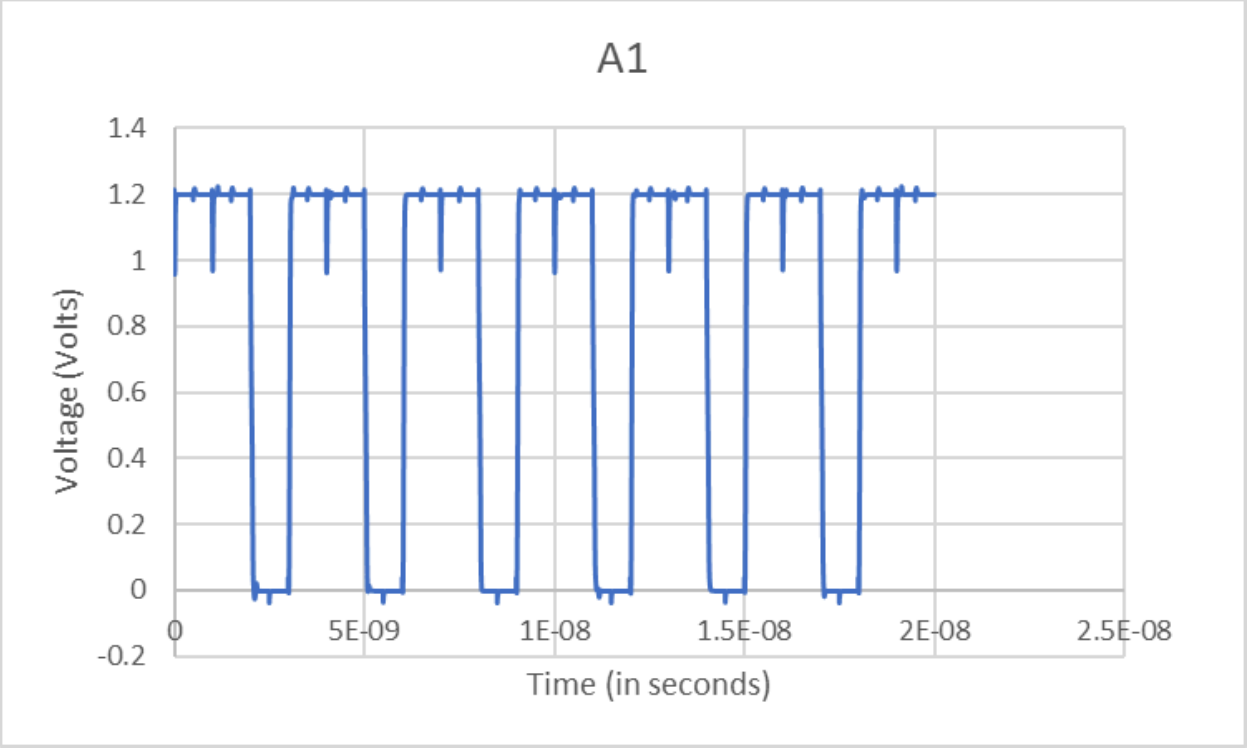


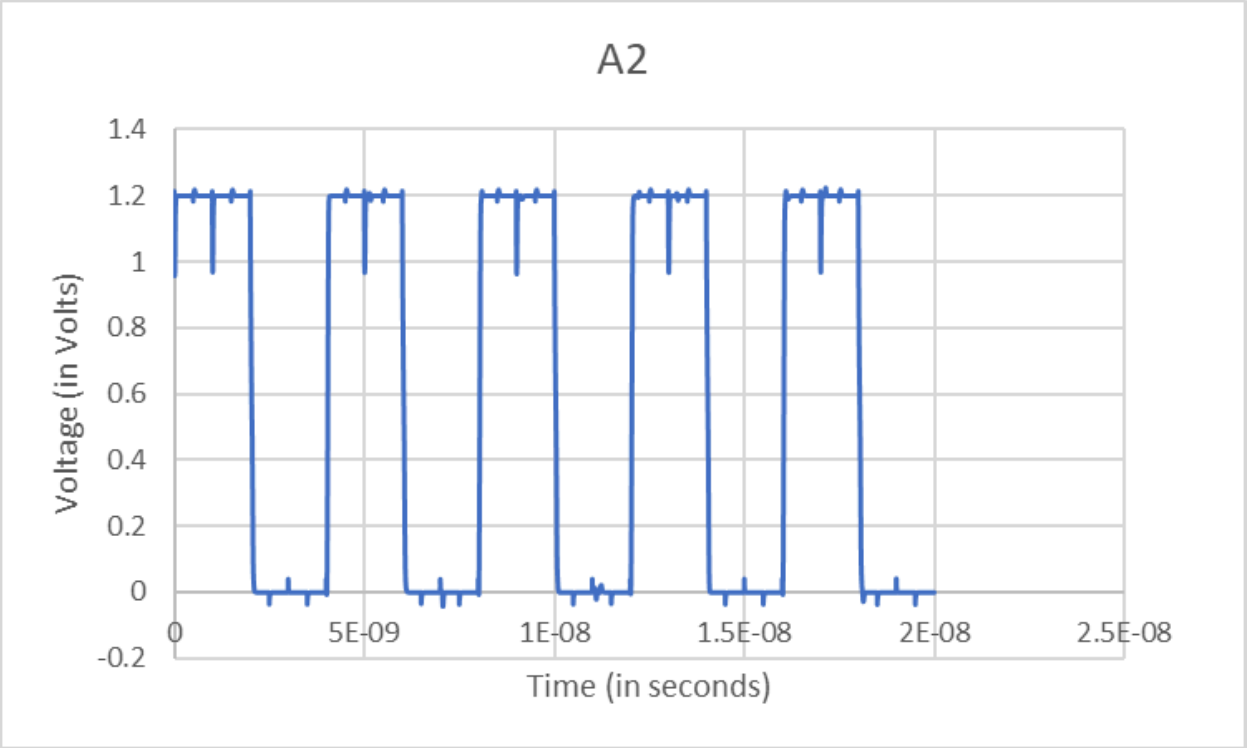
Semi Dynamic Flip Flop Symbol:

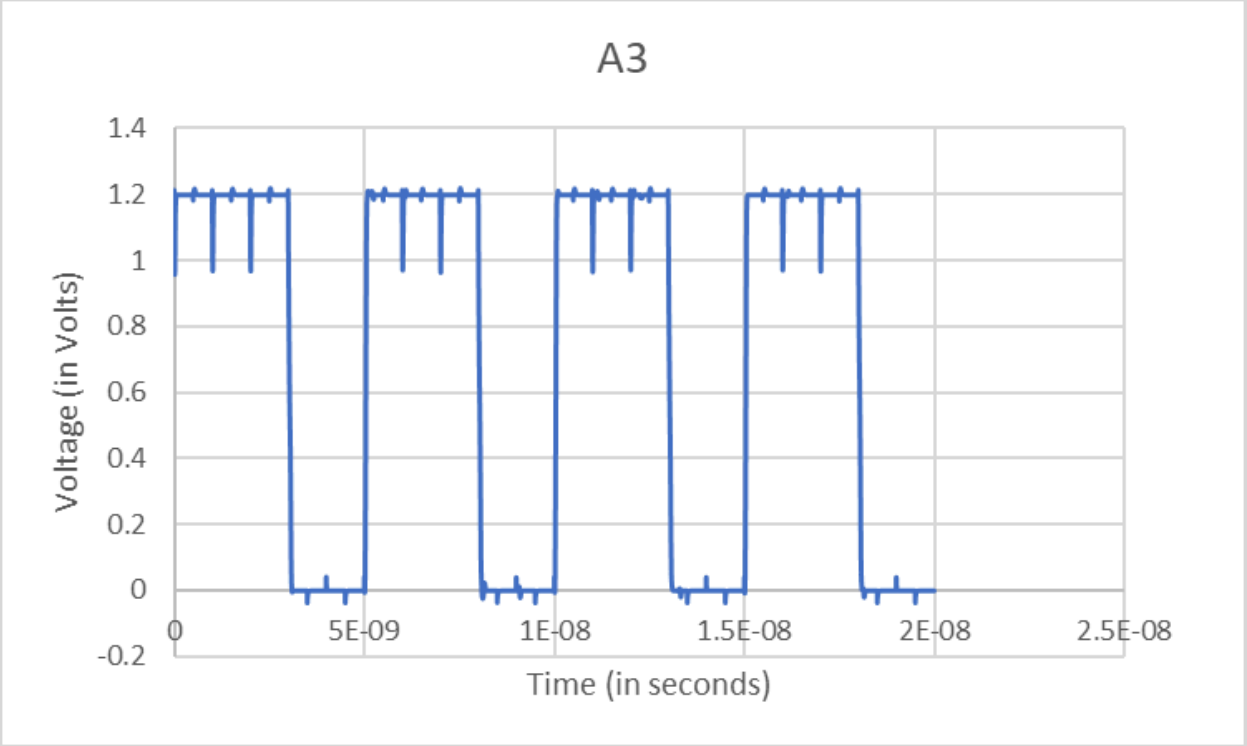


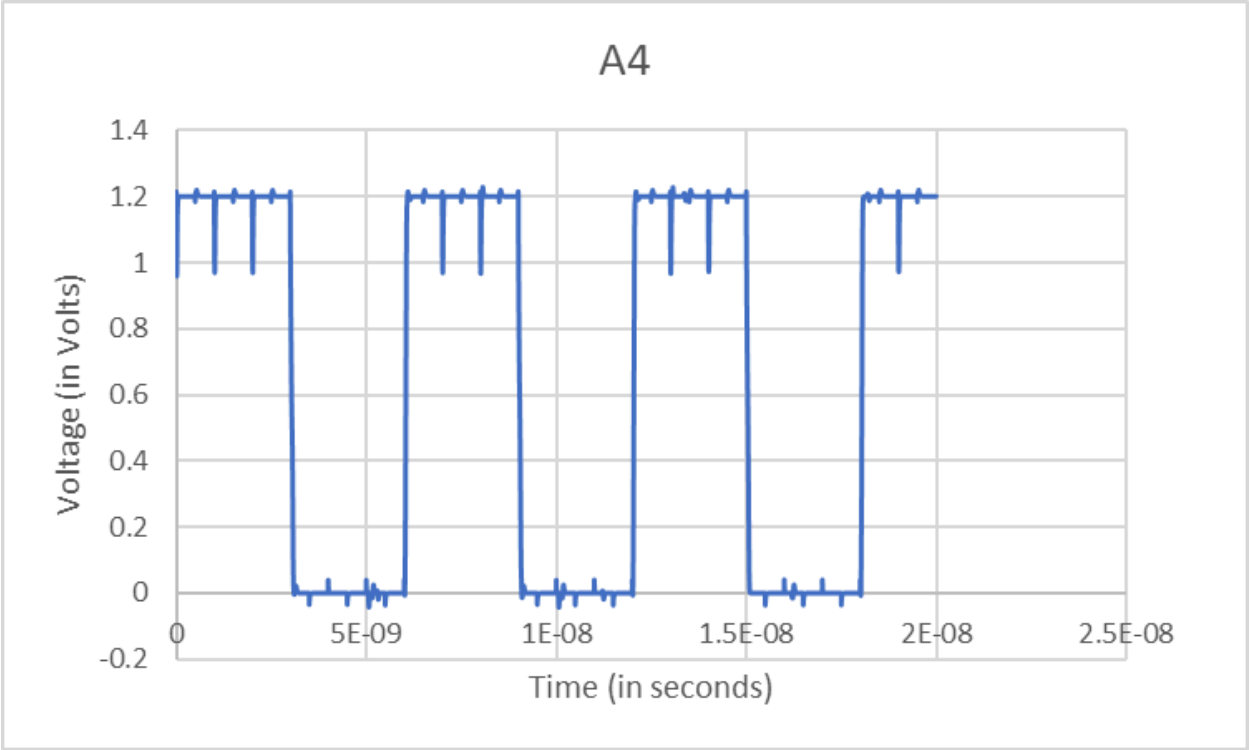
Signal A (A0 - A7) (8 bit):

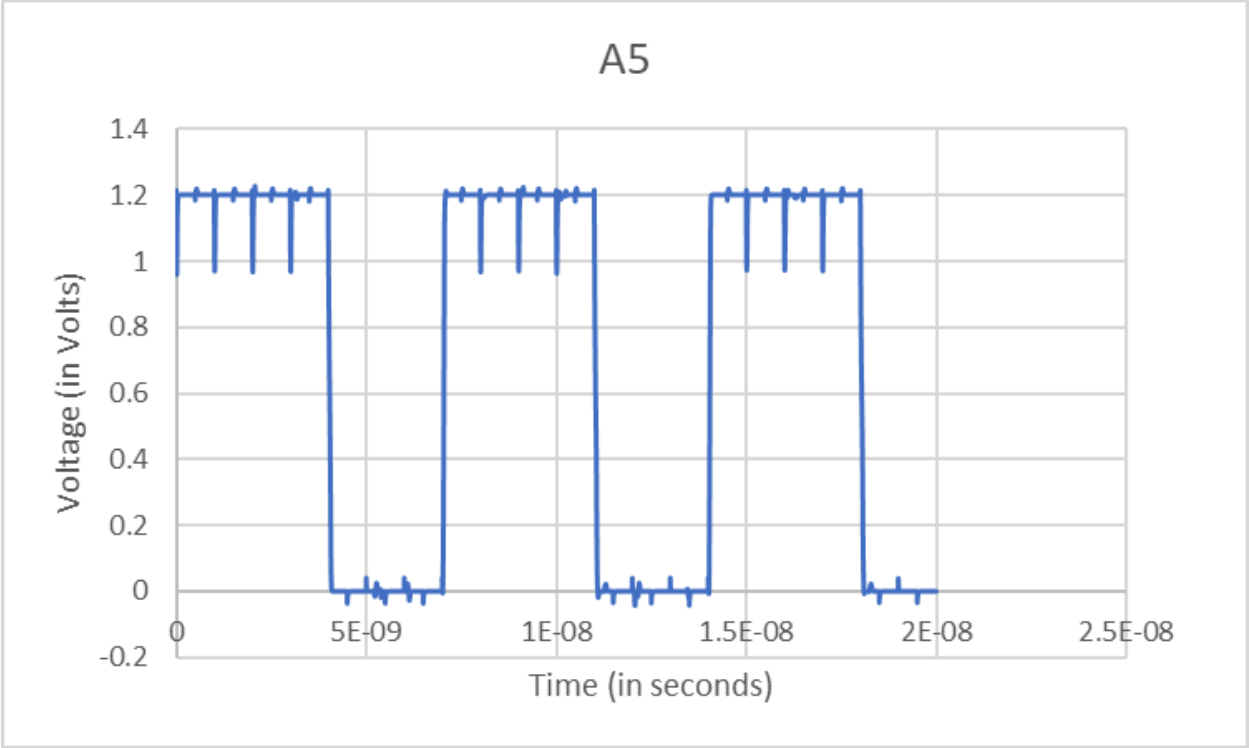


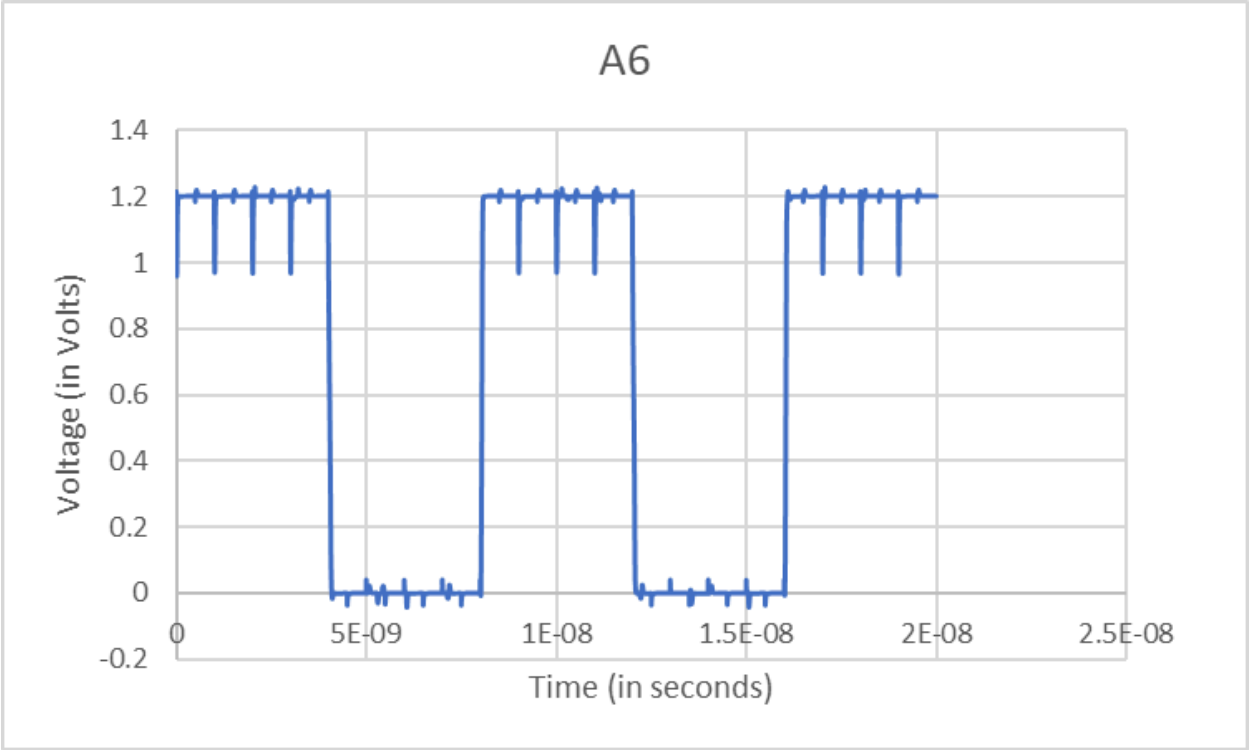


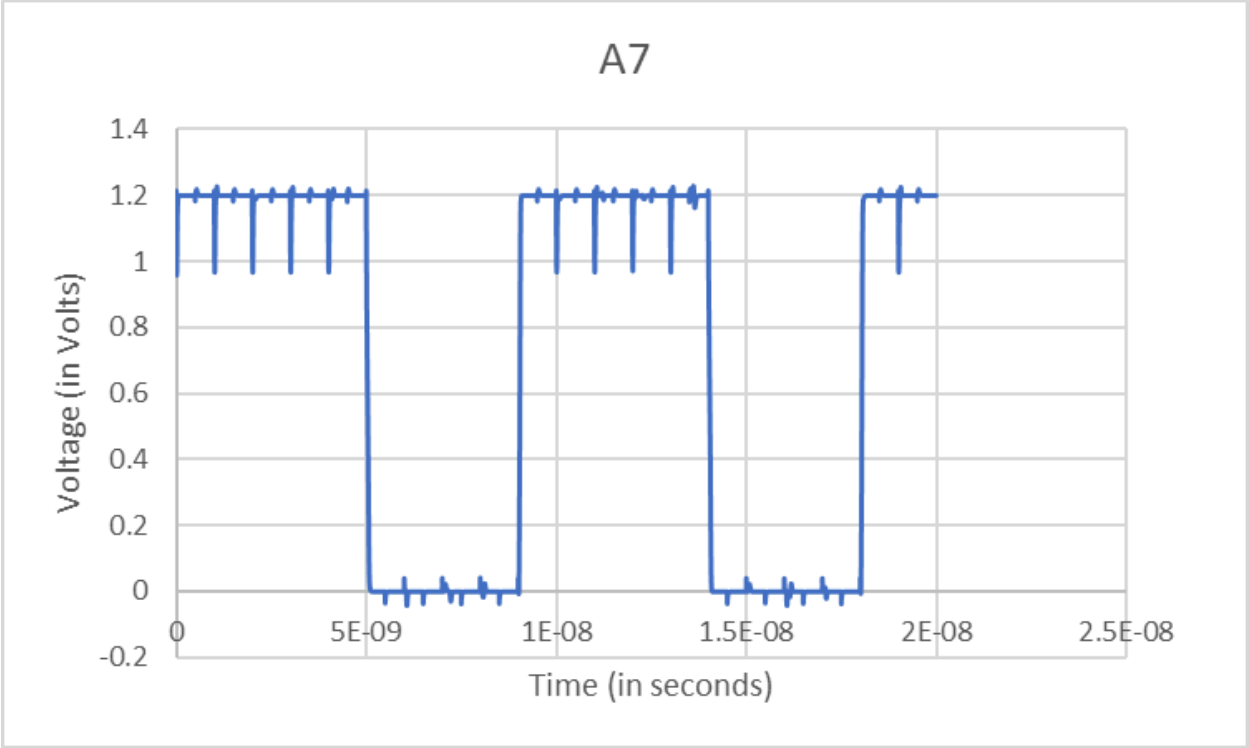

A2
Voltage (in Volts)
1.4
1.2
1
0.8
0.6
0.4
0.2
0
-0.2
0
5E-09
1E-08
1.5E-08
2E-08
2.5E-08
Time (in seconds)


A3
Voltage (in Volts)
1.4
1.2
1
0.8
0.6
0.4
0.2
0
-0.2
0
5E-09
1E-08
1.5E-08
2E-08
2.5E-08
Time (in seconds)

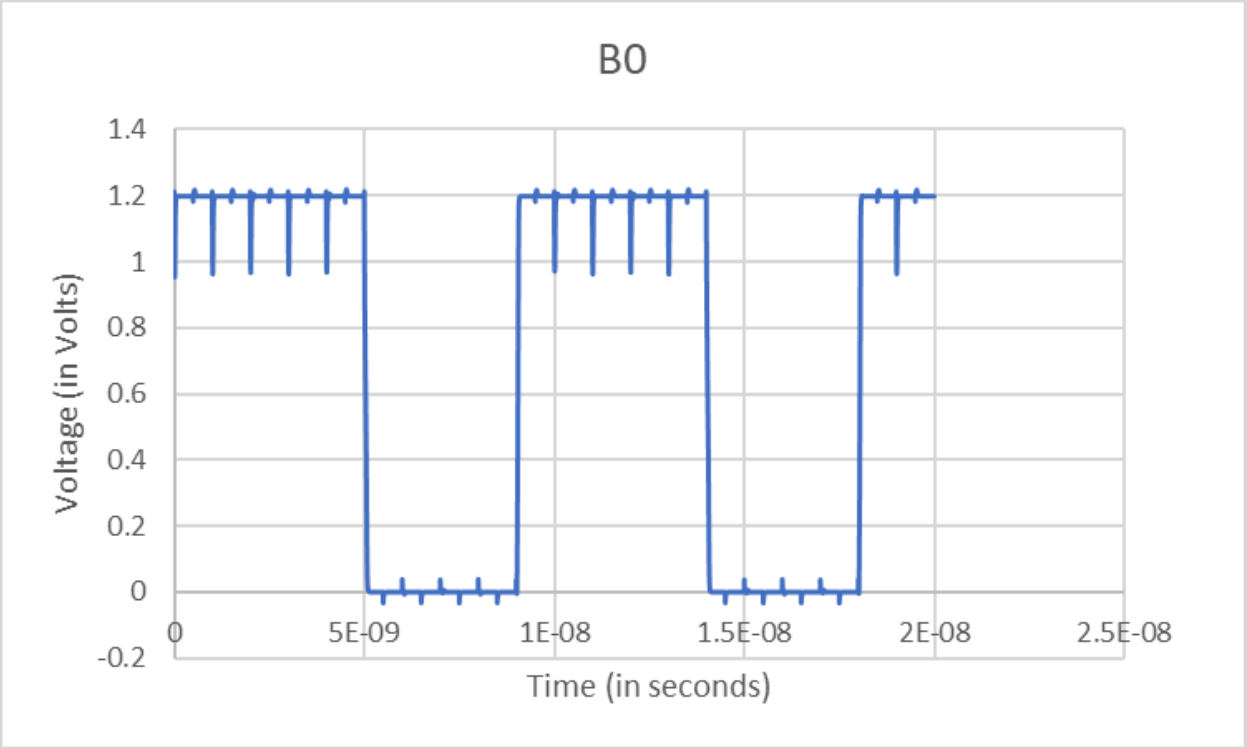

A4
1.4
1.2
1
0.8
0.6
0.4
0.2
0
-0.2
Voltage (in Volts)
0
5E-09
1E-08
1.5E-08
2E-08
2.5E-08
Time (in seconds)

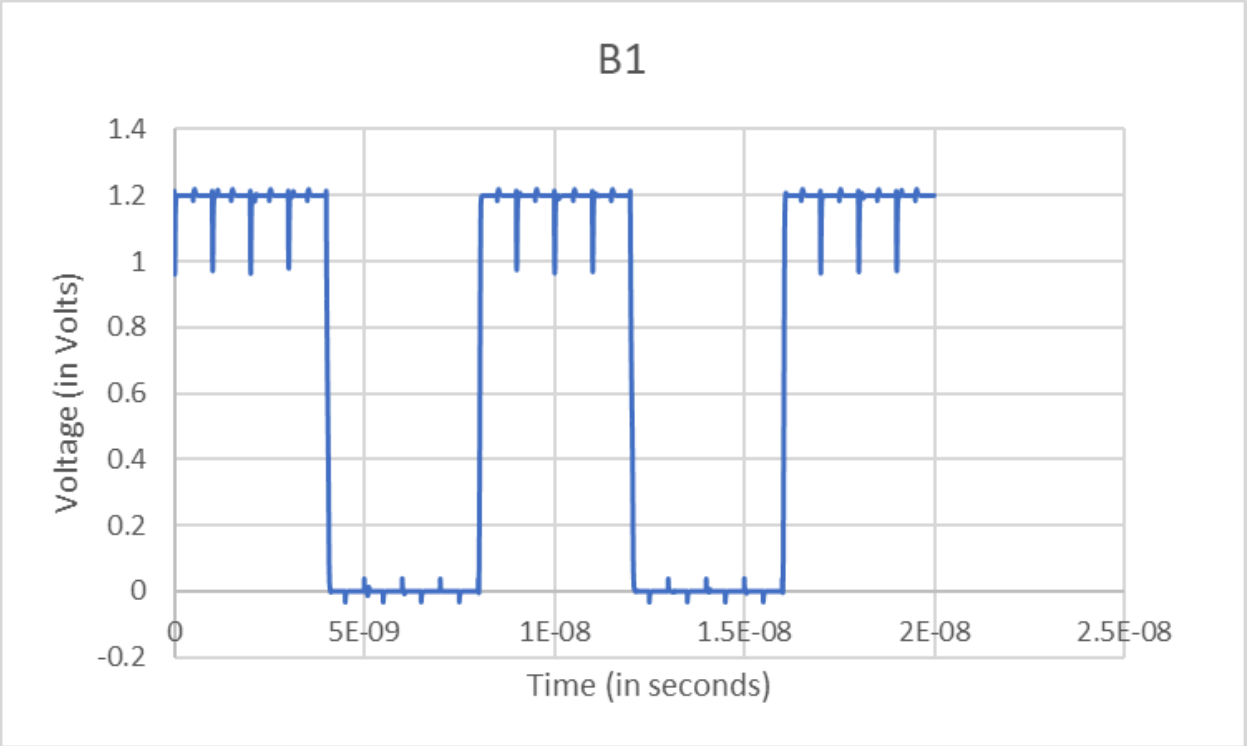

A5
1.4
1.2
1
0.8
0.6
0.4
0.2
0
-0.2
Voltage (in Volts)
0
5E-09
1E-08
1.5E-08
2E-08
2.5E-08
Time (in seconds)

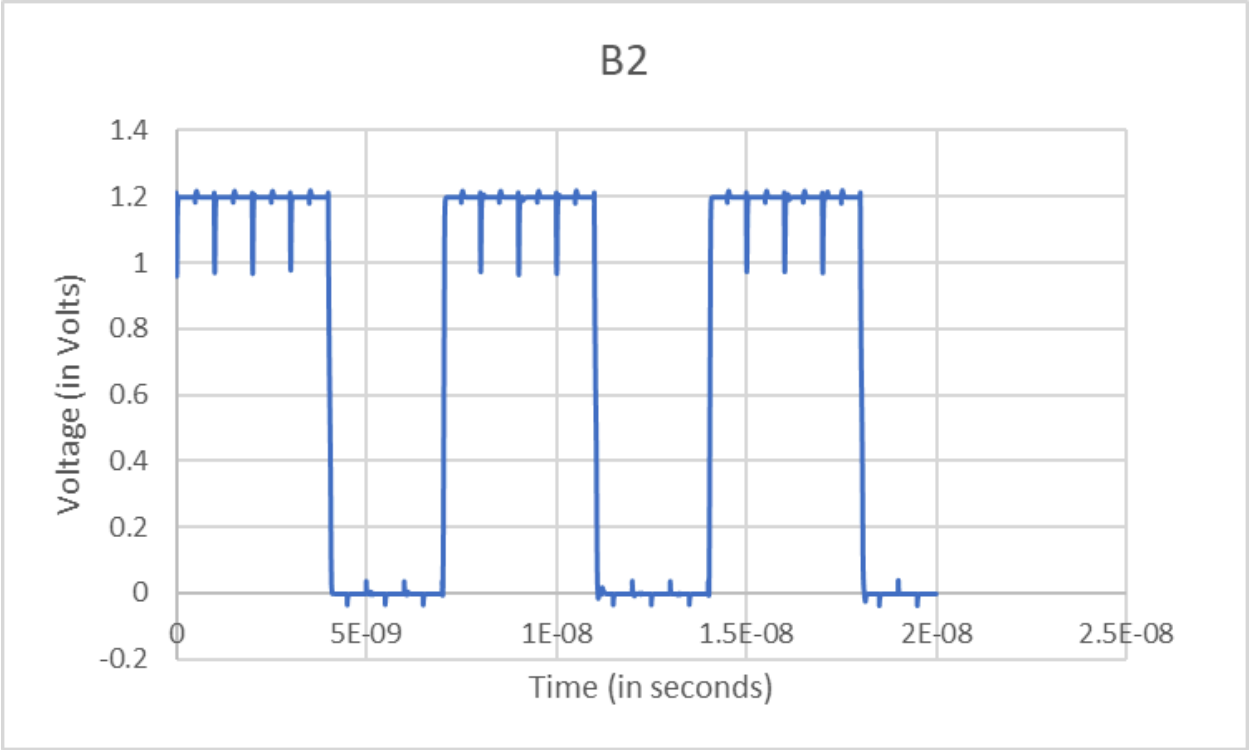

A6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
-0.2
Voltage (in Volts)
0
5E-09
1E-08
1.5E-08
2E-08
2.5E-08
Time (in seconds)

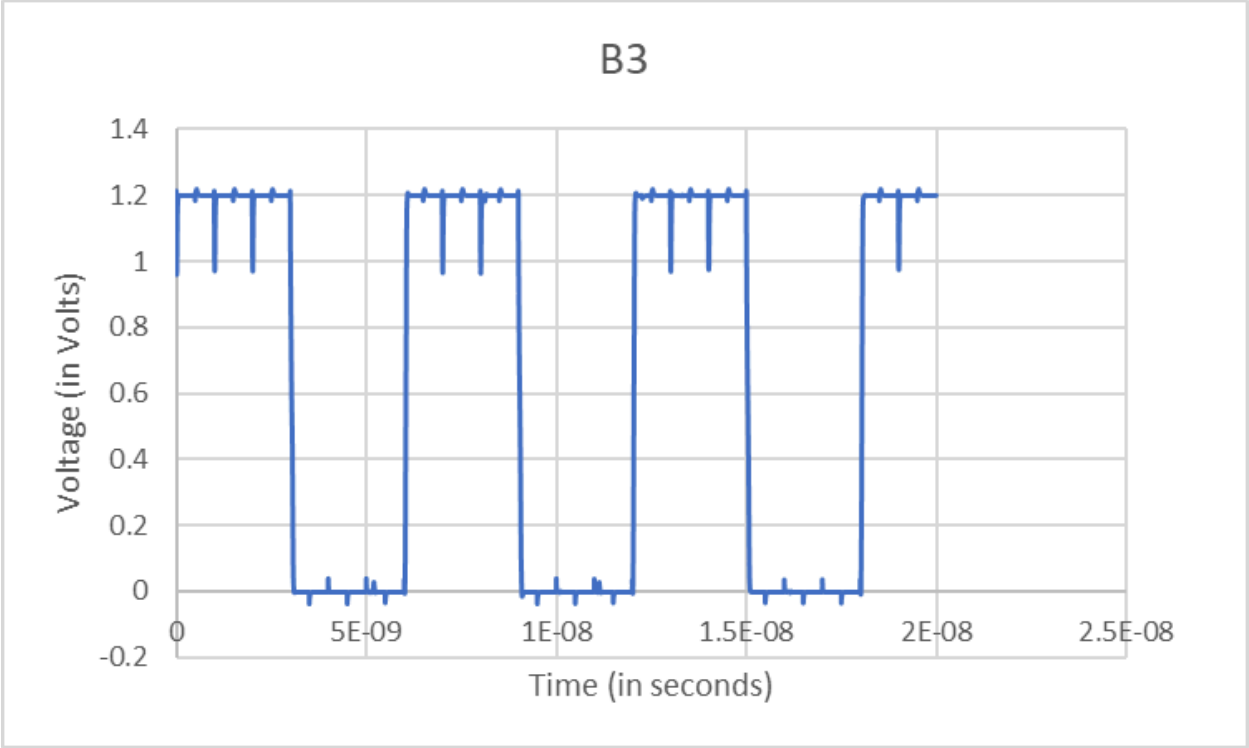

A7
1.4
1.2
1
0.8
0.6
0.4
0.2
0
-0.2
Voltage (in Volts)
0
5E-09
1E-08
1.5E-08
2E-08
2.5E-08
Time (in seconds)

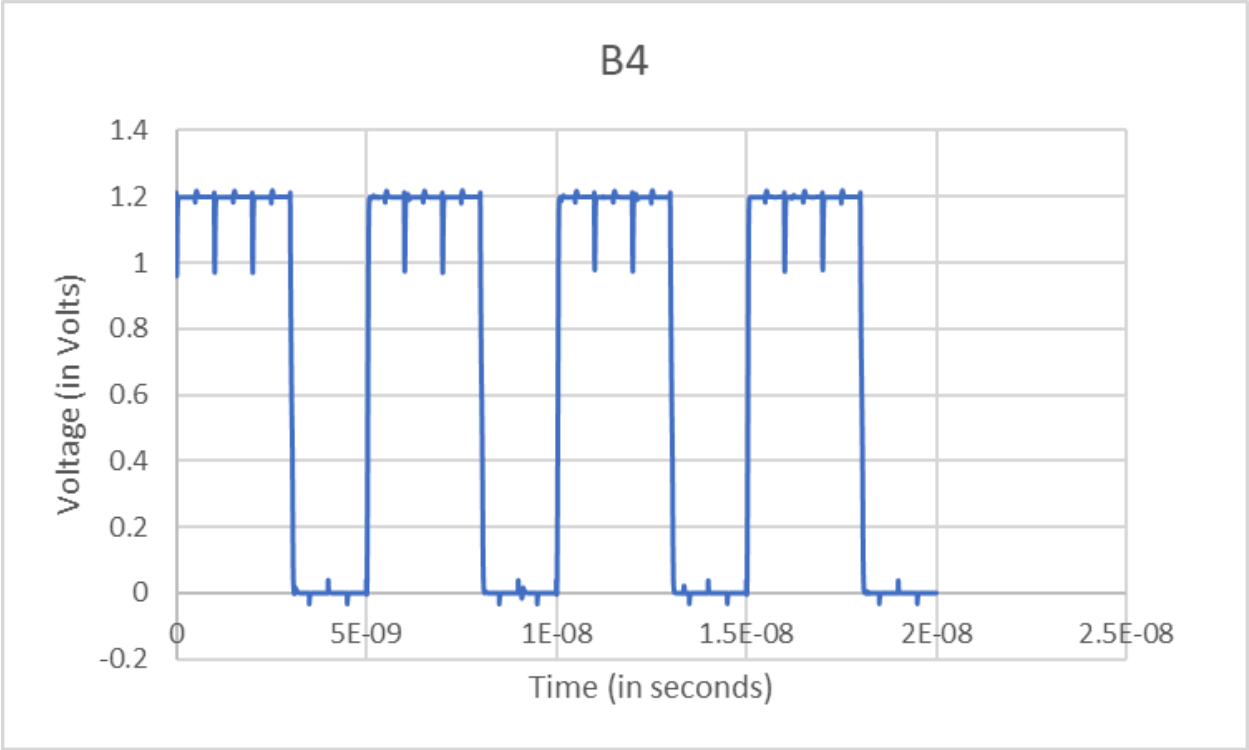
Signal B (B0 - B7) (8 bit):

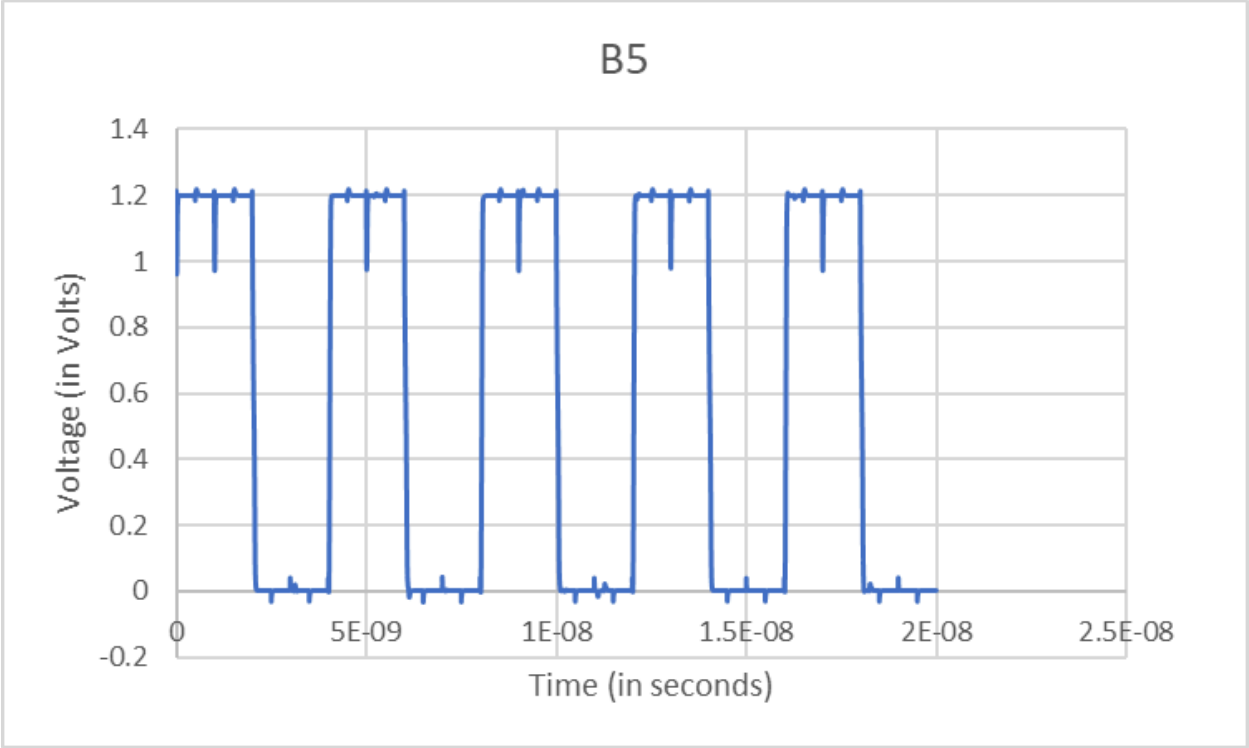


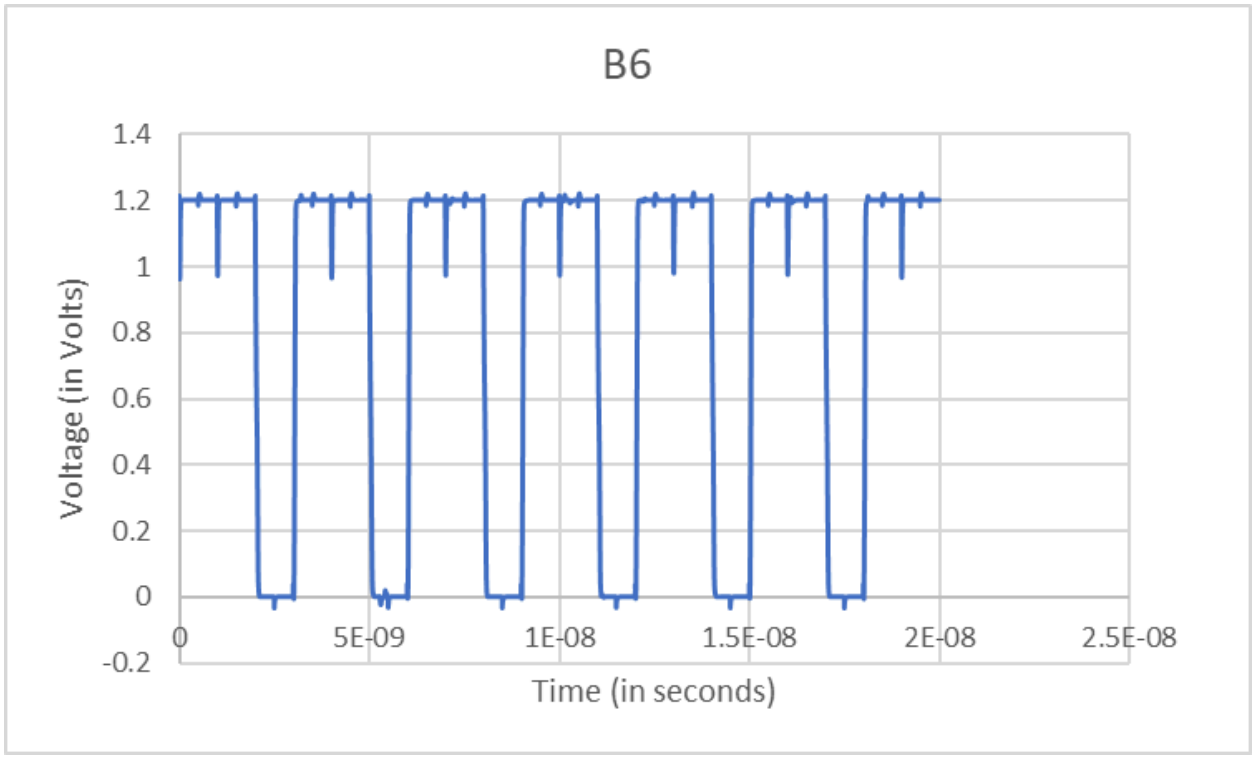


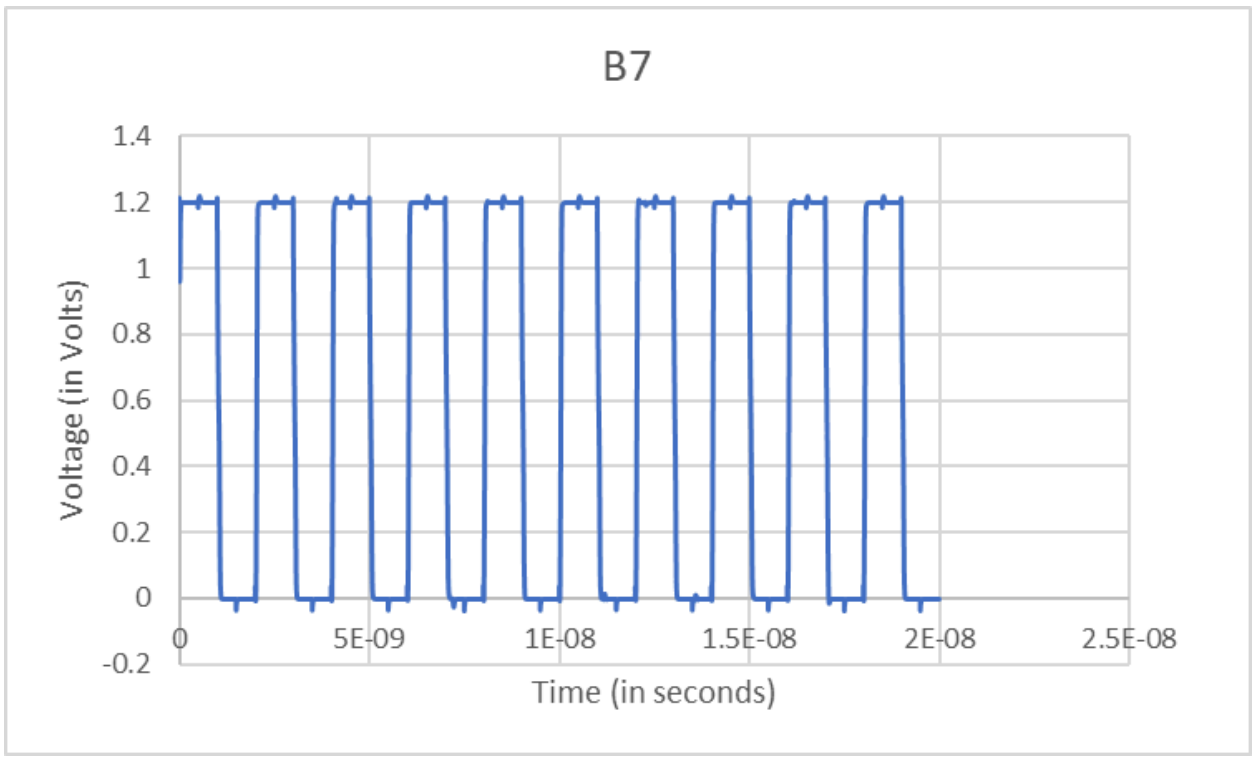

B2
1.4
1.2
1
0.8
0.6
0.4
0.2
0
-0.2
Voltage (in Volts)
0
5E-09
1E-08
1.5E-08
2E-08
2.5E-08
Time (in seconds)


B3
1.4
1.2
1
0.8
0.6
0.4
0.2
0
-0.2
Voltage (in Volts)
0
5E-09
1E-08
1.5E-08
2E-08
2.5E-08
Time (in seconds)

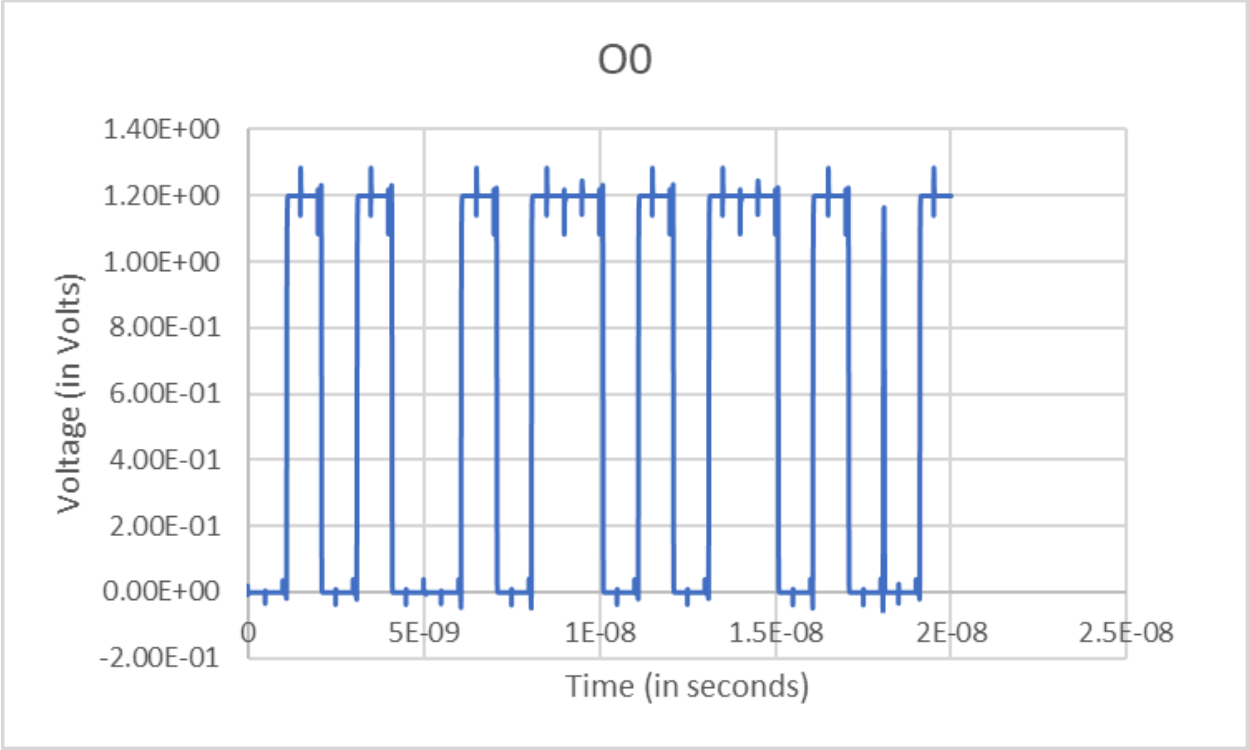

B4
1.4
1.2
1
0.8
0.6
0.4
0.2
0
-0.2
Voltage (in Volts)
0
5E-09
1E-08
1.5E-08
2E-08
2.5E-08
Time (in seconds)

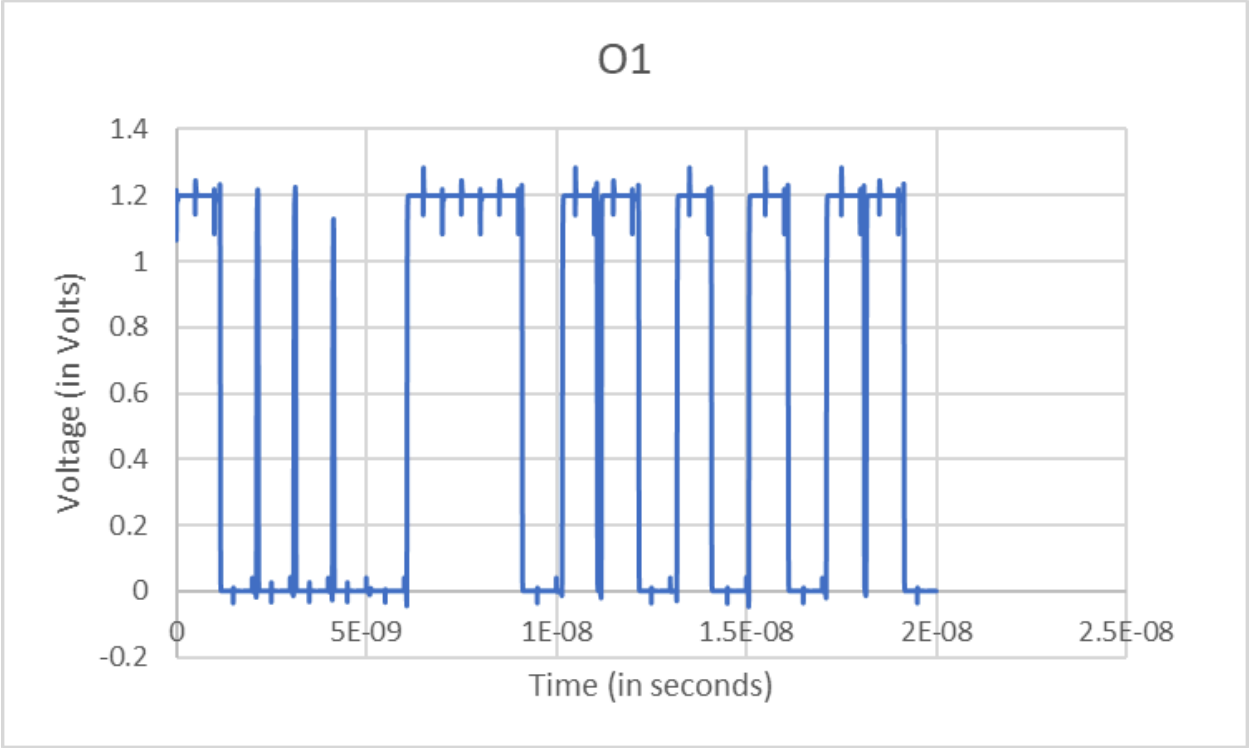

B5
1.4
1.2
1
0.8
0.6
0.4
0.2
0
-0.2
Voltage (in Volts)
0
5E-09
1E-08
1.5E-08
2E-08
2.5E-08
Time (in seconds)

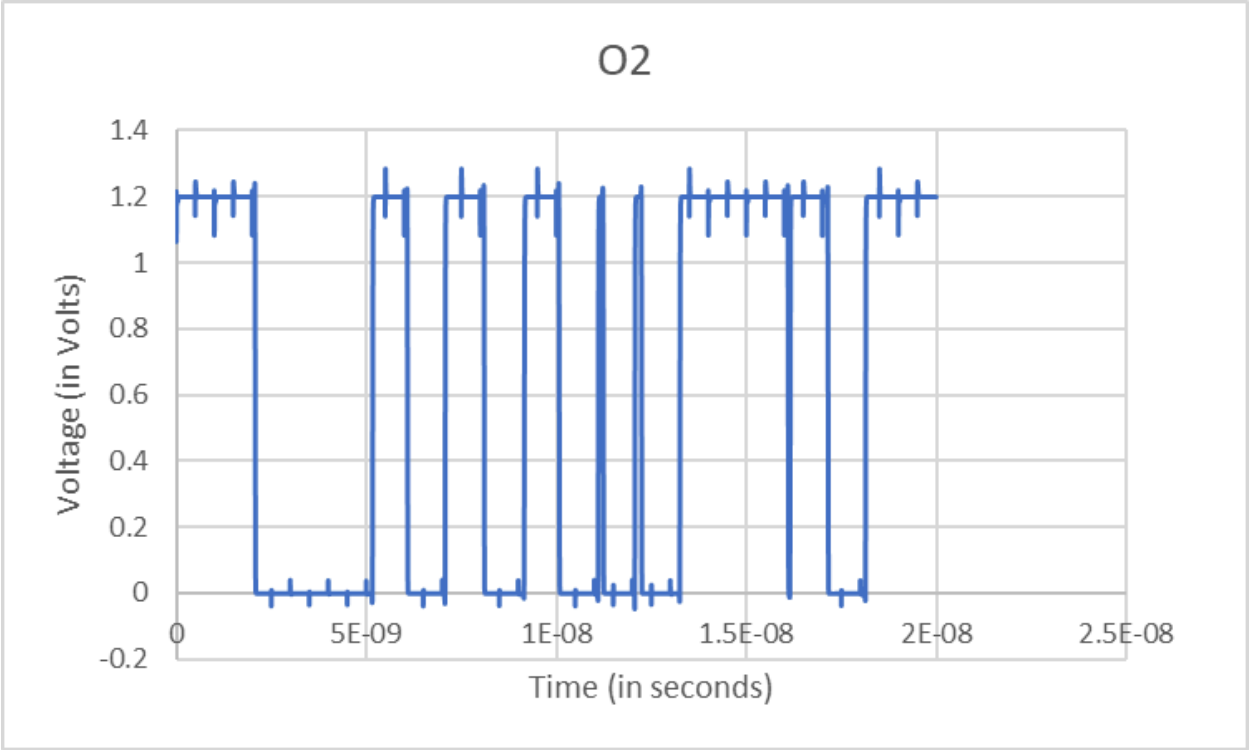

B6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
-0.2
Voltage (in Volts)
0
5E-09
1E-08
1.5E-08
2E-08
2.5E-08
Time (in seconds)

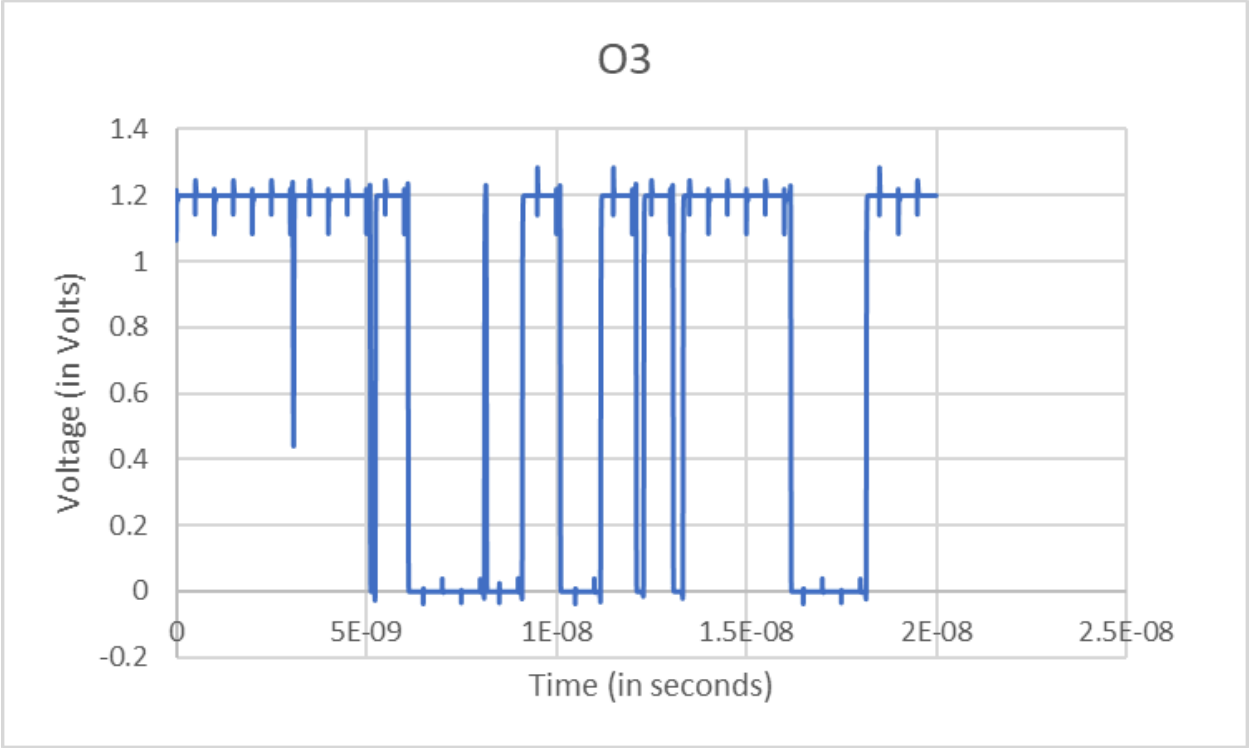

B7
1.4
1.2
1
0.8
0.6
0.4
0.2
0
-0.2
Voltage (in Volts)
0
5E-09
1E-08
1.5E-08
2E-08
2.5E-08
Time (in seconds)

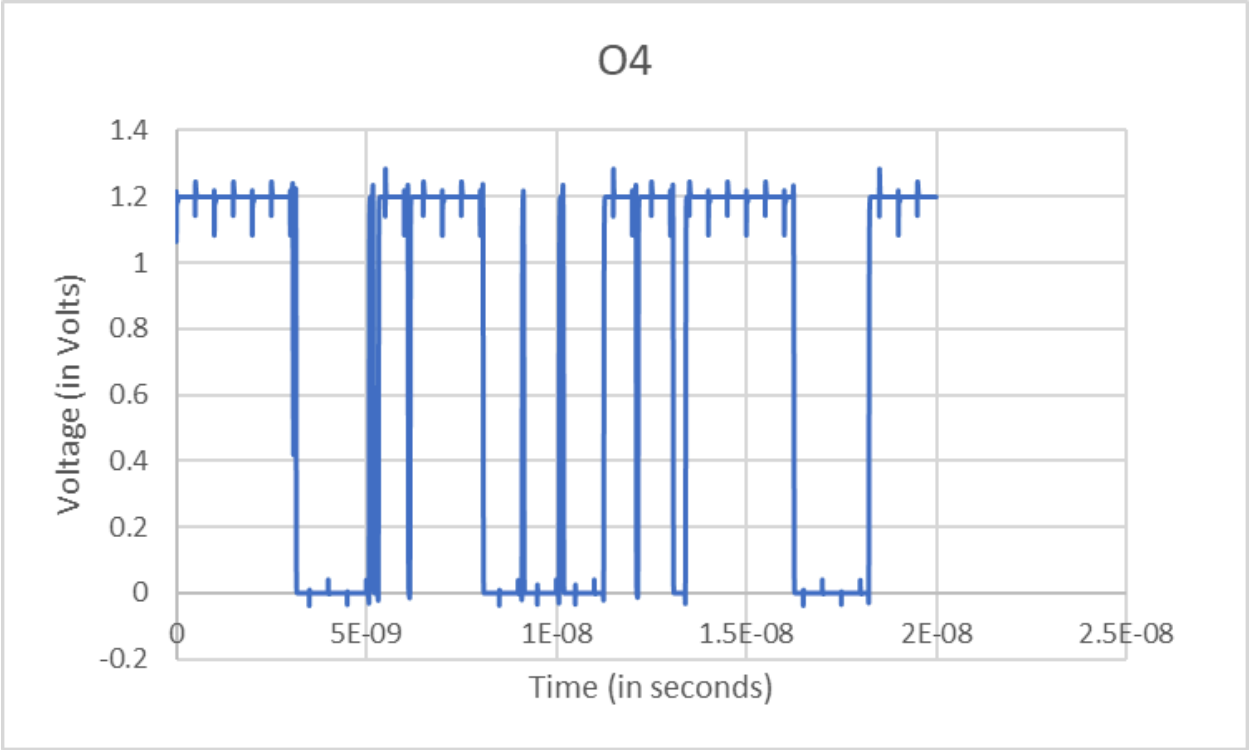
Output O (O0 - O7) (8 bit):

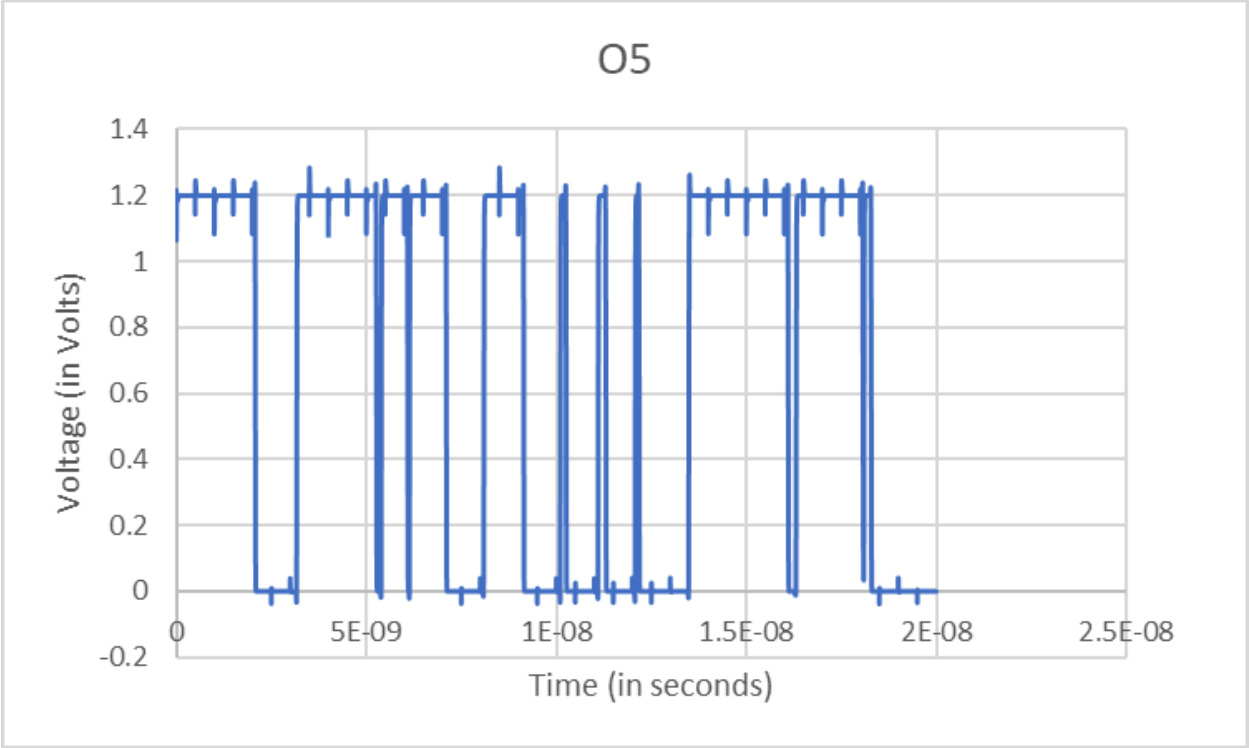


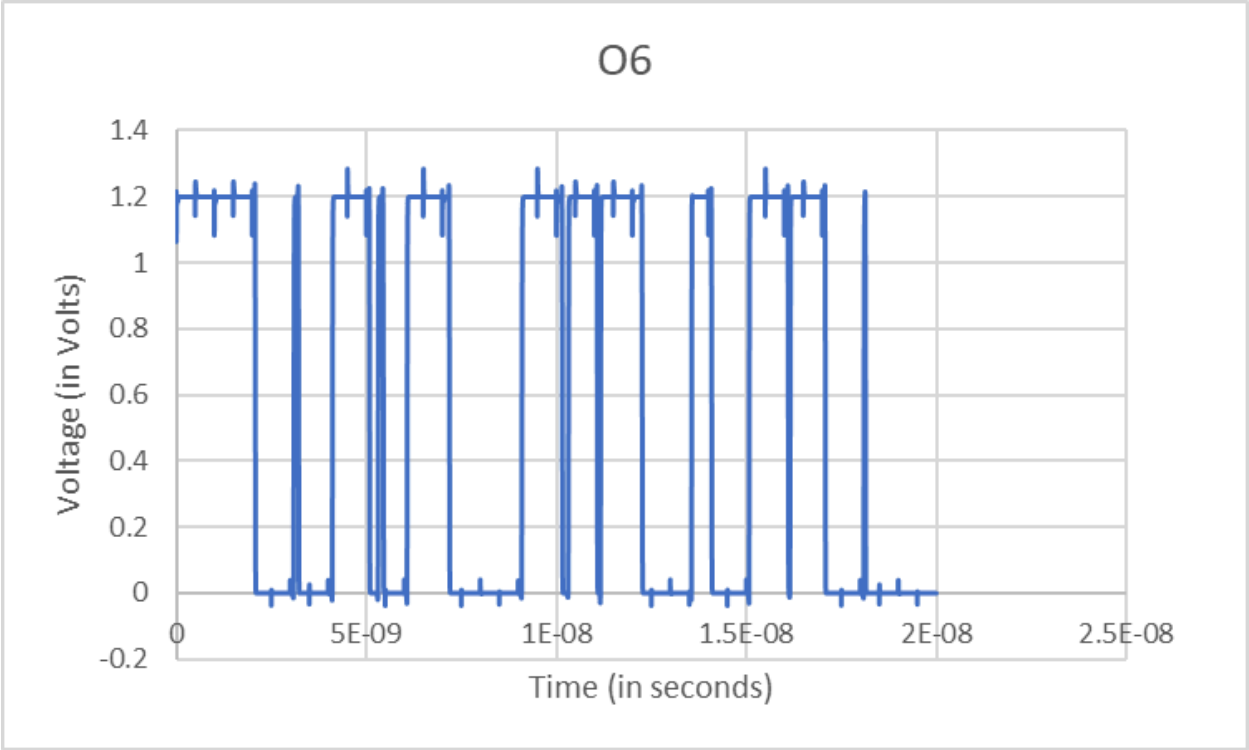


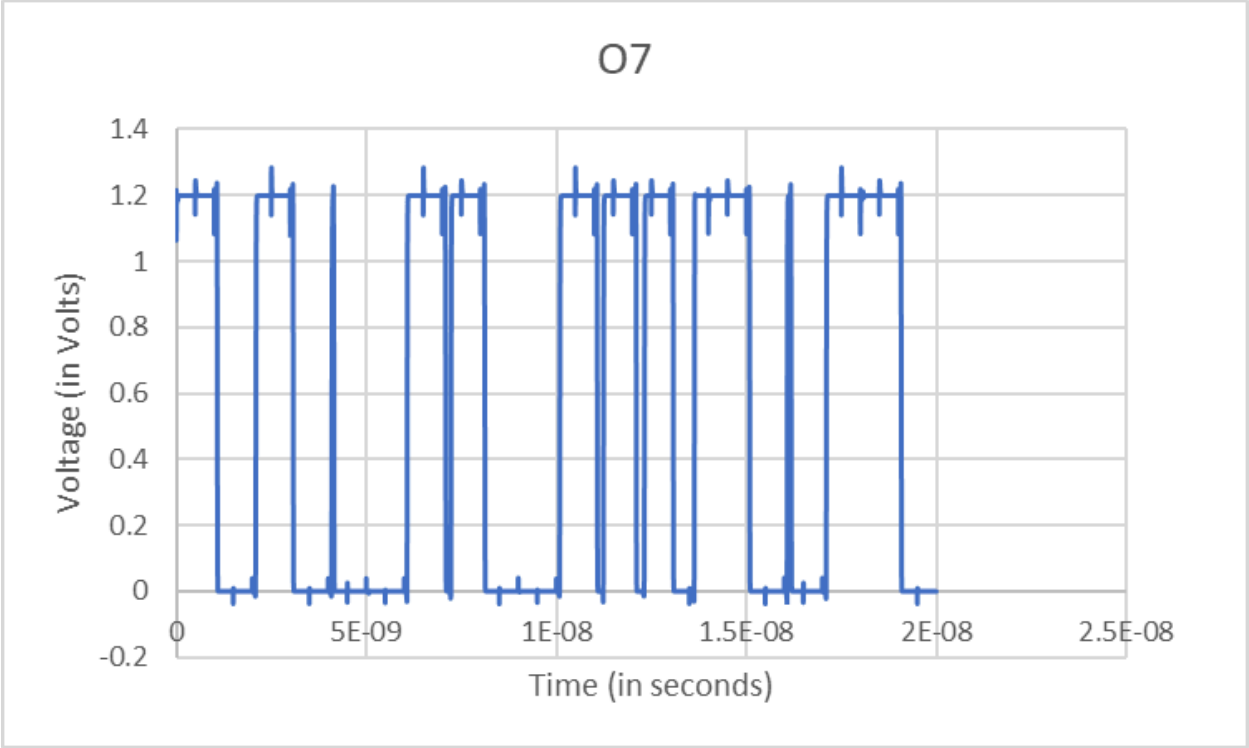

O2
1.4
1.2
1
0.8
0.6
0.4
0.2
0
-0.2
Voltage (in Volts)
0
5E-09
1E-08
1.5E-08
2E-08
2.5E-08
Time (in seconds)


O3
1.4
1.2
1
0.8
0.6
0.4
0.2
0
-0.2
Voltage (in Volts)
0
5E-09
1E-08
1.5E-08
2E-08
2.5E-08
Time (in seconds)

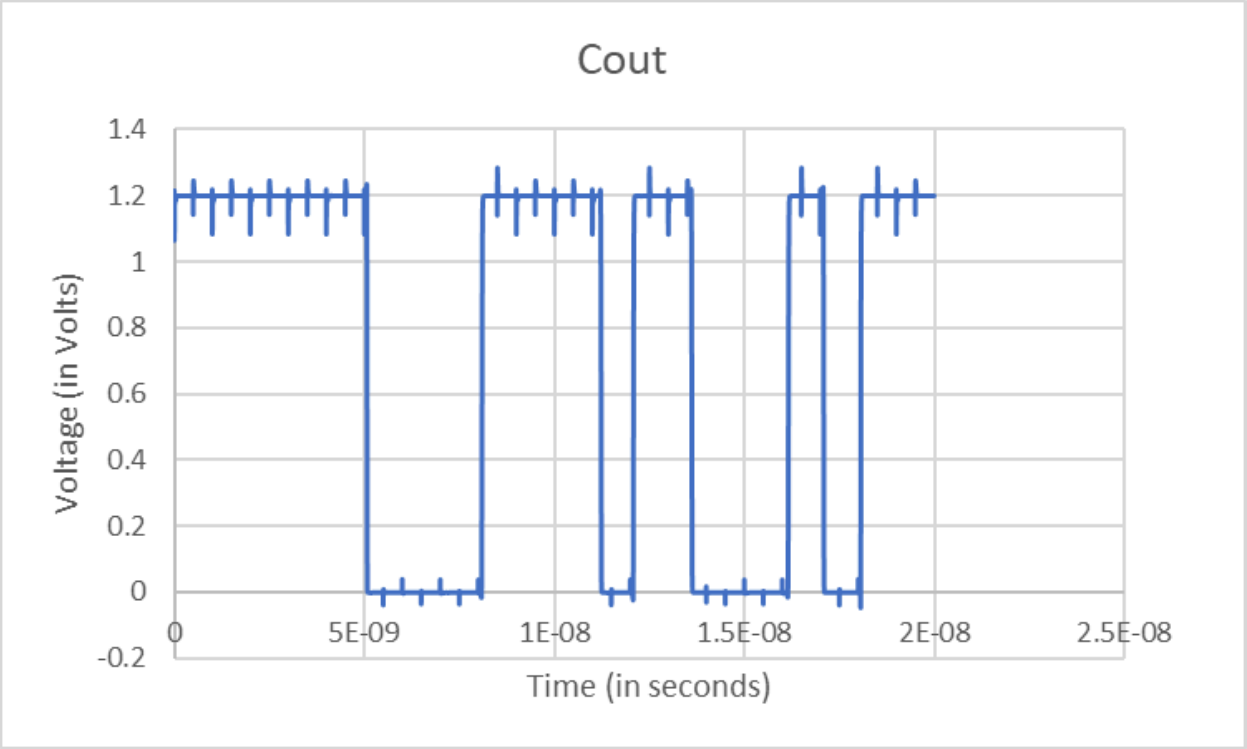

O4
1.4
1.2
1
0.8
0.6
0.4
0.2
0
-0.2
Voltage (in Volts)
0
5E-09
1E-08
1.5E-08
2E-08
2.5E-08
Time (in seconds)


O5
1.4
1.2
1
0.8
0.6
0.4
0.2
0
-0.2
Voltage (in Volts)
0
5E-09
1E-08
1.5E-08
2E-08
2.5E-08
Time (in seconds)


O6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
-0.2
Voltage (in Volts)
0
5E-09
1E-08
1.5E-08
2E-08
2.5E-08
Time (in seconds)


O7
1.4
1.2
1
0.8
0.6
0.4
0.2
0
-0.2
Voltage (in Volts)
0
5E-09
1E-08
1.5E-08
2E-08
2.5E-08
Time (in seconds)

Cout (1 bit):



STA

T_{pd} = (4.61364 – 4.10588) ns = **some_value ps**

T_{pcq} = (1.1340 – 1.0000) = **some_value ps**

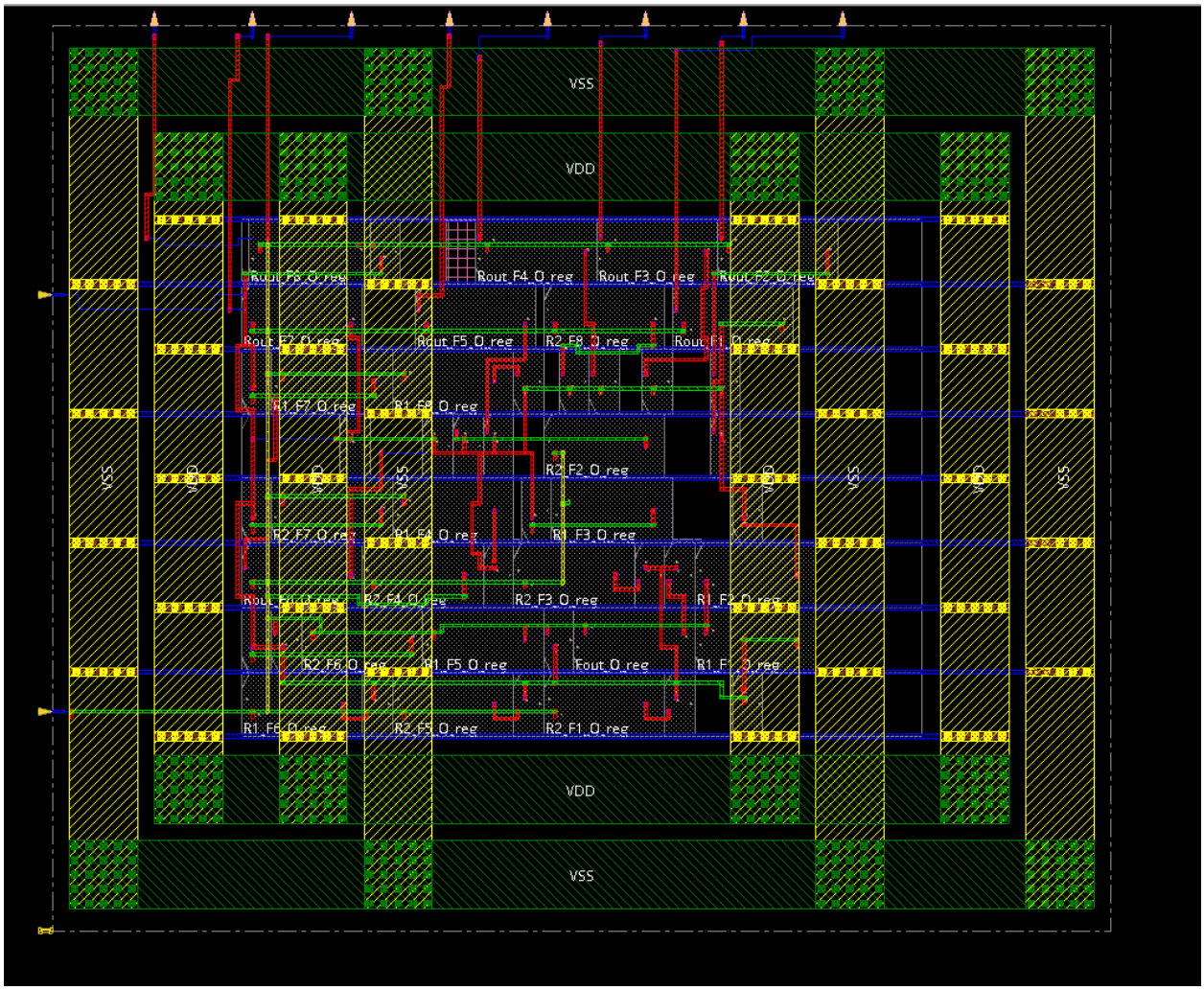
From Assignment 1, for the semi-dynamic flip flop we found that:

t_{setup} = **-20.2247 ps**

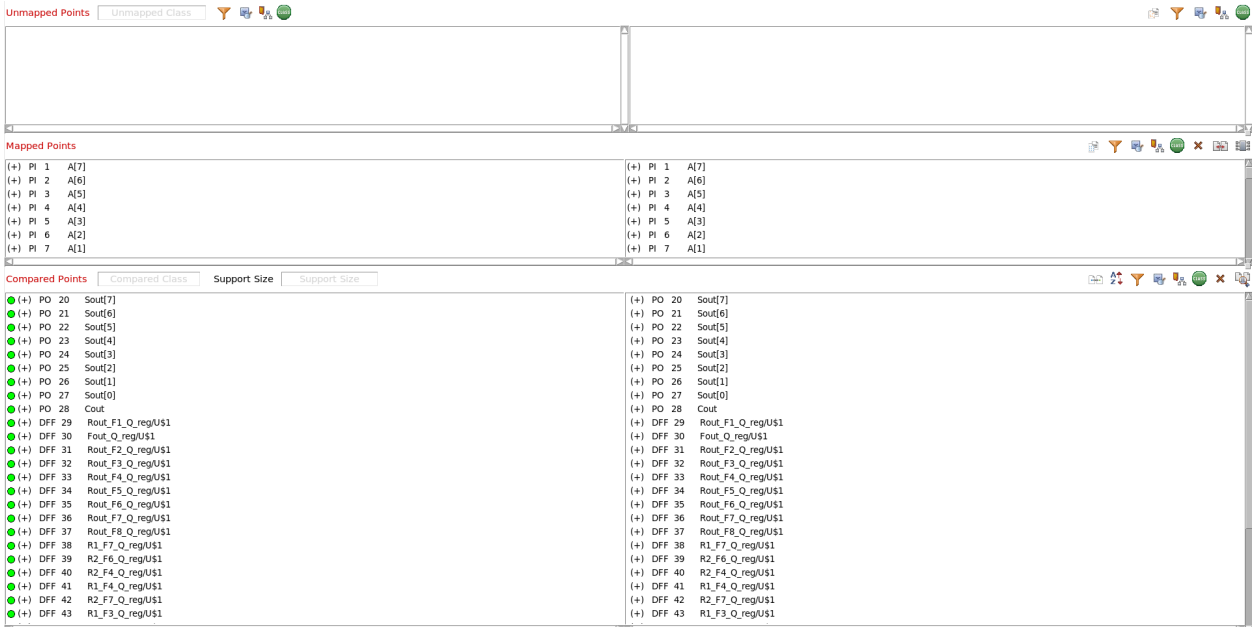
For minimum delay constraint: $T_C \geq t_{setup} + t_{pd} + t_{pcq}$

Hence Tc =

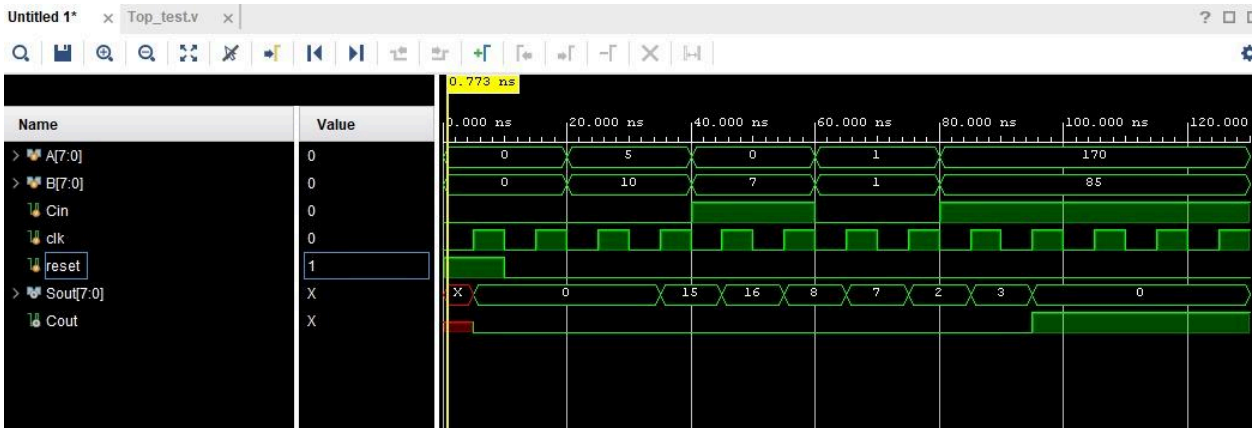
Layout:



Pin Mapping:


Unmapped Points
Unmapped Class
Mapped Points
(+) PI 1 A[7]
(+) PI 2 A[6]
(+) PI 3 A[5]
(+) PI 4 A[4]
(+) PI 5 A[3]
(+) PI 6 A[2]
(+) PI 7 A[1]
Compared Points
Compared Class
Support Size
Support Size
(+) PO 20 Sout[7]
(+) PO 21 Sout[6]
(+) PO 22 Sout[5]
(+) PO 23 Sout[4]
(+) PO 24 Sout[3]
(+) PO 25 Sout[2]
(+) PO 26 Sout[1]
(+) PO 27 Sout[0]
(+) PO 28 Cout
(+) DFF 29 Rout_F1_Q_reg/U$1
(+) DFF 30 Fout_Q_reg/U$1
(+) DFF 31 Rout_F2_Q_reg/U$1
(+) DFF 32 Rout_F3_Q_reg/U$1
(+) DFF 33 Rout_F4_Q_reg/U$1
(+) DFF 34 Rout_F5_Q_reg/U$1
(+) DFF 35 Rout_F6_Q_reg/U$1
(+) DFF 36 Rout_F7_Q_reg/U$1
(+) DFF 37 Rout_F8_Q_reg/U$1
(+) DFF 38 R1_F7_Q_reg/U$1
(+) DFF 39 R2_F6_Q_reg/U$1
(+) DFF 40 R2_F4_Q_reg/U$1
(+) DFF 41 R1_F4_Q_reg/U$1
(+) DFF 42 R2_F7_Q_reg/U$1
(+) DFF 43 R1_F3_Q_reg/U$1

Behavioural Simulation of the adder:



Code (Verilog)

Top Module:

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 03/26/2025 11:00:44 AM
// Design Name:
// Module Name: Top
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module Top(
    input [7:0] A,
    input [7:0] B,
```

```
    input Cin,
    input clk,
    input reset,
    output [7:0] Sout,
    output Cout
    );

    wire [7:0] A_reg, B_reg;

    Register R1(A, clk, reset, A_reg);
    Register R2(B, clk, reset, B_reg);

    wire [7:0] Out;
    wire carryout;

    RippleCarryAdder RCA(A_reg, B_reg, Cin, Out, carryout);

    Register Rout(Out, clk, reset, Sout);
    FlipFlop Fout(carryout, clk, reset, Cout);
endmodule
```

Adder Module:

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 03/25/2025 08:59:05 PM
// Design Name:
```

```
// Module Name: Adder
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////
module Adder(
    input A,
    input B,
    input Cin,
    output S,
    output Cout
);

    assign S = A ^ B ^ Cin;  // XOR for sum
    assign Cout = (A & B) | (B & Cin) | (A & Cin); // Corrected Carry-out

endmodule
```

Ripple Carry Adder:

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
```

```
// Company:
// Engineer:
//
// Create Date: 03/25/2025 09:16:49 PM
// Design Name:
// Module Name: RippleCarryAdder
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module RippleCarryAdder(
    input [7:0] A,
    input [7:0] B,
    input Cin,
    output [7:0] Out,
    output Cout
    );
```

```
    wire C1;
    Adder A1(A[0], B[0], Cin, Out[0], C1);

    wire C2;
    Adder A2(A[1], B[1], C1, Out[1], C2);

    wire C3;
    Adder A3(A[2], B[2], C2, Out[2], C3);

    wire C4;
    Adder A4(A[3], B[3], C3, Out[3], C4);

    wire C5;
    Adder A5(A[4], B[4], C4, Out[4], C5);

    wire C6;
    Adder A6(A[5], B[5], C5, Out[5], C6);

    wire C7;
    Adder A7(A[6], B[6], C6, Out[6], C7);

    Adder A8(A[7], B[7], C7, Out[7], Cout);
endmodule
```

Flip_Flop Module:

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
```

```
//
// Create Date: 03/25/2025 08:50:45 PM
// Design Name:
// Module Name: FlipFlop
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module FlipFlop(
    input D,
    input clk,
    input reset,
    output reg Q
    );

    always @(posedge clk)
    begin
        if (reset == 1'b1)
        begin
```

```
        Q <= 1'b0;
    end
    else
    begin
        Q <= D;
    end
  end
endmodule
```

Register Module:

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 03/25/2025 08:54:37 PM
// Design Name:
// Module Name: Register
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
```

//

```
module Register(
    input [7:0] Din,
    input clk,
    input reset,
    output [7:0] Dout
    );

    FlipFlop F1(Din[7], clk, reset, Dout[7]);
    FlipFlop F2(Din[6], clk, reset, Dout[6]);
    FlipFlop F3(Din[5], clk, reset, Dout[5]);
    FlipFlop F4(Din[4], clk, reset, Dout[4]);
    FlipFlop F5(Din[3], clk, reset, Dout[3]);
    FlipFlop F6(Din[2], clk, reset, Dout[2]);
    FlipFlop F7(Din[1], clk, reset, Dout[1]);
    FlipFlop F8(Din[0], clk, reset, Dout[0]);
endmodule
```

TestBench:

Top Module:

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 03/26/2025 04:57:16 PM
// Design Name:
// Module Name: Top_test
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////

`timescale 1ns / 1ps

module Top_test;
```

```
// Inputs
reg [7:0] A;
reg [7:0] B;
reg Cin;
reg clk;
reg reset;

// Outputs
wire [7:0] Sout;
wire Cout;

// Instantiate the Top module
Top uut (
    .A(A),
    .B(B),
    .Cin(Cin),
    .clk(clk),
    .reset(reset),
    .Sout(Sout),
    .Cout(Cout)
);

// Clock generation: 10ns period (50MHz)
always #5 clk = ~clk;

// Test sequence
initial begin
    // Initialize inputs
    clk = 0;
```

```
reset = 1;
A = 8'b00000000;
B = 8'b00000000;
Cin = 0;

// Apply reset
#10 reset = 0;

// Test case 1: A = 5, B = 10, Cin = 0
#10 A = 8'b00000101;  // 5
   B = 8'b00001010;  // 10
   Cin = 0;

// Test case 2: A = 100, B = 200, Cin = 1
#20 A = 8'b00000000;  // 100
   B = 8'b00000111;  // 200
   Cin = 1;

// Test case 3: A = 255, B = 1, Cin = 0 (Checking Carry)
#20 A = 8'b00000001;  // 255
   B = 8'b00000001;  // 1
   Cin = 0;

// Test case 4: Random values
#20 A = 8'b10101010;
   B = 8'b01010101;
   Cin = 1;

// End simulation
```

```
    #50 $finish;
  end

  // Monitor outputs
  initial begin
    $monitor("Time=%0t | A=%b | B=%b | Cin=%b | Sout=%b | Cout=%b",
          $time, A, B, Cin, Sout, Cout);
  end

endmodule
```

Genus Reports

Timing:

```
============================================================
 Generated by:          Genus(TM) Synthesis Solution 21.10-p002_1
 Generated on:          Mar 26 2025  12:07:37 pm
 Module:                bottom
 Technology library:    slow_vdd1v0 1.0
 Operating conditions:  PVT_0P9V_125C (balanced_tree)
 Wireload mode:         enclosed
 Area mode:             timing library
============================================================

     Pin            Type       Fanout Load Slew Delay Arrival
                               (fF) (ps)  (ps)   (ps)
-------------------------------------------------------------------------
(clock clk)         launch                          0 R
R1_F8_Q_reg/CK                          100    +0       0 R
R1_F8_Q_reg/Q       DFFHQX1         1  0.8   27  +228     228 R
g531__5115/B                              +0     228
g531__5115/CO       ADDFX1          1  0.8   43  +196     424 R
g528__6131/A                              +0     424
g528__6131/CO       ADDFX1          1  0.8   43  +206     630 R
g525__8246/A                              +0     630
g525__8246/CO       ADDFX1          1  0.6   39  +204     834 R
g522__1705/CI                             +0     834
g522__1705/CO       ADDFX1          1  0.6   39  +186    1020 R
g519__1617/CI                             +0    1020
```

```
g519__1617/CO       ADDFX1          1  0.6   39  +186    1206 R
g516__6783/CI                         +0    1206
g516__6783/CO       ADDFX1          1  0.6   39  +186    1392 R
g513__8428/CI                         +0    1392
g513__8428/CO       ADDFX1          1  0.6   39  +186    1578 R
g510__6260/CI                         +0    1578
g510__6260/S        ADDFX1          1  0.2   33  +255    1833 R
g508__2398/AN                         +0    1833
g508__2398/Y        NOR2BX1         1  0.2   34   +89    1922 R
Rout_F1_Q_reg/D  <<<  DFFQXL                  +0    1922
Rout_F1_Q_reg/CK     setup                  100   +96    2018 R
- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
(clock clk)          capture                       10000 R
                     uncertainty                  -10    9990 R
---------------------------------------------------------------------
Cost Group   : 'clk' (path_group 'clk')
Timing slack :    7972ps
Start-point  : R1_F8_Q_reg/CK
End-point    : Rout_F1_Q_reg/D
```

Power

Instance: /bottom

Power Unit: W

PDB Frames: /stim#0/frame#0

```
-----------------------------------------------------------------------
  Category       Leakage     Internal    Switching       Total    Row%
-----------------------------------------------------------------------
    memory    0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
  register    2.57161e-09  4.92196e-06  9.88200e-08  5.02335e-06  77.88%
     latch    0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
```

```
    logic    1.71465e-09  8.05168e-07  2.15014e-07  1.02190e-06  15.84%
     bbox    0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
    clock    0.00000e+00  0.00000e+00  4.05000e-07  4.05000e-07   6.28%
      pad    0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
       pm    0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
---------------------------------------------------------------------------
  Subtotal    4.28627e-09  5.72713e-06  7.18834e-07  6.45025e-06 100.00%
Percentage         0.07%       88.79%       11.14%      100.00% 100.00%
---------------------------------------------------------------------------
```

Area

```
==============================================================
  Generated by:           Genus(TM) Synthesis Solution 21.10-p002_1
  Generated on:           Mar 26 2025  12:07:37 pm
  Module:                 bottom
  Technology library:     slow_vdd1v0 1.0
  Operating conditions:   PVT_0P9V_125C (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
==============================================================

Instance Module  Cell Count  Cell Area  Net Area   Total Area   Wireload
-----------------------------------------------------------------------------
bottom                 58    212.040     0.000      212.040 <none> (D)
  (D) = wireload is default in technology library
```

Power Report:

Power Net Detected:

Voltage	Name
0V	VSS
0.9V	VDD

Using Power View: setup.

Load RC corner of view setup

Begin Power Analysis

0V	VSS
0.9V	VDD

Begin Processing Timing Library for Power Calculation

Ended Processing Timing Library for Power Calculation: (cpu=0:00:00, real=0:00:00, mem(process/total/peak)=3086.73MB/unknown/unknown)

Begin Processing Power Net/Grid for Power Calculation

Ended Processing Power Net/Grid for Power Calculation: (cpu=0:00:00, real=0:00:00, mem(process/total/peak)=3086.73MB/unknown/unknown)

Begin Processing Timing Window Data for Power Calculation

clk(100MHz) CK: assigning clock clk to net clk

Ended Processing Timing Window Data for Power Calculation: (cpu=0:00:00, real=0:00:00, mem(process/total/peak)=3086.73MB/unknown/unknown)

Begin Processing User Attributes

Ended Processing User Attributes: (cpu=0:00:00, real=0:00:00, mem(process/total/peak)=3086.73MB/unknown/unknown)

Begin Processing Signal Activity

Starting Levelizing

2025-Mar-26 12:05:09 (2025-Mar-26 16:05:09 GMT)

2025-Mar-26 12:05:09 (2025-Mar-26 16:05:09 GMT): 10%

2025-Mar-26 12:05:09 (2025-Mar-26 16:05:09 GMT): 20%

2025-Mar-26 12:05:09 (2025-Mar-26 16:05:09 GMT): 30%

2025-Mar-26 12:05:09 (2025-Mar-26 16:05:09 GMT): 40%

2025-Mar-26 12:05:09 (2025-Mar-26 16:05:09 GMT): 50%

2025-Mar-26 12:05:09 (2025-Mar-26 16:05:09 GMT): 60%

2025-Mar-26 12:05:09 (2025-Mar-26 16:05:09 GMT): 70%

2025-Mar-26 12:05:09 (2025-Mar-26 16:05:09 GMT): 80%

2025-Mar-26 12:05:09 (2025-Mar-26 16:05:09 GMT): 90%

Finished Levelizing

2025-Mar-26 12:05:09 (2025-Mar-26 16:05:09 GMT)

Starting Activity Propagation

2025-Mar-26 12:05:09 (2025-Mar-26 16:05:09 GMT)

** INFO: (VOLTUS_POWR-1356): No default input activity has been set. Defaulting to 0.2.

Use 'set_default_switching_activity -input_activity' command to change the default activity value.

2025-Mar-26 12:05:09 (2025-Mar-26 16:05:09 GMT): 10%

2025-Mar-26 12:05:09 (2025-Mar-26 16:05:09 GMT): 20%

2025-Mar-26 12:05:09 (2025-Mar-26 16:05:09 GMT): 30%

Finished Activity Propagation

2025-Mar-26 12:05:09 (2025-Mar-26 16:05:09 GMT)

Ended Processing Signal Activity: (cpu=0:00:00, real=0:00:00, mem(process/total/peak)=3086.73MB/unknown/unknown)

Begin Power Computation

# of cell(s) missing both power/leakage table: 0

# of cell(s) missing power table: 0

# of cell(s) missing leakage table: 0

Starting Calculating power

2025-Mar-26 12:05:09 (2025-Mar-26 16:05:09 GMT)

... Calculating switching power

2025-Mar-26 12:05:09 (2025-Mar-26 16:05:09 GMT): 10%

2025-Mar-26 12:05:09 (2025-Mar-26 16:05:09 GMT): 20%

2025-Mar-26 12:05:09 (2025-Mar-26 16:05:09 GMT): 30%

2025-Mar-26 12:05:09 (2025-Mar-26 16:05:09 GMT): 40%

2025-Mar-26 12:05:09 (2025-Mar-26 16:05:09 GMT): 50%

... Calculating internal and leakage power

2025-Mar-26 12:05:09 (2025-Mar-26 16:05:09 GMT): 60%

2025-Mar-26 12:05:09 (2025-Mar-26 16:05:09 GMT): 70%

2025-Mar-26 12:05:09 (2025-Mar-26 16:05:09 GMT): 80%

2025-Mar-26 12:05:09 (2025-Mar-26 16:05:09 GMT): 90%

Finished Calculating power

2025-Mar-26 12:05:09 (2025-Mar-26 16:05:09 GMT)

# of MSMV cell(s) missing power_level: 0

Ended Power Computation: (cpu=0:00:00, real=0:00:00, mem(process/total/peak)=3086.73MB/unknown/unknown)

Begin Processing User Attributes

Begin Processing set_power

Ended Processing set_power: (cpu=0:00:00, real=0:00:00,

mem(process/total/peak)=3086.73MB/unknown/unknown)

Ended Processing User Attributes: (cpu=0:00:00, real=0:00:00, mem(process/total/peak)=3086.73MB/unknown/unknown)

Ended Power Analysis: (cpu=0:00:00, real=0:00:00, mem(process/total/peak)=3086.73MB/unknown/unknown)

Begin Boundary Leakage Calculation

Ended Boundary Leakage Calculation: (cpu=0:00:00, real=0:00:00,

mem(process/total/peak)=3088.07MB/unknown/unknown)

Begin Static Power Report Generation

*----------

* Innovus 23.13-s082_1 (64bit) 11/13/2024 13:42 (Linux 3.10.0-693.el7.x86_64)

*

*

* Date & Time: 2025-Mar-26 12:05:09 (2025-Mar-26 16:05:09 GMT)

*

*----------

```
*
*        Design: bottom
*
*        Liberty Libraries used:
*                setup: ../lib/slow_vdd1v0_basicCells.lib
*
*        Parasitic Files used:
*
*     Power View : setup
*
*     User-Defined Activity : N.A.
*
*     Activity File: N.A.
*
*     Hierarchical Global Activity: N.A.
*
*     Global Activity: N.A.
*
*     Sequential Element Activity: 0.200000
*
*     Primary Input Activity: 0.200000
*
*     Default icg ratio: N.A.
*
*     Global Comb ClockGate Ratio: N.A.
*
*        Power Units = 1mW
*
*        Time Units = 1e-09 secs
```

```
*
*      report_power
*
-----------------------------------------------------------------------------
*
```

Total Power

```
-----------------------------------------------------------------------------
Total Internal Power:        0.00616537           90.6891%
Total Switching Power:       0.00062870           9.2478%
Total Leakage Power:         0.00000429           0.0631%
Total Power:                 0.00679836
-----------------------------------------------------------------------------
```

Group	Internal Power	Switching Power	Leakage Power	Total Power	Percentage (%)
Sequential	0.005044	0.0002677	2.571e-06	0.005314	78.17
Macro	0	0	0	0	0
IO	0	0	0	0	0
Combinational	0.001121	0.000361	1.718e-06	0.001484	21.83
Clock (Combinational)	0	0	0	0	0
Clock (Sequential)	0	0	0	0	0
Total	0.006165	0.0006287	4.288e-06	0.006798	100

Rail	Voltage	Internal Power	Switching Power	Leakage Power	Total Power	Percentage (%)
VDD	0.9	0.006165	0.0006287	4.288e-06	0.006798	100

---

* Power Distribution Summary:

* Highest Average Power: R1_F6_Q_reg (DFFHQX1): 0.0002376

* Highest Leakage Power: R1_F7_Q_reg (DFFHQX1): 1.205e-07

* Total Cap: 6.22814e-14 F

* Total instances in design: 58

* Total instances in design with no power: 0

* Total instances in design with no activty: 0

* Total Fillers and Decap: 0

** INFO: (VOLTUS_POWR-3465): There are 0 decaps and 0 fillers in the design

Ended Static Power Report Generation: (cpu=0:00:00, real=0:00:00, mem(process/total/peak)=3088.07MB/unknown/unknown)

Bottom Report:

```
#####################################################################
#  Generated by:      Cadence Innovus 23.13-s082_1
#  OS:                Linux x86_64(Host ID cadencea16)
```

```
#  Generated on:      Wed Mar 26 12:04:45 2025
#  Design:            bottom
#  Command:           report_timing > bottom_report.txt
#####################################################################
Path 1: MET Setup Check with Pin Rout_F1_Q_reg/CK
Endpoint:   Rout_F1_Q_reg/D (^) checked with  leading edge of 'clk'
Beginpoint: R1_F8_Q_reg/Q   (^) triggered by  leading edge of 'clk'
Path Groups: {clk}
Analysis View: setup
Other End Arrival Time          0.001
- Setup                         0.136
+ Phase Shift                  10.000
- Uncertainty                   0.010
= Required Time                 9.855
- Arrival Time                  1.958
= Slack Time                    7.897
     Clock Rise Edge                0.000
     + Clock Network Latency (Prop)  -0.000
     = Beginpoint Arrival Time       -0.000
     +--------------------------------------------------------------------+
     |   Instance   |    Arc     |  Cell   | Delay | Arrival | Required |
     |              |            |         |       |  Time   |   Time   |
     |--------------+------------+---------+-------+---------+----------|
     | R1_F8_Q_reg  | CK ^       |         |       |  -0.000 |    7.897 |
     | R1_F8_Q_reg  | CK ^ -> Q ^  | DFFHQX1 | 0.185 |   0.185 |    8.082 |
     | g531__5115   | B ^ -> CO ^  | ADDFX1  | 0.201 |   0.386 |    8.283 |
     | g528__6131   | A ^ -> CO ^  | ADDFX1  | 0.213 |   0.599 |    8.496 |
     | g525__8246   | A ^ -> CO ^  | ADDFX1  | 0.226 |   0.825 |    8.723 |
     | g522__1705   | CI ^ -> CO ^ | ADDFX1  | 0.206 |   1.031 |    8.928 |
```

g519__1617	CI ^ -> CO ^	ADDFX1	0.190	1.221	9.118
g516__6783	CI ^ -> CO ^	ADDFX1	0.185	1.406	9.303
g513__8428	CI ^ -> CO ^	ADDFX1	0.185	1.591	9.488
g510__6260	CI ^ -> S ^	ADDFX1	0.259	1.850	9.747
g508__2398	AN ^ -> Y ^	NOR2BX1	0.108	1.958	9.855
Rout_F1_Q_reg	D ^	DFFQXL	0.000	1.958	9.855
+--+

Bottom Area:

Hinst Name	Module Name	Inst Count	Total Area
bottom		58	171.103