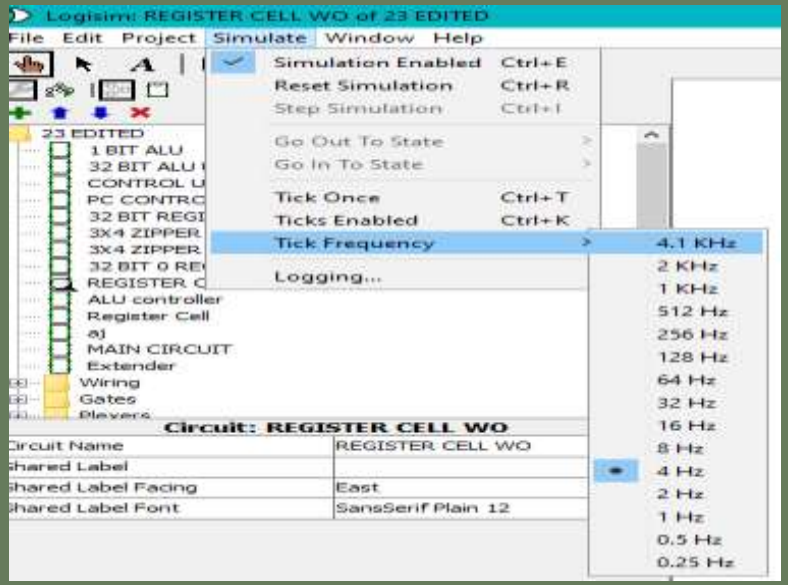
DESIGN OF 32-BIT SINGLE CYCLE MIPS PROCESSOR

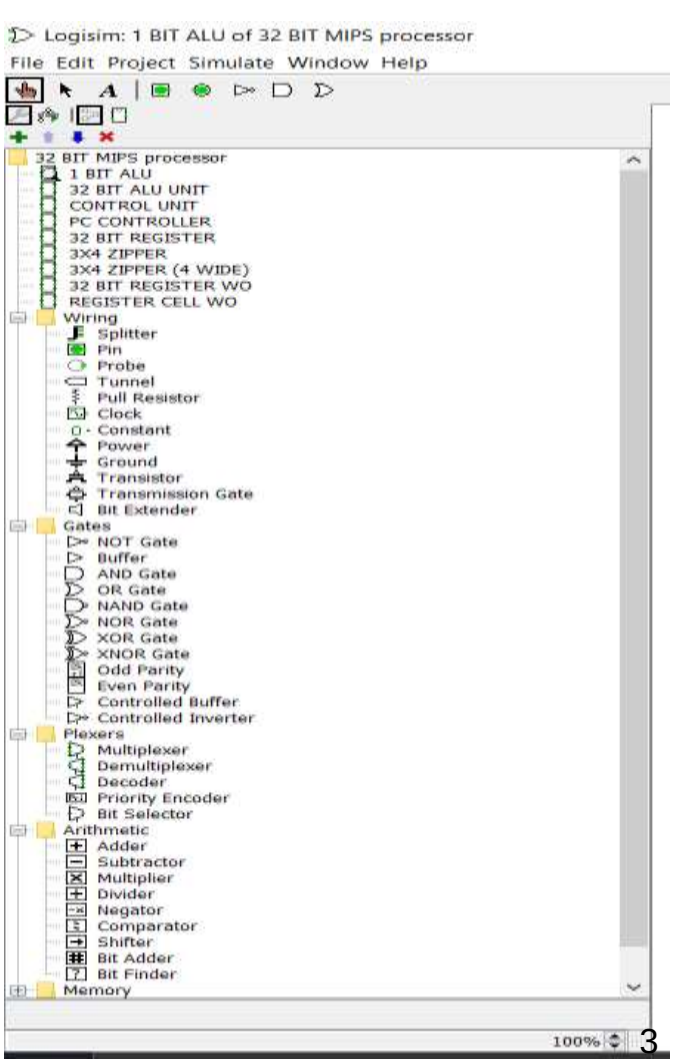
OBJECTIVE :

To design a 32-Bit single cycle processor based on MIPS architecture by designing the basic blocks of the processor using Logisim.

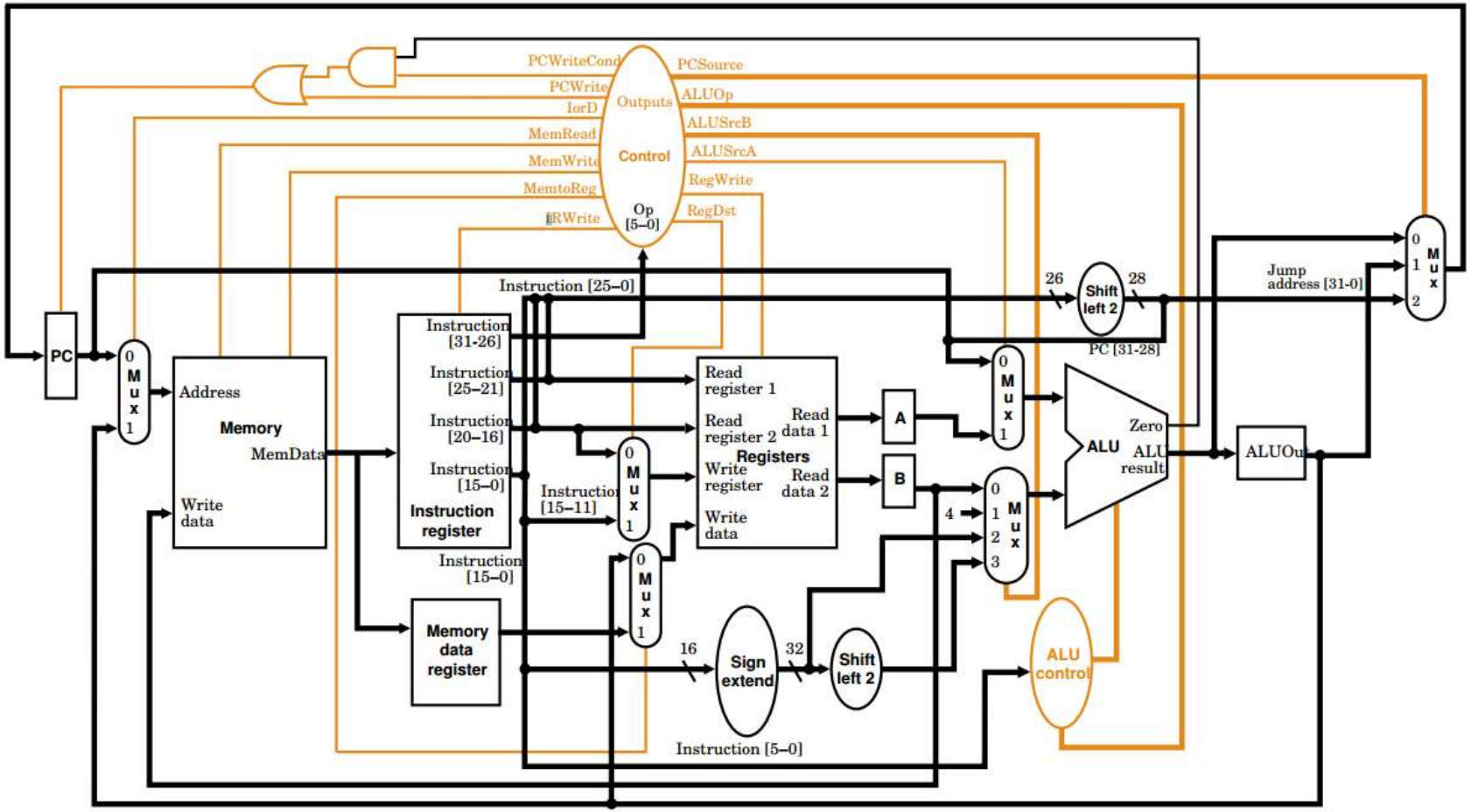
TOOL USED - LOGISIM

Logisim is an educational tool for **designing and simulating digital logic circuits**. With its simple toolbar interface and simulation of circuits as they are built, it is simple enough to facilitate learning the most basic concepts related to logic circuits.





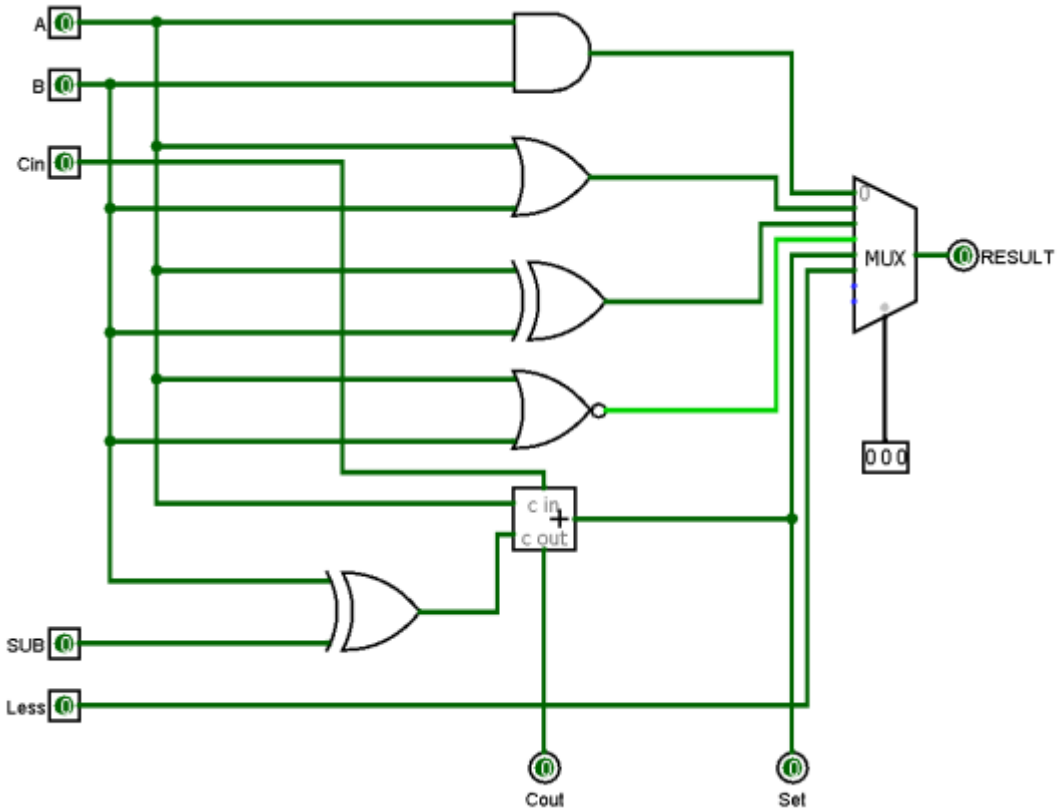
MIPS ARCHITECTURE

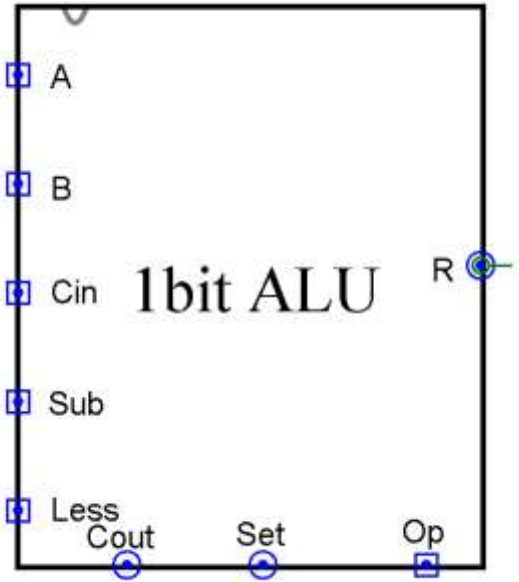


LIST OF BASIC BLOCKS

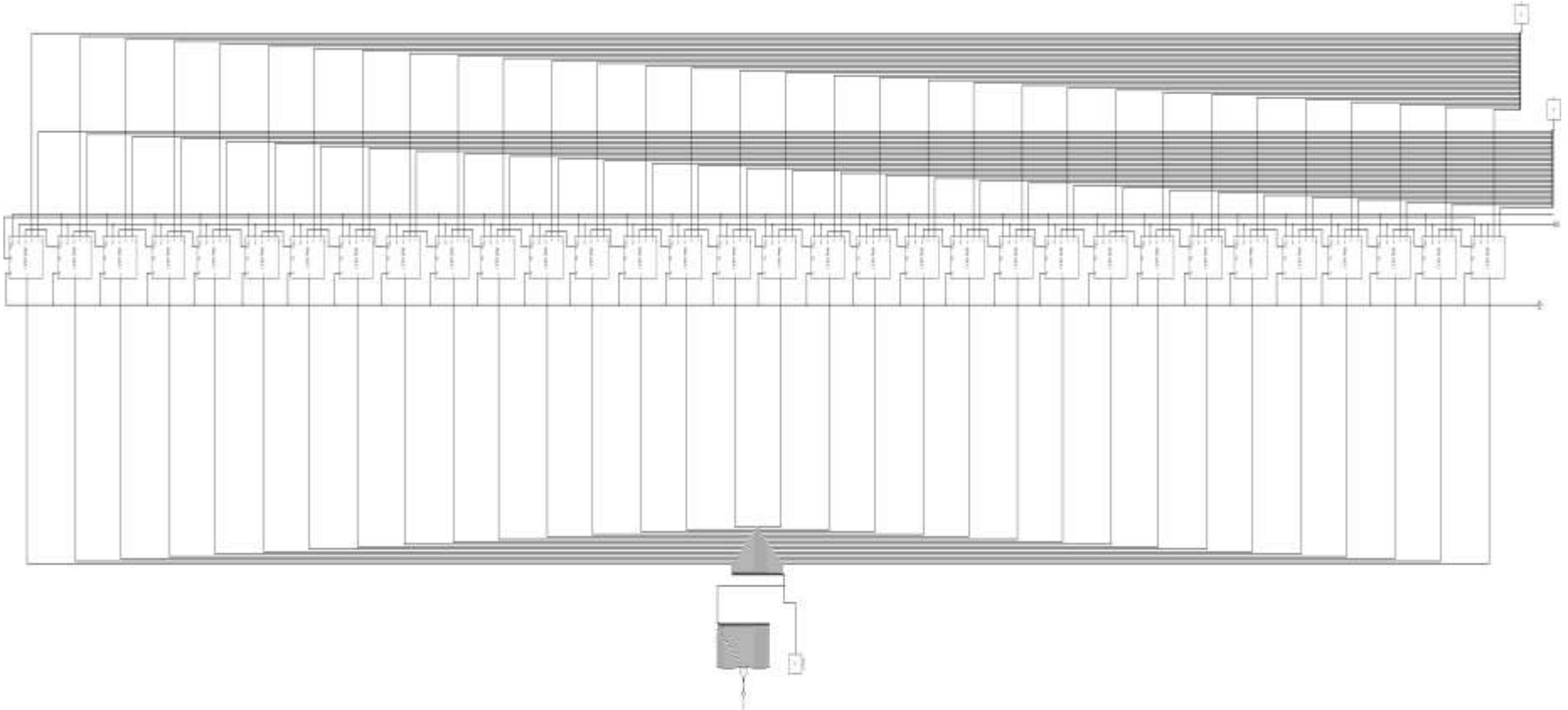
- 1-BIT ALU
- 32 BIT ALU
- PC CONTROLLER
- 3X4 ZIPPER (4 WIDE)
- 3X4 ZIPPER
- CONTROL UNIT
- REGISTER FILE
- 32 BIT REGISTER W/O
- REGISTER CELL W/O
- ALU CONTROLLER
- EXTENDER

1 BIT ALU

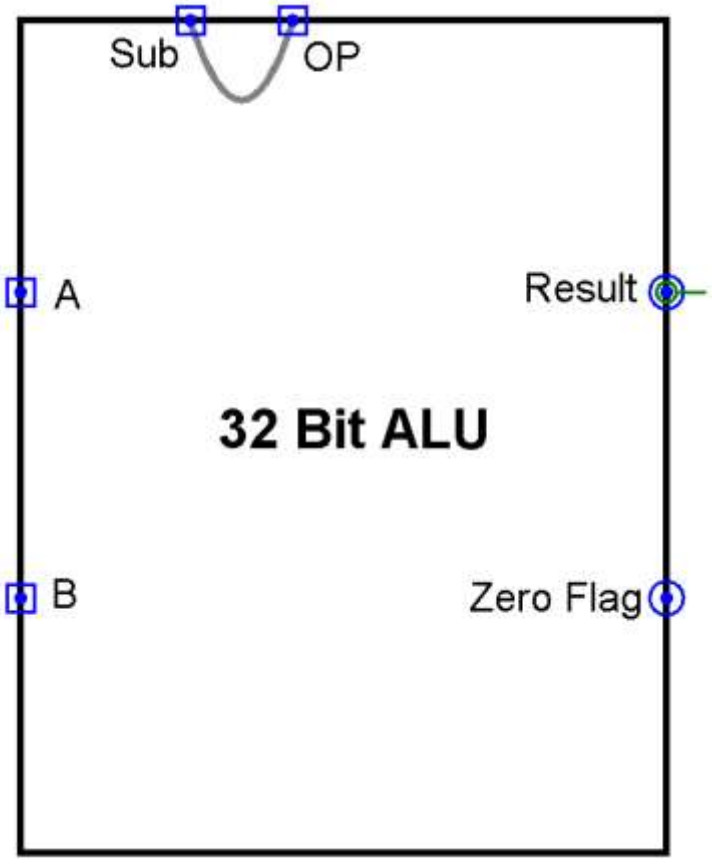

A
B
Cin
SUB
Less
MUX
RESULT
000
c in
c out
Cout
Set


A
B
Cin
Sub
Less
1bit ALU
R
Cout
Set
Op

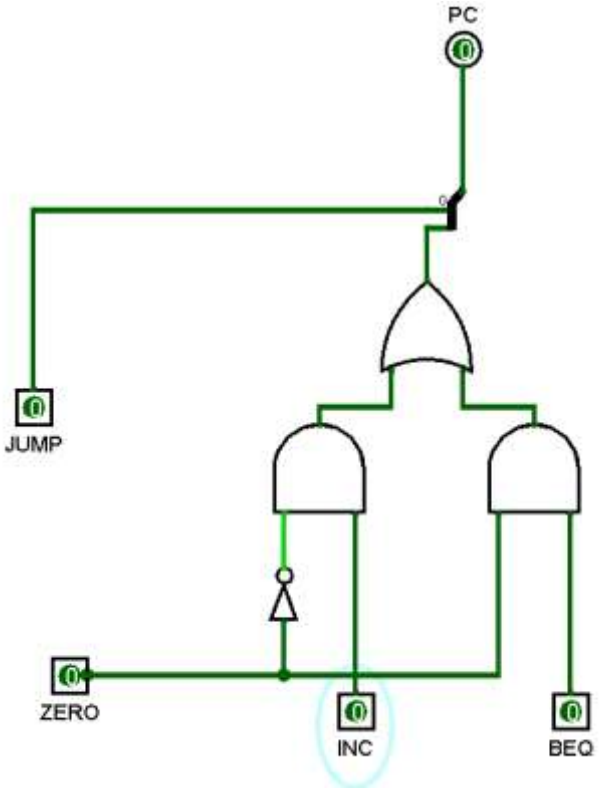
32 BIT ALU

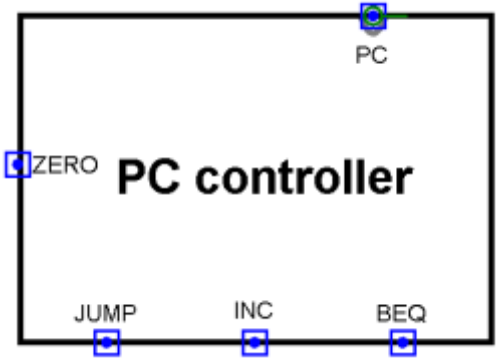


32 BIT ALU

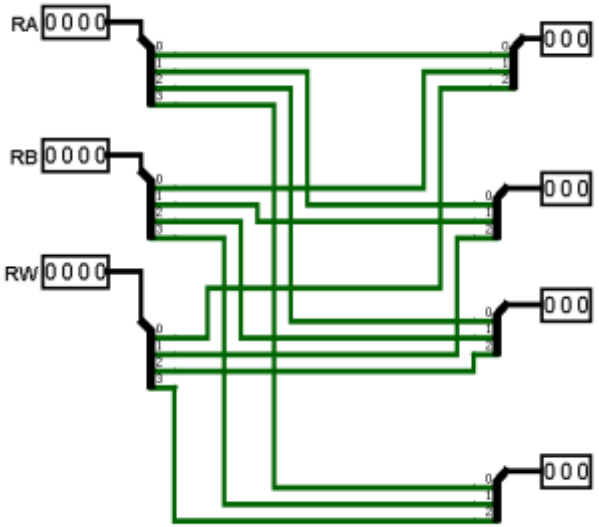


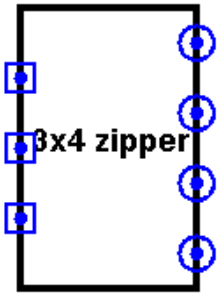
PC CONTROLLER



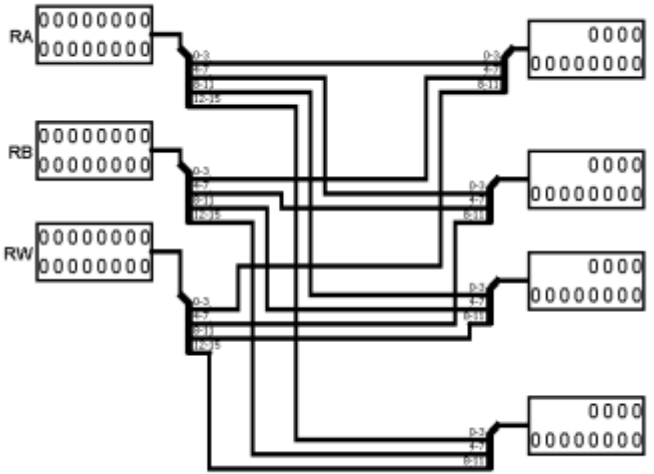


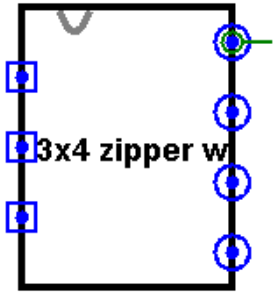
3X4 ZIPPER



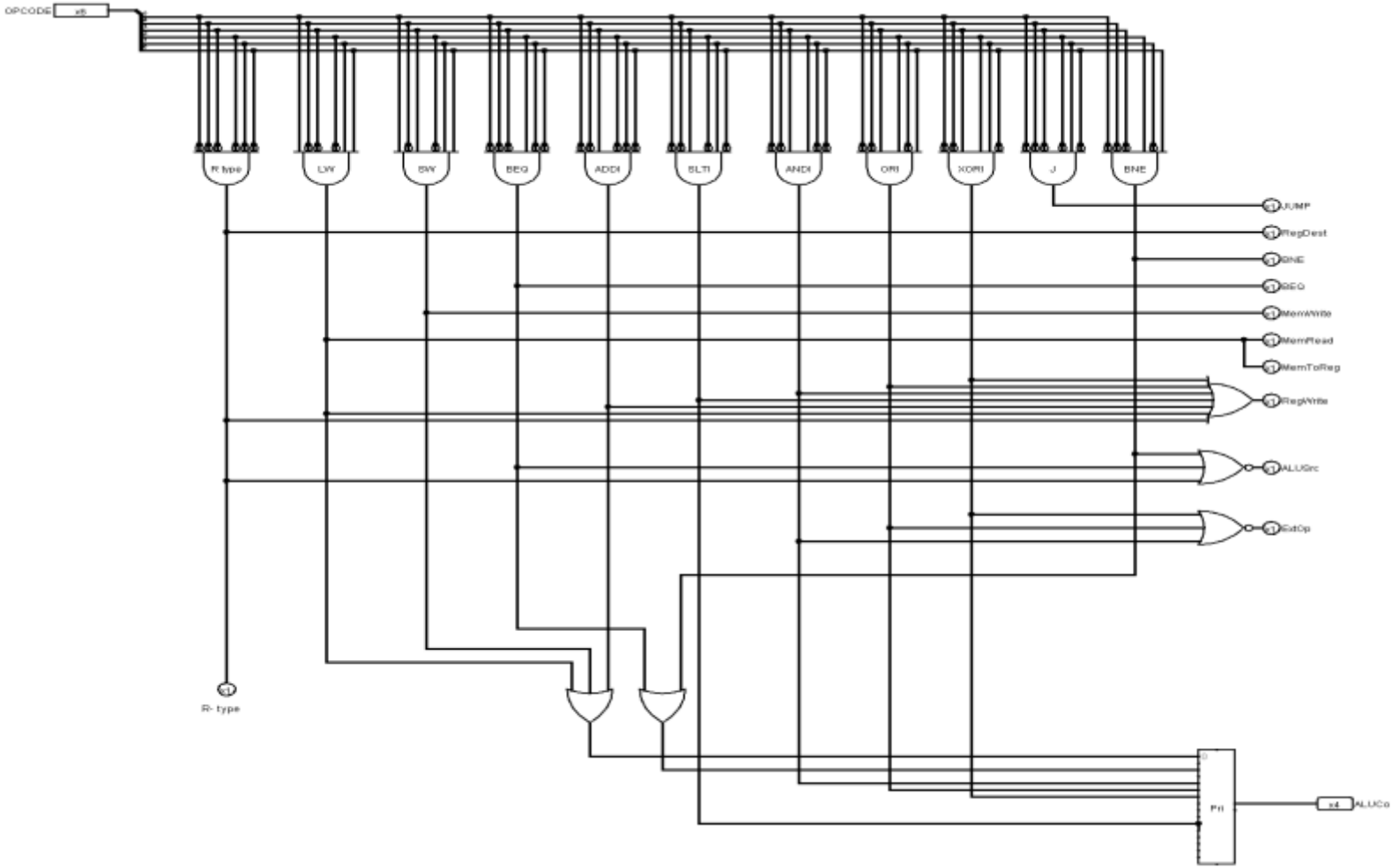


3X4 ZIPPER (4 WIDE)





CONTROL UNIT



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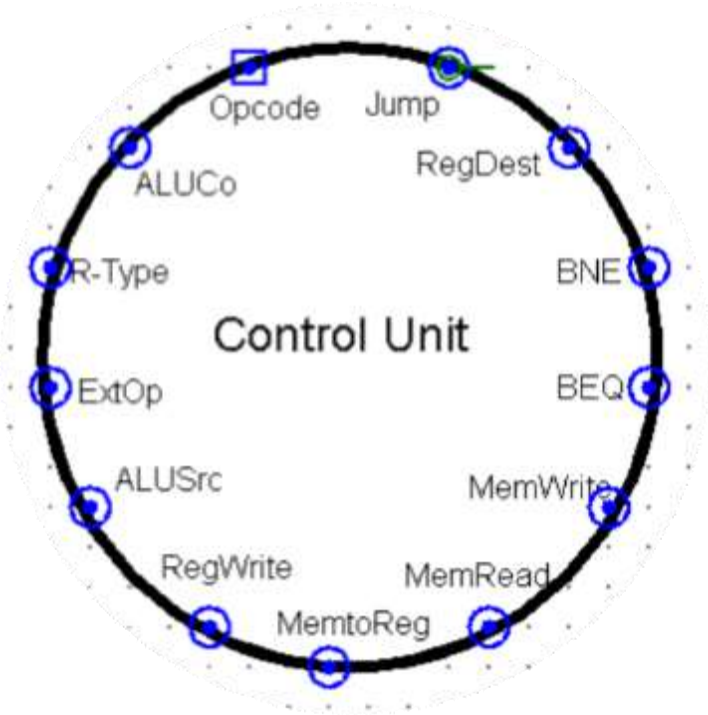
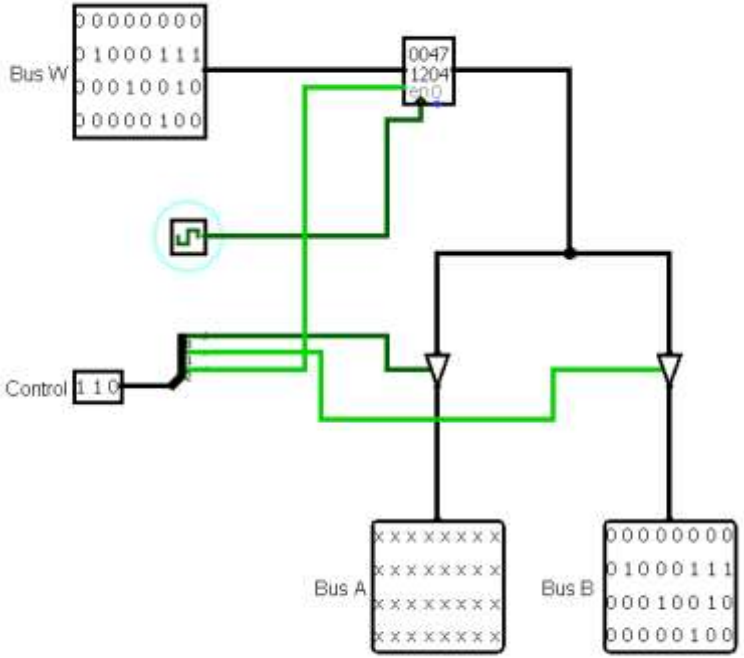
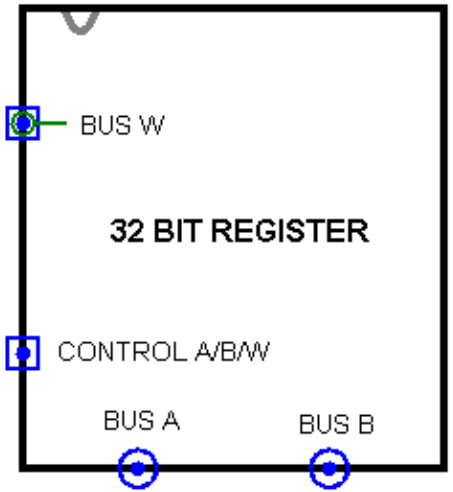
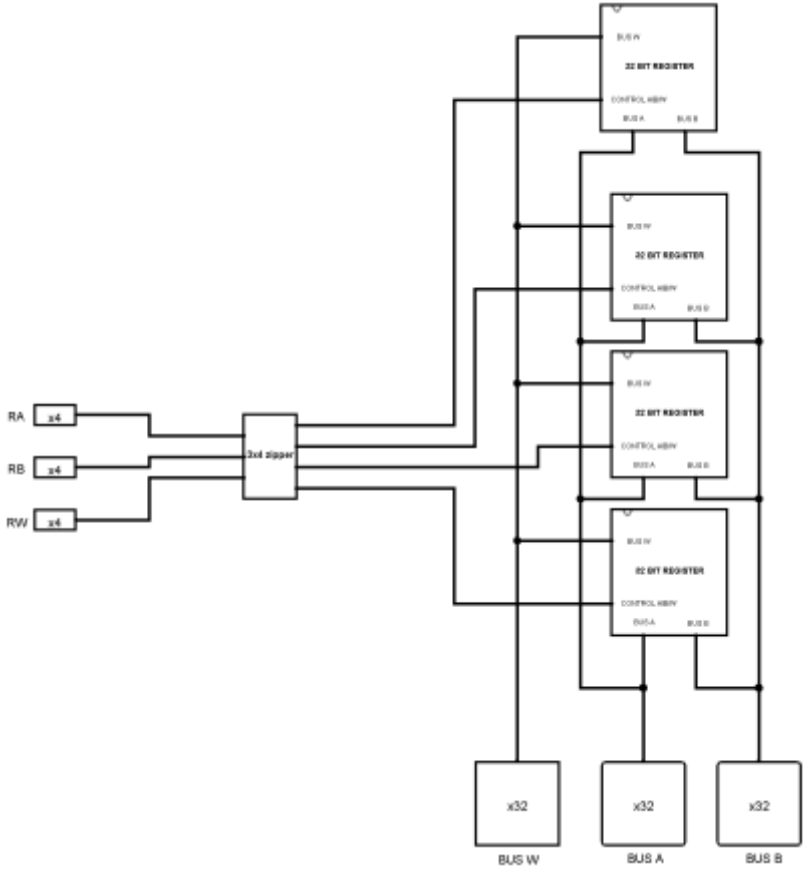


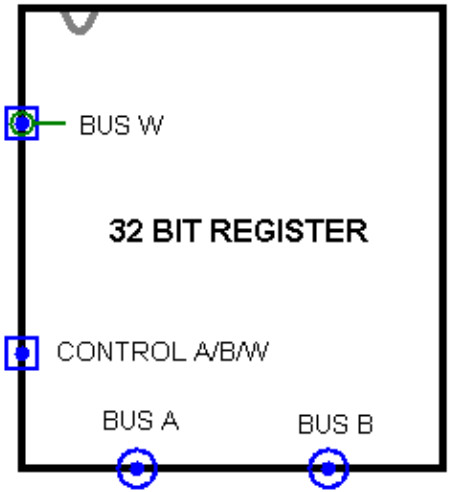
REGISTER FILE



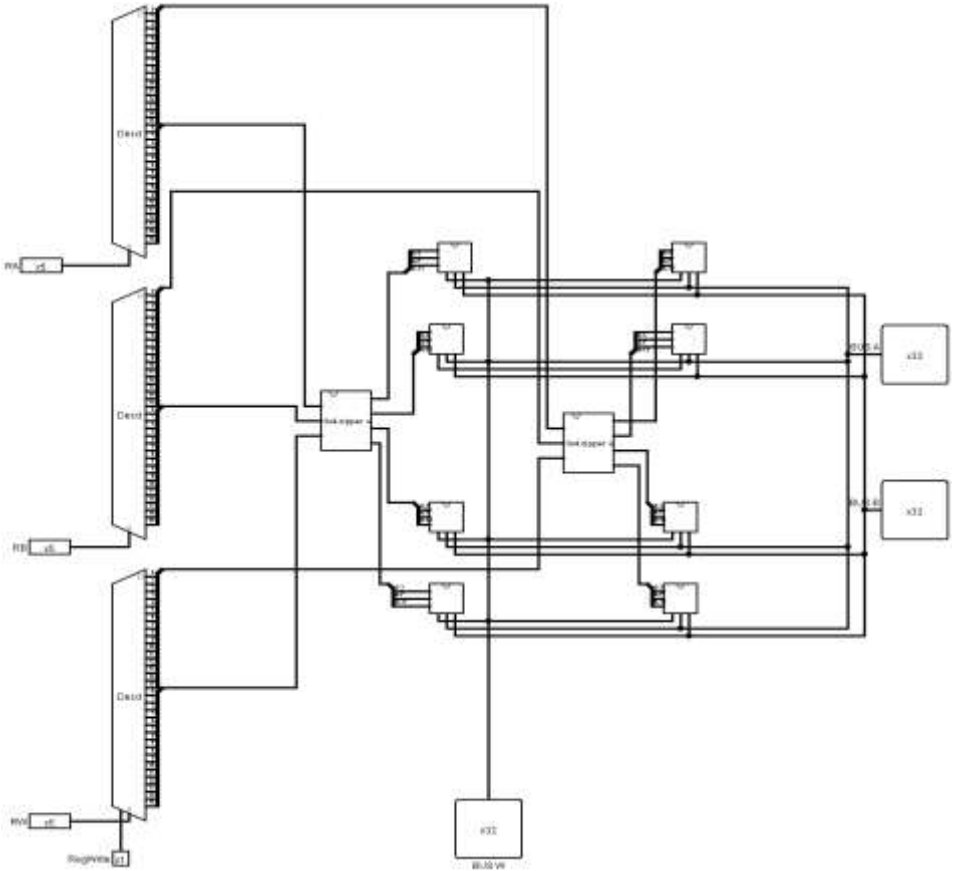


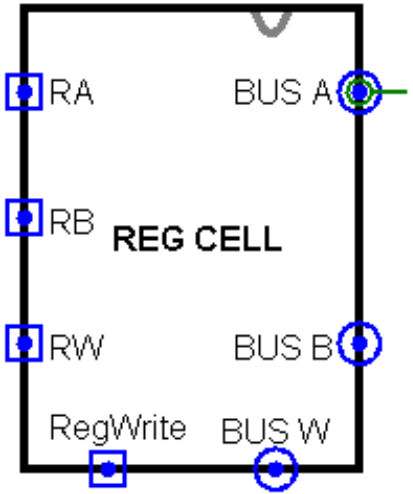
REGISTER CELL WO



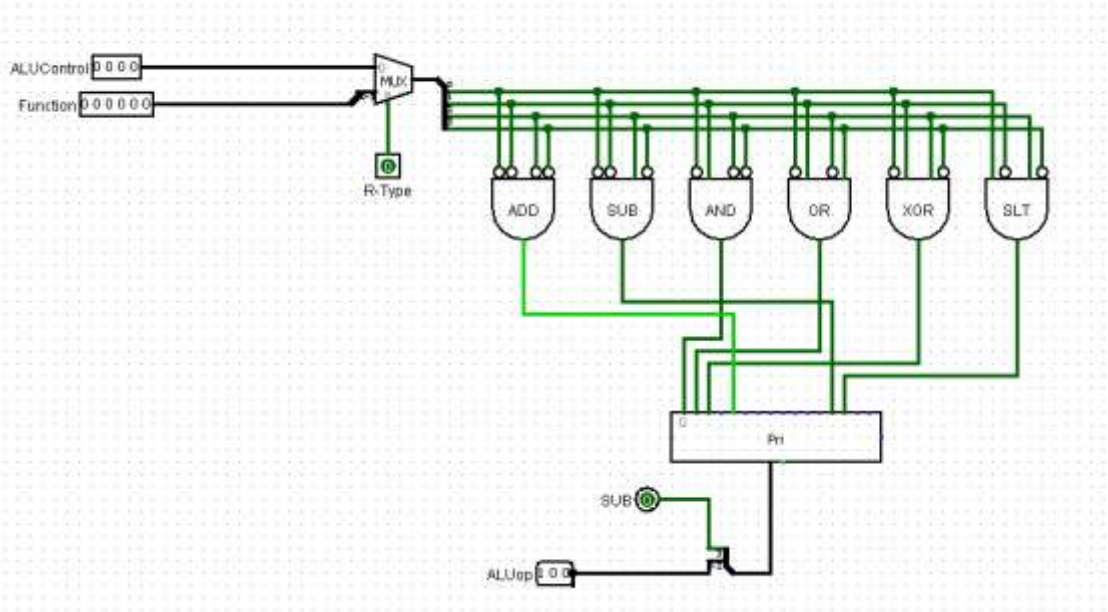


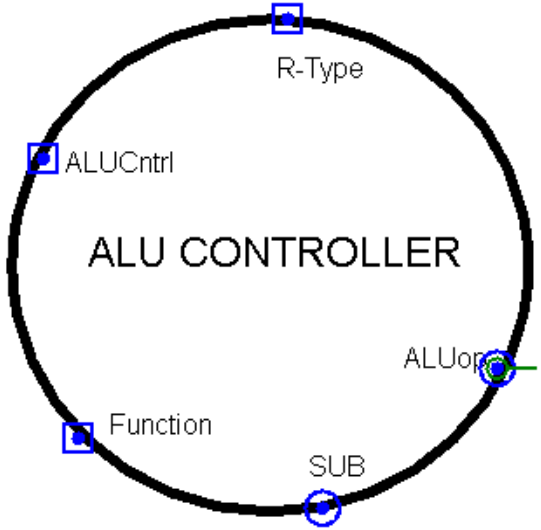
REGISTER CELL



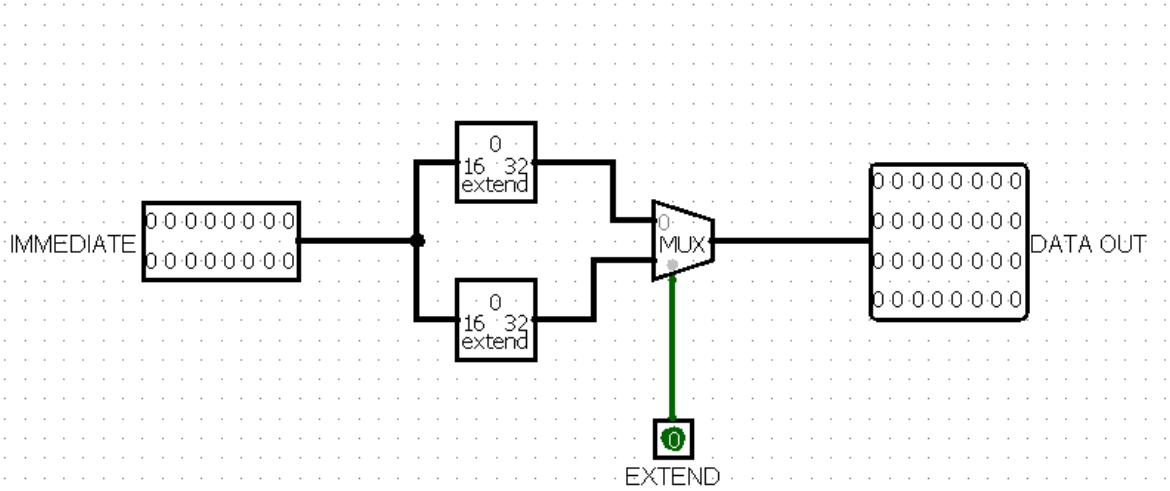


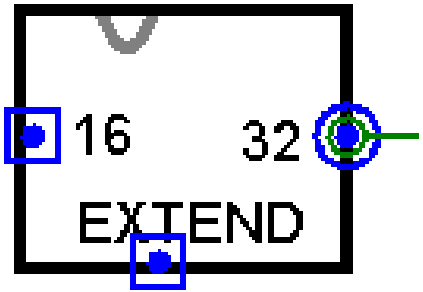
ALU CONTROLLER





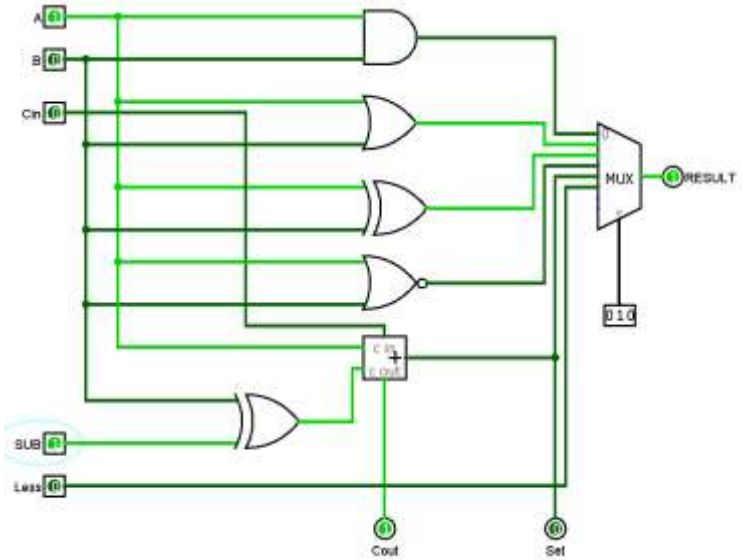
EXTENDER


IMMEDIATE
0
16 32
extend
0
16 32
extend
0
MUX
DATA OUT
0
EXTEND

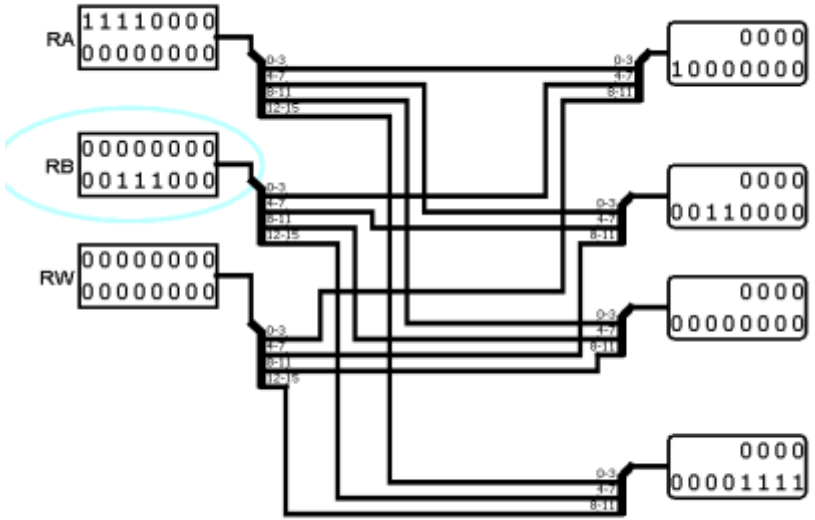

16
32
EXTEND

OUTPUT

1 Bit ALU

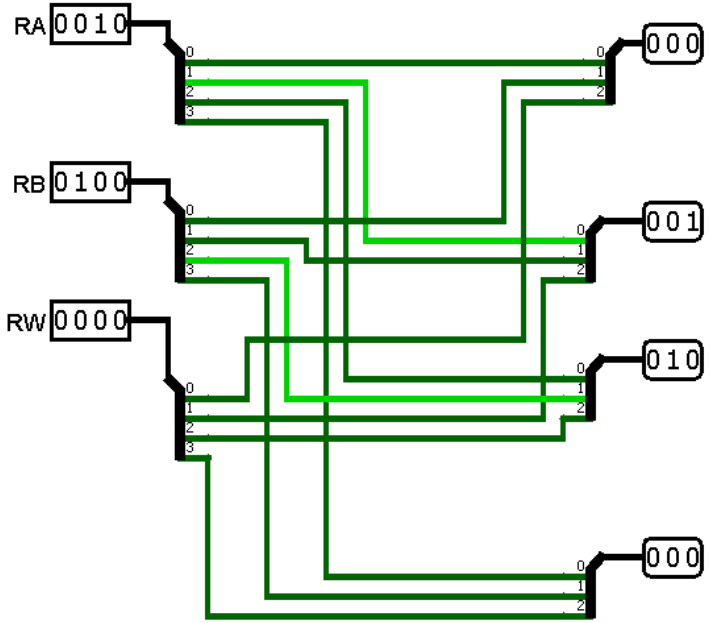


3X4 ZIPPER (4 WIDE)

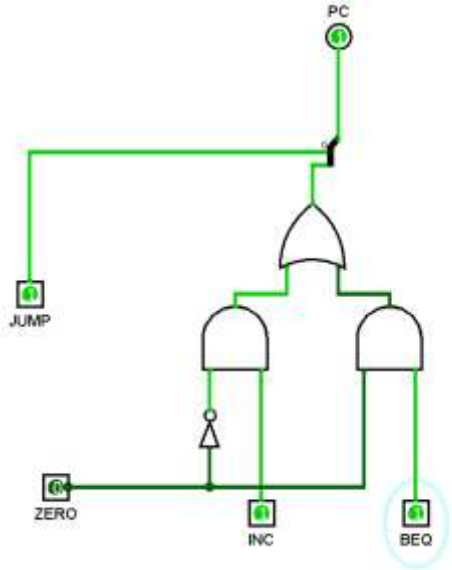


OUTPUT

3X4 ZIPPER

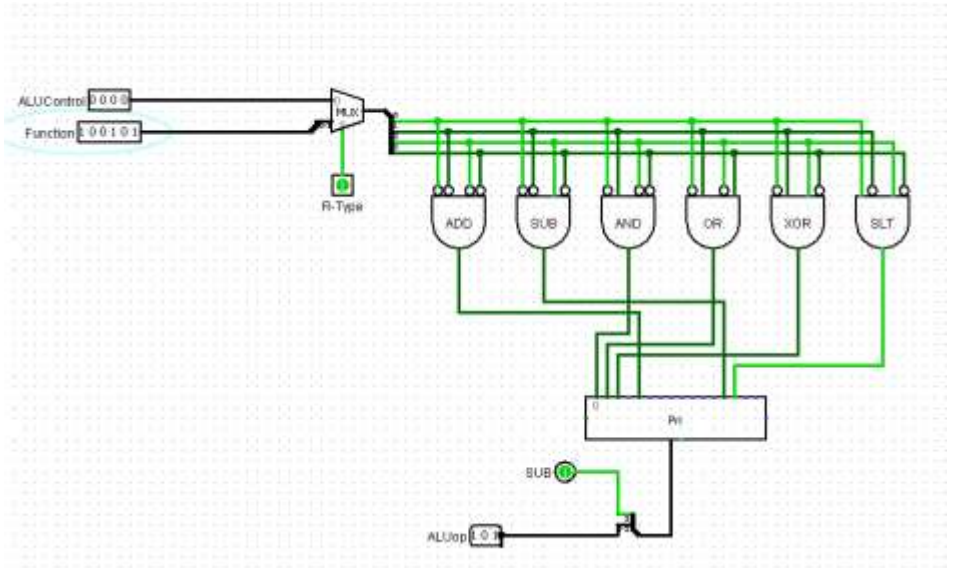


PC CONTROLLER

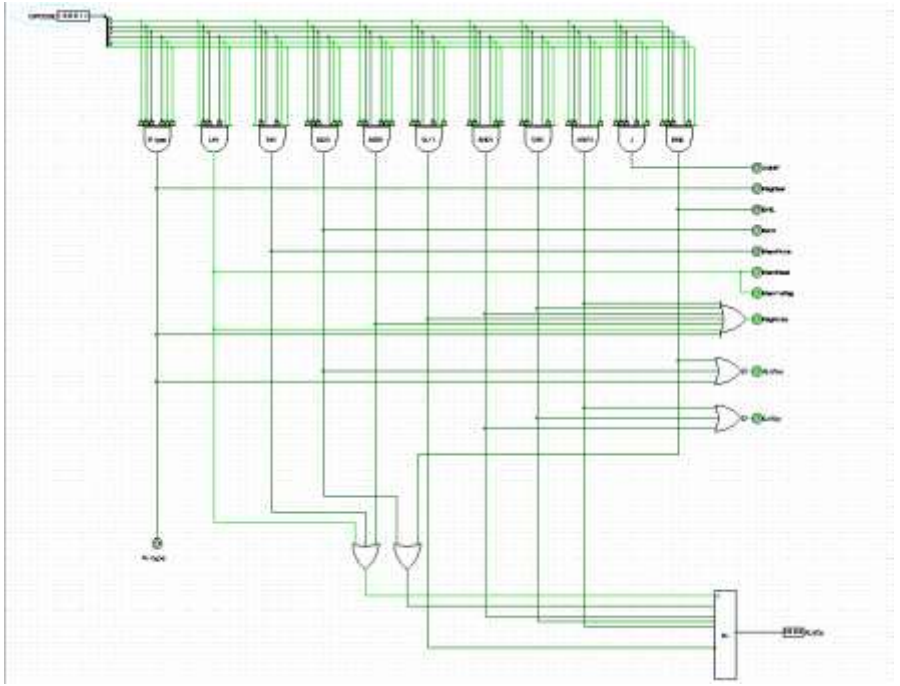


OUTPUT

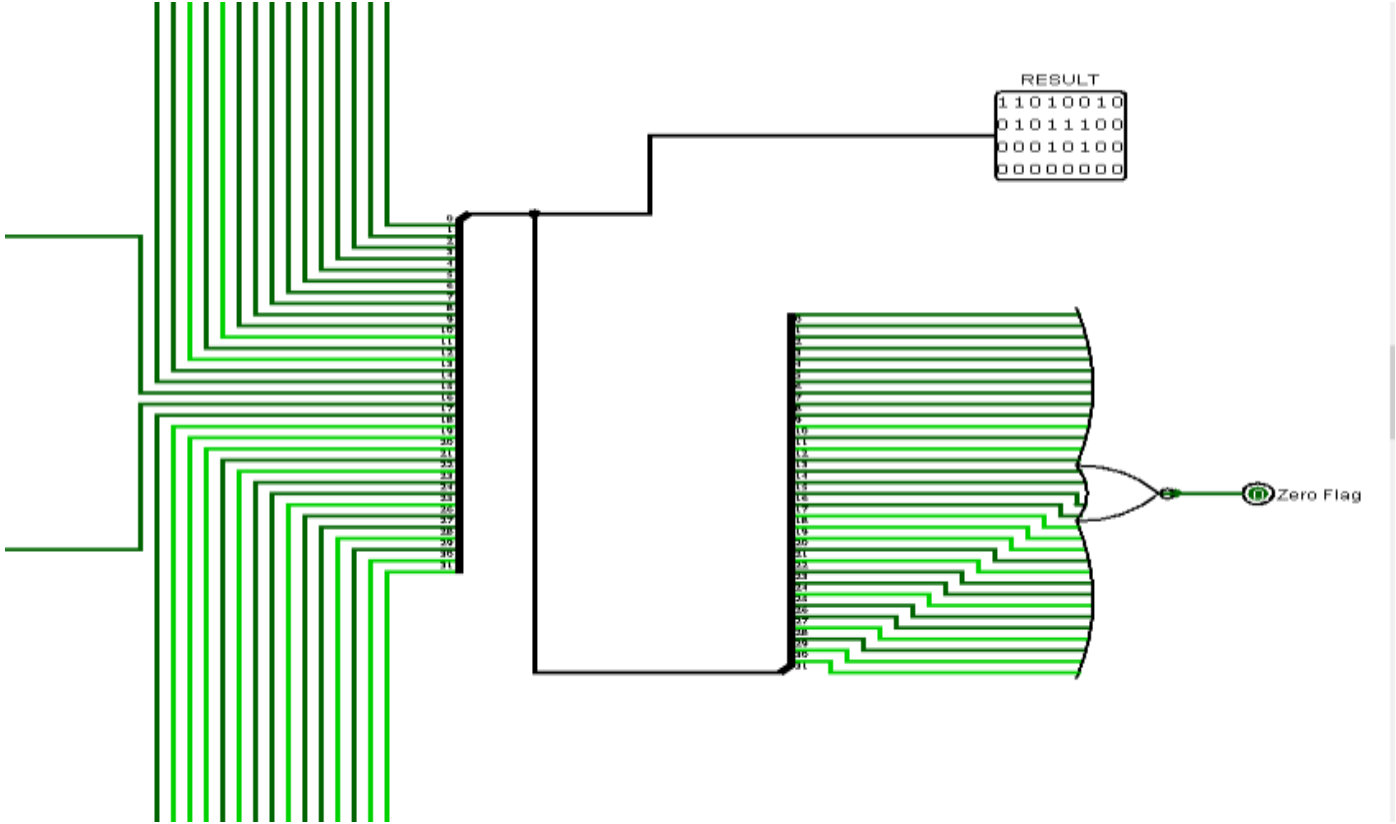
ALU CONTROLLER



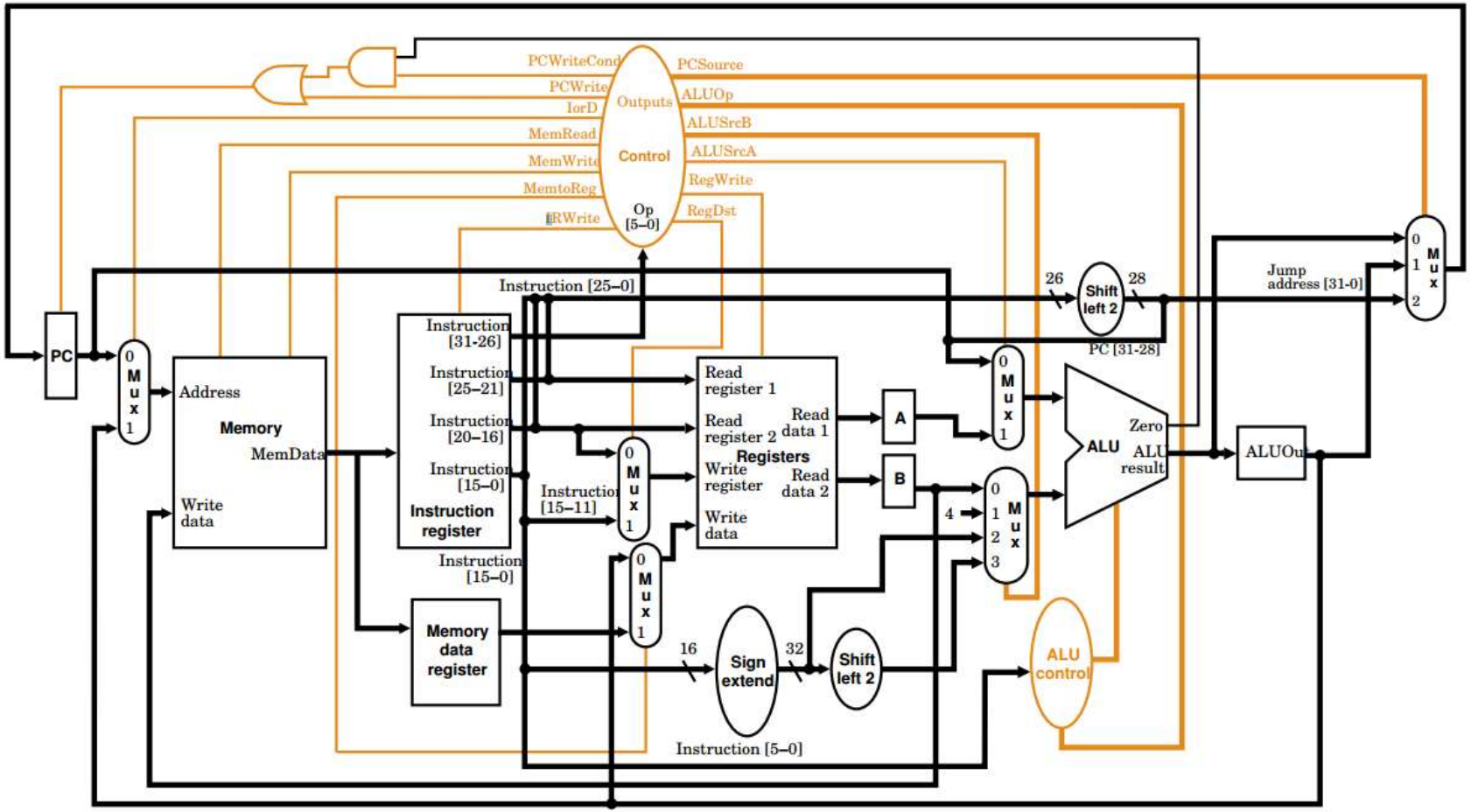
CONTROL UNIT



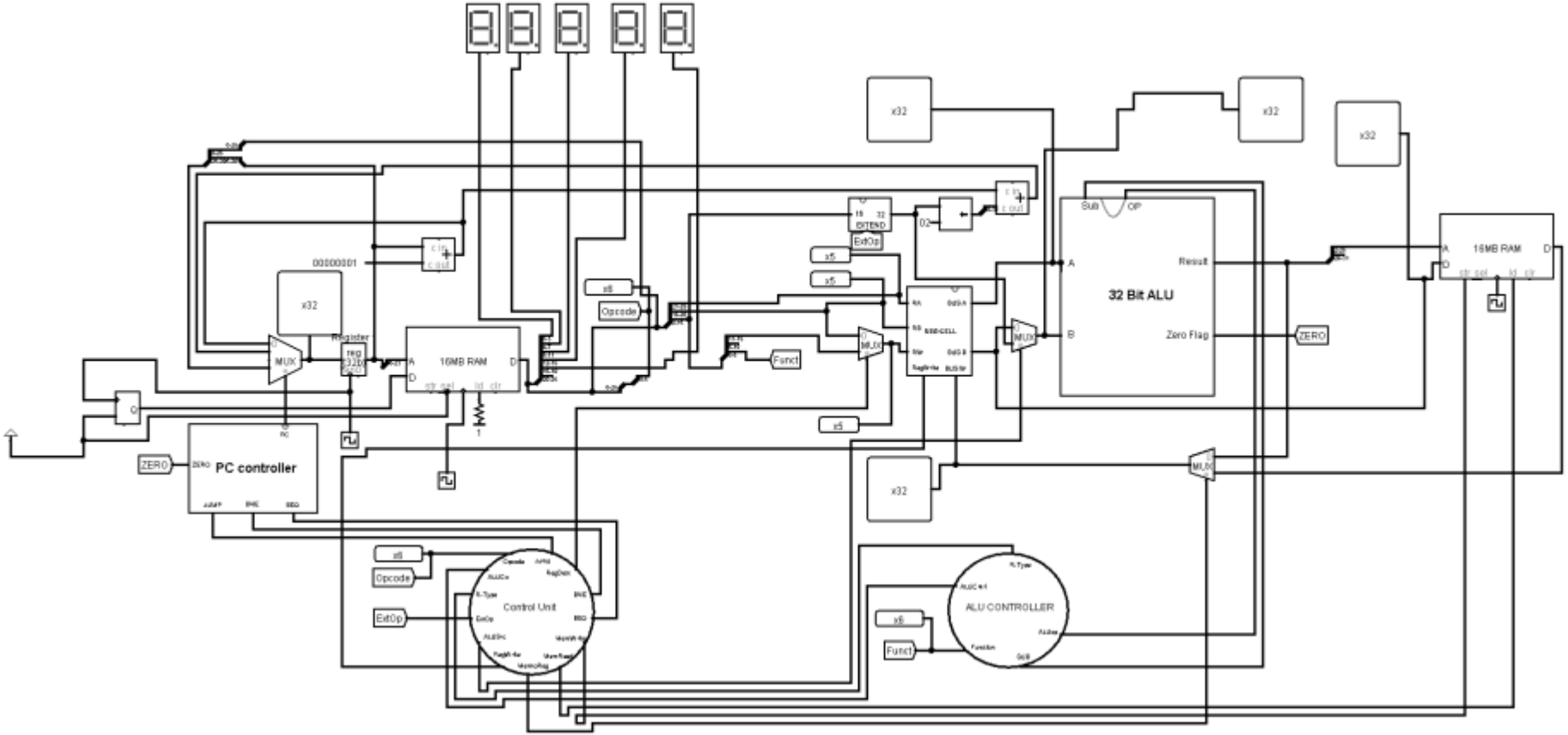
OUTPUT
32 BIT ALU



MIPS ARCHITECTURE



MAIN CIRCUIT



REFERENCE

- https://ieeexplore.ieee.org/document/9758396

- Sharda P. Katke, G.P. Jain,"Design and Implementation of 5 Stages Pipelined Architecture in 32 Bit RISC Processor", IJETAE, Volume 2. Issue 4. April 2012, pp. 340-346.

- Liu Q, Zhang G, Wang Z. (2017) Design and implementation of pipeline CPU based on MIPS instruction Set. Laboratory Research and exploration, 36:148 - 152

THANKYOU