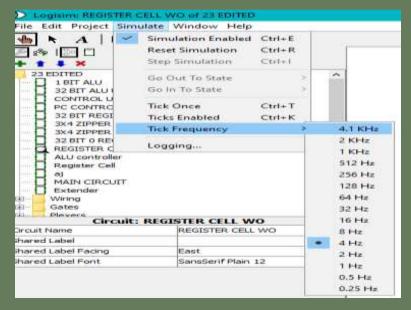
#### DESIGN OF 32-BIT SINGLE CYCLE MIPS PROCESSOR

# **OBJECTIVE**:

To design a 32-Bit single cycle processor based on MIPS architecture by designing the basic blocks of the processor using Logisim.

#### TOOL USED - LOGISIM

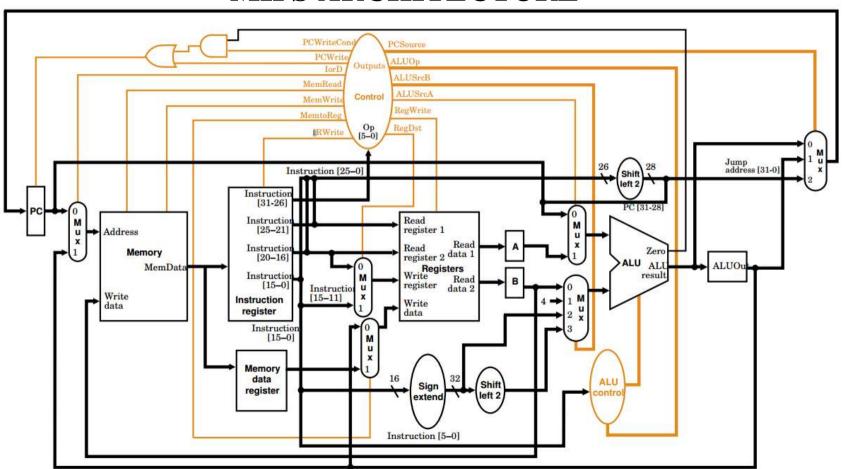
Logisim is an educational tool for **designing and simulating digital logic circuits**. With its simple toolbar interface and simulation of circuits as they are built, it is simple enough to facilitate learning the most basic concepts related to logic circuits.



D Logisim: 1 BIT ALU of 32 BIT MIPS processor File Edit Project Simulate Window Help  $A \mid \blacksquare \otimes \triangleright \square \square$ BIT MIPS processor 1 BIT ALU 32 BIT ALU UNIT CONTROL UNIT PC CONTROLLER 32 BIT REGISTER 3X4 ZIPPER 3X4 ZIPPER (4 WIDE) 32 BIT REGISTER WO REGISTER CELL WO Wiring F Splitter O Probe <□ Tunnel **Pull Resistor** [ Clock O - Constant ◆ Power r Ground A Transistor Transmission Gate Bit Extender Gates > NOT Gate C> Buffer AND Gate OR Gate > NAND Gate > NOR Gate > XOR Gate > XNOR Gate Odd Parity Even Parity C> Controlled Buffer D> Controlled Inverter Plexers Multiplexer Demultiplexer Decoder Ell Priority Encoder Bit Selector Arithmetic + Adder Subtractor Multiplier Divider Negator Comparator → Shifter Bit Adder

7 Bit Finder Memory 100%

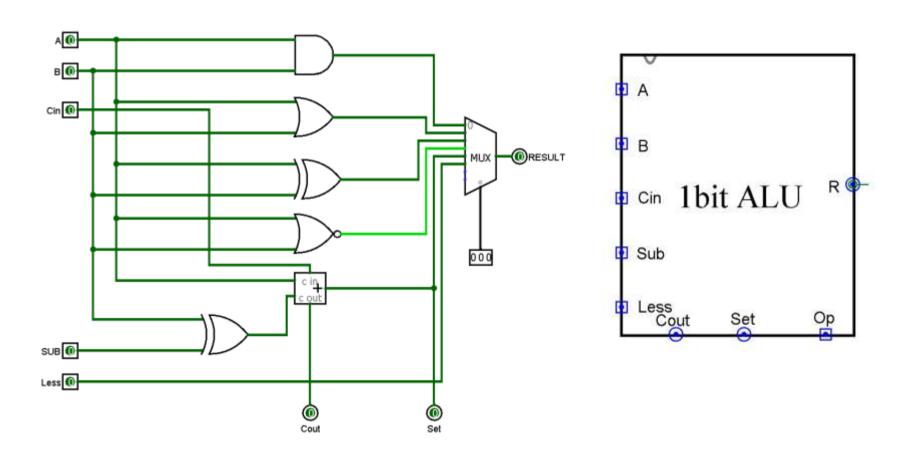
#### MIPS ARCHITECTURE



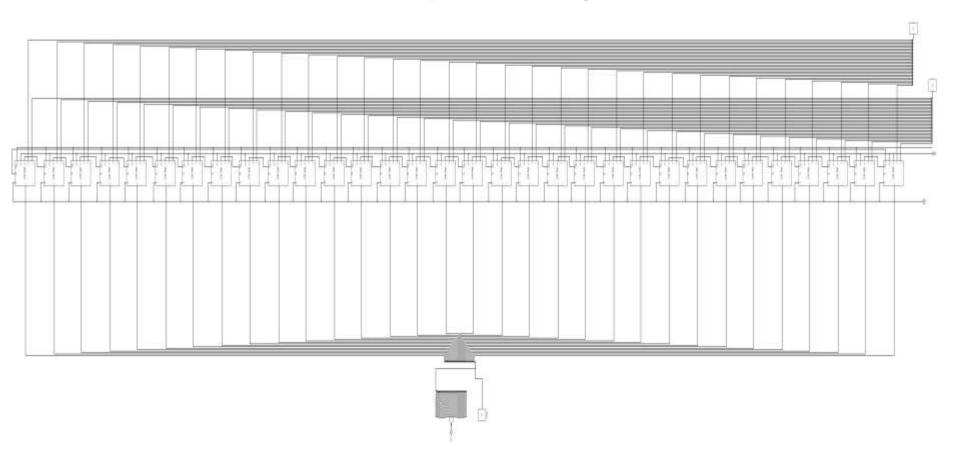
#### LIST OF BASIC BLOCKS

- 1-BIT ALU
- 32 BIT ALU
- PC CONTROLLER
- 3X4 ZIPPER (4 WIDE)
- 3X4 ZIPPER
- CONTROL UNIT
- REGISTER FILE
- 32 BIT REGISTER W/O
- REGISTER CELL W/O
- ALU CONTROLLER
- EXTENDER

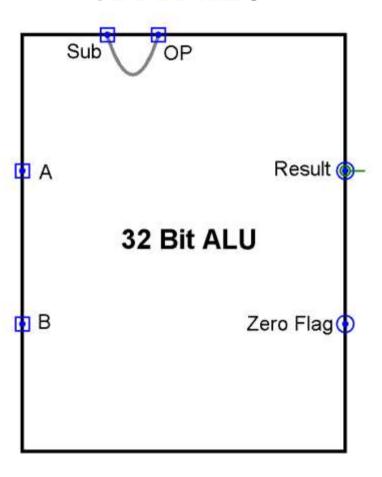
#### 1 BIT ALU



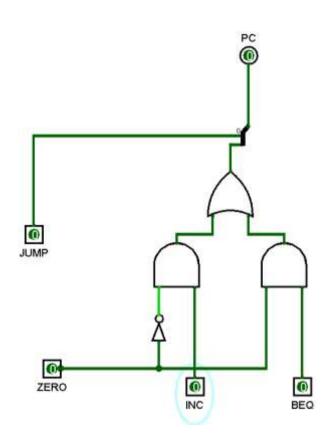
#### 32 BIT ALU

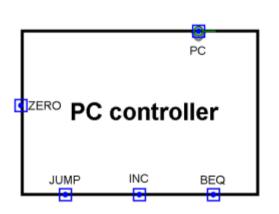


# 32 BIT ALU



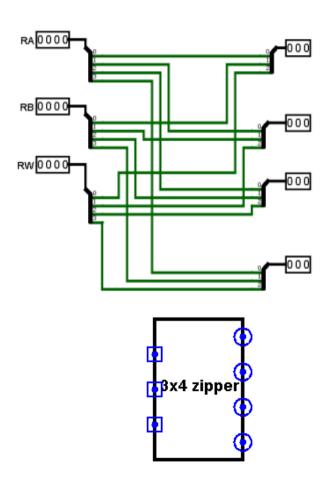
## PC CONTROLLER

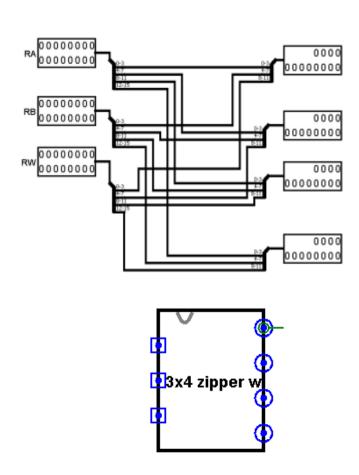




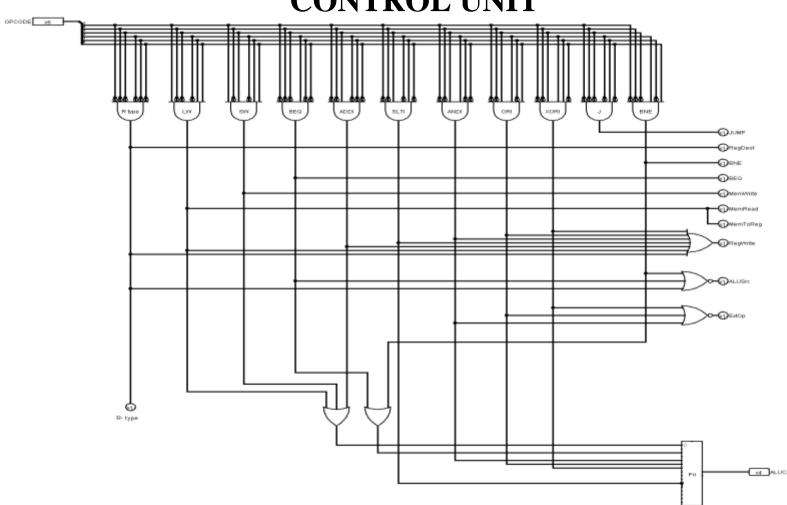
#### **3X4 ZIPPER**

# 3X4 ZIPPER (4 WIDE)

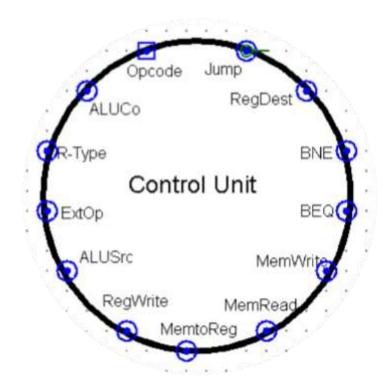




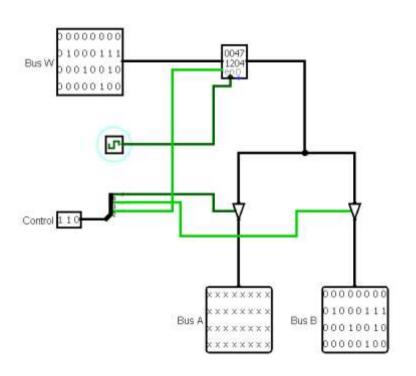
## **CONTROL UNIT**

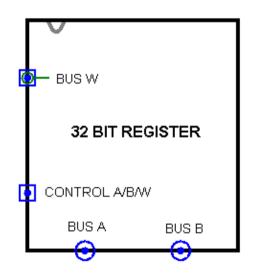


## **CONTROL UNIT**

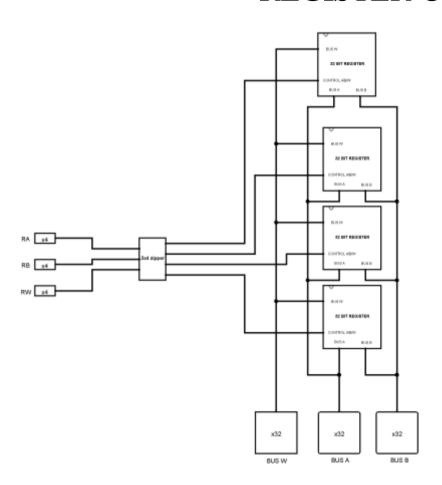


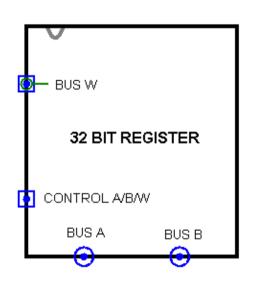
#### REGISTER FILE



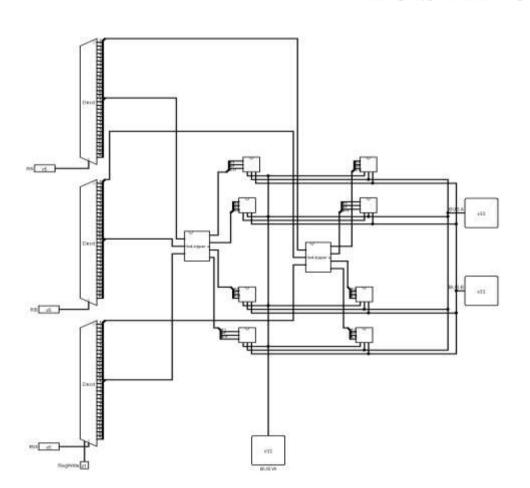


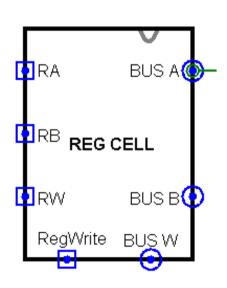
#### REGISTER CELL WO



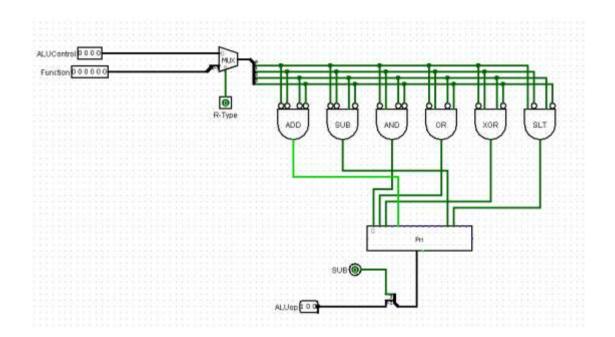


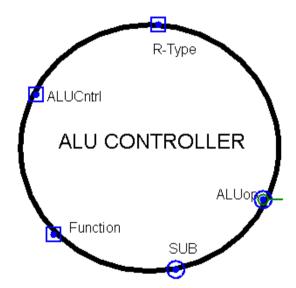
#### REGISTER CELL



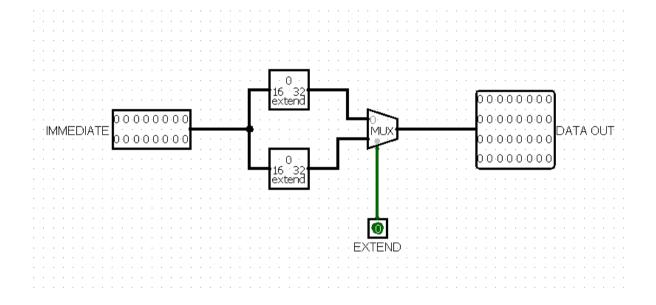


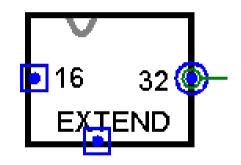
#### ALU CONTROLLER





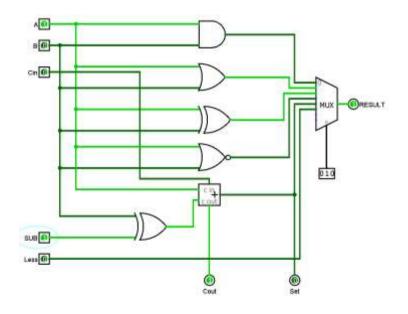
#### **EXTENDER**



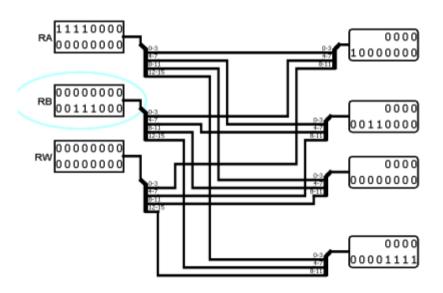


#### **OUTPUT**

#### 1 Bit ALU

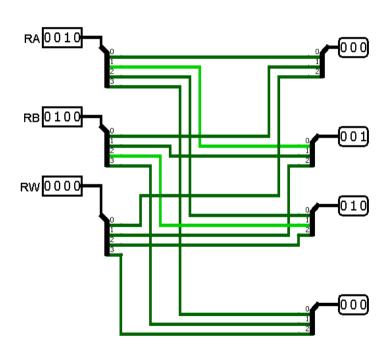


# 3X4 ZIPPER (4 WIDE)

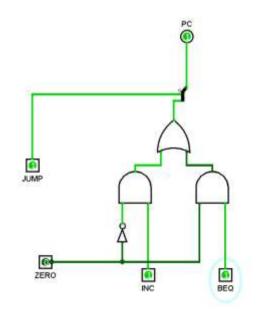


#### **OUTPUT**

#### **3X4 ZIPPER**



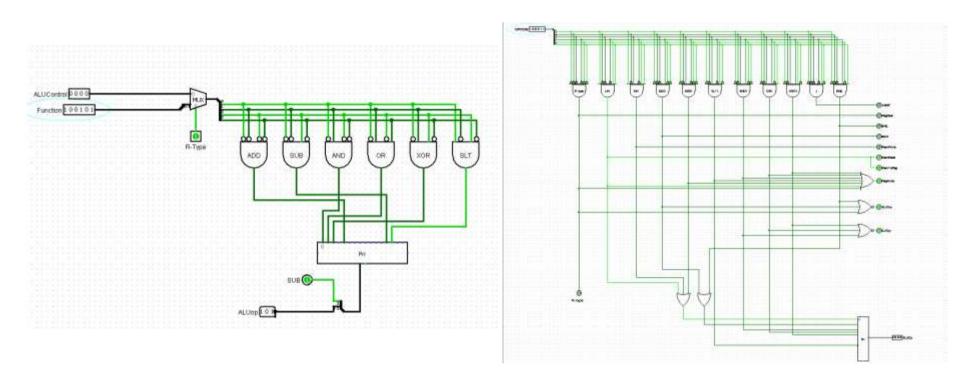
#### PC CONTROLLER



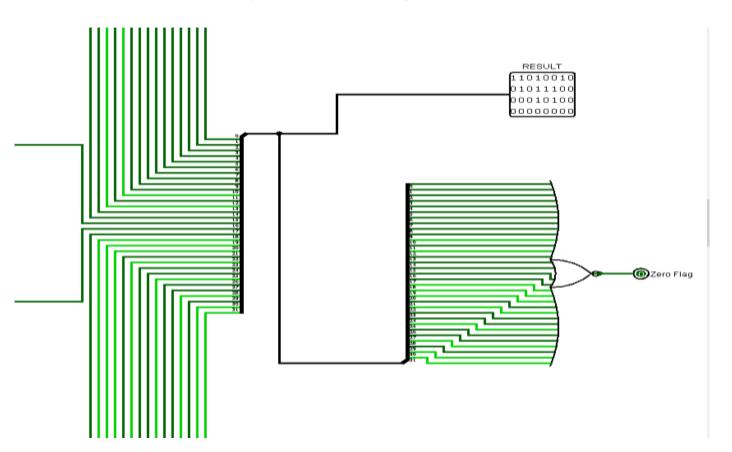
#### **OUTPUT**

## **ALU CONTROLLER**

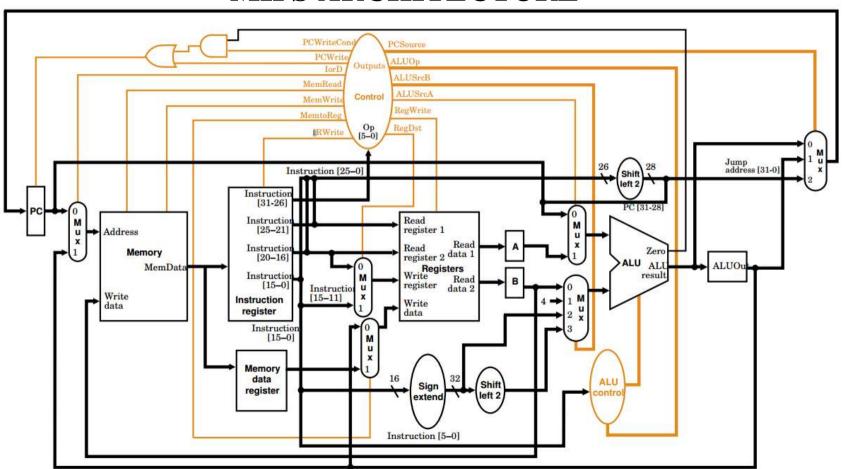
## **CONTROL UNIT**



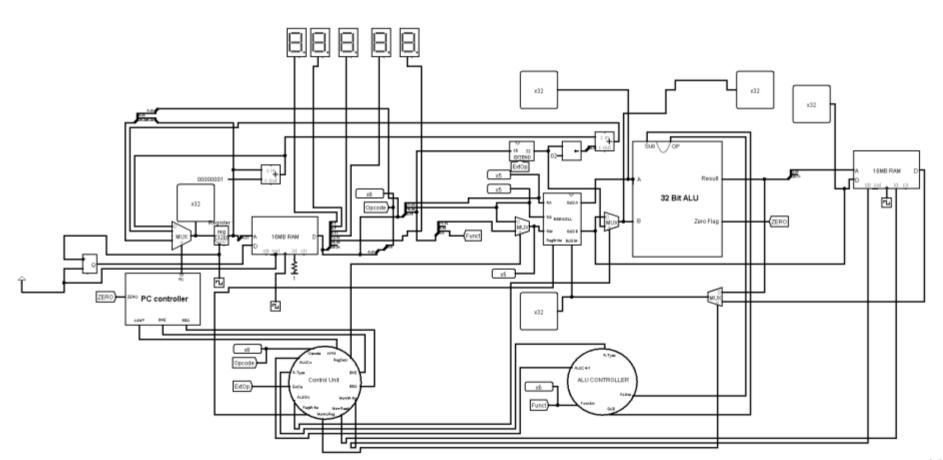
# OUTPUT 32 BIT ALU



#### MIPS ARCHITECTURE



## **MAIN CIRCUIT**



# REFERENCE

- <a href="https://ieeexplore.ieee.org/document/9758396">https://ieeexplore.ieee.org/document/9758396</a>
- Sharda P. Katke, G.P. Jain, "Design and Implementation of 5 Stages Pipelined Architecture in 32 Bit RISC Processor", IJETAE, Volume 2. Issue 4. April 2012, pp. 340-346.
- Liu Q, Zhang G, Wang Z. (2017) Design and implementation of pipeline CPU based on MIPS instruction Set. Laboratory Research and exploration, 36:148 152

# THANKYOU

