

PROJECT TITLE

1

DIGITAL LOCKER USING VERILOG HDL

OBJECTIVE:

To design a electronic digital locker using Verilog HDL using Logisim and implementation using FPGA Kit

SOFTWARE USED - LOGISIM

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LOGISIM :

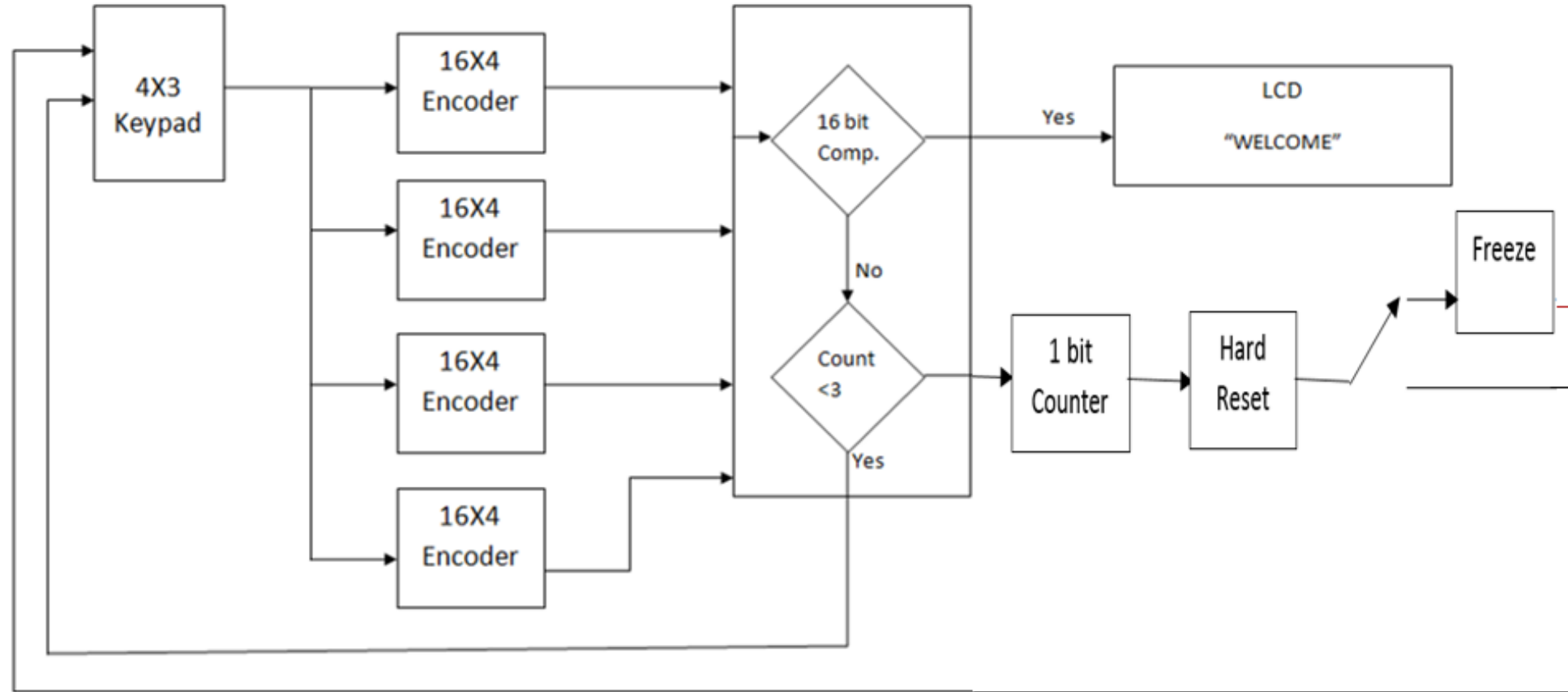
Logisim is a tool for designing and simulating digital logic circuits. With its simple tool bar interface and simulation of circuits as you build them , it is simple enough to facilitate learning the most basic concept related to logic circuit.

LANGUAGE USED – VERILOG

IMPLEMENTATION-FPGA KIT

BLOCK DIAGRAM:

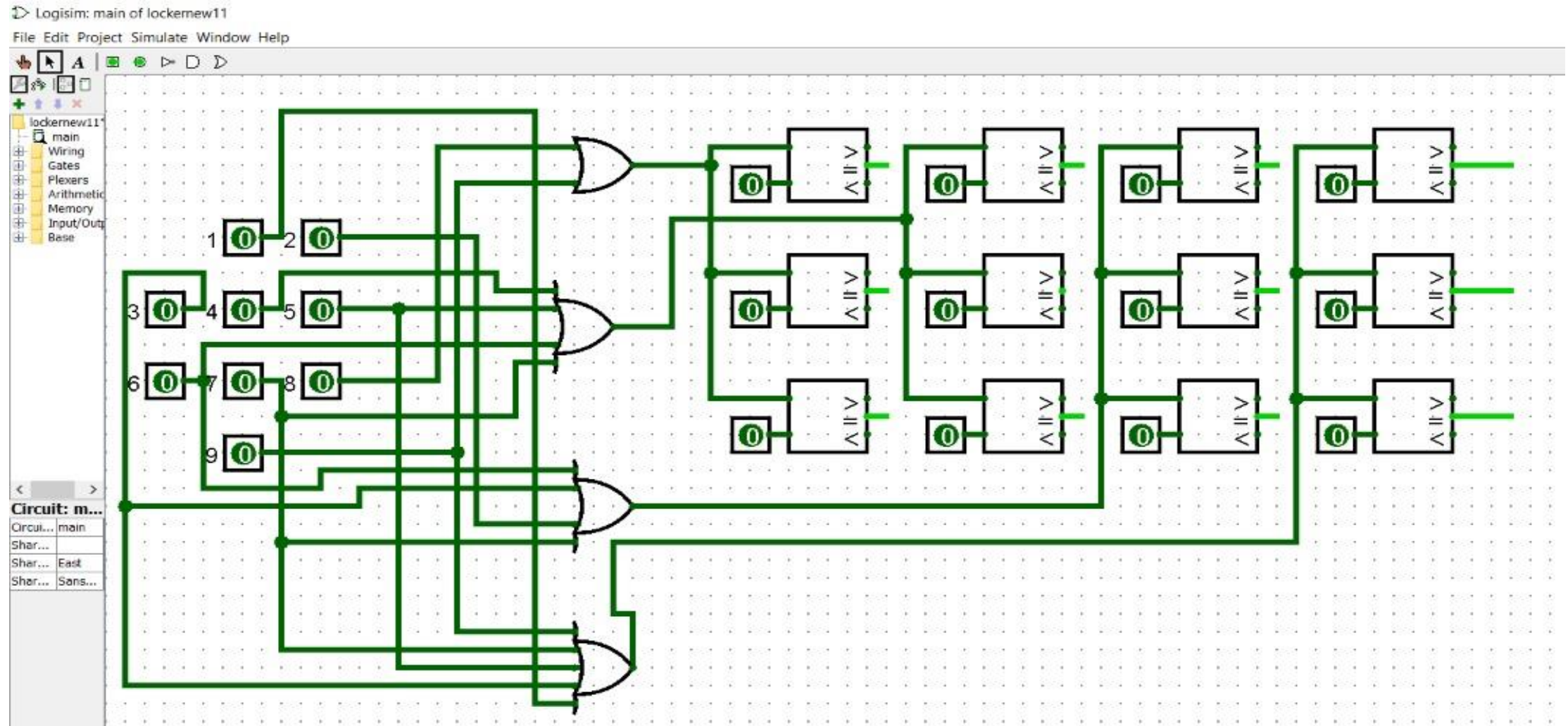
4



PROCEDURE

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STEP 1:

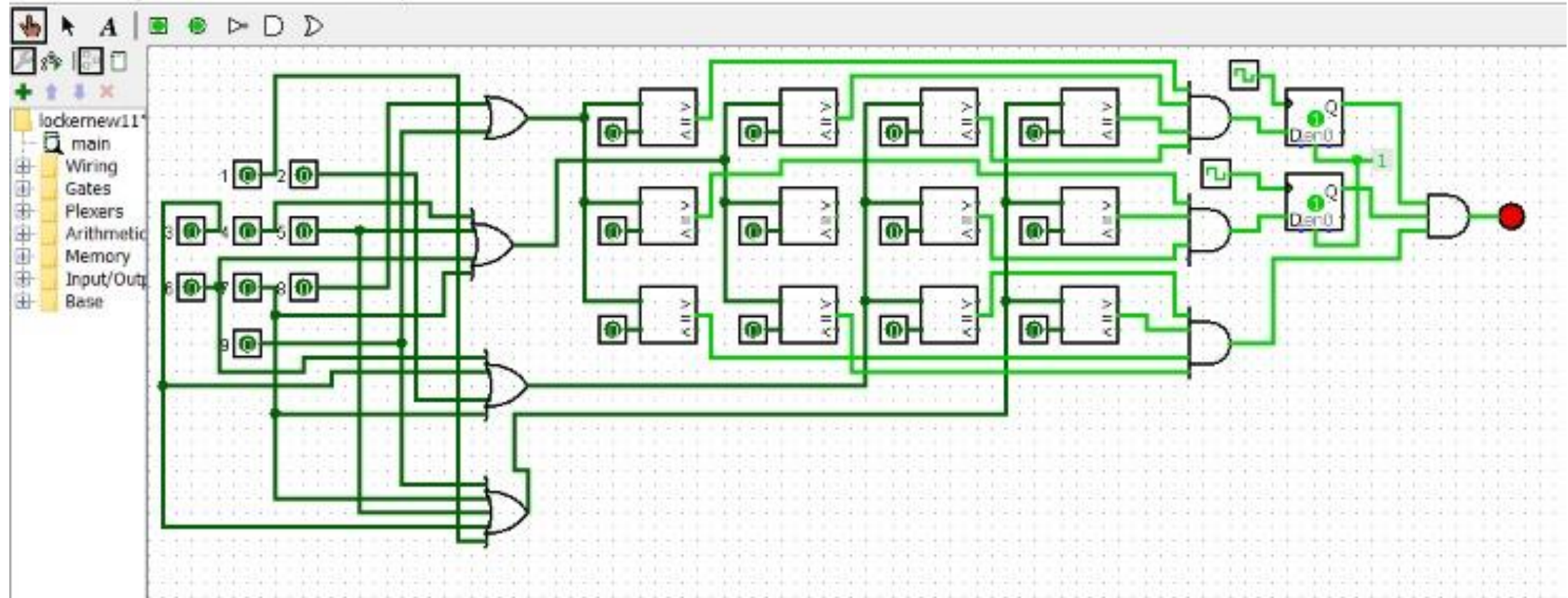


STEP 2:

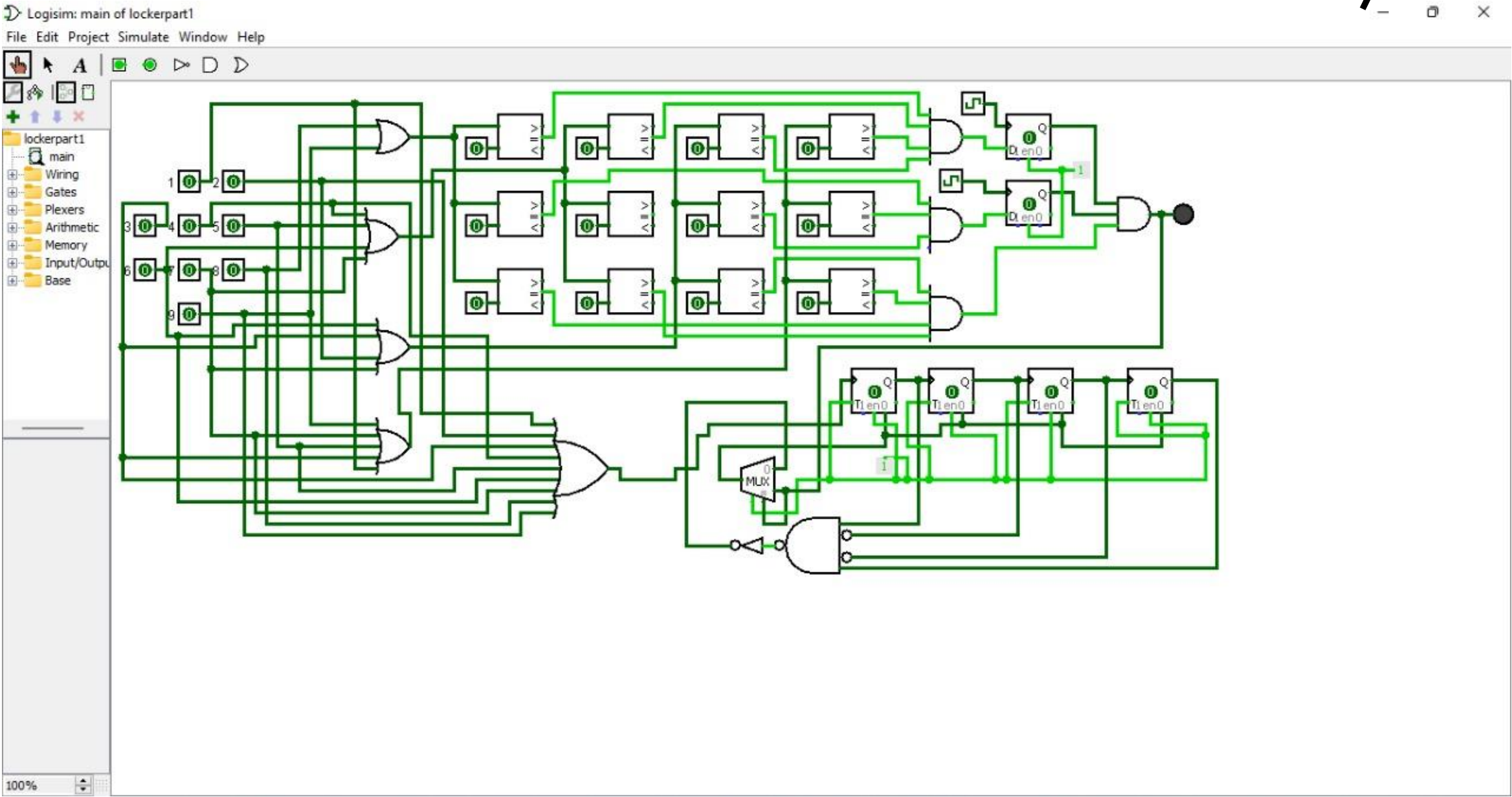
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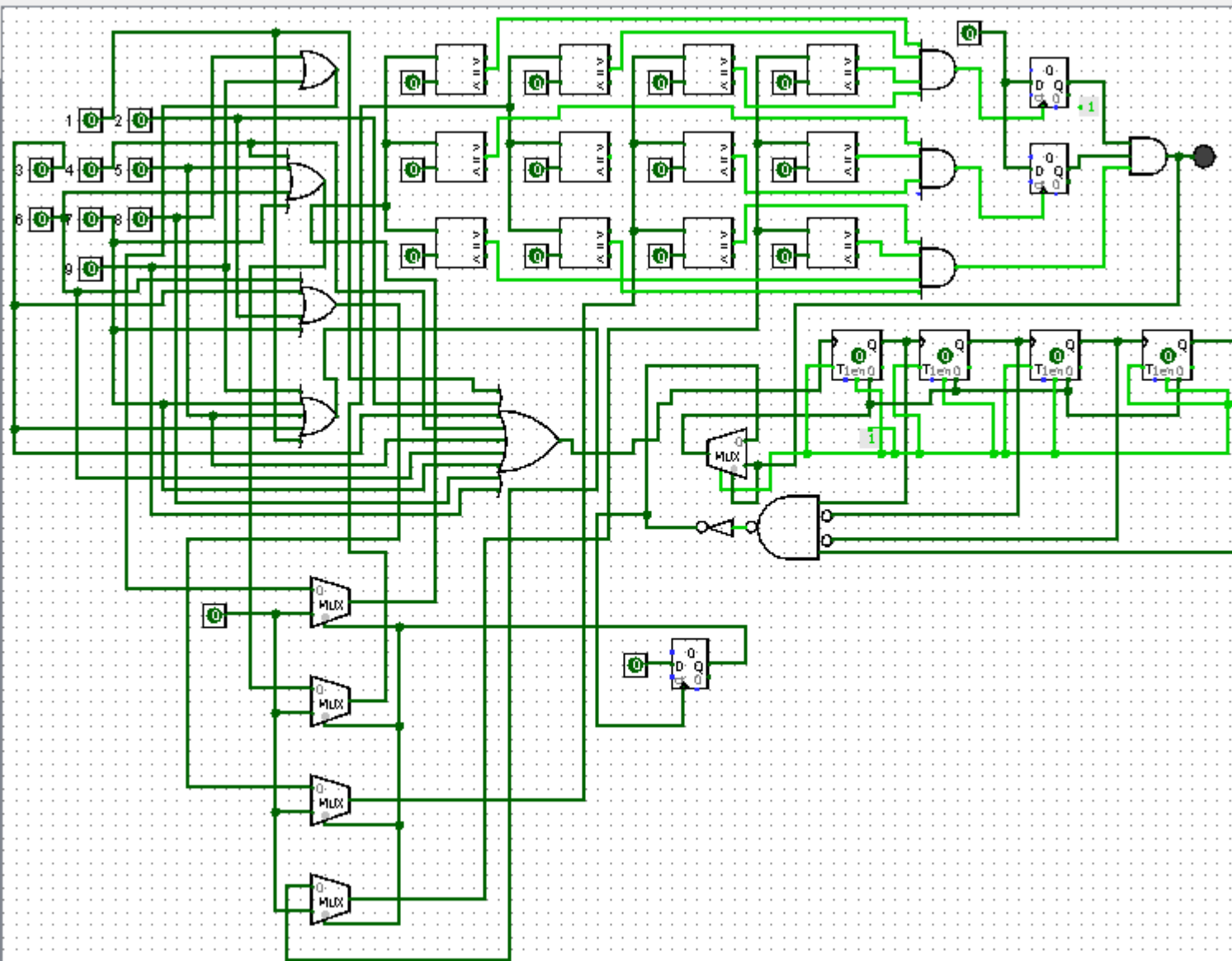
Logisim: main of lockemew11

File Edit Project Simulate Window Help

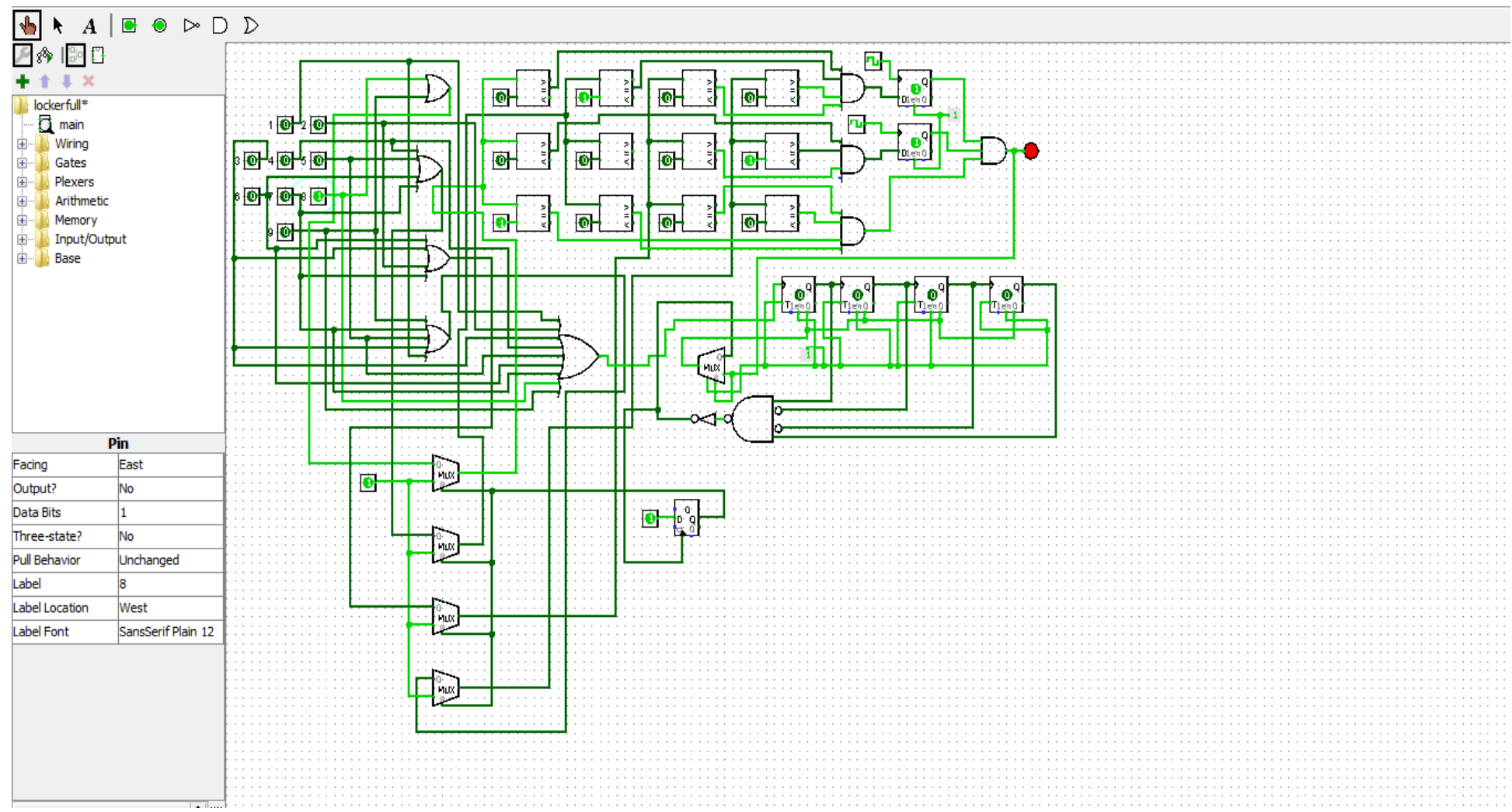


STEP 3:



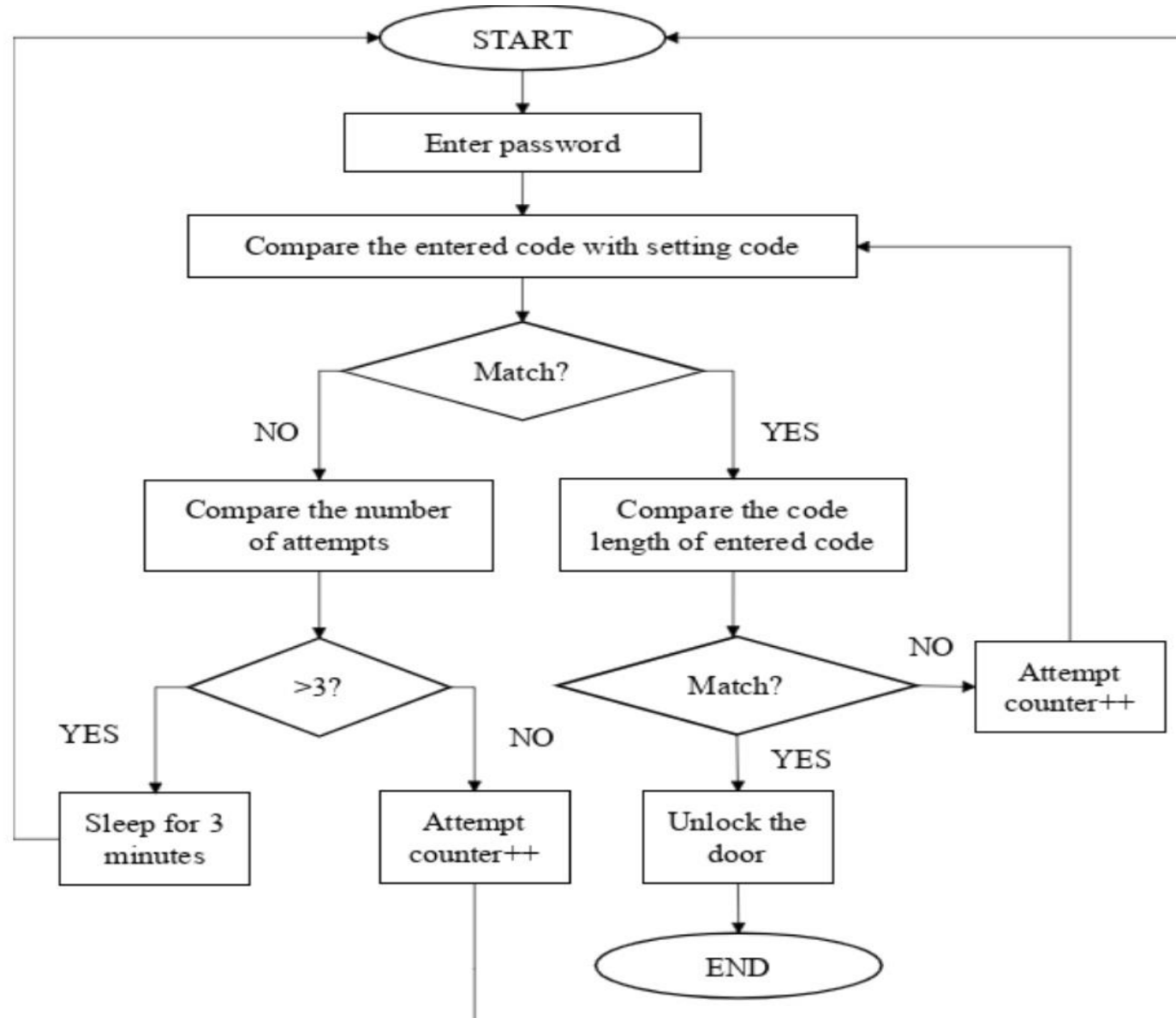


SCHEMATIC DIAGRAM :

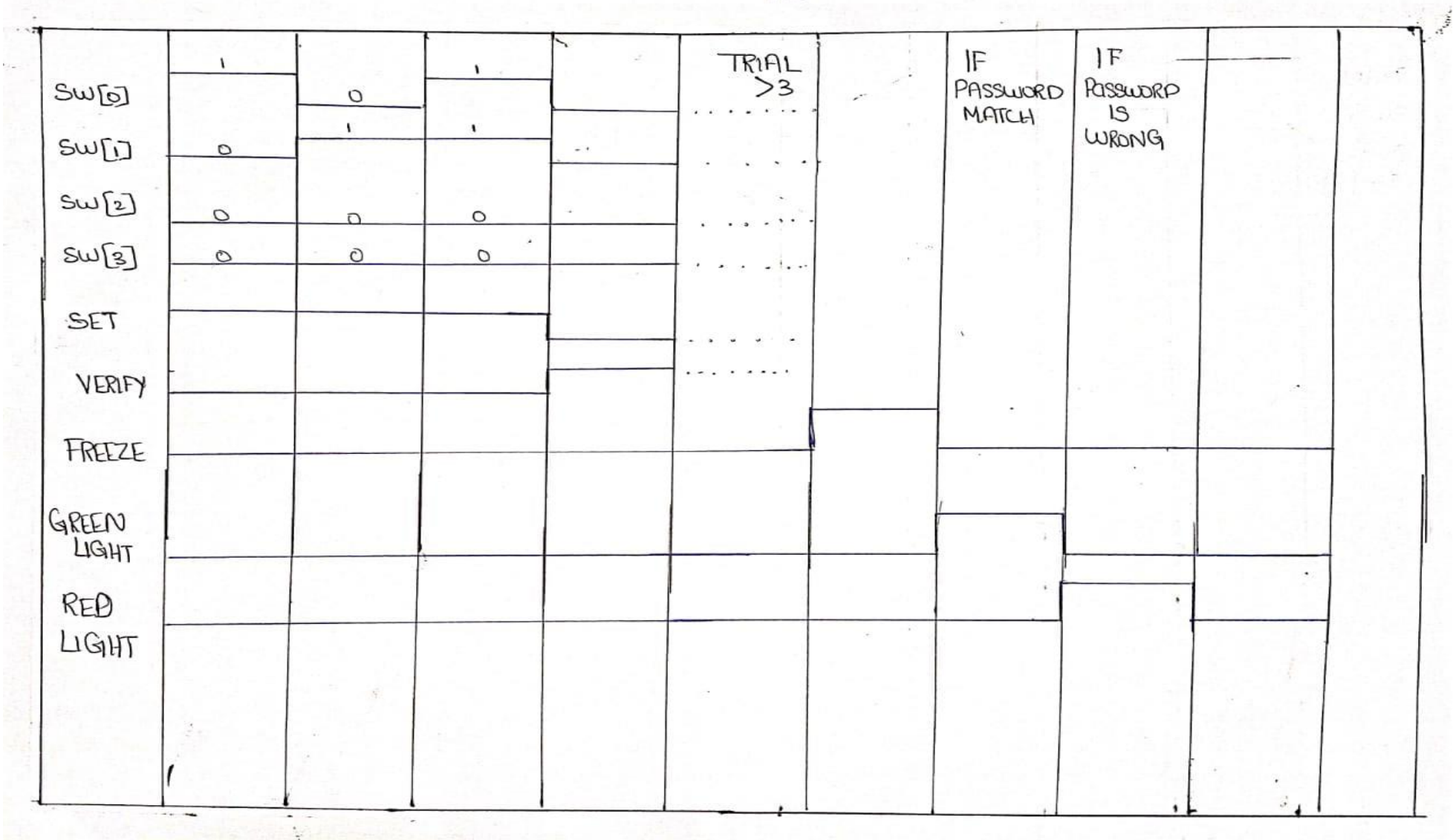


FLOW CHART :

10

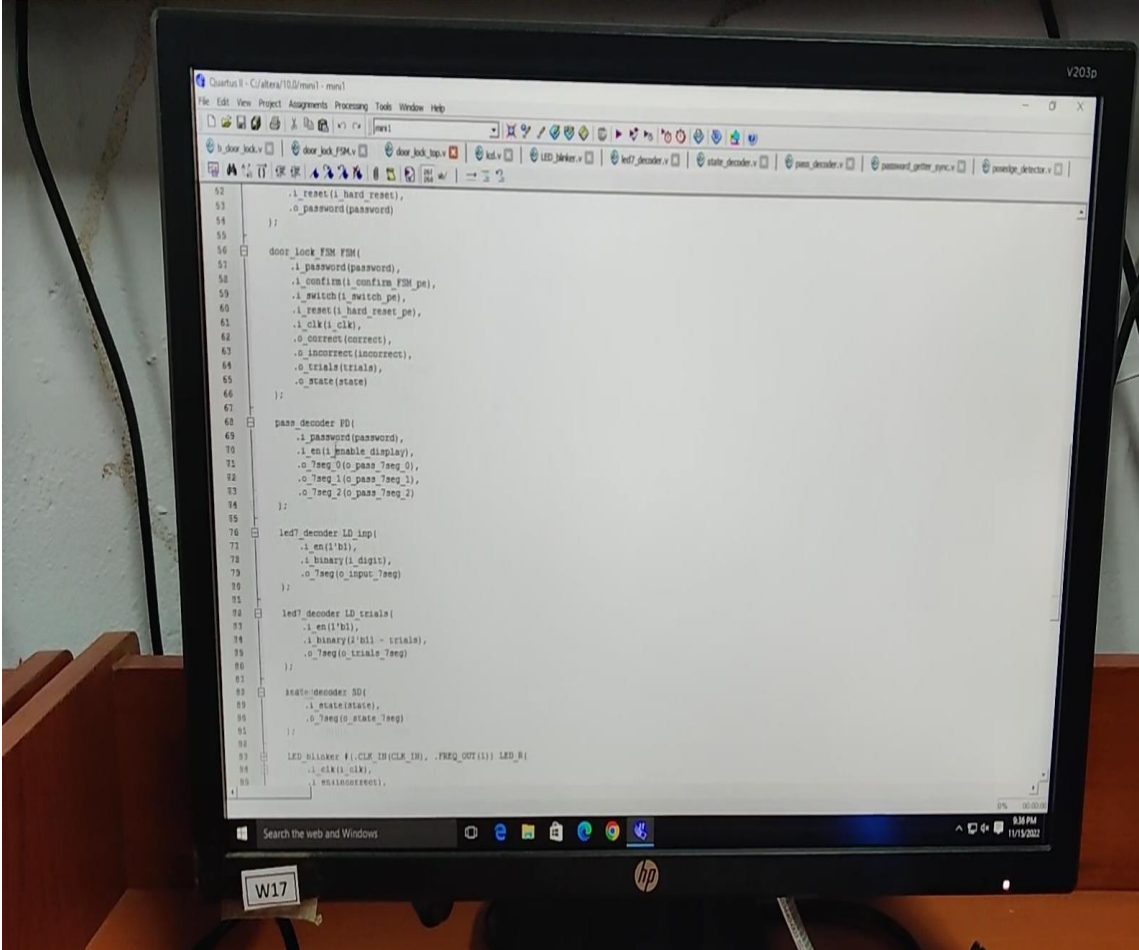
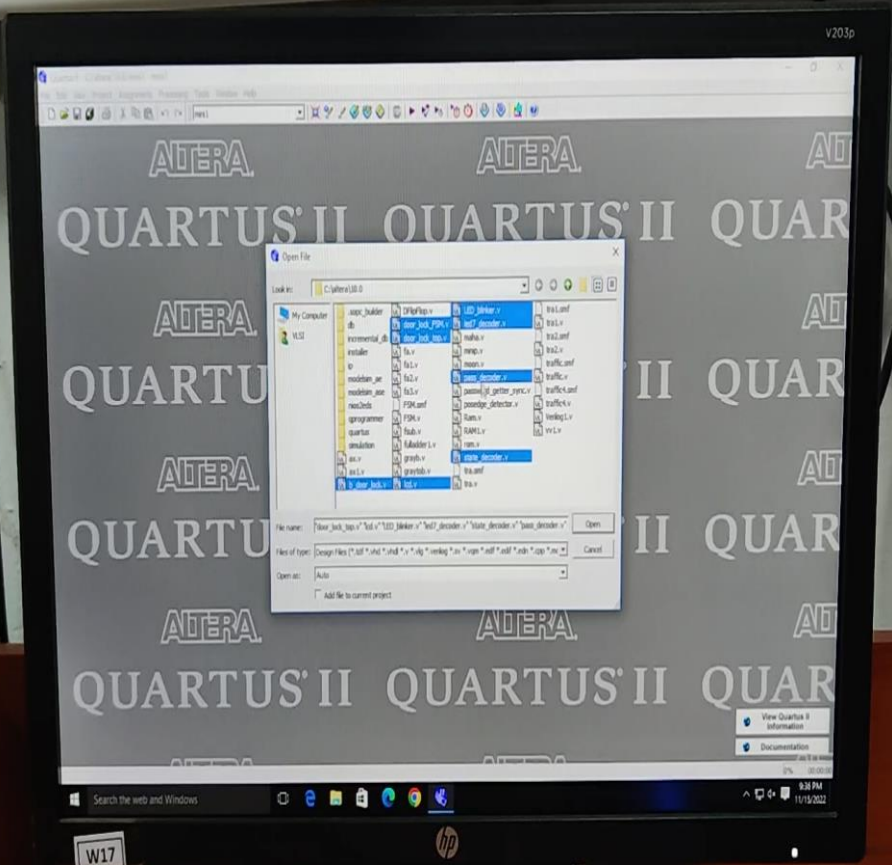


OUTPUT WAVEFORM :



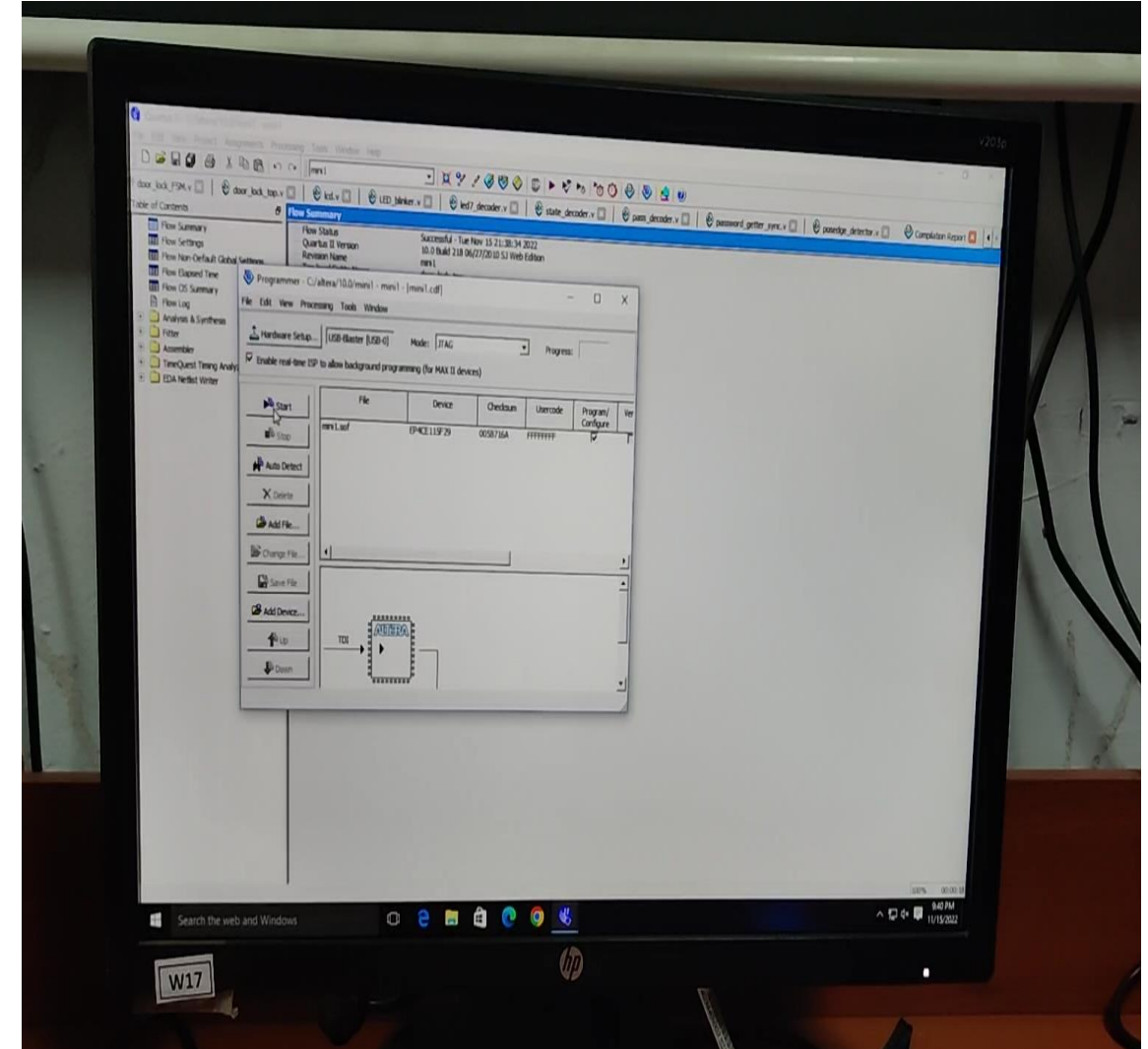
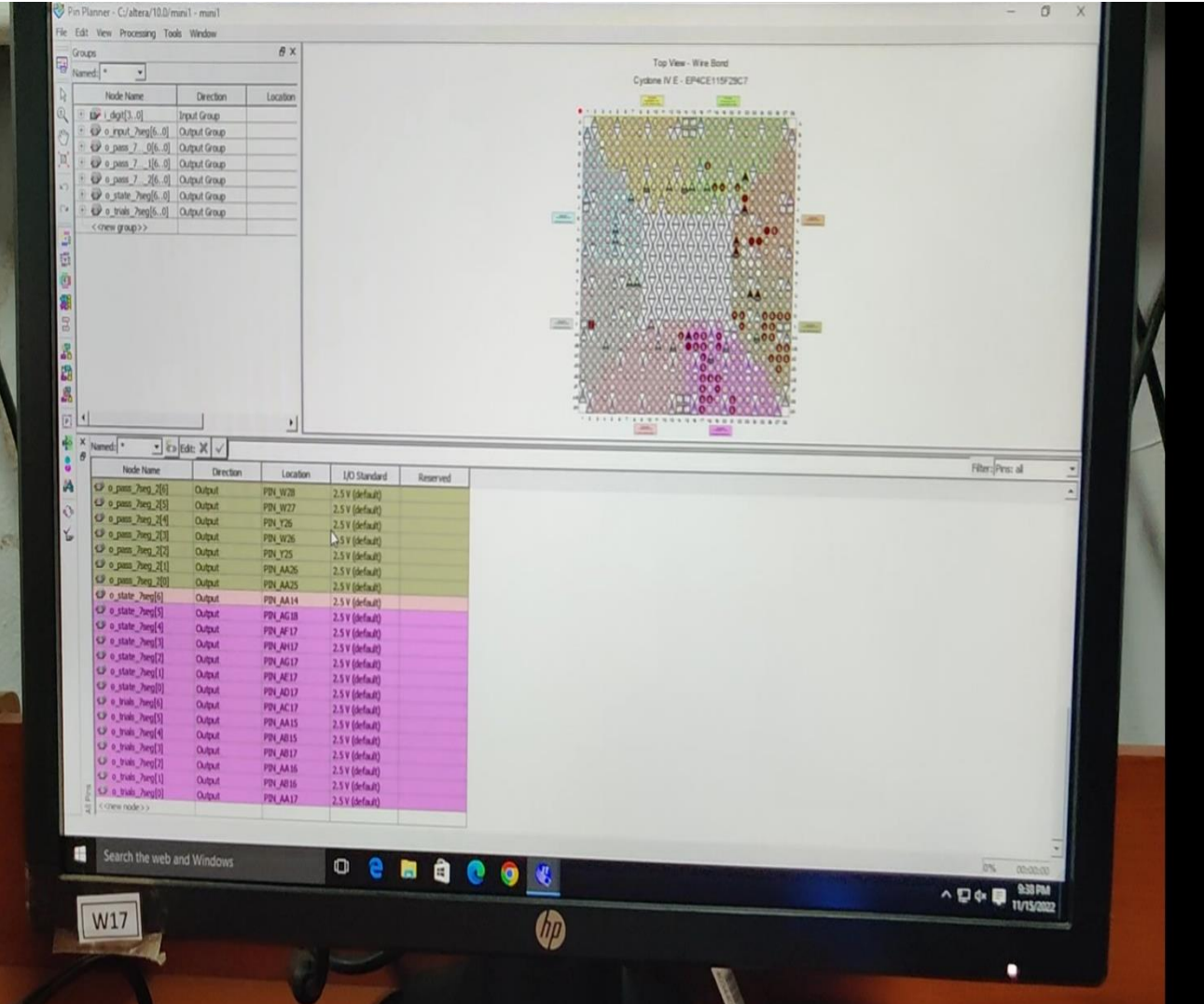
VERILOG CODE IN QUARTUS-II SOFTWARE :

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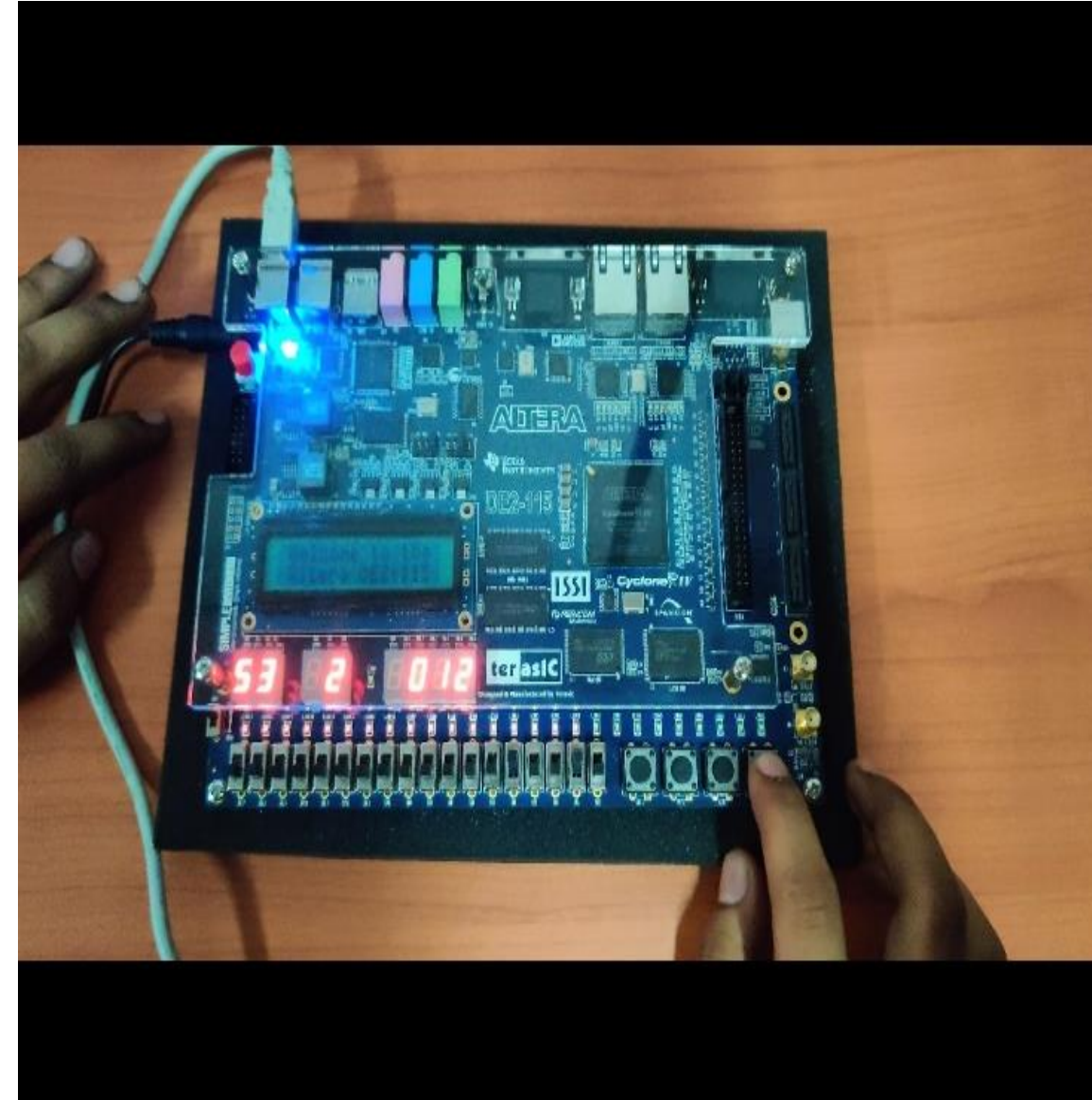
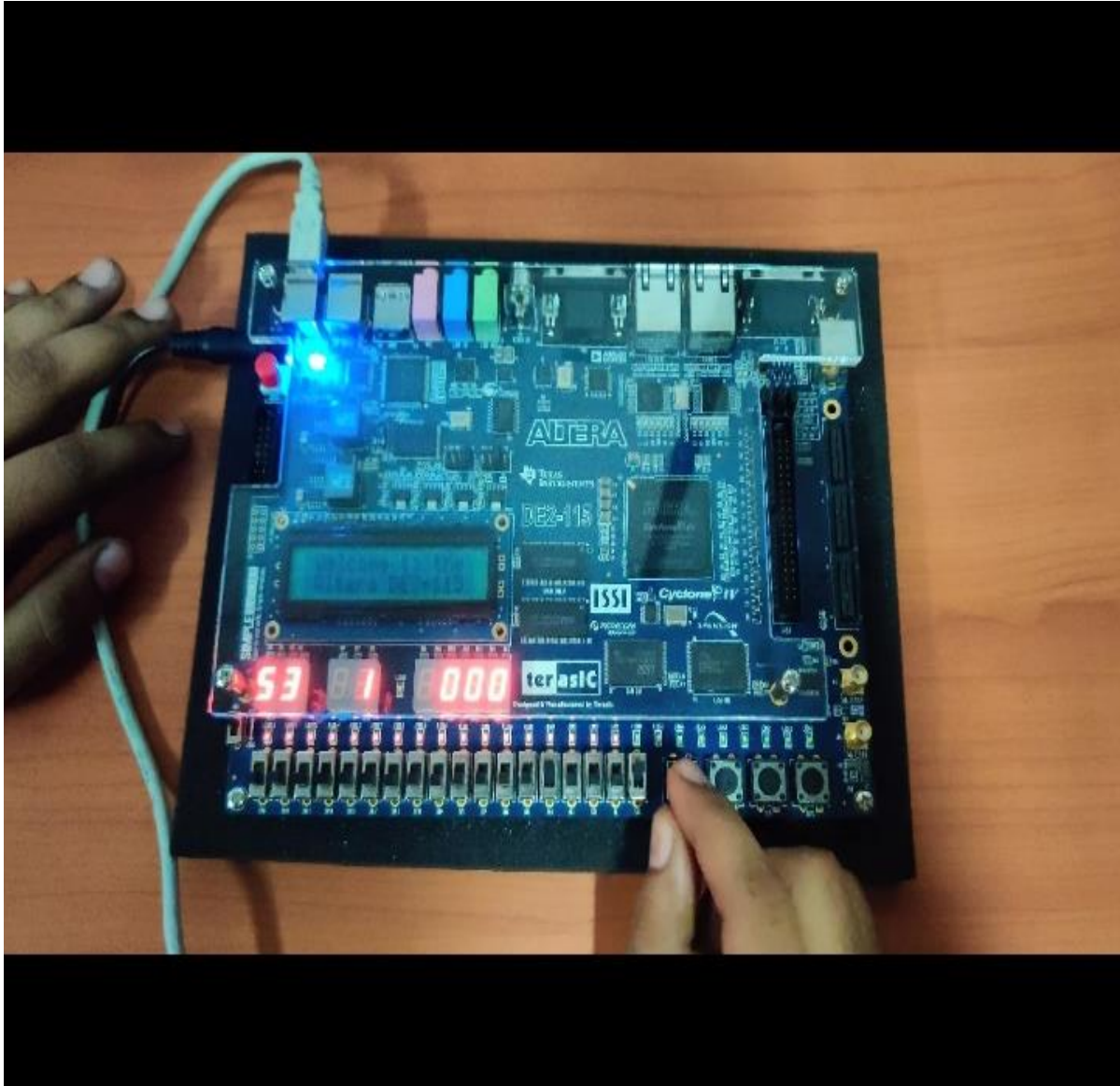
VERILOG CODE IN QUARTUS-II SOFTWARE :

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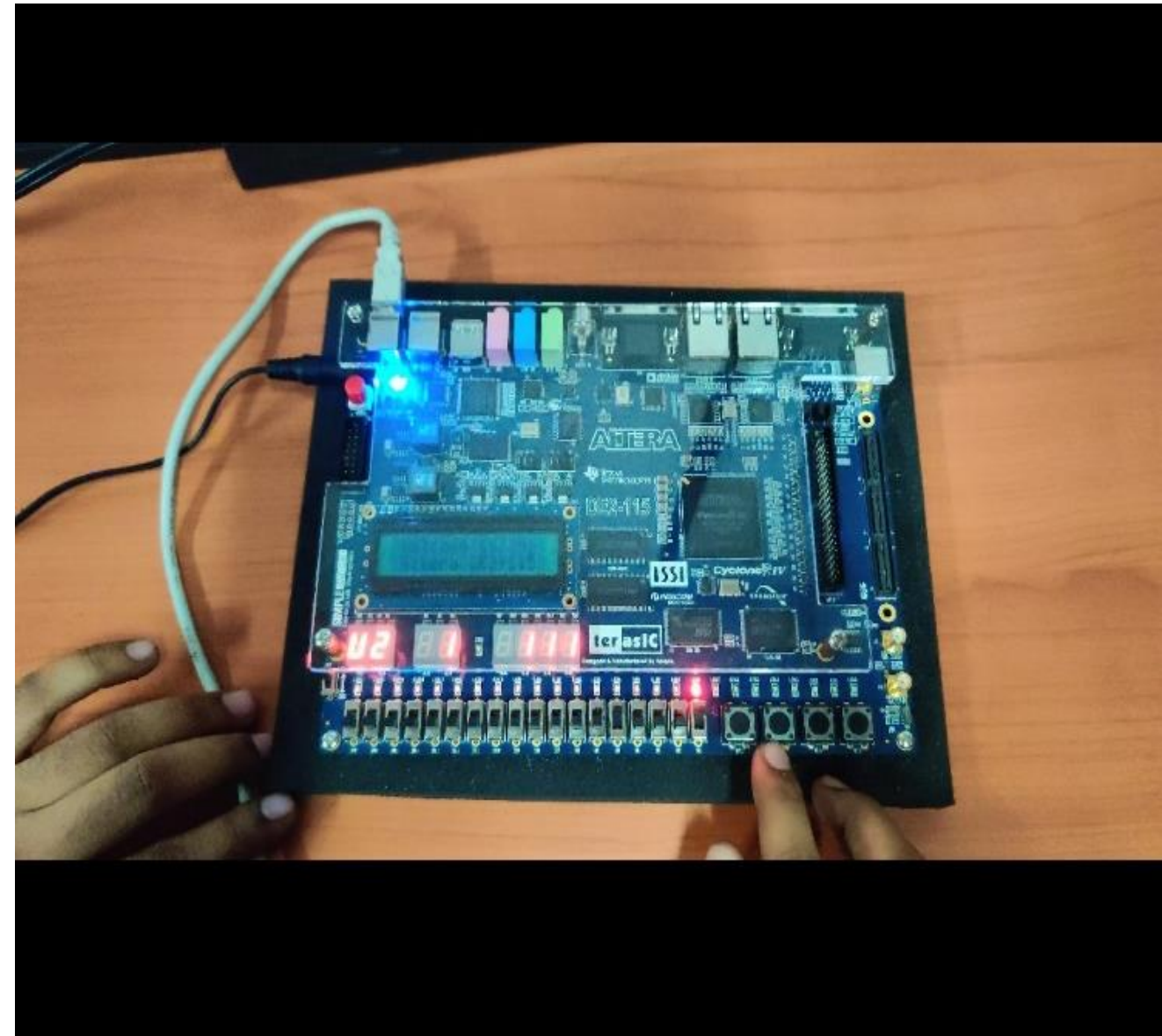
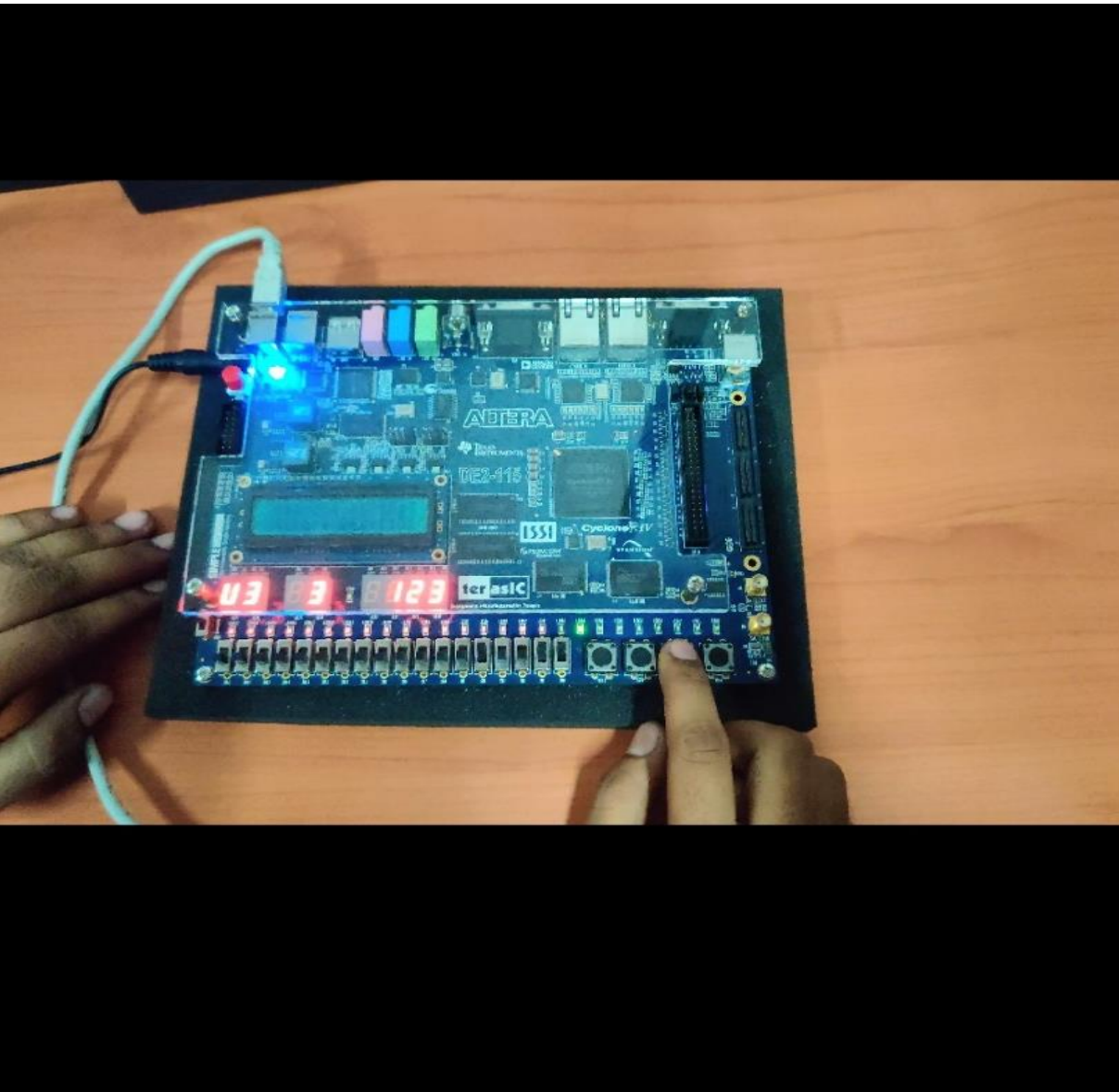
KIT IMPLEMENTATION IN FPGA KIT :

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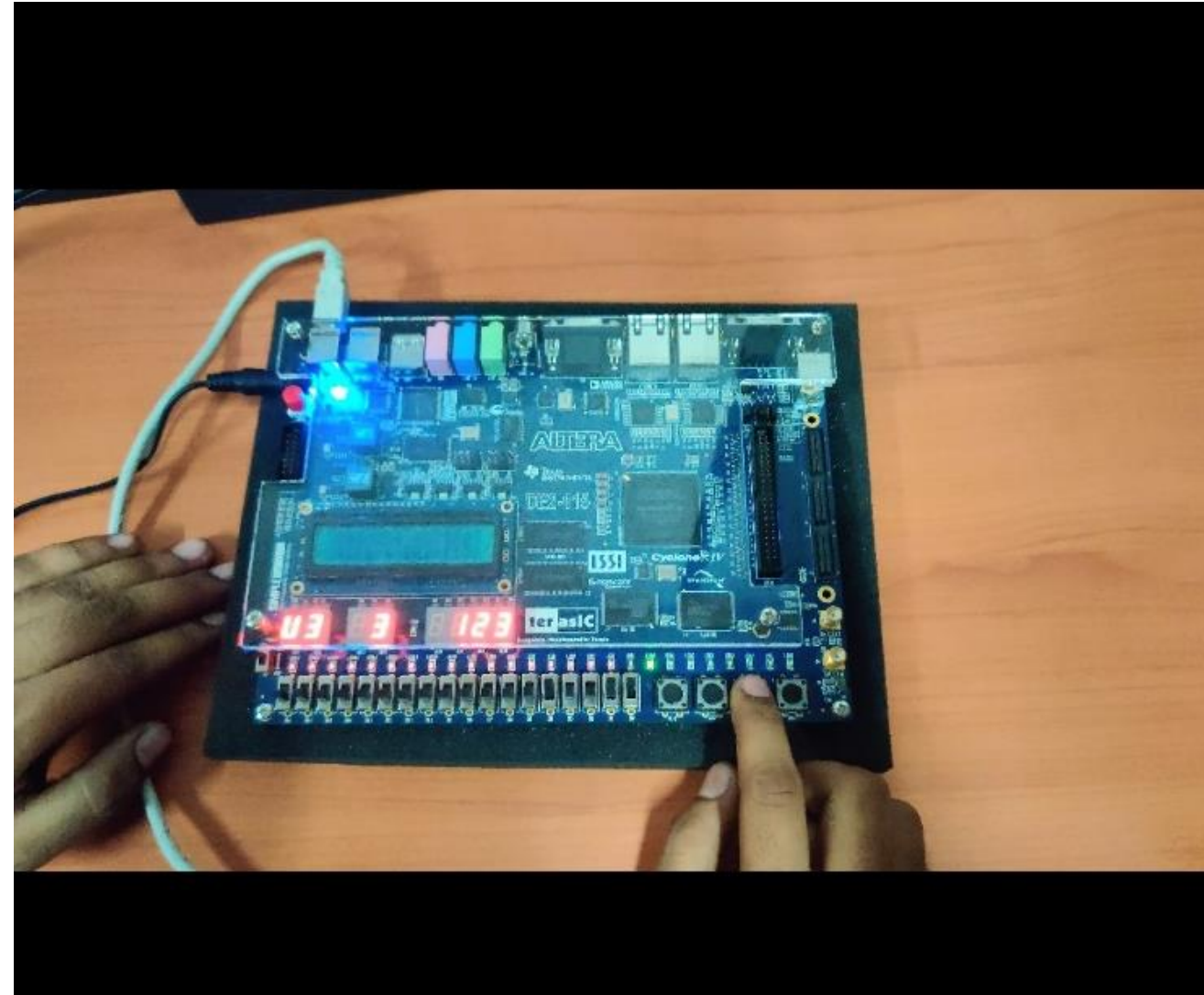
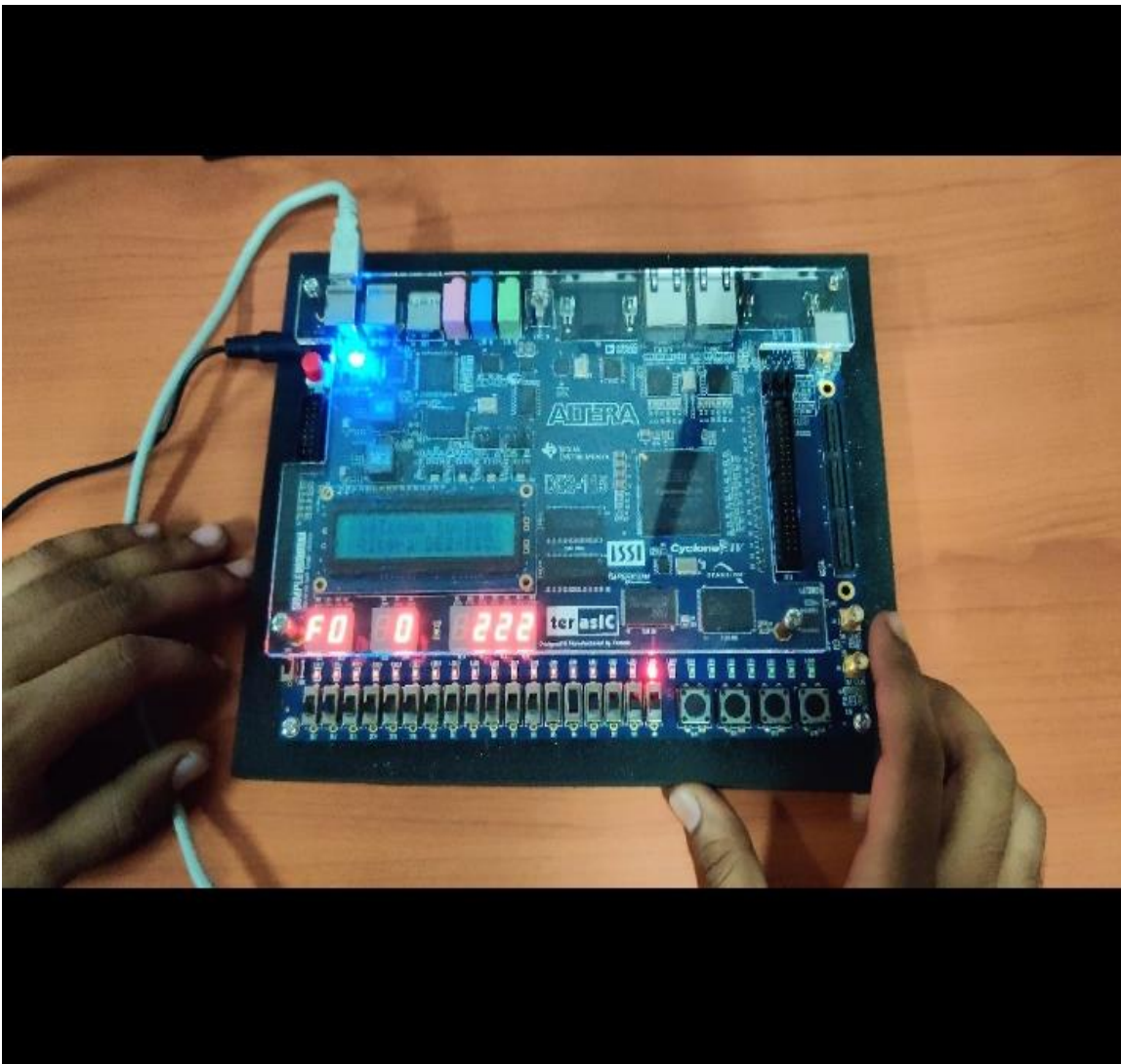
KIT IMPLEMENTATION IN FPGA KIT :

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KIT IMPLEMENTATION IN FPGA KIT :

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FPGA KIT DEMONSTRATION VIDEO:

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<https://drive.google.com/drive/folders/1bBPgs8-IQYcbvaz6iMaDZXlyYE9bi7g6>

REFERENCE:

- **Digital Logic and Computer Design** - M.Morris Mano (2017 edition)
- **A Guide To Digital Design And Synthesis** – Samir Palnitkar (1996 edition)
- **System Verilog For Verification** – Chris Spear & Greg Tumbush (2006 edition)
- **Research Article** – International Journal of Advance Technology and Engineering Exploration

WEBSITES

- <https://ieeexplore.ieee.org>
- <https://www.cornell.edu>
- <https://www.design-reuse.com>
- <https://www.edn.com>

THANK YOU!