SET 3

SR 22

St. Peter's Engineering College (Autonomous) Dullapally (P), Medchal, Hyderabad – 500100. II - Mid Term Examination – November 2024						Dept.	:	CSM, CSC, CSD
						Academic Year 2024-25		
Subject Code	:	AS22-05PC06	**Subject**	:	**COMPUTER ORGANIZATION AND ARCHITECTURE**			
Class/Section	:	**B. Tech.**	**Year**	:	**II**	**Semester**	:	**I**
Duration	:	120 Min	**Max. Marks**	:	**30**	**Date:**	:	

BLOOMS LEVEL					
Remember	**L1**	**Understand**	**L2**	**Apply**	**L3**
Analyze	**L4**	**Evaluate**	**L5**	**Create**	**L6**

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PART – A (10x1M = 10M)

Note: Answer all Questions. Each Question carries equal marks.

Q. No	Question (s)	Marks	BL	CO
	UNIT - III			
1	**a.** Find the 2's complement of the following eight-digit binary number a. 10101110 b. 10000001	**1M**	L2	C213.5
	b. Explain why should the sign of the remainder after a division be the same as the sign of the dividend	**1M**	L2	C213.5
	UNIT – IV			
	c. Define Priority Interrupt	**1M**	L1	C213.3
	d. What are Auxiliary and Cache memory	**1M**	L1	C213.3
	e. Write one operational difference between the main memory and the auxiliary memory	**1M**	L1	C213.3
	f. Draw the timing diagram of Source initiated handshaking	**1M**	L3	C213.3
	UNIT – V			
	g. What is hardware interlock?	**1M**	L1	C213.4
	h. Discuss the difference between tightly coupled and loosely coupled multiprocessors	**1M**	L2	C213.4
	i. What are the three major pipeline conflicts?	**1M**	L1	C213.4
	j. Define LRU and FIFO	**1M**	L1	C213.4

PART – B (20M)

Q. No	Question (s)	Marks	BL	CO
	UNIT - III			
2	a. Draw the flowchart of Booth algorithm of Multiplication	**4M**	L3	C213.5

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	OR			
3	b. Draw and explain the hardware for signed–magnitude addition and subtraction.	**4M**	L2	C213.5
	UNIT – IV			
4	a. What is meant by handshaking? Explain with a neat diagram	**4M**	L2	C213.3
	b. What is the difference between isolated I/O and memory-mapped I/O?	**4M**	L2	C213.3
	OR			
5	a. Calculate the 128x8 RAM and 512x8 ROM chips required to design a computer system that needs 512 bytes of RAM and 512 bytes of ROM. Also, give the memory address map	**4M**	L3	C213.3
	b. Explain the cache memory mapping techniques	**4M**	L2	C213.3
	UNIT – V			
6	Explain three major pipeline conflicts.	**4M**	L1	C213.4
	Explain the instruction pipeline in detail with a suitable example. Also, discuss the difficulties that cause the instruction pipeline to deviate from its normal operation	**4M**	L2	C213.4
	OR			
7	Explain Mutual Exclusion with a Semaphore	**4M**	L2	C213.4
	Discuss about SIMD Array processors	**4M**	L2	C213.4

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