

UNIT-2

2Marks Questions

1) What is minterm and maxterm?

Ans Minterm: A product term which contains all the variables of the function either in complemented or uncomplemented form is known as Minterm.

It is denoted by ' m_i '.

Ex: $f(A, B, C) = AB + B\bar{C} + \bar{A}\bar{B}$ \rightarrow minterm.

Max-term: A sum term which contains each of 'n' variables in either complemented or uncomplemented form is called a Maxterm. It is denoted by ' M_i '.

Ex: $f(A, B, C) = (A+B+\bar{C}) \cdot (B+\bar{C}) \cdot (A+\bar{B})$ \rightarrow maxterm.

2) Simplify $F(x, y, z) = \sum m(0, 1, 3, 4, 6)$ using K-map.

Ans

	$\bar{y}\bar{z}$	$\bar{y}z$	yz	$y\bar{z}$
\bar{x}	1	1	1	
x	1	4	5	6

Result:

Pair = 3

equation:

$$f = \bar{y}\bar{z} + \bar{x}z + x\bar{z}$$

3) Write the differences between Multiplexer and Demultiplexer.

Ans Differences:

Multiplexer	Demultiplexer
1) The circuit which accepts multiple inputs but presents only one output is known as Multiplexer.	1) The circuit which accepts only one input and presents multiple outputs is known as Demultiplexer.
2) The Multiplexer is commonly known as Data selector.	2) The Demultiplexer is commonly known as data distributor.
3) It works with the principle of many to one.	3) It works with the principle of One-to Many.
4) Ex: 2x1 MUX, 4x1 MUX, 8x1 MUX, 16x1 MUX etc.	4) Ex: 1x2 Demux, 1x4 Demux, 1x8 Demux, 1x16 Demux etc.

4) What is combinational circuit? Give examples.

Ans. Combinational circuits are used in digital electronics such as computers to perform operations on data.

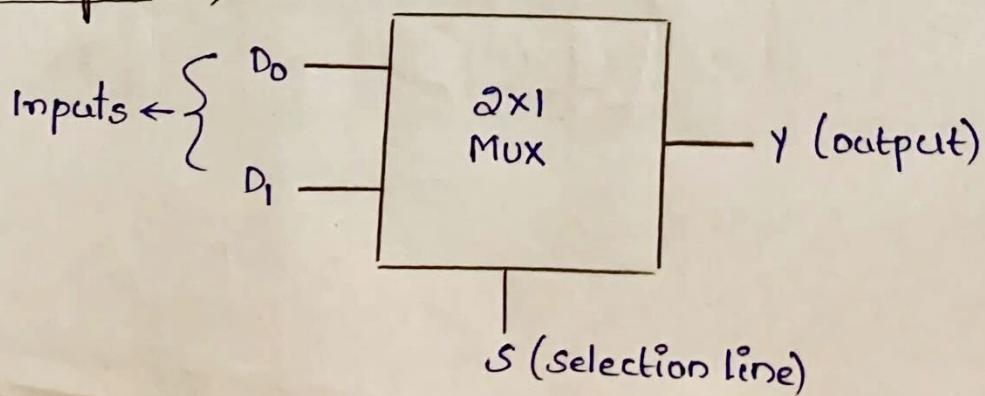
Combinational circuits are digital logic circuits whose instantaneous output depends only on the combination of their inputs.

Ex: Multiplexer, Demultiplexer, Encoder, Decoder.

5) Explain 2x1 Multiplexer with neat logic diagram.

Ans A 2x1 Multiplexer is a combinational logic circuit that has only two inputs, 1 selection line and only one output.

Logic diagram:



3-Marks Questions

- 1) Convert $F(A, B, C, D) = B\bar{C} + A\bar{C}D + \bar{A}BC + \bar{A}\bar{B}$ into standard SOP and standard POS.

Ans $f = B\bar{C} + A\bar{C}D + \bar{A}BC + \bar{A}\bar{B}$

$$= (1)B\bar{C}(1) + A(1)\bar{C}D + \bar{A}BC(1)(1) + \bar{A}\bar{B}(1)(1) \quad (\because A + \bar{A} = 1)$$

$$= (A + \bar{A})B\bar{C}(D + \bar{D}) + A(B + \bar{B})\bar{C}D + \bar{A}BC(D + \bar{D}) + \bar{A}\bar{B}(C + \bar{C})(D + \bar{D})$$

$$= (A + \bar{A})(B\bar{C}D + B\bar{C}\bar{D}) + AB\bar{C}D + A\bar{B}\bar{C}D + \bar{A}BC\bar{D} + \bar{A}\bar{B}(CD + C\bar{D} + \bar{C}D + \bar{C}\bar{D})$$

$$= AB\bar{C}D + AB\bar{C}\bar{D} + \bar{A}B\bar{C}D + \bar{A}B\bar{C}\bar{D} + AB\bar{C}D + A\bar{B}\bar{C}D + \bar{A}BC\bar{D} + \bar{A}BC\bar{D} + \bar{A}\bar{B}CD + \bar{A}\bar{B}C\bar{D} + \bar{A}\bar{B}\bar{C}D + \bar{A}\bar{B}\bar{C}\bar{D}.$$

110 1100 0101 0100 1101 1001 0111 0110
 ⑬ ⑫ ⑤ ④ ⑮ ⑯ ⑦ ⑥
 0011 0010 0001 0000
 ③ ② ① ⑩

(Min term)
 $A \rightarrow 1$
 $\bar{A} \rightarrow 0$

The standard SOP is: $f = \sum m(0, 1, 2, 3, 4, 5, 6, 7, 9, 12, 13)$

The standard POS is: $f = \prod M(8, 10, 11, 14, 15)$

- 2) Implement the following boolean function using K-map

$$F(A, B, C, D) = \sum m(0, 2, 6, 10, 11, 12, 13) + d(3, 8, 14) \text{ and draw the logic diagram.}$$

Ans.

AB \ CD	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	0	1	X	1
$\bar{A}B$	4	5	3	6
AB	12	13	15	14
$A\bar{B}$	8	9	11	10

Result: \Rightarrow

$$\text{Quad} = 2$$

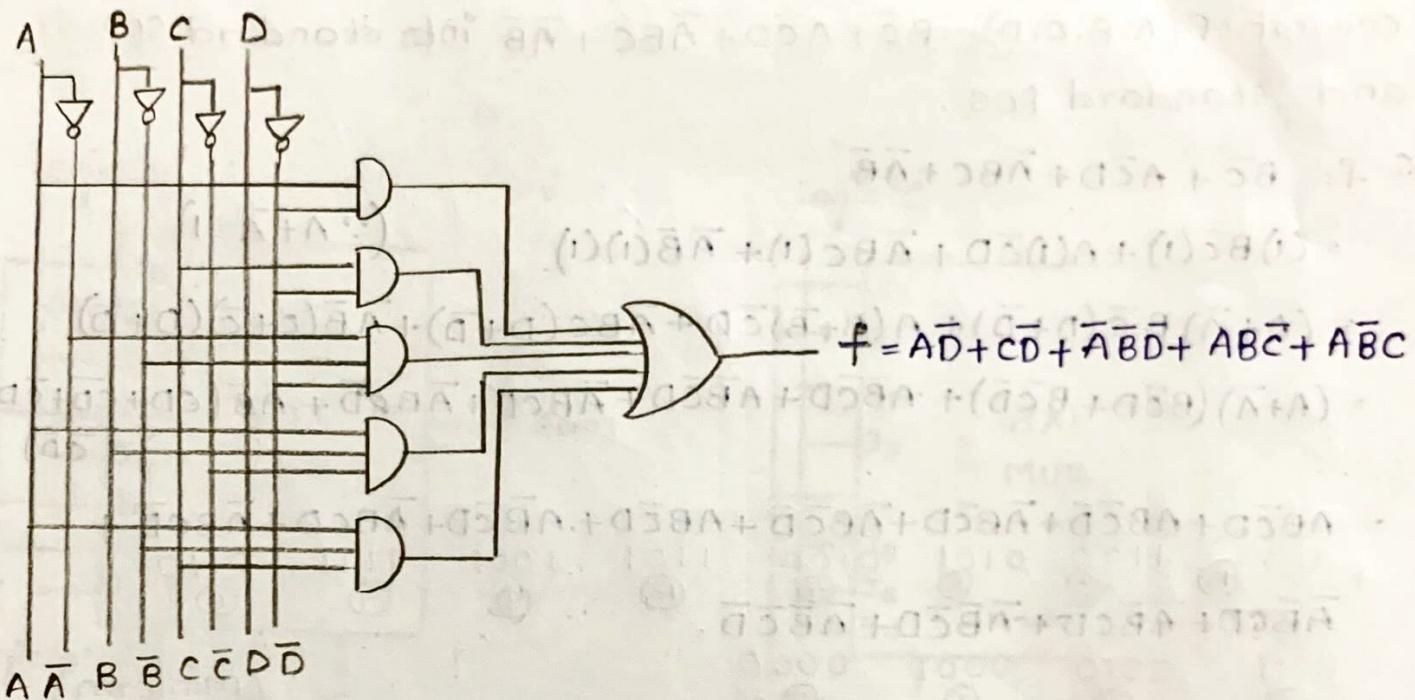
$$\text{Pair} = 3$$

equation: \Rightarrow

$$f = A\bar{D} + C\bar{D} + \bar{A}\bar{B}\bar{D} + AB\bar{C} + A\bar{B}C$$

0	0	0	0
1	1	0	0
1	0	1	0
0	1	1	0
1	0	0	1
1	1	1	1
1	1	1	1

Logic diagram:



3) Implement a full adder circuit using 8:1 Multiplexer.

Ans. Implementation of full adder using 8x1 MUX:

Truth table of full adder:

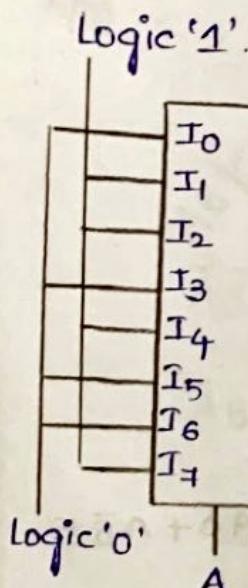
A	B	C	sum	carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

$$\text{equations: } \text{sum} = \Sigma m(1, 2, 4, 7)$$

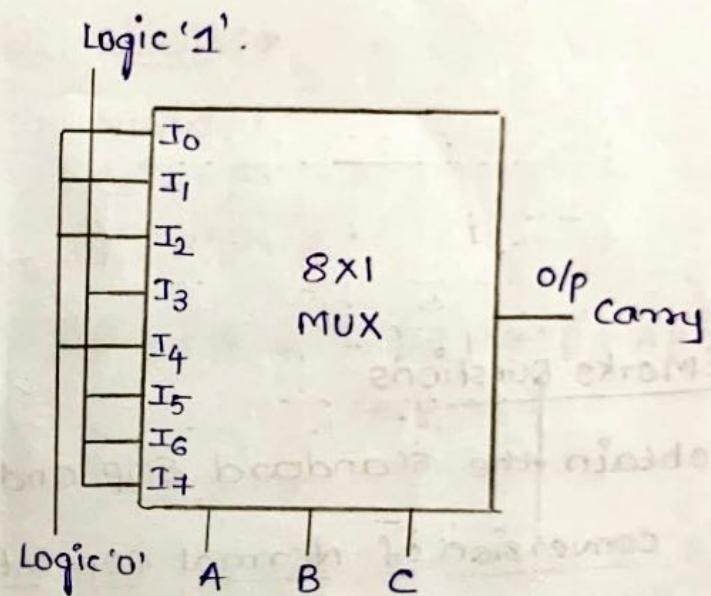
$$\text{Carry} = \Sigma m(3, 5, 6, 7)$$

Realization of circuit using 8x1 MUX :-

For sum :-



For carry :-



4) construct 4:1 MUX using logic gates and Truth table.

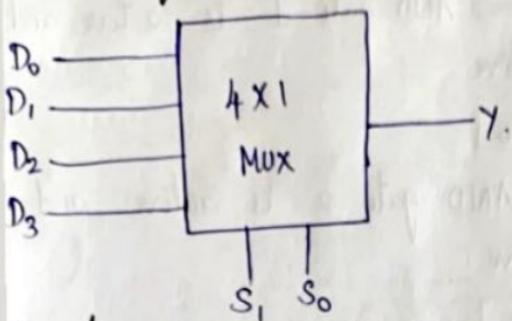
4:1 Multiplexer :-

The number of input lines are four and there will be two select lines.

There will be one output line.

4 : 1
→ 2 → Two Select lines.

Block diagram:



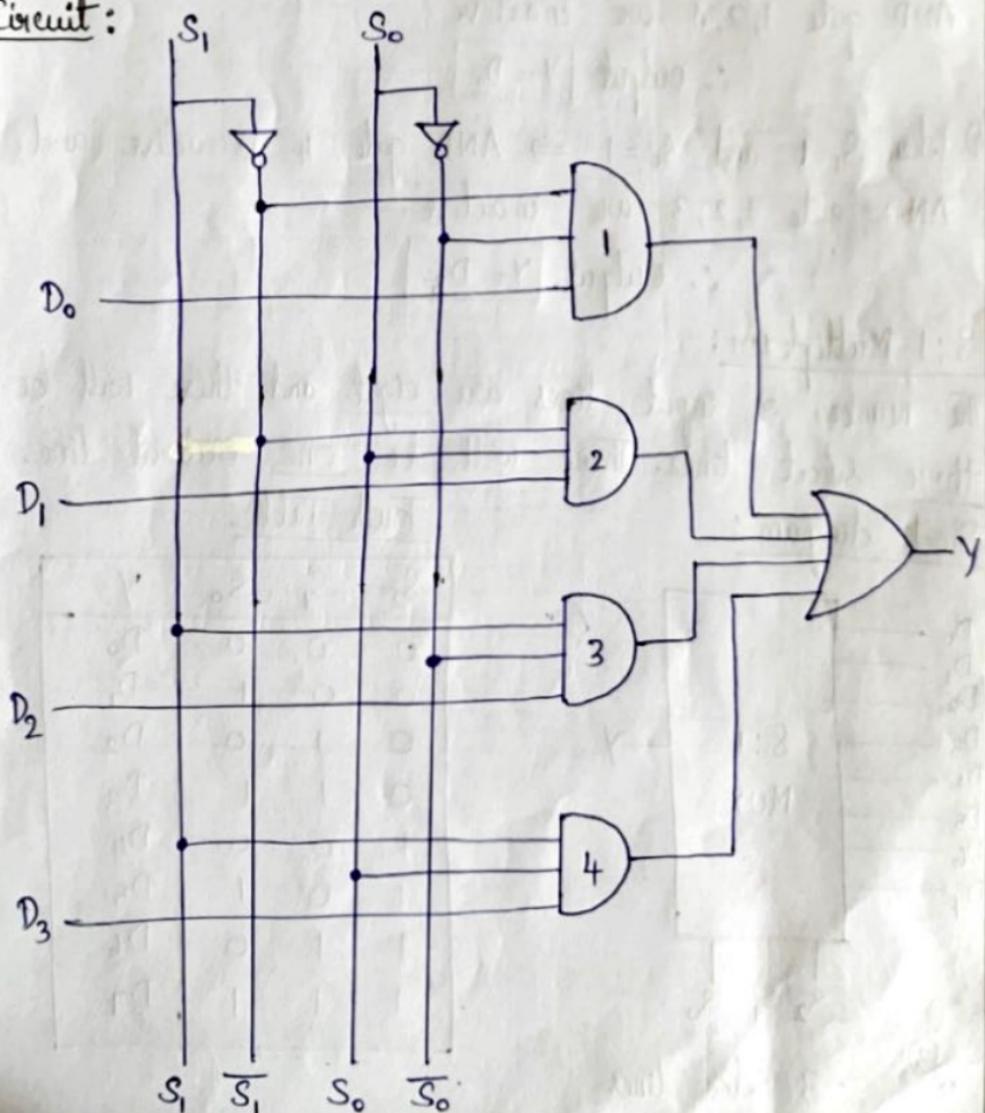
Truth Table:

S_1	S_0	Y
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3

Equation:

$$Y = \overline{S_1} \overline{S_0} D_0 + \overline{S_1} S_0 D_1 + S_1 \overline{S_0} D_2 + S_1 S_0 D_3$$

Circuit:



Operation:

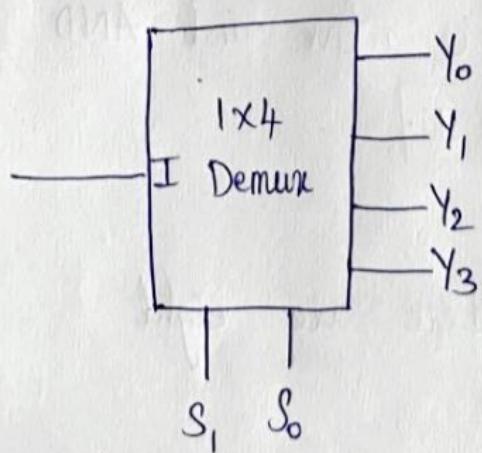
- 1) When $S_1 = 0$ and $S_0 = 0 \Rightarrow$ AND gate 1 is active and AND gate 2, 3, 4 are inactive
 \therefore output $Y = D_0$
- 2) When $S_1 = 0$ and $S_0 = 1 \Rightarrow$ AND gate 2 is active and AND gate 1, 3, 4 are inactive.
 \therefore output $Y = D_1$
- 3) When $S_1 = 1$ and $S_0 = 0 \Rightarrow$ AND gate 3 is active and AND gate 1, 2, 4 are inactive.
 \therefore output $Y = D_2$
- 4) When $S_1 = 1$ and $S_0 = 1 \Rightarrow$ AND gate 4 is active and AND gate 1, 2, 3 are inactive.
 \therefore output $Y = D_3$

5) construct 1:4 Demux using logicgates and -truthtable

Ans 1x4 Demux :-

It has one input and four outputs. The number of selection lines are two.

Block diagram :



Truth Table :

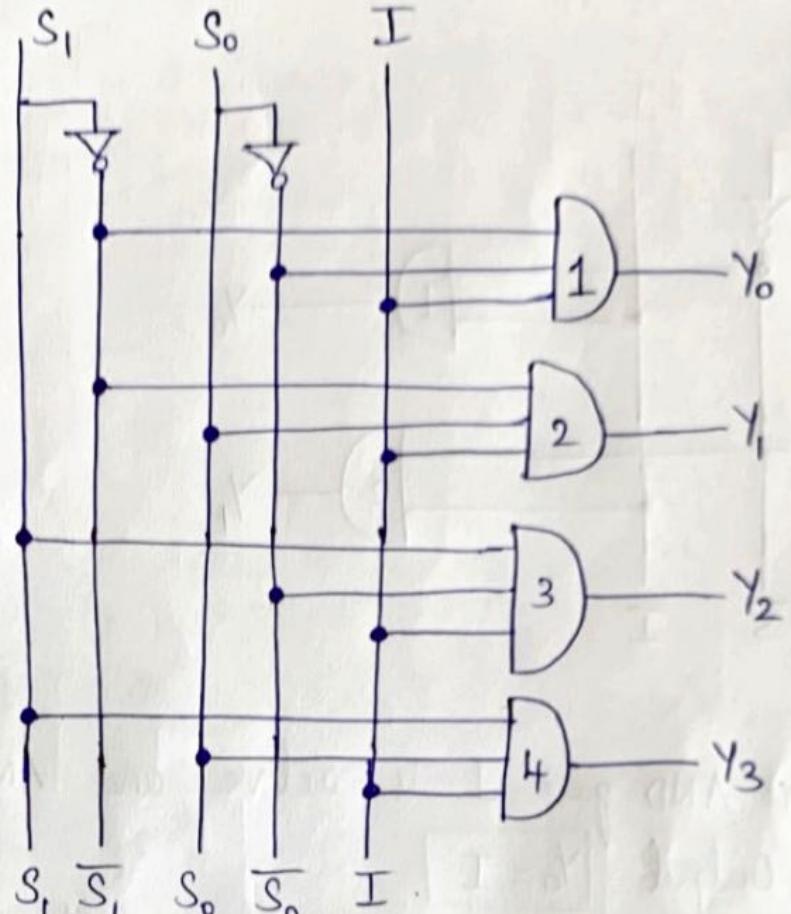
S ₁	S ₀	Y ₃	Y ₂	Y ₁	Y ₀
0	0	0	0	0	I
0	1	0	0	I	0
1	0	0	I	0	0
1	1	I	0	0	0

Equation : $Y_0 = \overline{S}_1 \overline{S}_0 I$ $Y_1 = \overline{S}_1 S_0 I$

$$Y_2 = S_1 \overline{S}_0 I$$

$$Y_3 = S_1 S_0 I$$

Circuit :-



Operation :

- 1) When $S_1=0$ and $S_0=0 \Rightarrow$ AND gate 1 is active and AND gate 2, 3, 4 are inactive. Output $Y_0 = I$
- 2) When $S_1=0$ and $S_0=1 \Rightarrow$ AND gate 2 is active and AND gate 1, 3, 4 are inactive. Output $Y_1 = I$
- 3) When $S_1=1$ and $S_0=0 \Rightarrow$ AND gate 3 is active and AND gate 1, 2, 4 are inactive. Output $Y_2 = I$
- 4) When $S_1=1$ and $S_0=1 \Rightarrow$ AND gate 4 is active and AND gate 1, 2, 3 are inactive. Output $Y_3 = I$

5 Marks Questions

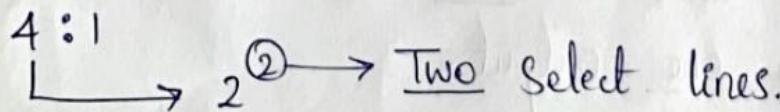
1st Question is in page 19

2) Design a 4×1 Multiplexer.

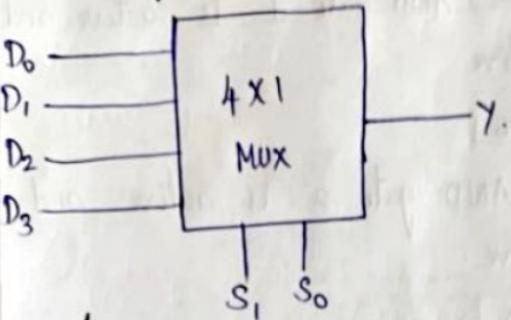
Ans 4:1 Multiplexer :-

The number of input lines are four and there will be two select lines.

There will be one output line.

$4:1$  Two Select lines.

Block diagram:



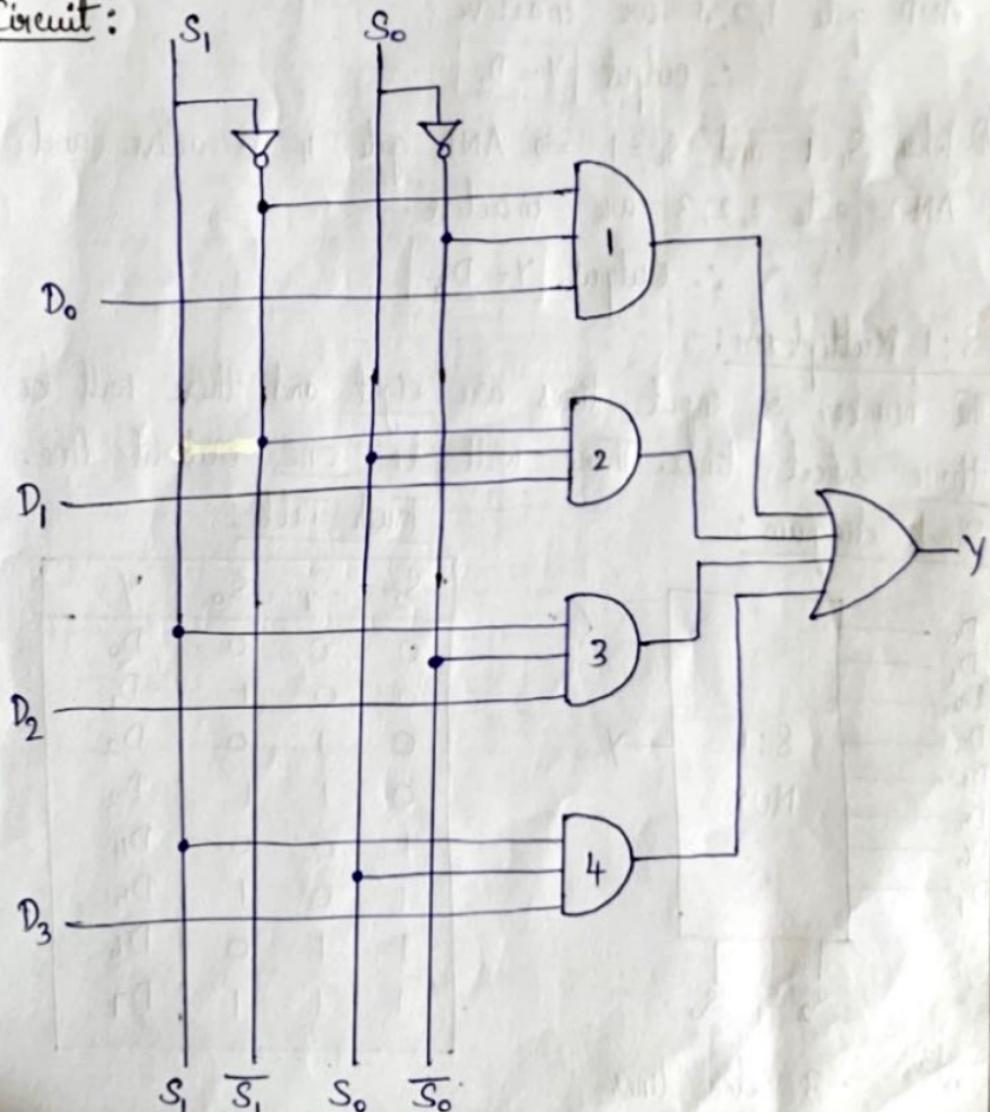
Truth Table:

S_1	S_0	Y
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3

Equation:

$$Y = \overline{S_1} \overline{S_0} D_0 + \overline{S_1} S_0 D_1 + S_1 \overline{S_0} D_2 + S_1 S_0 D_3$$

Circuit:



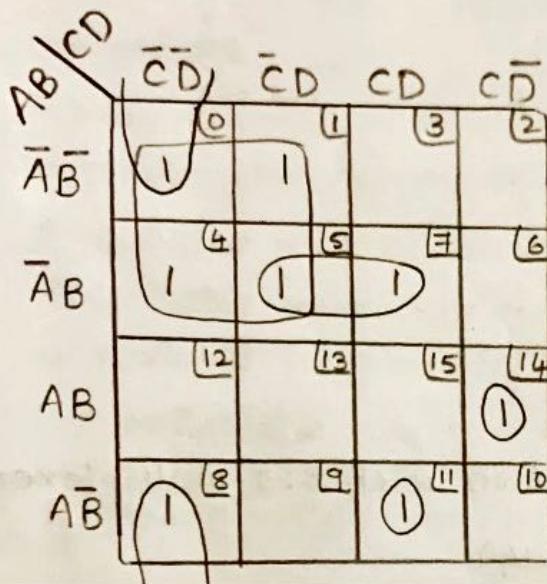
Operation:

- When $S_1 = 0$ and $S_0 = 0 \Rightarrow$ AND gate 1 is active and AND gate 2, 3, 4 are inactive
 \therefore Output $Y = D_0$
- When $S_1 = 0$ and $S_0 = 1 \Rightarrow$ AND gate 2 is active and AND gate 1, 3, 4 are inactive.
 \therefore Output $Y = D_1$
- When $S_1 = 1$ and $S_0 = 0 \Rightarrow$ AND gate 3 is active and AND gate 1, 2, 4 are inactive.
 \therefore Output $Y = D_2$
- When $S_1 = 1$ and $S_0 = 1 \Rightarrow$ AND gate 4 is active and AND gate 1, 2, 3 are inactive.
 \therefore Output $Y = D_3$

3) Simplify the Boolean function using K-map
 $f(A, B, C, D) = \sum m(0, 1, 4, 5, 7, 8, 11, 14)$ and draw the logic diagram.

Ans.

K-map: →



Result: →

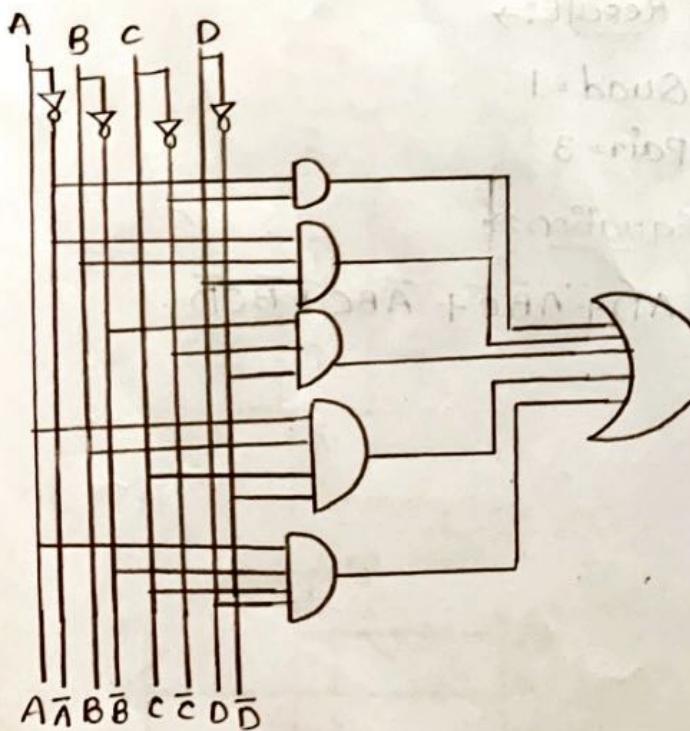
Quad = 1

Pair = 2

equation: →

$$F = \bar{A}\bar{C} + \bar{A}BD + \bar{C}\bar{D}\bar{B} + ABC\bar{D} + A\bar{B}CD$$

Logic diagram: →



$$F = \bar{A}\bar{C} + \bar{A}BD + \bar{B}\bar{C}\bar{D} + ABC\bar{D} + A\bar{B}CD$$

4) Simplify the following boolean expression using K-map and implement it with AOI logic gates.

$$F(A, B, C, D) = \sum m(1, 6, 7, 11, 15) + d(0, 2, 3, 5)$$

Ans

K-Map: →

		$\bar{C}\bar{D}$		$\bar{C}D$		CD		$C\bar{D}$								
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14
$\bar{A}\bar{B}$	X	1		X	X											
	4	5			7											6
$\bar{A}B$		X		1												
	12	13			15											14
AB				1												
	8	9			11											10
$A\bar{B}$																

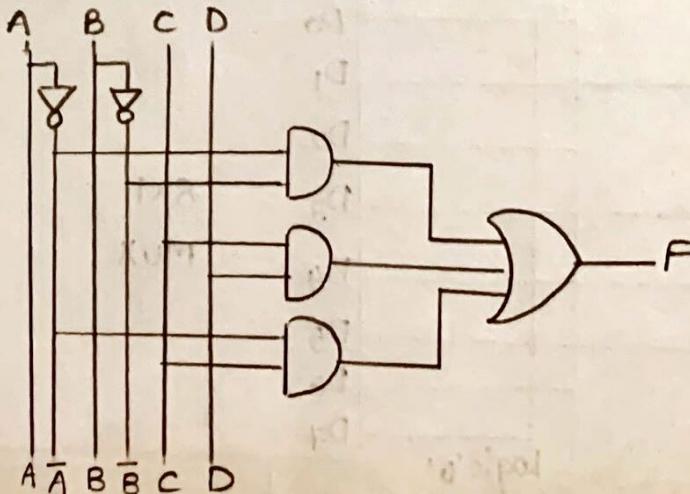
Result: →

Quad = 3.

equation: →

$$F = \bar{A}\bar{B} + CD + \bar{A}C$$

Logic diagram: →

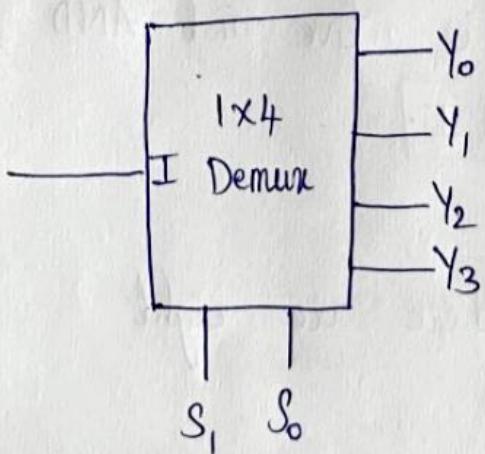


5) Design 1:4 Demultiplexer

Ans. 1x4 Demux :-

It has one input and four outputs. The number of selection lines are two.

Block diagram :-



Truth Table :-

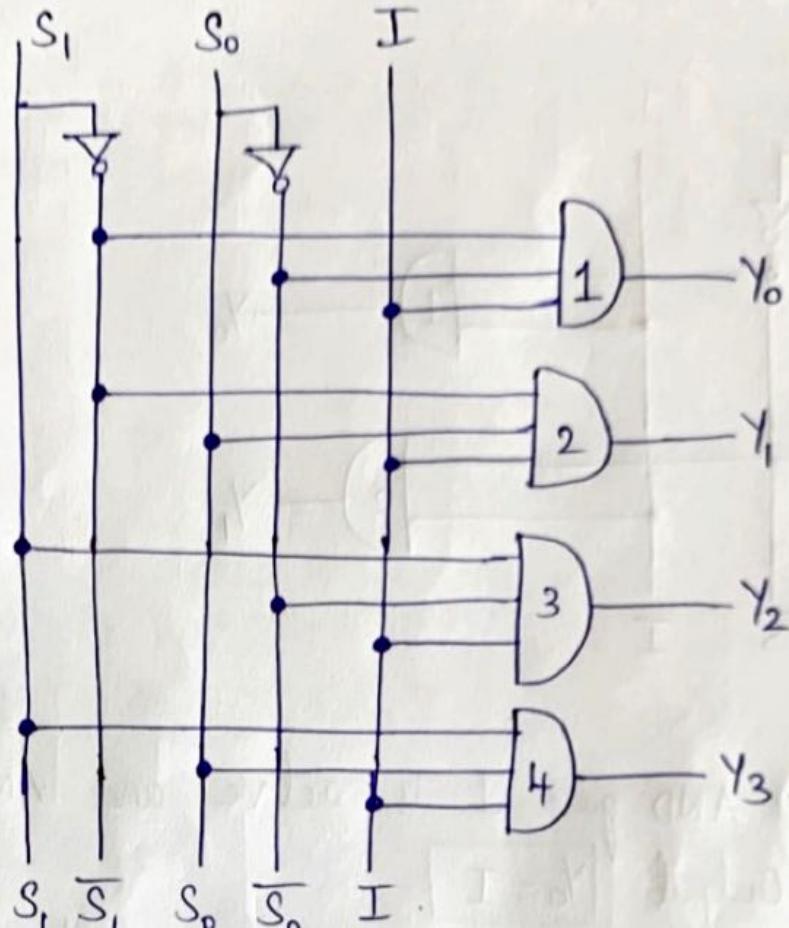
S ₁	S ₀	Y ₃	Y ₂	Y ₁	Y ₀
0	0	0	0	0	I
0	1	0	0	I	0
1	0	0	I	0	0
1	1	I	0	0	0

Equation :- $Y_0 = \overline{S}_1 \overline{S}_0 I$ $Y_1 = \overline{S}_1 S_0 I$

$$Y_2 = S_1 \overline{S}_0 I$$

$$Y_3 = S_1 S_0 I$$

Circuit :-



Operation :

- 1) When $S_1=0$ and $S_0=0 \Rightarrow$ AND gate 1 is active and AND gate 2, 3, 4 are inactive. Output $Y_0 = I$
- 2) When $S_1=0$ and $S_0=1 \Rightarrow$ AND gate 2 is active and AND gate 1, 3, 4 are inactive. Output $Y_1 = I$
- 3) When $S_1=1$ and $S_0=0 \Rightarrow$ AND gate 3 is active and AND gate 1, 2, 4 are inactive. Output $Y_2 = I$
- 4) When $S_1=1$ and $S_0=1 \Rightarrow$ AND gate 4 is active and AND gate 1, 2, 3 are inactive. Output $Y_3 = I$

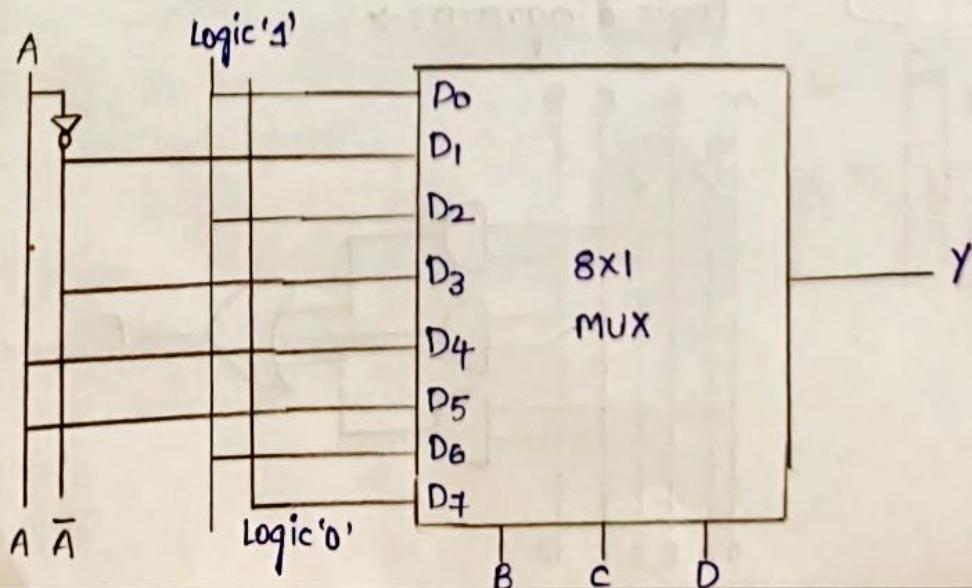
10 marks Questions .

- 1(a) Implement the following boolean function with 8:1 multiplexers
 $F(A, B, C, D) = \sum m(0, 2, 6, 10, 12, 13) + d(1, 3, 8, 14)$

Ans (a) Implementation table: →

	D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇
\bar{A}	0	1	2	3	4	5	6	7
A	8	9	10	11	12	13	14	15
	1	\bar{A}	1	\bar{A}	A	A	1	0

(b) Multiplexer Implementation: →



b) Write short notes on K-Map. Implement the following Boolean function by using K-Map $f(A_1B_1C_1D_1) = \sum m(1, 6, 7, 10, 13, 15) + \sum d(0, 2, 9, 11)$

Ans K-Map: \rightarrow

Karnaugh Map is a graphical method of simplifying boolean expressions.

K-Map consists of boxes called as cells and each cell represents a particular combination of input.

2 variable map consists of $2^2 = 4$ cells.

3 variable map consists of $2^3 = 8$ cells.

4 variable map consists of $2^4 = 16$ cells.

'n' variable K-Map can have ' 2^n ' cells.

K-Map Simplification: \rightarrow

AB/CD	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	(6) X	(1)		(2) X
$\bar{A}B$	(4)	(5)	(7) X	(6)
$A\bar{B}$	(12)	(13)	(15)	(14)
$A\bar{B}$	(8) X	(9) X	(11) X	(10) X

Result: \rightarrow

Quad = 1

Pair = 3

Equation: \rightarrow

$$f = AD + \bar{A}\bar{B}\bar{C} + \bar{A}BC + \bar{B}CD.$$

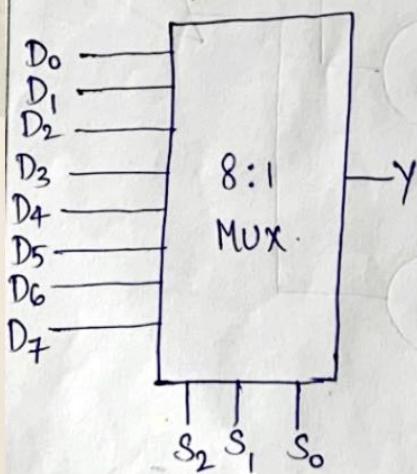
Q) construct 8:1 MUX using logic gates and truthtable.

Ans

8:1 Multiplexer :-

The number of input lines are eight and there will be one output line.
three select lines. There will be one output line.

Block diagram :



Truth Table:

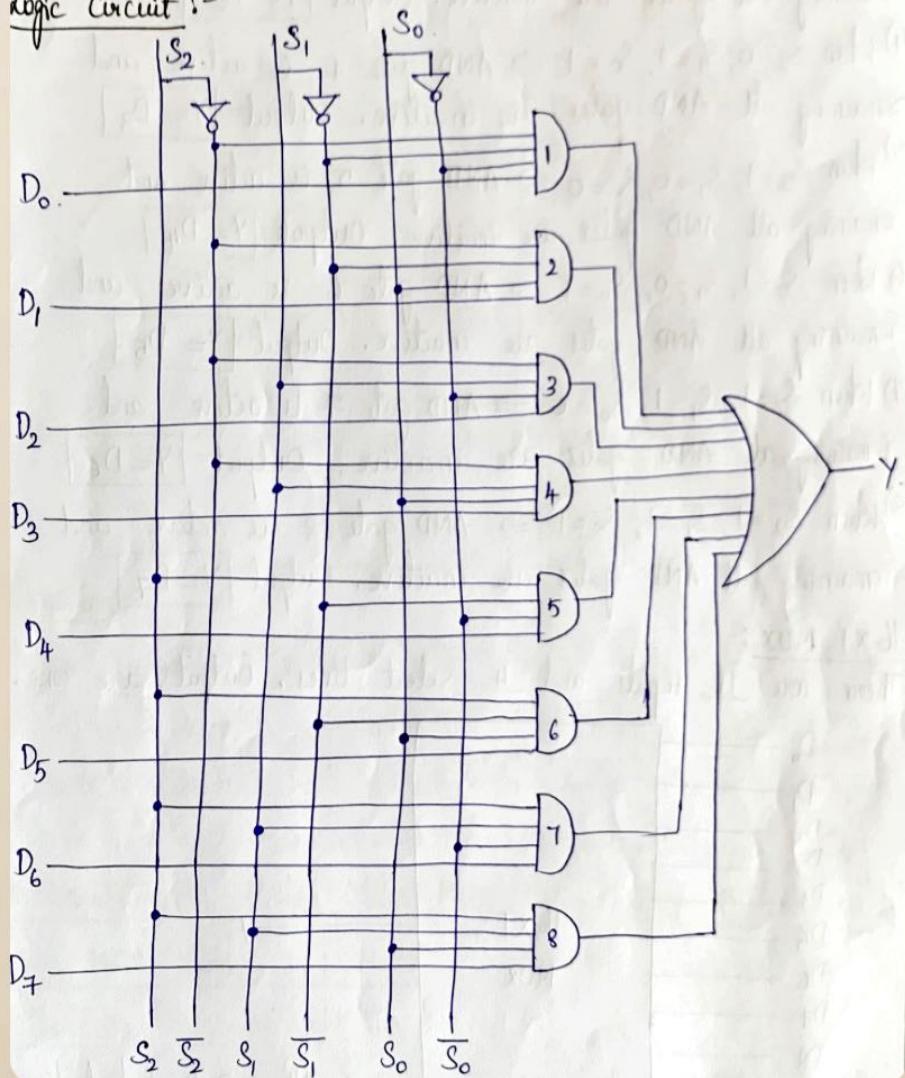
S_2	S_1	S_0	Y
0	0	0	D_0
0	0	1	D_1
0	1	0	D_2
0	1	1	D_3
1	0	0	D_4
1	0	1	D_5
1	1	0	D_6
1	1	1	D_7

$\alpha^3 \rightarrow 3$ Select lines.

Equation :

$$Y = \overline{S_2} \overline{S_1} \overline{S_0} D_0 + \overline{S_2} \overline{S_1} S_0 D_1 + \overline{S_2} S_1 \overline{S_0} D_2 + \overline{S_2} S_1 S_0 D_3 + S_2 \overline{S_1} \overline{S_0} D_4 + \\ S_2 \overline{S_1} S_0 D_5 + S_2 S_1 \overline{S_0} D_6 + S_2 S_1 S_0 D_7$$

Logic Circuit :-



Operation :-

- 1). When $S_2=0, S_1=0, S_0=0 \Rightarrow$ AND gate 1 is active and remaining all AND gates are inactive. Output $\boxed{Y=D_0}$.
- 2). When $S_2=0, S_1=0, S_0=1 \Rightarrow$ AND gate 2 is active and remaining all AND gates are inactive. Output $\boxed{Y=D_1}$.
- 3). When $S_2=0, S_1=1, S_0=0 \Rightarrow$ AND gate 3 is active and remaining all AND gates are inactive. Output $\boxed{Y=D_2}$.
- 4). When $S_2=0, S_1=1, S_0=1 \Rightarrow$ AND gate 4 is active and remaining all AND gates are inactive. Output $\boxed{Y=D_3}$.
- 5). When $S_2=1, S_1=0, S_0=0 \Rightarrow$ AND gate 5 is active and remaining all AND gates are inactive. Output $\boxed{Y=D_4}$.
- 6). When $S_2=1, S_1=0, S_0=1 \Rightarrow$ AND gate 6 is active and remaining all AND gates are inactive. Output $\boxed{Y=D_5}$.
- 7). When $S_2=1, S_1=1, S_0=0 \Rightarrow$ AND gate 7 is active and remaining all AND gates are inactive. Output $\boxed{Y=D_6}$.
- 8). When $S_2=1, S_1=1, S_0=1 \Rightarrow$ AND gate 8 is active and remaining all AND gates are inactive. Output $\boxed{Y=D_7}$.

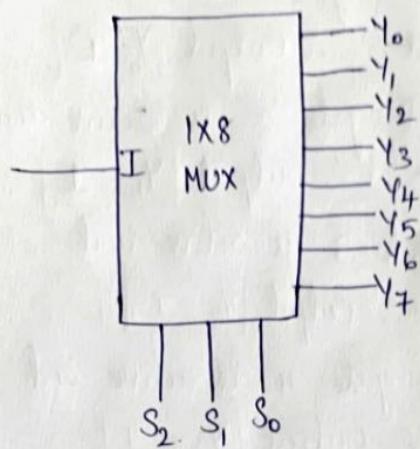
3) Design 1:8 DeMUX using logic gates and truth table

Ans | 1X8 Demux :-

The number of inputs are one and there are eight output lines.

There are three selection lines.

Block diagram:



Truth Table:

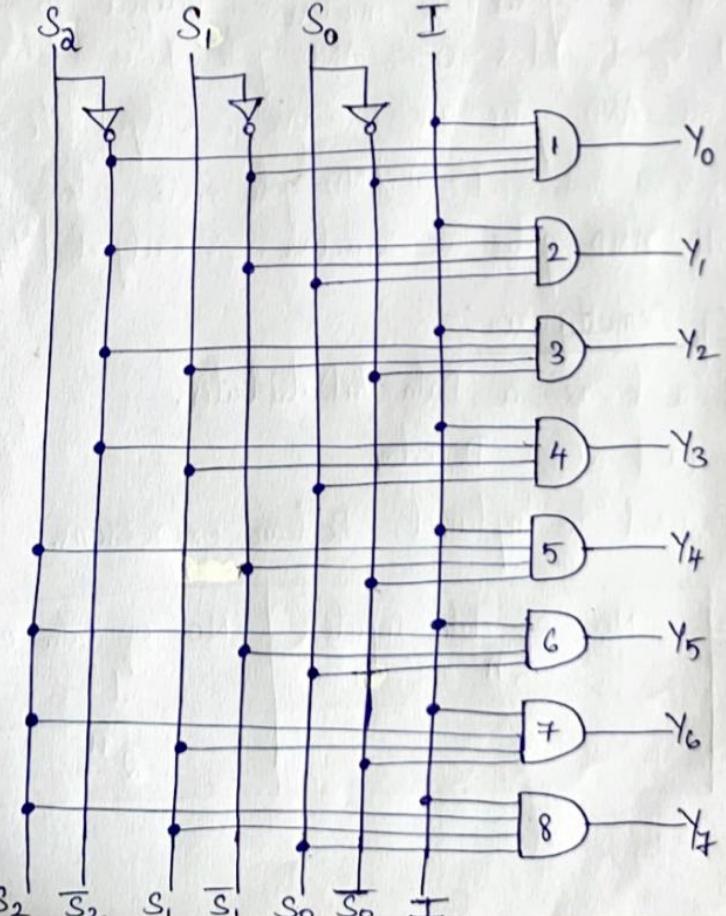
S ₂	S ₁	S ₀	Y ₇	Y ₆	Y ₅	Y ₄	Y ₃	Y ₂	Y ₁	Y ₀
0	0	0	0	0	0	0	0	0	0	I
0	0	1	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	I	0
0	1	1	0	0	0	0	0	I	0	0
1	0	0	0	0	I	0	0	0	0	0
1	0	1	0	0	I	0	0	0	0	0
1	1	0	0	I	0	0	0	0	0	0
1	1	1	I	0	0	0	0	0	0	0

Equation: $Y_0 = \overline{S_2} \overline{S_1} S_0 I$, $Y_1 = \overline{S_2} \overline{S_1} S_0 I$, $Y_2 = \overline{S_2} S_1 \overline{S_0} I$

$Y_3 = S_2 \overline{S_1} S_0 I$, $Y_4 = S_2 \overline{S_1} \overline{S_0} I$, $Y_5 = S_2 \overline{S_1} S_0 I$

$Y_6 = S_2 S_1 \overline{S_0} I$ $Y_7 = S_2 S_1 S_0 I$

Circuit :-



Operation:

- 1) When $S_2 = 0$, $S_1 = 0$ and $S_0 = 0 \Rightarrow$ AND gate 1 is active and remaining all AND gates are inactive. \therefore output $Y_0 = I$
- 2) When $S_2 = 0$, $S_1 = 0$ and $S_0 = 1 \Rightarrow$ AND gate 2 is active and remaining all AND gates are inactive. \therefore output $Y_1 = I$
- 3) When $S_2 = 0$, $S_1 = 1$ and $S_0 = 0 \Rightarrow$ AND gate 3 is active and remaining all AND gates are inactive. \therefore output $Y_2 = I$
- 4) When $S_2 = 0$, $S_1 = 1$ and $S_0 = 1 \Rightarrow$ AND gate 4 is active and remaining all AND gates are inactive. \therefore output $Y_3 = I$
- 5) When $S_2 = 1$, $S_1 = 0$ and $S_0 = 0 \Rightarrow$ AND gate 5 is active and remaining all AND gates are inactive. \therefore output $Y_4 = I$
- 6) When $S_2 = 1$, $S_1 = 0$ and $S_0 = 1 \Rightarrow$ AND gate 6 is active and remaining all AND gates are inactive. \therefore output $Y_5 = I$
- 7) When $S_2 = 1$, $S_1 = 1$ and $S_0 = 0 \Rightarrow$ AND gate 7 is active and remaining all AND gates are inactive. \therefore output $Y_6 = I$
- 8) When $S_2 = 1$, $S_1 = 1$ and $S_0 = 1 \Rightarrow$ AND gate 8 is active and remaining all AND gates are inactive. \therefore output $Y_7 = I$

5 Marks Question

i) obtain the standard SOP and POS for $F(A, B, C) = \overline{AB} + A\overline{C} + A\overline{B}\overline{C}$.

Ans Conversion of Normal SOP into Standard SOP :→

$$f = \overline{AB} + A\overline{C} + A\overline{B}\overline{C}$$

$$f = \overline{A}B(1) + A(1)\overline{C} + A\overline{B}\overline{C}$$

$$= \overline{A}B(C + \overline{C}) + A(B + \overline{B})\overline{C} + A\overline{B}\overline{C} \quad (\because A + \overline{A} = 1)$$

$$= \overline{A}BC + \overline{A}B\overline{C} + AB\overline{C} + A\overline{B}\overline{C} + A\overline{B}\overline{C}$$

011	010	110	100	100
③	②	⑥	④	④

Minterm
 $A \rightarrow 1$
 $\overline{A} \rightarrow 0$

Standard SOP : A SOP expression is referred to as standard SOP, if all product terms are minterms.

Standard SOP : $f = \Sigma m(2, 3, 4, 6)$

Standard POS : A POS expression is referred to as standard POS, if all sumterms are maxterms.

Standard POS : $f = \prod M(0, 1, 5, 7)$.