Unit -5

1 Mark

1. Define PLA

A. A PLA is a combinational PLD (Programmable Logic Device) with both Programmable AND and OR arrays.

2. How is the memory size specified.

A. The memory size is specified as M x N bits where M is the number of locations and N is the number of bits in each location.

3. What are the advantages of Programmable logic device over fixed function IC's.

A. The advantages of PLDs over fixed function ICs are:

(a) Low development cost
(b) Less space requirement
(c) Less Power requirement
(d) High reliability
(e) Easy circuit testing
(f) Easy design modification
(g) High design Security
(h) Less design time.

4. State the advantages of FPGA

A. 1. Better Performance
2. Cost Efficiency
3. Parallel Task Performance
4. Programmability

5. ~~Explain~~ D

5. Define PROM

A. A PROM is a field Programmable ROM. It is not Programmed during the manufacturing Processes but is custom Programmed by the user. Once Programmed, the data Cannot be altered. PROMs are manufactured with fusible links.

3 Marks

1. Define ROM. What are the classification of the ROM?

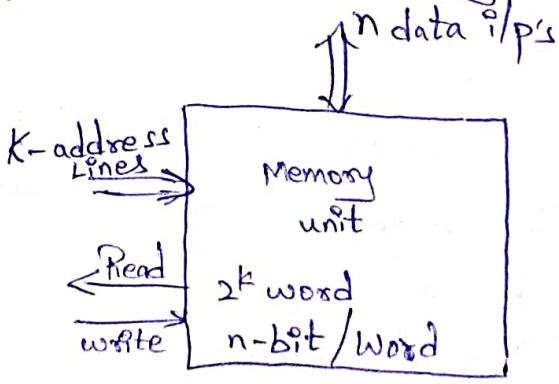
A. ROM (Read Only Memory) : We can't write the data in this memory. It is non-Volatile memory. i.e, it can hold data even if Power is turned off.

Classification of ROM:-

1. Masked ROM
2. Programmable ROM
3. Erasable PROM
4. Electrically Erasable PROM
5. Flash Memory

2. Explain the Block Diagram of the Memory.

A Block Diagram of Memory:



* A memory unit stores binary information in groups of bits called words.
* A Word having group of 8-bits is called byte.
* The basic structure of memory can be identified with data i/ps, address line, Read & write Parameters.
* A memory contains k-address lines using which we can access 2^k memory words.

3. Write about Programmable Logic Devices.

A. A PLD contains a large number of gates, flip flops and registers that are interconnected on the chip. Many of the connections, however are fusible links that can be broken The IC is said to be Programmable because the specific function of the IC for a given application is determined by the Selective breaking of Some of the interconnections while leaving other ~~input~~ intact.

The 'fuse blowing' Process can be done either by manufacturer in according to customer's instructions, (or) by Customer himself. This Process is called 'Programming' because it Produces desired circuit Pattern interconnecting the gates, FIFS, registers etc.

PLDS Can be reprogrammed in a few Seconds and hence gives more flexibility to Experiment with designs.

* Advantages of PLDs over fixed function ICs

1. Low development cost
2. Less Space requirement

3. Less Power requirement
4. High reliability
5. Easy circuit testing
6. Easy design modification
7. High design Security
8. Less design time
9. High Switching Speed.

4. What is FPGA?

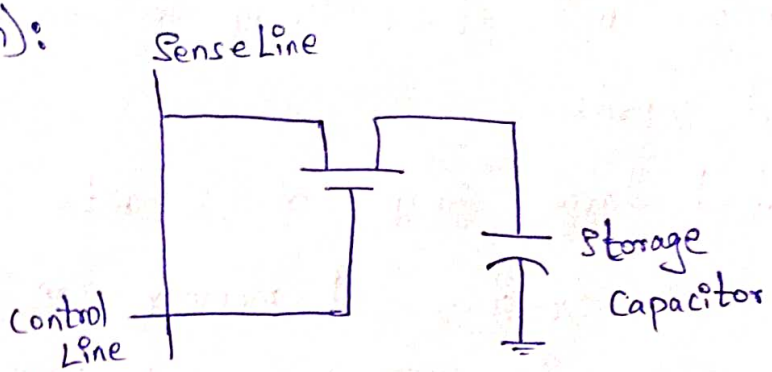
A. An FPGA (Field Programmable Gate Array) is an IC (Integrated Circuit) Programmed for Performing Customized Operations for a Specified application. A designer or customer can Configure it after manufacturing, thus termed field-Programmable.

* FPGA has thousands of gates, and an HDL (Hardware description Language) Similar to the one used for an ASIC (application-Specific integrated Circuit) usually Specifies its Configuration.

* FPGAs Contain an assemblage of Programmable logic blocks along with a hierarchy of reconfigurable interconnects. These helps the blocks wire together just like many logic gates inter-wired in various Configurations.

5. Explain Dynamic Ram.

A. Dynamic Ram (DRAM):



Dynamic Ram stores the data as a charge on the capacitor A Dynamic Ram contains thousands of such memory cells. when COLUMN (sense) and ROW (control) lines go high, the mosfets. conducts and charges the capacitor. When the column and Row lines go low, the MOSFET opens and the capacitor retains its charge. In this way it stores 1 bit.

5 Marks

1. Write a short notes on (i) EPROM (ii) EEPROM

A. (i) EPROM (Erasable Programmable Read Only Memory):-

* EPROM use MOS circuitry. They store 1s and 0s as Packet of charge in buried layer of IC chip.
* EPROMs can be Programmed by the user with a Special EPROM Programmer.
* we can erase the stored data in the EPROM by exposing the chip to ultraviolet light through the quartz window for 15 to 20 minutes.
* It is not Possible to erase Selective information, when erased the entire information is lost
* The chip can be reProgrammed.

(iii) EEPROM (Electrically Erasable Programmable ROM):

* EEPROMs also use MOS Circuitry very Similar to that of EPROM
* The data is Stored as charge (or) no charge on an insula-ted layer (or) an insulated floating gate in the device.
* The insulated layer is made very thin (< 200A)
* EEPROM allows Selective erasing at the register level rather than erasing all the information Since the information can be changed by using electric Signals.
* EEPROM also has a Special chip erase mode by which entire chip can be erased in 10m Sec.
* EEPROMs are most expensive.

2. Differentiate Between RAM and ROM

⇒ A.

RAM	ROM
* RAM Stands for Random Access Memory	* ROM Stands for Read Only Memory
* RAM is volatile Memory and it loses data when Power is turn off.	* ROM is Non-Volatile Memory and it retains data even when Power is off.
* RAM data can be Modified.	* ROM data Can not be Modified
* RAM Performs both Read and Write	* ROM Perform read only
* RAM Speed is higher than ROM	* ROM Speed is slower than RAM
* RAM is used as CPU cache, Primary Memory.	* ROM is used as Firmware by Microcontrollers.

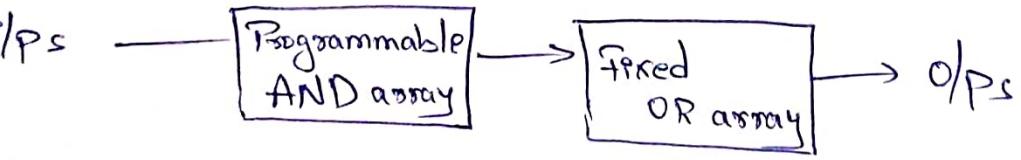
RAM	ROM
* CPU can Directly access data Stored on RAM.	* Data is copied from ROM to RAM so that CPU can access its Data.
* RAM stores Data temporarily	* ROM Stores Data permanently
* RAM is in Form of chip.	* ROM is generally optical drivers made of Magnetic Tapes.
* RAM is Expensive than ROM.	* ROM is cheaper as compared to RAM.
* Examples: SRAM & DRAM	* Examples :- PROM, EPROM & EEPROM

3. Implement the Following function using a PAL

$F(A,B,C,D) = \Sigma m\,(0,1,2,3,4,5,7,10,11,12,13,14,15)$

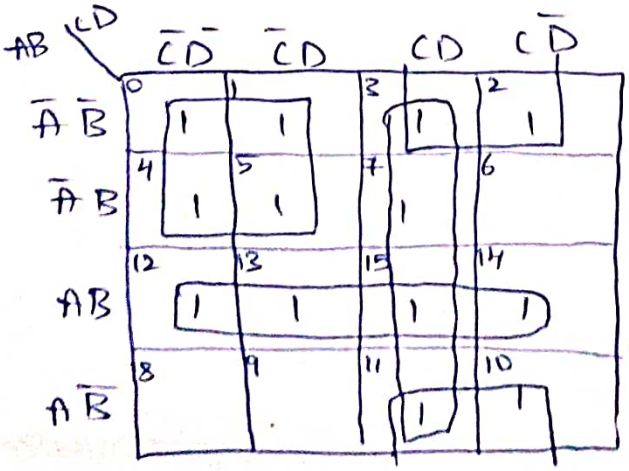
A. For PAL, The AND array is Programmable and will be having of fixed OR array

* PAL has Programmable AND array and a fixed OR array.



$F = \Sigma m(0,1,2,3,4,5,7,10,11,12,13,14,15)$

k-map:

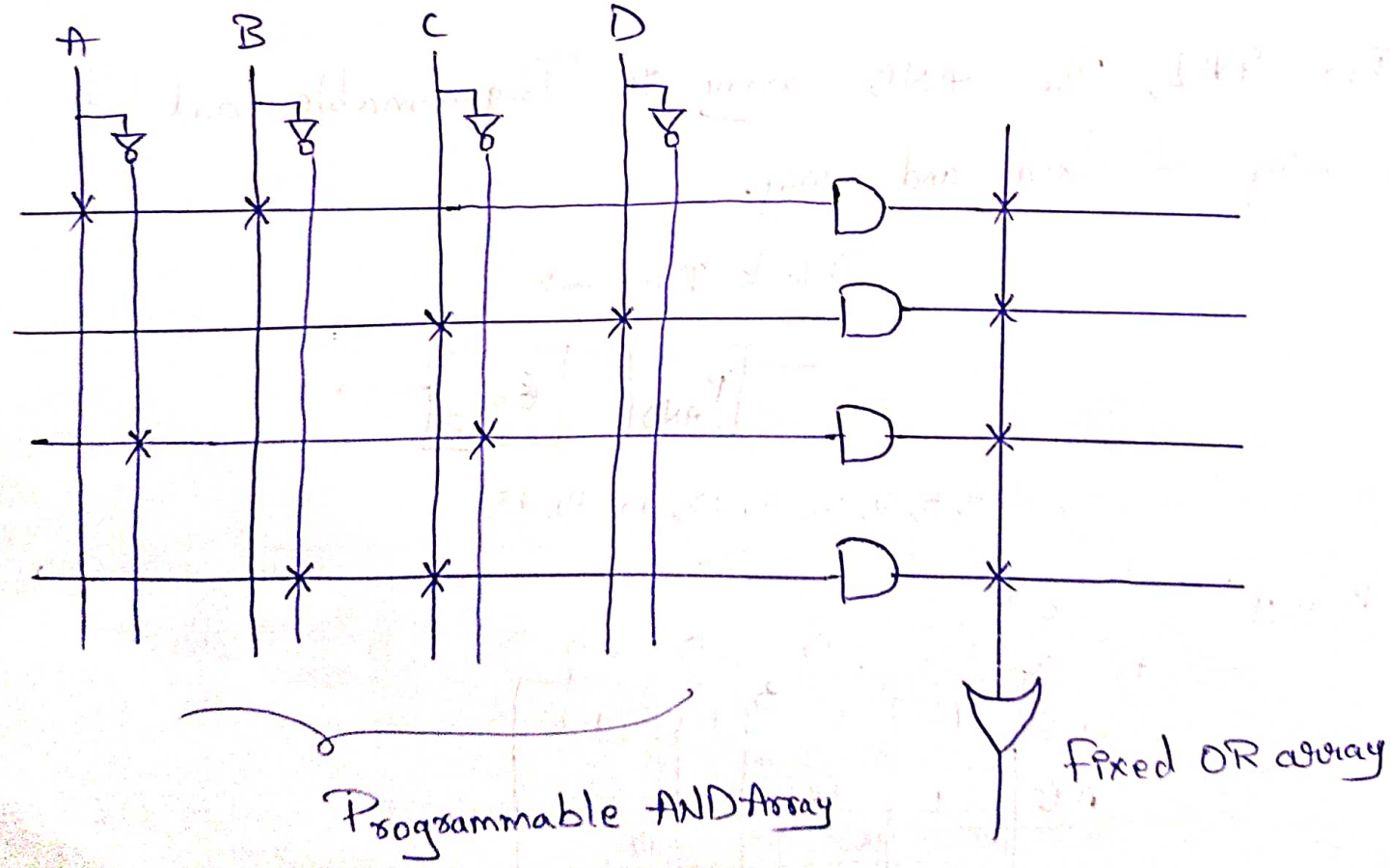


$$F = AB + CD + A\bar{C} + \bar{B}C$$

Programming Table of PAL:

Product terms	AND gate inputs A	B	C	D	Equation
1	1	1	–	–	$\bar{F} = AB + CD + \bar{A}\bar{C} + \bar{B}C$
2	–	–	1	1	
3	0	–	0	–	
4	–	0	1	–	

Realization of the given function using PAL:



4. Differentiate Static and Dynamic RAM.

=> A.

SRAM	DRAM
* This contains less Memory Cells Per unit area.	* This contains more memory cells Per unit area.
* It has less access time so these are faster (time required to access the data is less)	* It has more access time so, these are slower in operation (time required to access the data is more)
* These are constructed by Flip-Flops.	* These are constructed by MOS transistors.
* Cost is more	* Cost is less
* It requires no refreshment	* It requires continous refreshment
* Package density is low	* Package density is high
* H/w Complexity is less	* H/w Complexity is high

5. Write the Comparison Between PROM, PLA and PAL?

=> A.

PROM	PLA	PAL
* AND array is fixed OR array is Programmable.	* Both AND & OR array are Programmable.	* OR array is fixed and AND array is Programmable.
* cheaper and Simple to use.	* costlier and more complex than PAL, PROM	* cheaper and Simpler.
* All min terms are decoded	* AND array can be Programmed to get desined min terms	* AND array can be Programmed to get desined min terms.

PROM	PLA	PAL
* Only Boolean function in standard SOP form can be impleme-nted using PROM	* Any Boolean function in SOP form can be implemented using PLA	* Any Boolean function in SOP form can be implemented using PAL

UNIT-5

10 Marks

1. Implement the following Boolean function using PAL with four inputs and also write the PAL Programming table.

$f_1(A,B,C,D) = \Sigma m(1,2,8,12,13)$

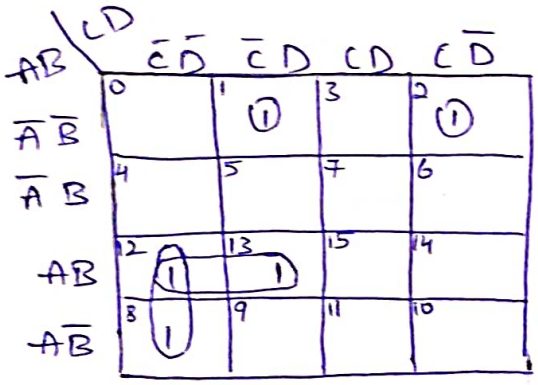
$f_2(A,B,C,D) = \Sigma m(0,2,3,4,5,6,7,8,10,11,15)$

$f_3(A,B,C,D) = \Sigma m(7,8,9,10,11,12,13,14,15)$

$f_4(A,B,C,D) = \Sigma m(2,12,13)$

Ans Step 1 :- k-map Simplification

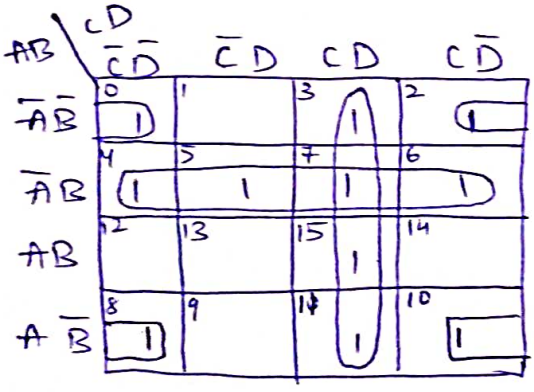
f_1 :-



Result : Pairs = 2

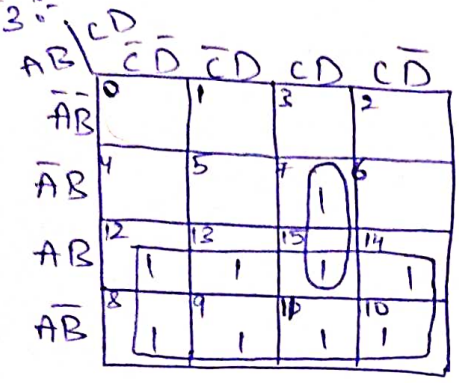
Eq :- $f_1 = AB\bar{C} + A\bar{C}\bar{D} + \bar{A}\bar{B}CD + \bar{A}\bar{B}C\bar{D}$

f_2 :-



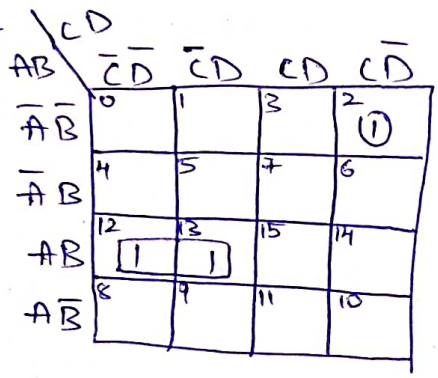
Eq :- $\bar{A}B + CD + \bar{B}\bar{D} = f_2$

F_3 :-



Eq :- $A + B\,CD = F_3$

F_4 :-



Eq :- $AB\bar{C} + \bar{A}\bar{B}C\bar{D} = F_4$

Step 2 :- Write the Programming table

Function F_1 has 4 Product terms

F_2 has 3 Product terms

F_3 has 2 Product terms

F_4 has 2 Product terms

PAL Programming table :-

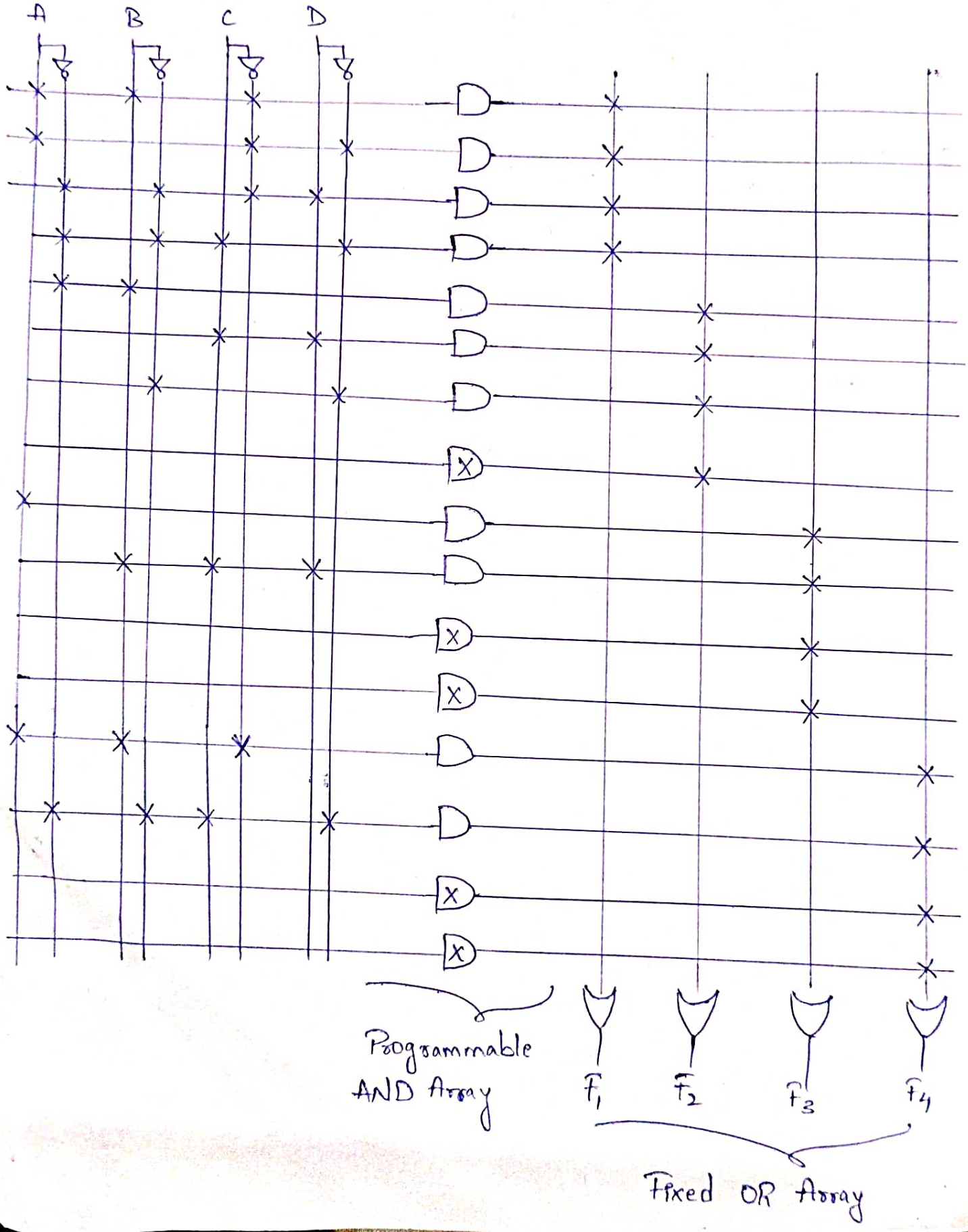
Product term	AND gate i/p's A	B	C	D	outputs
1	1	1	0	–	$F_1 = AB\bar{C} + A\bar{C}\bar{D} + \bar{A}\bar{B}CD + \bar{A}\bar{B}C\bar{D}$
2	1	–	0	0	
3	0	0	0	1	
4	0	0	1	0	
5	0	1	–	–	$F_2 = \bar{A}B + CD + \bar{B}\bar{D}$
6	–	–	1	1	
7	–	0	–	0	
8	–	–	–	–	
9	1	–	–	–	$F_3 = A + BCD$
10	–	1	1	1	
11	–	–	–	–	
12	–	–	–	–	
13	1	1	0	–	$F_4 = AB\bar{C} + \bar{A}\bar{B}C\bar{D}$
14	0	0	1	0	
15	–	–	–	–	
16	–	–	–	–	

Step 3 :- Realization of the function using Programmable Array Logic

→ For each '1' or '0' in the table we mark the corresponding intersection in the diagram with the symbol for an intact fuse.

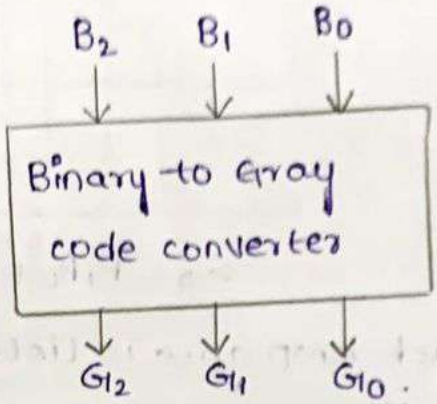
→ For each dash, we mark the diagram with blown fuses in both the true and complement inputs.

→ A Symbol 'x' inside the AND gate is used to indicate that all it's input fuses are intact.



2. Design a 3 bit binary-to Gray code converter using PLA.

Ans. Block diagram :→



B_2, B_1 and B_0 are the binary inputs and G_{12}, G_{11} and G_{10} are the Gray outputs.

Truth table :→

Binary			Gray		
B_2	B_1	B_0	G_{12}	G_{11}	G_{10}
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	1
0	1	1	0	1	0
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

From the table, the expressions for the outputs are:

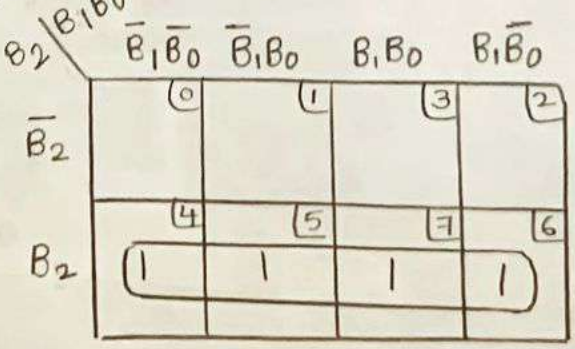
$G_{12} = \Sigma m(4,5,6,7)$

$G_{11} = \Sigma m(2,3,4,5)$

$G_{10} = \Sigma m(1,2,5,6)$

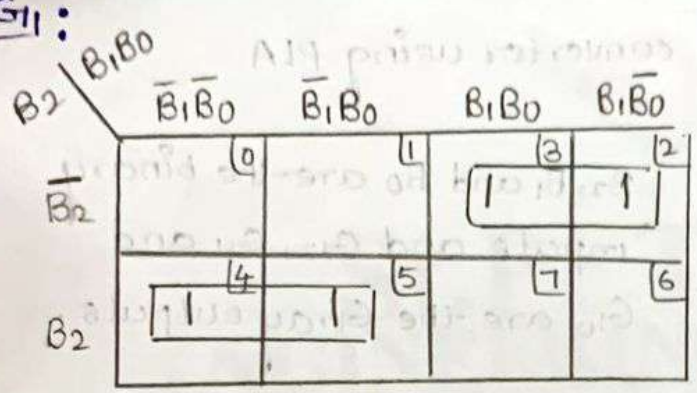
k-Map :→

G_{12} :



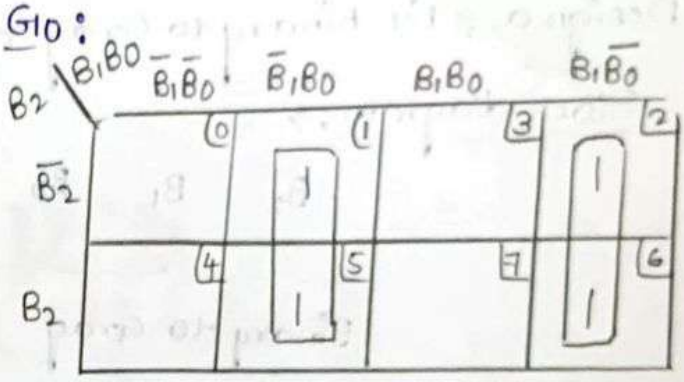
$G_{12} = B_2$

G_{11} :



$G_{11} = B_1\bar{B}_2 + \bar{B}_1B_2$

G_{10} :



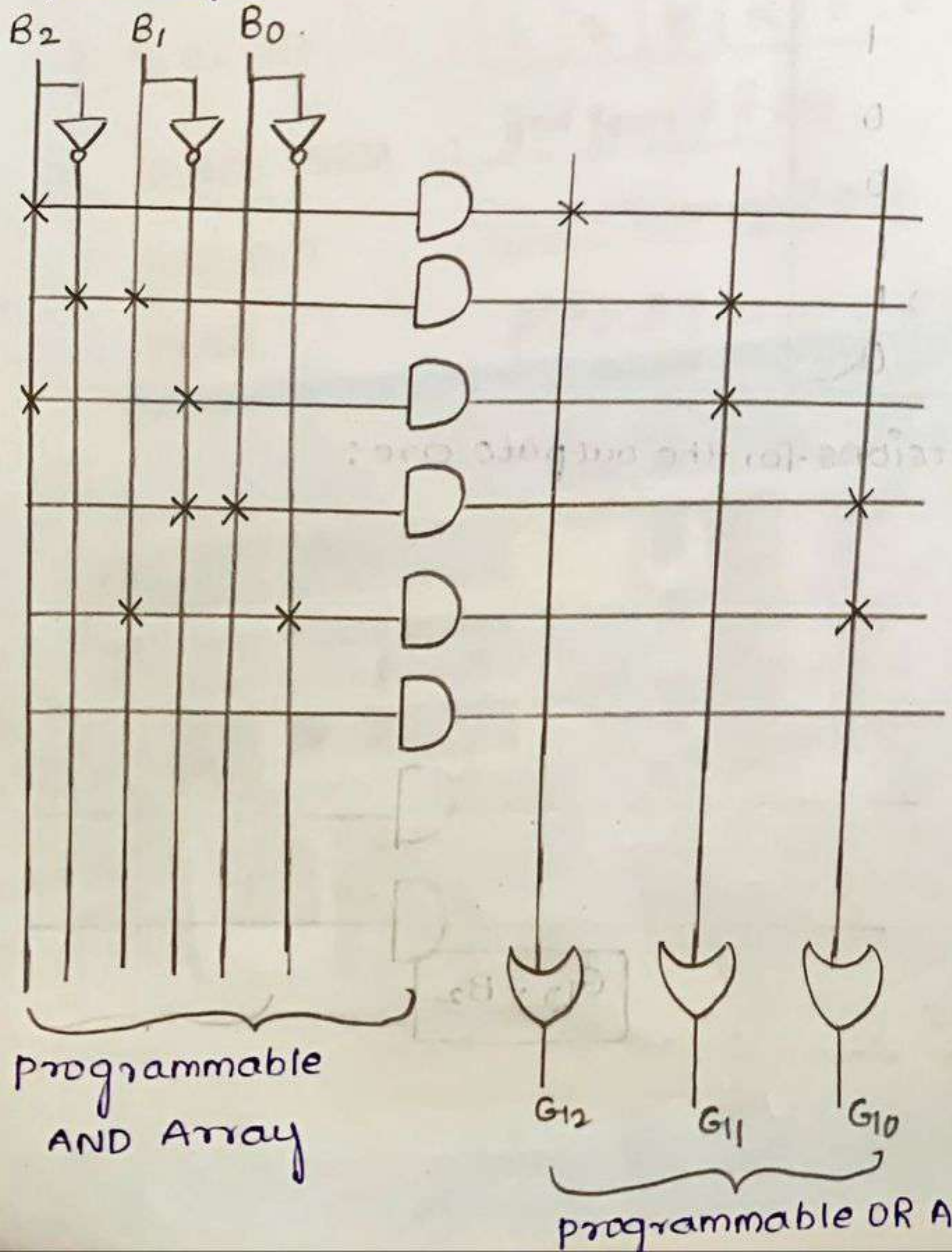
$G_{10} = \bar{B}_1B_0 + B_1\bar{B}_0$

The product term generated in each AND gate is listed along the output of the gate in the logic diagram.

The product term is determined from the inputs whose cross points are connected and marked by a symbol 'x'.

The output of an OR gate gives the logic sum of selected product terms.

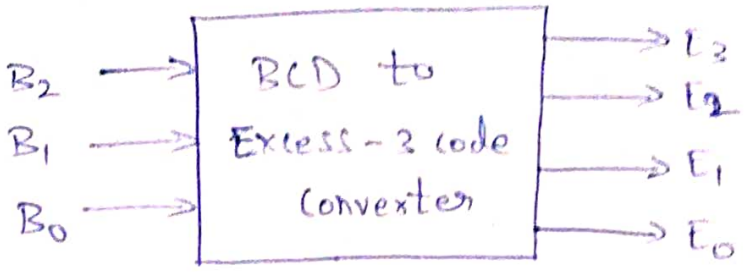
Logic diagram :→



3. Realize the BCD to EXCESS-3 code converter using PROM

Ans:

Block Diagram:



The BCD number is converted into Excess-3 code then it is called as BCD to Excess-3 code converter.

Truth Table:-

dec	B_2	B_1	B_0	E_3	E_2	E_1	E_0
0	0	0	0	0	0	1	1
1	0	0	1	0	1	0	0
2	0	1	0	0	1	0	1
3	0	1	1	0	1	1	0
4	1	0	0	0	1	1	1
5	1	0	1	1	0	0	0
6	1	1	0	1	0	0	1
7	1	1	1	1	0	1	0

Equations:

$E_3 = \Sigma m(5, 6, 7)$

$E_2 = \Sigma m(1, 2, 3, 4)$

$E_1 = \Sigma m(0, 3, 4, 7)$

$E_0 = \Sigma m(0, 2, 4, 6)$

The input is a 3-bit binary number.

So, the PROM (Programmable Read Only Memory) requires a 3x8 Decoder. It generates the equivalent Excess-3 code Hence, it has four outputs and requires four 'OR' gates.

Since, the PROM has fixed AND gates, no minimization is required.

1. To realize E_3, the address Lines 5, 6, 7 are used to connect to the output line.
2. To realize E_2, the address Lines 1, 2, 3, 4 are used to Connect to the Output Line.
3. To realize E_1, the address Lines 0, 3, 4, 7 are used to connect to the output line.
4. To realize E_0, the address Lines 0, 2, 4, 6 are used to connect to the output line.

Logic Diagram: