UNIT - III

a) Encode the decimal Number $(46)_{10}$ to Gray code?

Ans Step 1 : Convert $(46)_{10}$ to binary.

$(46)_{10} = (101110)_2$

Step 2: Convert binary Number to Gray code

i.e first bit of binary & Gray Code must be Same and each Subsequent of Gray Code is obtained by XORing Current bit of binary Number with previous bit

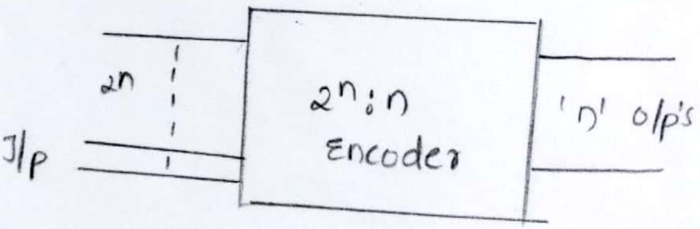
Gray Code is 111001_{gray}.

b) Define Encoder and draw its block diagram?

Encoder is an Combinational circuit which have 2^n inputs and n outputs.

- Enable is denoted by E
- when E=0 irrespective of Inputs output is 0. If E=1, only we get outputs.

Block diagram :



c) Explain the Truthtable of Half Adder?

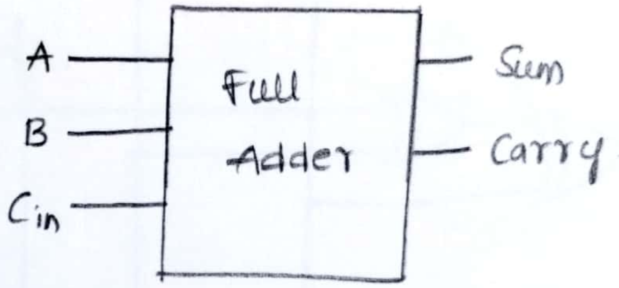
A Half Adder is a Combinational Circuit that performs Addition of two Single-bit binary Numbers.

Truth table :

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

d) Draw the Circuit of Full Adder ?

Full Adder is a Combinational logic circuit which perform Addition operation on three bit (A, B, C_{in}).



e) what is parity Generator.

A parity Generator is a logic circuit that adds an extra bit to binary data to make the total numbers of 1's either even or odd

This extra bit is Called a parity bit.

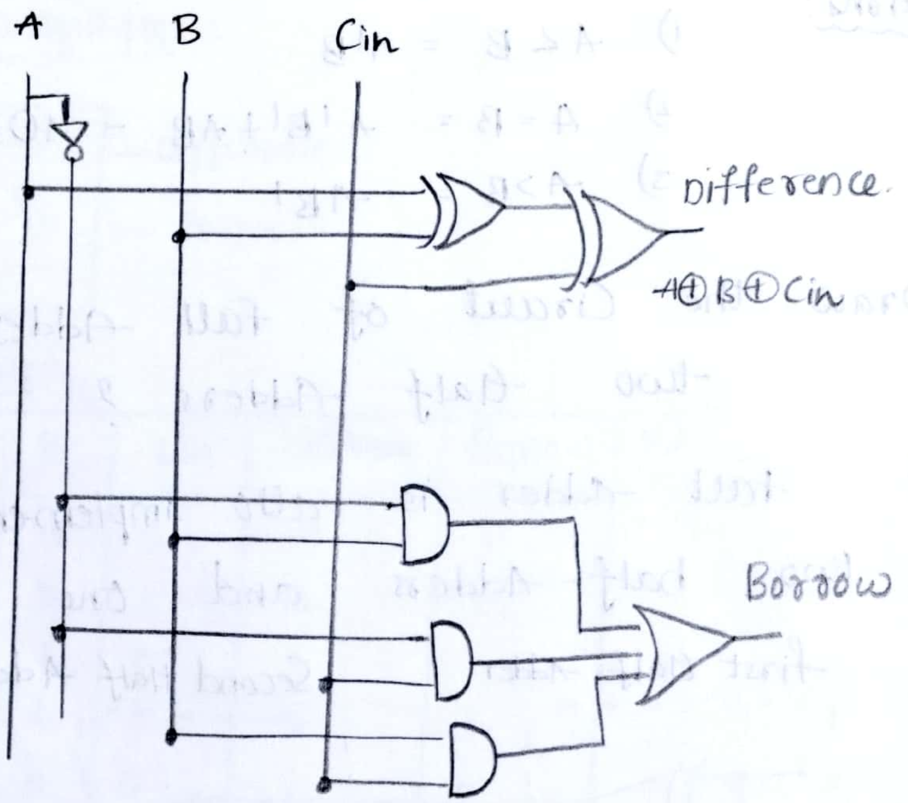
3 Marks

2a) Draw the circuit of full Subractor ?

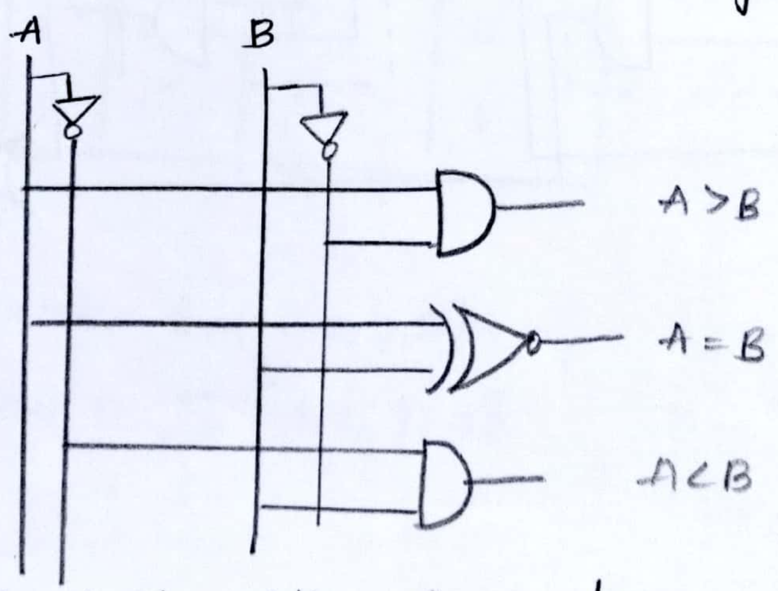
Circuit diagram of full subractor :

Equation of Difference : $A \oplus B \oplus C_{in}$

borrow : $\bar{A}B + \bar{A}C_{in} + BC_{in}$



b) Draw the Circuit of 1-bit magnitude Comparator?



logic Circuit of 1 bit Comparator:

Truthtable

A	B	A=B	A<B	A>B.
0	0	1	0	0
0	1	0	1	0
1	0	0	0	1
1	1	1	0	0

Equations:

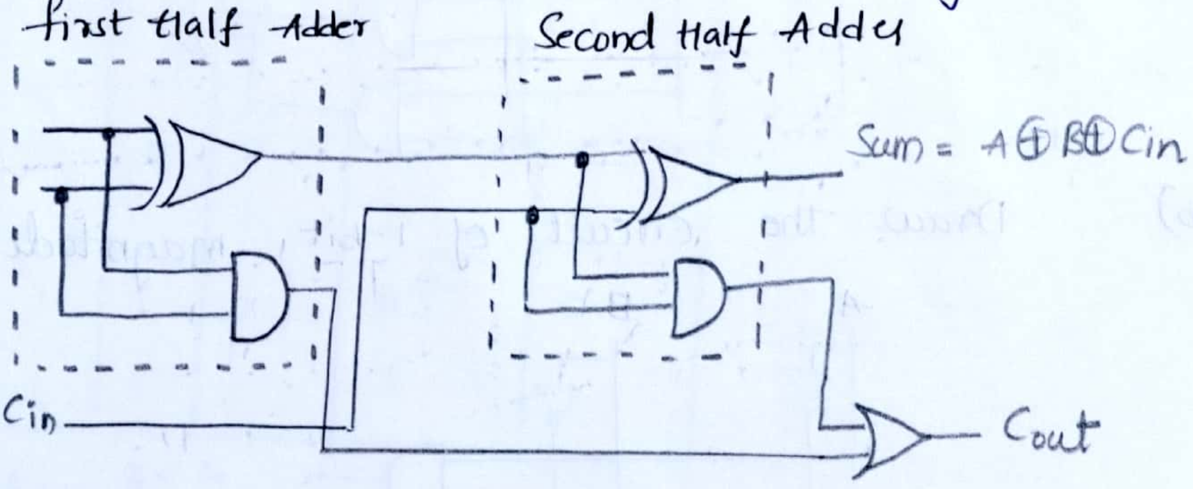
1) $A < B = A'B$

2) $A = B = A'B' + AB = A \odot B$

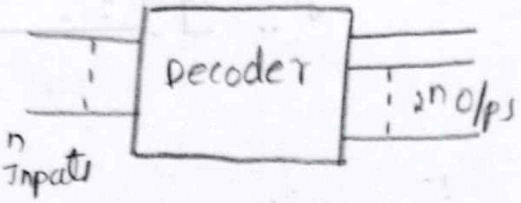
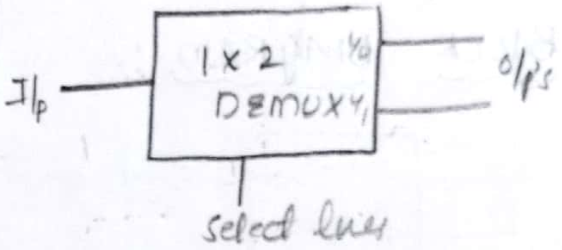
3) $A > B = AB'$

c) Draw the Circuit of full Adder using two Half Adders ?

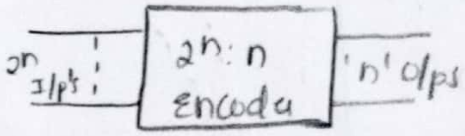
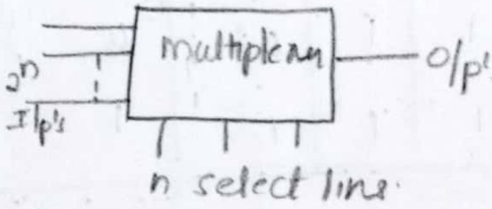
A full Adder is also implemented using two half-Adders and one OR gate



d) Compare Decoder and Demux.

Decoder	DEMUX.
• A decoder has 'n' input lines & max of 2^n - Output lines	• A Demux has Single input 'n' selection lines & max of 2^n outputs.
• Block DIAGRAM  	• Block DIAGRAM 
• Decoder is an Inverse of Encoder	• Demux is an Inverse of multiplexer.
• Decoder is used to detect bits, encoding data	• Demux is used in Switching, data distribution
• Decoder has no Select lines	• Demux Contains Select lines.

e)

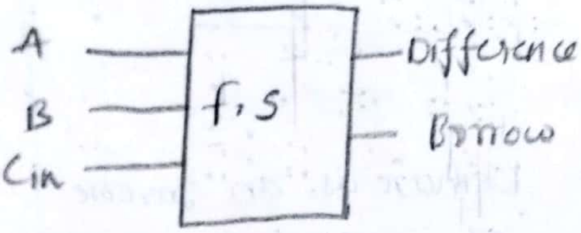
Encoder	Multiplexer.
• Block diagram  	• Block diagram. 
• In encoder the outputs are generate the binary Code, Corresponding to the Input value	• In Multiplexer selectors Input determines which Input line is Selected and routed to Single o/pline.
• Encoder is a many Inputs to many output devices	• Multiplexer is a many input to one output device

5 Marks

3 a) Explain the operation of full Subractor with neat circuit diagram.

i) full Subractor : It is a Combinational circuit which performs Subraction operation on three binary bits (A, B, Cin) and gives o/p difference & Borrow

2) Block DIAGRAM :



iii) Truth table :

A	B	Cin	Difference	Borrow
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

v)

iv) Equations :

Difference = $\Sigma m(1, 2, 4, 7)$

Borrow = $\Sigma m(1, 2, 3, 7)$.

v) Simplification

A \ BC	$\bar{B}\bar{C}_{in}$	$\bar{B}C_{in}$	BC_{in}	$B\bar{C}_{in}$
$\bar{A}$		1		1
A	1		1	

Difference : $\bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$

$= \bar{A}(B \oplus C) + A(B \odot C)$

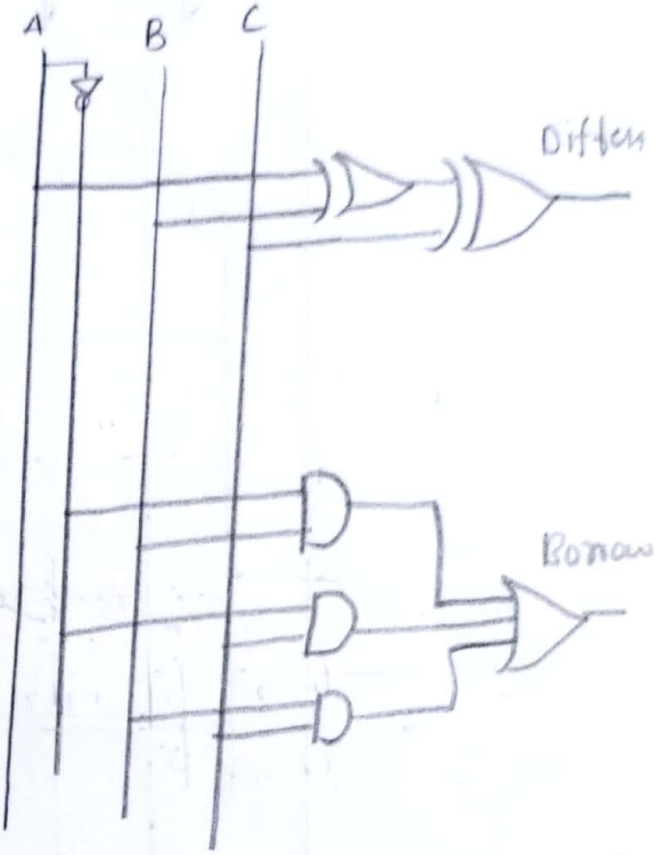
$= A \oplus B \oplus Cin$

Borrow:

A \ BC	$\bar{B}\bar{C}_{in}$	$\bar{B}C_{in}$	BC_{in}	$B\bar{C}_{in}$
$\bar{A}$		1	1	1
A			1	

Borrow = $\bar{A}B + \bar{A}C_{in} + BC_{in}$

vi Implementation

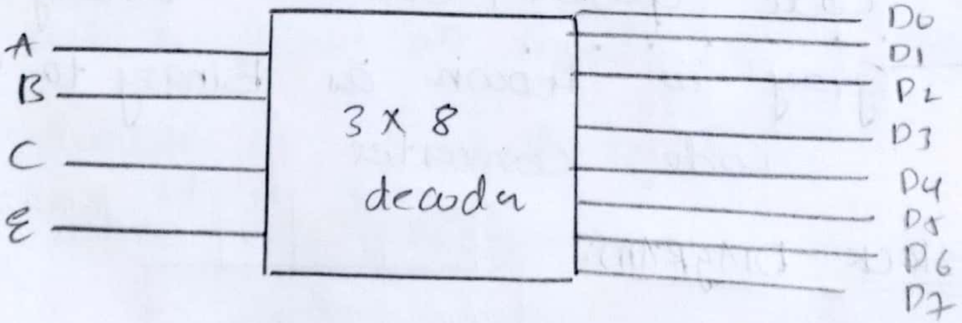


b) Design 3 to 8 decoder using NAND Gates

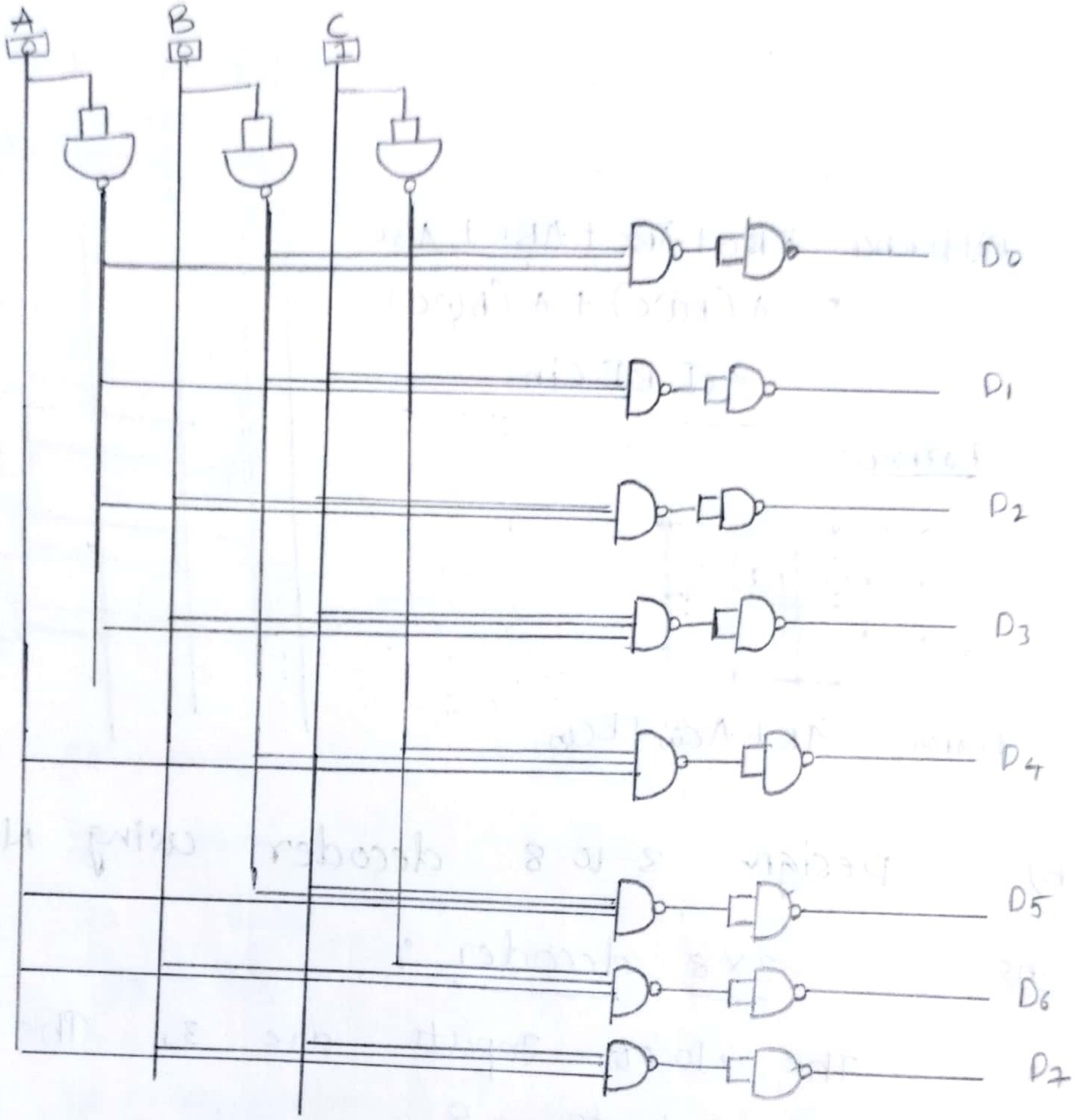
Ans 3×8 decoder :

The No. of Inputs are 3, The no. of outputs = 8

Block Diagram :



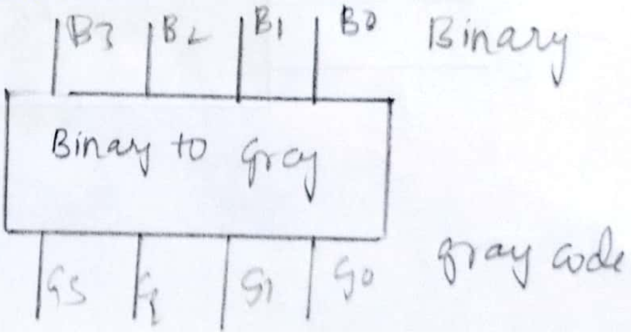
DESIGN of 3 to 8 decoder using NAND.



c) Design a Code Converter that Converts Binary into Gray Code

The Code which Converts binary to Gray is known as Binary to Gray Code Converter.

BLOCK DIAGRAM:



4bit Binary				4 bit Gray			
B_4	B_3	B_2	B_1	G_4	G_3	G_2	G_1
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0

K-maps

$G_4 = \Sigma m\,(8,9,10,11,12,13,14,15)$

$G_3 = \Sigma m\,(4,5,6,7,8,9,10,11)$

$G_2 = \Sigma m\,(2,3,4,5,10,11,12,13)$

$G_1 = \Sigma m\,(1,2,5,6,9,10,13,14)$.

B_4B_3 \ B_2B_1	00	01	11	10
00	0	1	3	2
01	4	5	7	6
11	12 1	13 1	15 1	14 1
10	8 1	9 1	11 1	10 1

$G_4 = B_4$

B_4B_2 \ B_2B_1	00	01	11	10
00	0	1	3	2
01	4 1	5 1	7 1	6 1
11	12	13	15	14
10	8 1	9 1	11 1	10 1

$G_3 = B_4 \oplus B_3$

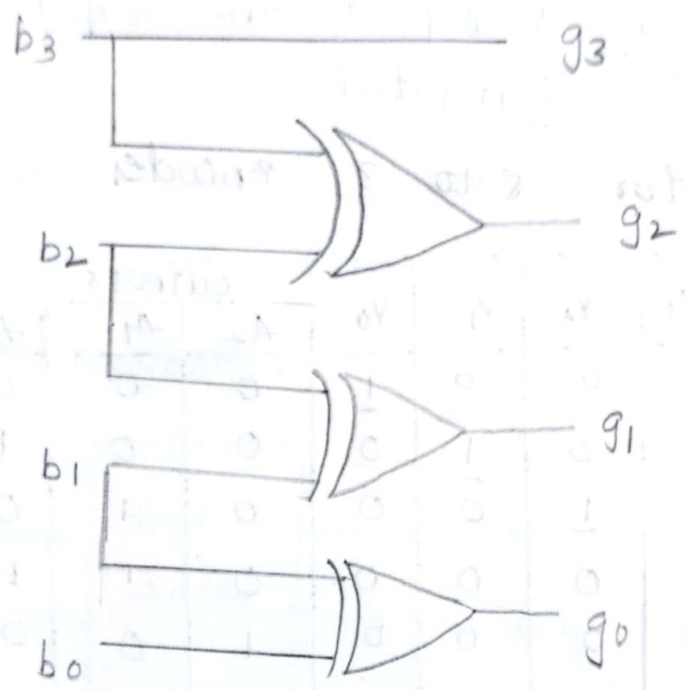
B_4B_3 \ B_2B_1	00	01	11	10
00	0	1	3 1	2 1
01	4 1	5 1	7	6
11	12 1	13 1	15	14
10	8	9	11 1	10 1

$G_2 = B_3 \oplus B_2$

B_4B_2 \ B_2B_1	00	01	11	10
00	0	1 1	3	2 1
01	4	5 1	7	6 1
11	12	13 1	15	14 1
10	8	9 1	10	10 1

$G_1 = B_2 \oplus B_1.$

Designing of Binary to Gray Code Converter.



where $g_0 = b_0 b_1' + b_1 b_0' = b_0 \oplus b_2$

$g_1 = b_2 b_1' + b_1 b_2' = b_1 \oplus b_2$

$g_2 = b_2 b_3' + b_3 b_2' = b_3 \oplus b_2$

$g_3 = b_3$.

d) What is encoder? Construct 8 to 3 Encoder using logic gates & Truth table?

Ans: Encoder: It is a Combinational circuit which have 2n inputs & n outputs

- Enable is denoted by E.
- when E=0, irrespective of inputs the output will be 0
- when E=1, only we get output

8 x 3 encoder.

- The no. of inputs are 8, The no. of outputs are 3.
- Depending on 8 Inputs the output Code is Generated.

Truth table for 8 to 3 encoder

Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0	OUTPUTS		
								A_2	A_1	A_0
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	1	0	0	0	1	0
0	0	0	0	1	0	0	0	0	1	1
0	0	0	1	0	0	0	0	1	0	0
0	0	1	0	0	0	0	0	1	0	1
0	1	0	0	0	0	0	0	1	1	0
1	0	0	0	0	0	0	0	1	1	1

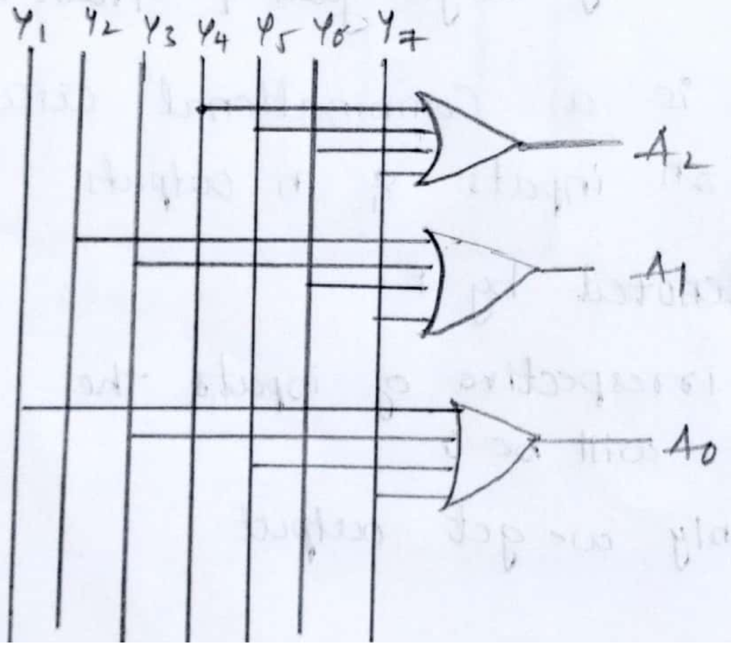
LOGICAL EXPRESSIONS for A_2 A_1 A_1

A_2 : $Y_7 + Y_6 + Y_5 + Y_4$

A_1 : $Y_7 + Y_6 + Y_3 + Y_2$

A_0 : $Y_7 + Y_5 + Y_3 + Y_1$.

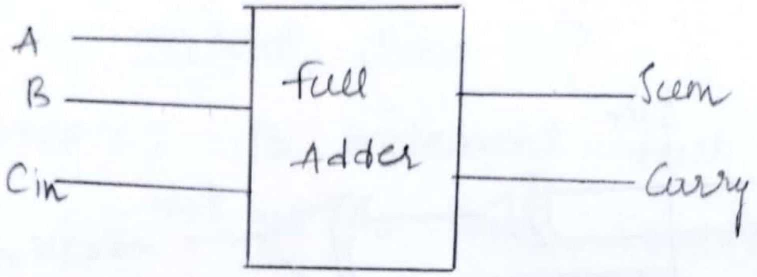
It Can be ~~HME~~ Implemented using OR Gates.



2 Explain the operation of full Adder with neat circuit diagram ?

Full Adder : It is a Combinational circuit which Performs Addition operation on three bits (A,B,Cin) i.e two are Significant bits and one is previous Carry and Gives the output as Sum & Carry.

Block DIAGRAM :



Truth table :

	A	B	Cin	Sum	Ca
0	0	0	0	0	0
1	0	0	1	1	0
2	0	1	0	1	0
3	0	1	1	0	1
4	1	0	0	1	0
5	1	0	1	0	1
6	1	1	0	0	1
7	1	1	1	1	1

Equation :

$$\text{Sum} = \Sigma m (1,2,4,7)$$

$$\text{Carry} = \Sigma m (3,5,6,7)$$

K-Map :

Sum :

A \ BC	$\bar{B}\bar{C}_{in}$	$\bar{B}C_{in}$	BC_{in}	$B\bar{C}_{in}$
$\bar{A}$		1		1
A	1		1	

$$\Rightarrow \bar{A}\bar{B}C_{in} + \bar{A}B\bar{C}_{in} + A\bar{B}\bar{C}_{in} + ABC_{in}$$

$$= \bar{A}(\bar{B}C_{in} + B\bar{C}_{in}] + A[\bar{B}\bar{C}_{in} + BC_{in}]$$

$$= \bar{A}(B \oplus C_{in}) + A(B \odot C_{in})$$

$$= \bar{A}(B \oplus C_{in}) + A(\overline{B \oplus C_{in}})$$

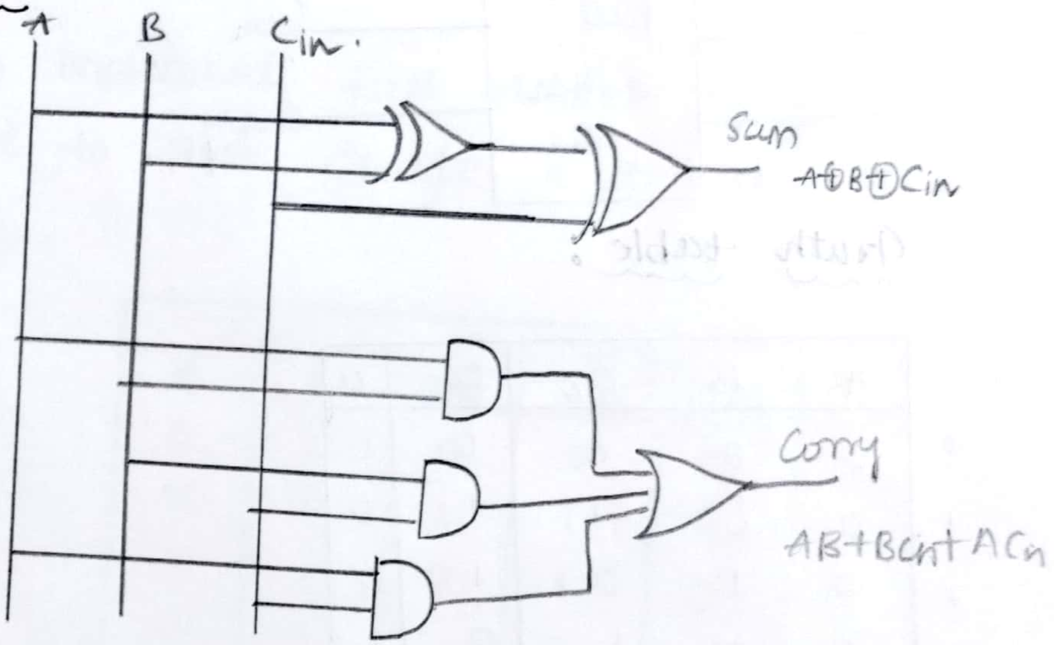
$$\text{Sum} = A \oplus B \oplus C_{in}$$

Carry:

A \ BC	$\bar{B}\bar{C}_{in}$	$\bar{B}C_{in}$	BC_{in}	$B\bar{C}_{in}$
$\bar{A}$			1	
A		1	1	1

$$\text{carry} = AB + BC_{in} + AC_{in}.$$

Logic circuit :



10 Marks

4 a) Implement full Adder Circuit using Multiplexer ?

Multiplexer and full Adder are two different Digital logic circuits. The Mux is digital Switch. It allows digital Information from Several Sources to be routed into Single output line.

Step 1: To implement full Adder using Mux we need to first Create truth table of full Adder

Truth table :

INPUTS			OUTPUT	
A	B	CIN	SUM	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Step 2: we need to find out minterms for Sum an Carry output for truth table

for Sum : $f(A, B, Cin) = \Sigma(1, 2, 4, 7)$

Carry : $f(A, B, Cin) = \Sigma(3, 5, 6, 7)$

Step 3: Now we need equations for Sum and Carry

IMPLEMENTATION TABLE : SUM

	D0	D1	D2	D3
$\bar{A}$	0	①	②	3
A	④	5	6	⑦
INPUT to MUX	A	$\bar{A}$	$\bar{A}$	A

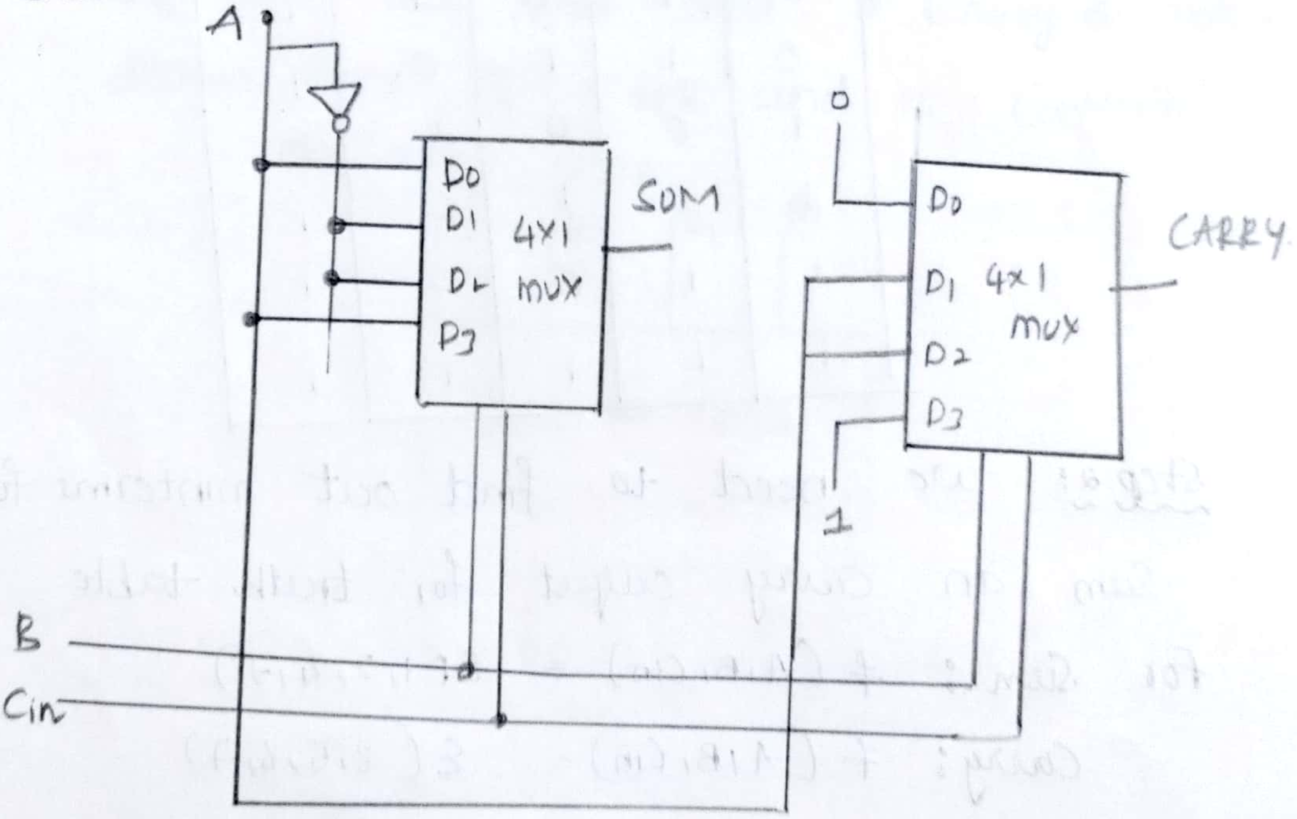
for Sum minterms are (1,2,4,7).

IMPLEMENTATION TABLE : CARRY

	D0	D1	D2	D3
$\bar{A}$	0	1	2	③
A	4	⑤	⑥	⑦
INPUT MUX	0	A	A	1

for Carry minterms are (3,5,6,7).

LOGIC CIRCUIT :



Explanation:

Inputs: The Input to M0 MUX is as per design table of Sum i.e $D_0 = A$, $D_1 = A'$, $D_2 = A'$, $D_3 = A$.

The Input to M_1 MUX as per design table of CARRY i.e $D_0 = 0$, $D_1 = A$, $D_2 = A$, $D_3 = 1$.

The Selection lines for Both M0 & M_1 are B & Cin.

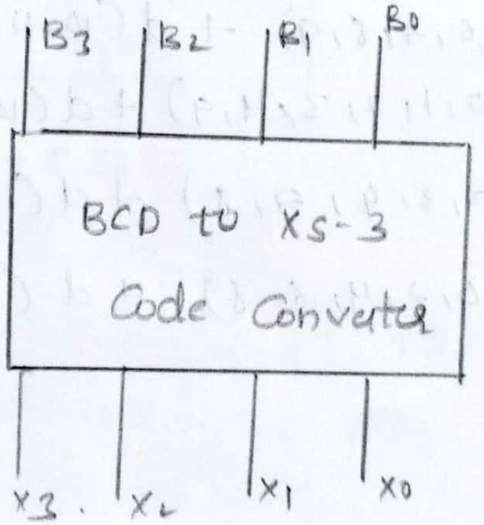
- The Outputs are Sum & CARRY.

b) Design a Code Converter that Converts BCD into excess-3 code.?

BCD to XS-3 Code Converter:

we are taking BCD code and it is Converted into XS-3 Code.

Now we can take that Binary decoded decimal (BCD) of 4 bit and it Converted to XS-3 CODE



Truth table:

BCD CODE INPUT				XS-3 Code Output			
B_3	B_2	B_1	B_0	X_3	X_2	X_1	X_0
0	0	0	0	0	0	1	1
0	0	0	1	0	1	0	0
0	0	1	0	0	1	0	1
0	0	1	1	0	1	1	1
0	1	0	0	1	0	0	0
0	1	0	1	1	0	0	1
0	1	1	0	1	0	1	0
0	1	1	1	1	0	1	1
1	0	0	0	1	1	0	0
1	0	0	1	x	x	x	x
1	0	1	0	x	x	x	x
1	0	1	1	x	x	x	x
1	1	0	0	x	x	x	x
1	1	0	1	x	x	x	x
1	1	1	0	x	x	x	x
1	1	1	1	x	x	x	x

Equations:

$$X_3 = \Sigma m(5,6,7,8,9) + d(10,11,12,13,14,15)$$

$$x_2 = \Sigma m(0,1,2,3,4,9) + d(10,11,12,13,14,15)$$

$$x_1 = \Sigma m(0,3,4,7,8) + d(10,11,12,13,14,15)$$

$$x_0 = \Sigma m(0,2,4,6,8) + d(10,11,12,13,14,10)$$

K map for X_3 :

B_3B_2 \ B_1B_0	$\bar{B_1}\bar{B_0}$	$\bar{B_1}B_0$	B_1B_0	$B_1\bar{B_0}$
$\bar{B_3}\bar{B_2}$	0	1	3	2
$\bar{B_3}B_2$	4	5 1	7 1	6 1
B_3B_2	12 X	13 X	15 X	14 X
$B_3\bar{B_2}$	8 1	9 1	11 X	10 X

Result: octet-1 Quad-2

$X_3 = B_3 + B_2B_0 + B_1B_2.$

K map for x_2 :

	$\bar{B_1}\bar{B_0}$	$\bar{B_1}B_0$	B_1B_0	$B_1\bar{B_0}$
$\bar{B_3}\bar{B_2}$		1	1	1
$\bar{B_3}B_2$	1			
B_3B_2	X	X	X	X
$B_2\bar{B_2}$		1	X	X

Result: Pair = 1, Quad = 2

Eqn: $x_2 = B_2\bar{B_1}\bar{B_0} + \bar{B_2}B_0 + \bar{B_2}B_1$

K map for x_1

	$\bar{B_1}\bar{B_0}$	$\bar{B_1}B_0$	B_1B_0	$B_1\bar{B_0}$
$\bar{B_3}\bar{B_2}$	1		1	
$\bar{B_3}B_2$	1		1	
B_3B_2	X		X	X
$B_3\bar{B_2}$	1		X	X

Result: Quad=2

Eqn: $\bar{B_1}\bar{B_0} + B_1B_0.$

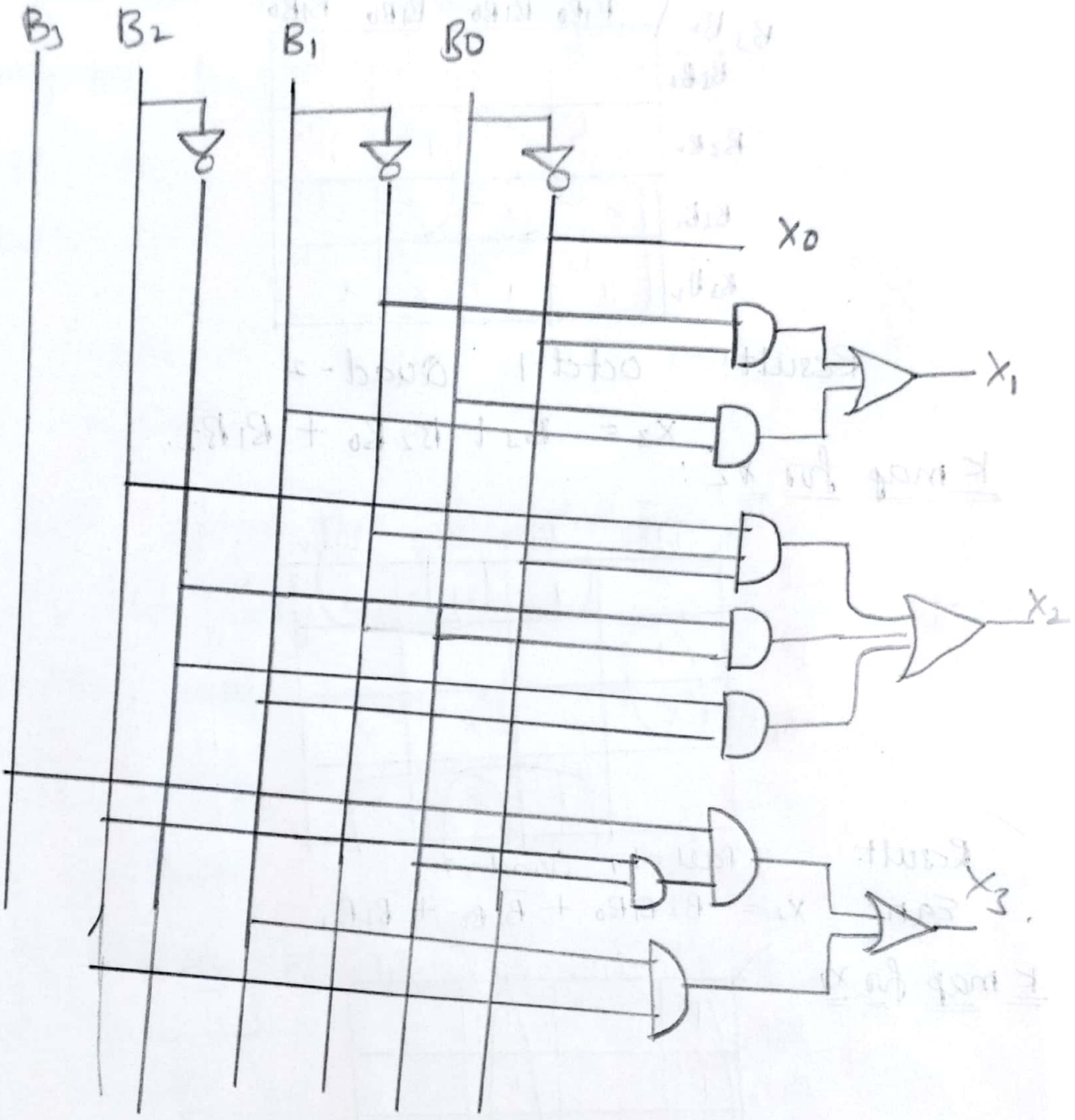
K map for x_0

	$\bar{B_1}\bar{B_0}$	$\bar{B_1}B_1$	B_1B_0	$B_1\bar{B_0}$
$\bar{B_3}\bar{B_2}$	1			1
$\bar{B_3}B_2$	1			1
B_3B_2	X	X	X	X
$B_3\bar{B_2}$	1		x	X

Result: octet = 1

Eqn: $\bar{B_0}$

LOGIC DIAGRAM:

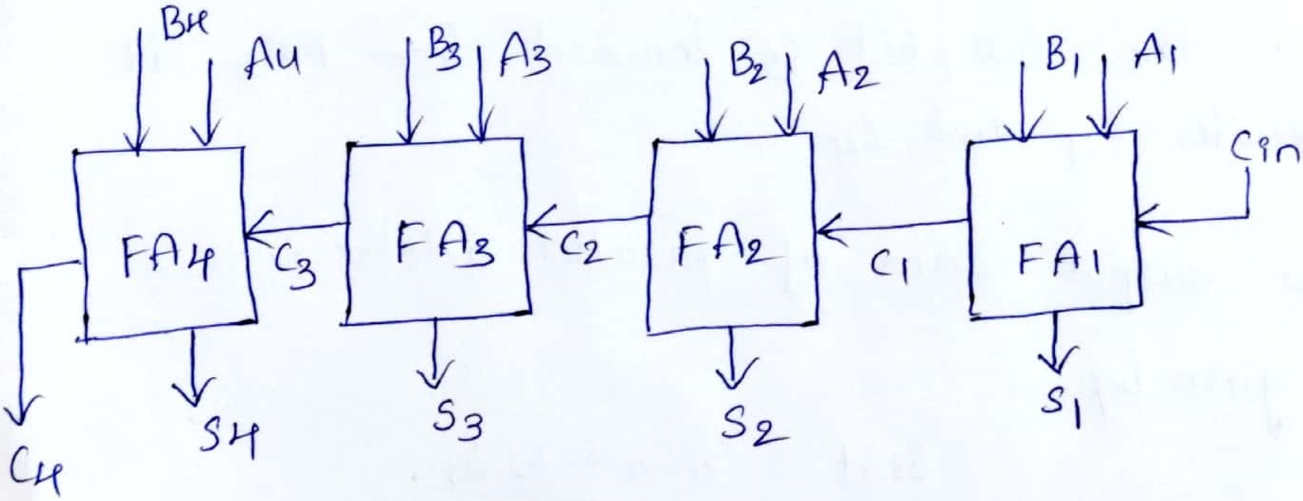


4C 4-bit parallel adder :-

→ A digital ~~ckt~~ circuit that adds two binary numbers of any bit length in parallel form and produces the sum of those number in parallel form is called parallel adder.

→ Two implement n-bit parallel adder, n full adders are required

→ n full adders are cascaded in such a way that the carry output from one stage is connected to the carry input of next stage.



Working of parallel Adder :-

Step1 :- Firstly, the full adder circuit FA_1 adds the bits A_1 and B_1 along with the input carry bit Cin to produce the sum bit S_1, where it is the LSB of output sum. A carry bit generated at this stage is transfered to the next full adder.

Step2:- The full adder circuit FA_2 adds bits A_2 and B_2 along with the carry bit C_1 from previous addition. It produce the sum bit S_2 which is the second bit of the output sum, and a carry bit C_2 is also produced

Step3:- The FA_3 adds inputs bit A_3 & B_3 along with carry bit C_2 from previous addition to produce sum bit S_3 & carry bit C_3 .

Step4:- The FA_4 adds input bits A_4 and B_4 along with the carry bit C_3 forward from FA_3. It generates S_4 and C_4.

The output sum of parallel adder is then given by

$$S_{out} = C_4 S_4 S_3 S_2 S_1 .$$