SET 2

SR 22

St. Peter's Engineering College (Autonomous) Dullapally (P), Medchal, Hyderabad – 500100. II - Mid Term Examination – November 2024						Dept.	:	CSM, CSC, CSD
						Academic Year 2024-25		
Subject Code	:	AS22-05PC06	**Subject**	:	**COMPUTER ORGANIZATION AND ARCHITECTURE**			
Class/Section	:	**B. Tech.**	**Year**	:	**II**	**Semester**	:	**I**
Duration	:	120 Min	**Max. Marks**	:	**30**	**Date:**	:	

BLOOMS LEVEL					
Remember	**L1**	**Understand**	**L2**	**Apply**	**L3**
Analyze	**L4**	**Evaluate**	**L5**	**Create**	**L6**

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PART – A (10x1M = 10M)

Note: Answer all Questions. Each Question carries equal marks.

Q. No	Question (s)	Marks	BL	CO
	UNIT - III			
1	**a.** Represent +6132.789 as a floating-point number	**1M**	L3	C213.5
	b. What is the purpose of the Decimal Arithmetic Unit?	**1M**	L2	C213.5
	UNIT – IV			
	c. Write one operational difference between the main memory and the auxiliary memory	**1M**	L1	C213.3
	d. What is meant by handshaking	**1M**	L2	C213.3
	e. What are Auxiliary and Cache memory	**1M**	L1	C213.3
	f. Draw the memory hierarchy in a computer system	**1M**	L2	C213.3
	UNIT – V			
	What are the three major pipeline conflicts?	**1M**	L1	C213.4
	Define LRU and FIFO	**1M**	L1	C213.4
	What is a hardware interlock?	**1M**	L1	C213.4
	Discuss the difference between tightly coupled and loosely coupled multiprocessors	**1M**	L2	C213.4

PART – B (20M)

Q. No	Question (s)	Marks	BL	CO
	UNIT - III			
2	a. Construct a Booths Multiplication Algorithm with a numerical example	**4M**	L3	C213.5
	OR			

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3	b. Draw and explain the hardware for signed–magnitude addition and subtraction.	**4M**	L2	C213.5
	UNIT – IV			
4	a. What is programmed I/O? Discuss the data transfer from an I/O device through an interface into the CPU.	**4M**	L1	C213.3
	b. Explain destination-initiated handshaking with the required timing diagram	**4M**	L2	C213.3
	OR			
5	a. Calculate the number of 128x8 RAM chips and 512x8 ROM chips required to design a computer system that needs 512 bytes of RAM and 512 bytes of ROM. Also, give the memory address map.	**4M**	L3	C213.3
	b. Explain the hardware organization of the associative memory in detail.	**4M**	L2	C213.3
	UNIT – V			
6	What are hardware interlocks?	**4M**	L1	C213.4
	Explain three major pipeline conflicts.	**4M**	L1	C213.4
	OR			
7	Discuss the difference between tightly coupled and loosely coupled multiprocessors.	**4M**	L2	C213.4
	Explain Mutual Exclusion with a Semaphore	**4M**	L2	C213.4

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