

4. What is Encoder? construct 4 to 2 encoder
using logic gates and truth table.

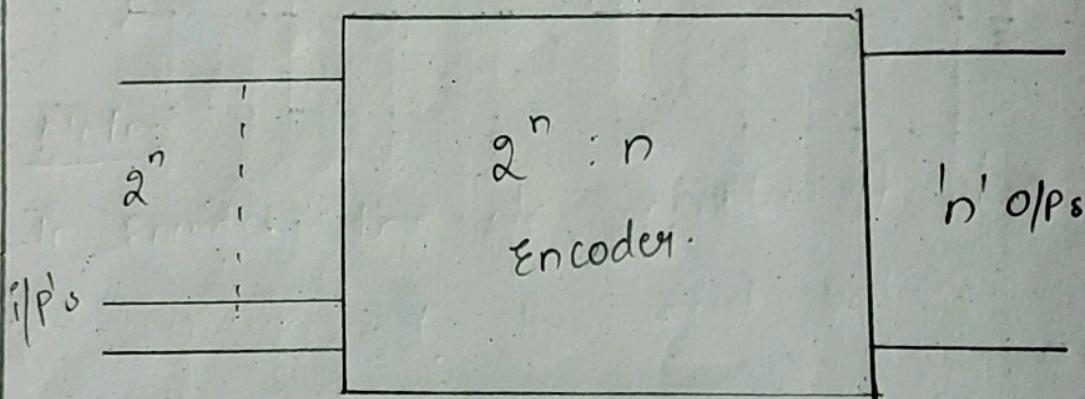
Encoder :-

It is a combinational circuit which have 2^n inputs and n outputs.

Enable Denoted is by E

- 1) from when $E=0$ irrespective of the inputs the output will be 0.
2) when $E=1$, then only we get the output.

Block Diagram :-



Examples :-

$$\text{When } n=2 \Rightarrow 2^2 : 2 = 4 : 2$$

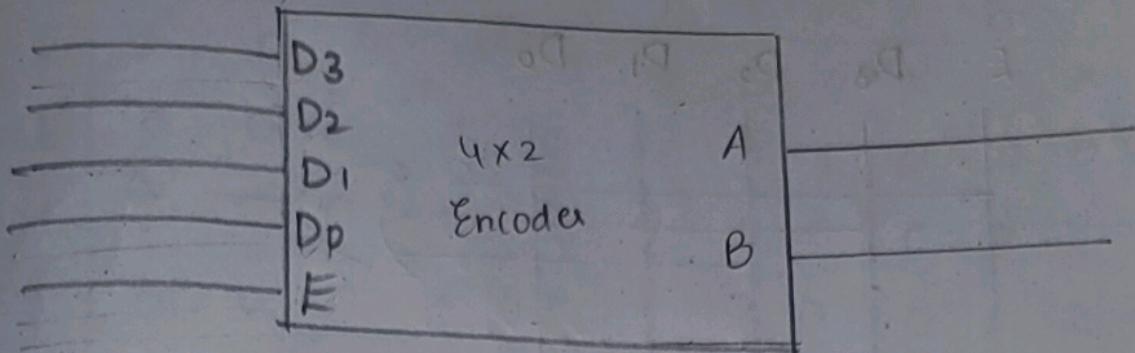
$$2^3 : 3 = 8 : 3.$$

4×2 Encoder :

The no. of inputs are 4, the no. of outputs are 2.

→ Depending upon the 4 input, the output code is generated.

Block Diagram:



The inputs are D_0, D_1, D_2, D_3

The o/p's are A, B.

Truth Table:

E	D_3	D_2	D_1	D_0	A	B
0	0	0	0	0	x	x
1	0	0	0	1	0	0 \rightarrow 0
1	0	0	1	0	0	1 \rightarrow 1
1	0	1	0	0	1	0 \rightarrow 2
1	1	0	0	0	1	1 \rightarrow 3

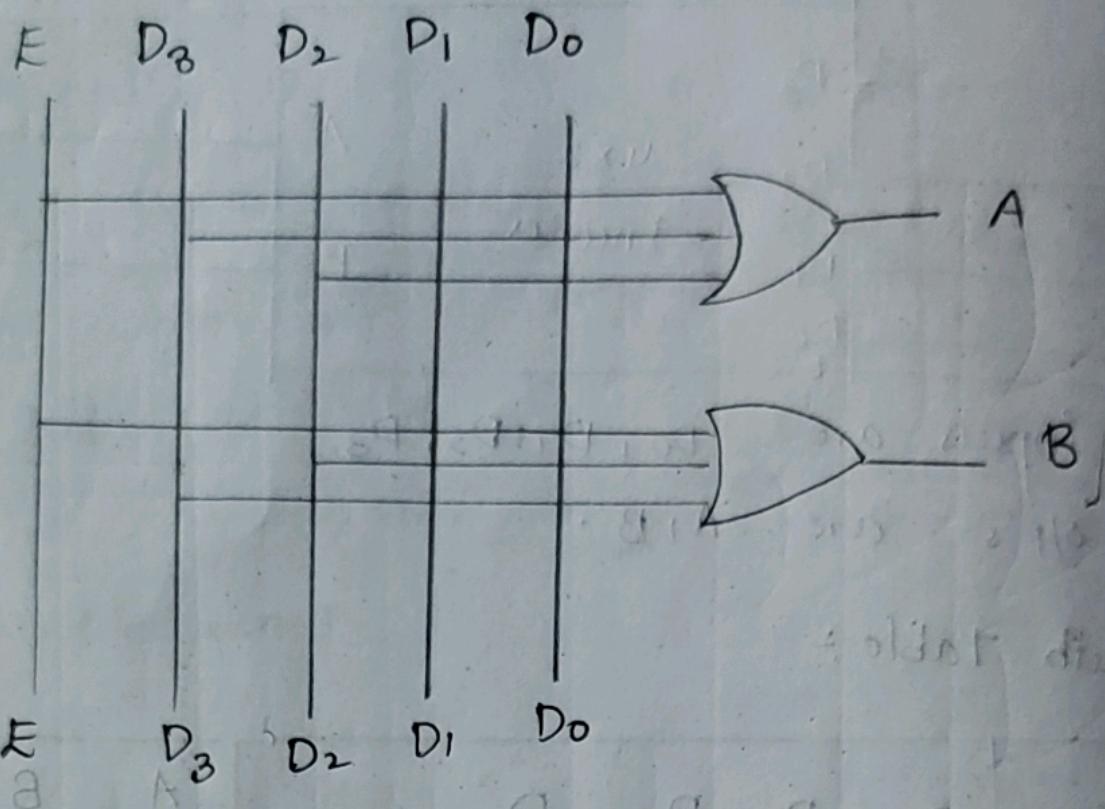
Equations:

$$\text{Output } A = D_2 + D_3$$

$$\text{Output } B = D_1 + D_3$$

Encoder
 2^n i/p's
 n o/p's

Logic Diagram:



Note:

In Encoders, the o/p generates the binary code corresponding to the input value.

5. What is Decoder? Construct 2 to 4

Decoder using logic gates and Truth Table -

1) Decoder :

It is a combinational circuit which has n inputs and 2^n outputs.

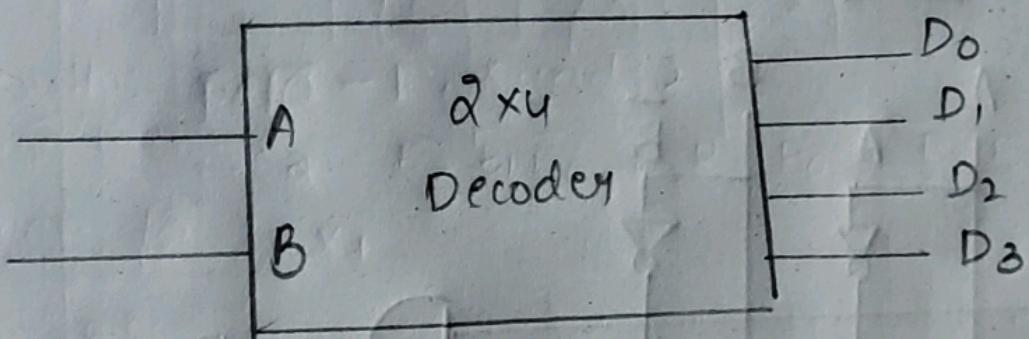
2 to 4 Decoder : 2x4 Decoder,

Here $n = 2$ (inputs)

2^n o/p's \Rightarrow $2^2 = 4$ outputs.

The no. of inputs are 2 and the no. of outputs are 4.

Block diagram :



Depending upon the 2 input, one of the outputs will be high.

Truth Table

E	A	B	D ₀	D ₁	D ₂	D ₃
0	x	x	0	0	0	0
1	0	0	1	0	0	0
1	0	1	0	1	0	0
1	1	0	0	0	1	0
1	1	1	0	0	0	1

Equations:

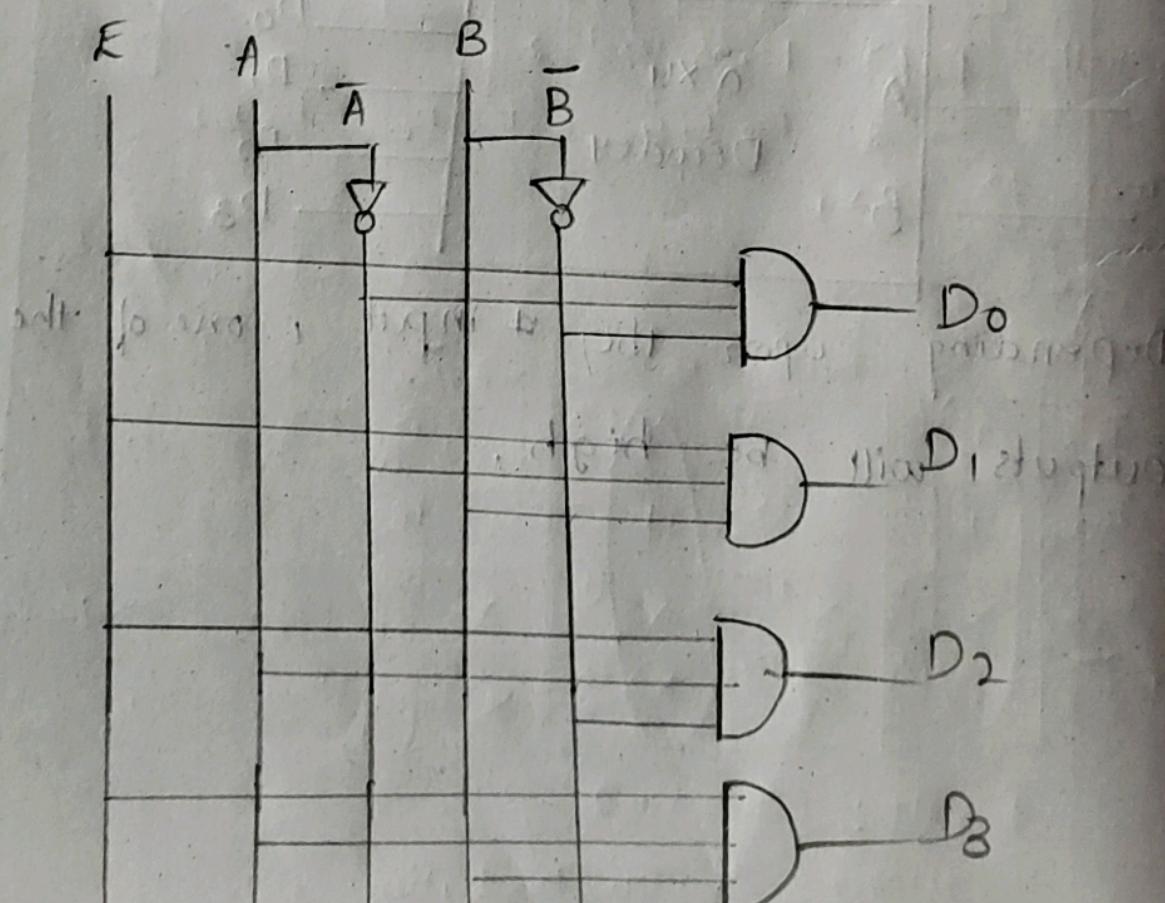
$$D_0 = E \bar{A} \bar{B}$$

$$D_1 = E \bar{A} B$$

$$D_2 = E A \bar{B}$$

$$D_3 = E A B$$

Logic diagram:



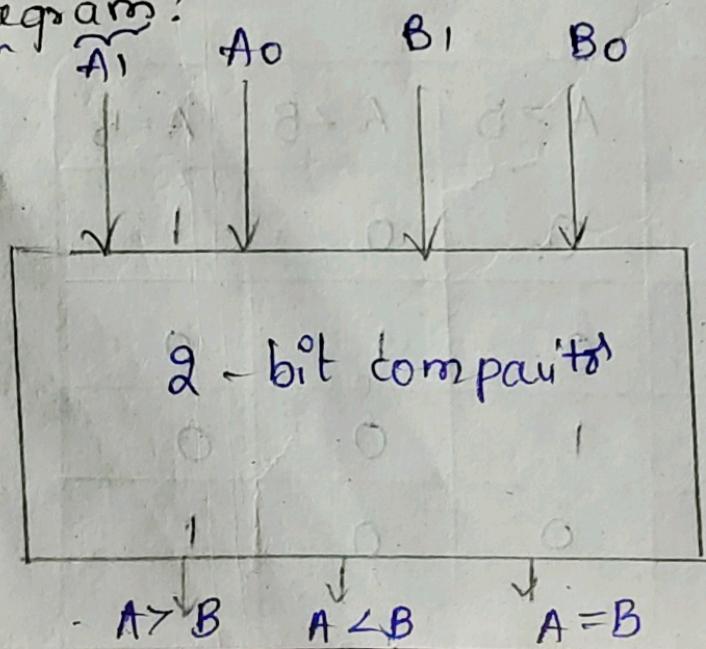
10M

1. Explain 2-bit Magnitude comparator with
neat logic diagram

two-bit
comparator

In two-bit
variable A has two bits A_1 and A_0
variable B has two bits B_1 and B_0

Block Diagram:



Truth Table :

	A ₁	A ₀	B ₁	B ₀	A > B	A = B	A < B
0	0	0	0	0	0	1	0
1	0	0	0	1	0	0	1
2	0	0	1	0	0	0	1
3	0	0	1	1	0	0	1
4	0	1	0	0	1	0	0
5	0	1	0	1	0	1	0
6	0	1	1	0	0	0	1
7	0	1	1	1	0	0	1
8	1	0	0	0	1	0	0
9	1	0	0	1	1	0	0
10	1	0	1	0	0	1	0
11	1	0	1	1	0	0	1
12	1	1	0	0	1	0	0
13	1	1	0	1	1	0	0
14	1	1	1	0	1	0	0
15	1	1	1	1	0	1	0

Equations:

$$1. A > B \equiv \sum m(4, 8, 9, 12, 13, 14)$$

$$2. A < B \equiv \sum m(1, 2, 3, 6, 7, 11)$$

$$3. A = B \equiv \sum m(0, 5, 10, 15)$$



K-map : $(A > B) = Q$

		$B_1 B_0$	$\bar{B}_1 \bar{B}_0$	$\bar{B}_1 B_0$	$B_1 B_0$	$B_1 \bar{B}_0$
		0	1	2	3	4
$A_1 A_0$	1	0	1	0	1	0
$\bar{A}_1 A_0$	0	1	0	1	0	1
$A_1 A_0$	1	0	1	0	1	0
$A_1 \bar{A}_0$	0	1	0	1	0	1

$$A > B = Q$$

Result : Quad = 1, Pair : 2

$$\text{Equation} : Q = A_1 \bar{B}_1 + \bar{B}_1 \bar{B}_0 A_0 + A_1 A_0 \bar{B}_0$$

K-map : $(A \leq B) = L$

		$B_1 B_0$	$\bar{B}_1 \bar{B}_0$	$\bar{B}_1 B_0$	$B_1 B_0$	$B_1 \bar{B}_0$
		0	1	2	3	4
$A_1 A_0$	1	0	1	0	1	0
$\bar{A}_1 A_0$	0	1	0	1	0	1
$A_1 A_0$	1	0	1	0	1	0
$A_1 \bar{A}_0$	0	1	0	1	0	1

Result : Pair : 2, Quad = 1

$$\text{Equation} : Q = \bar{A}_1 B_1 + \bar{A}_1 \bar{A}_0 B_0 + B_1 B_0 \bar{A}_0$$

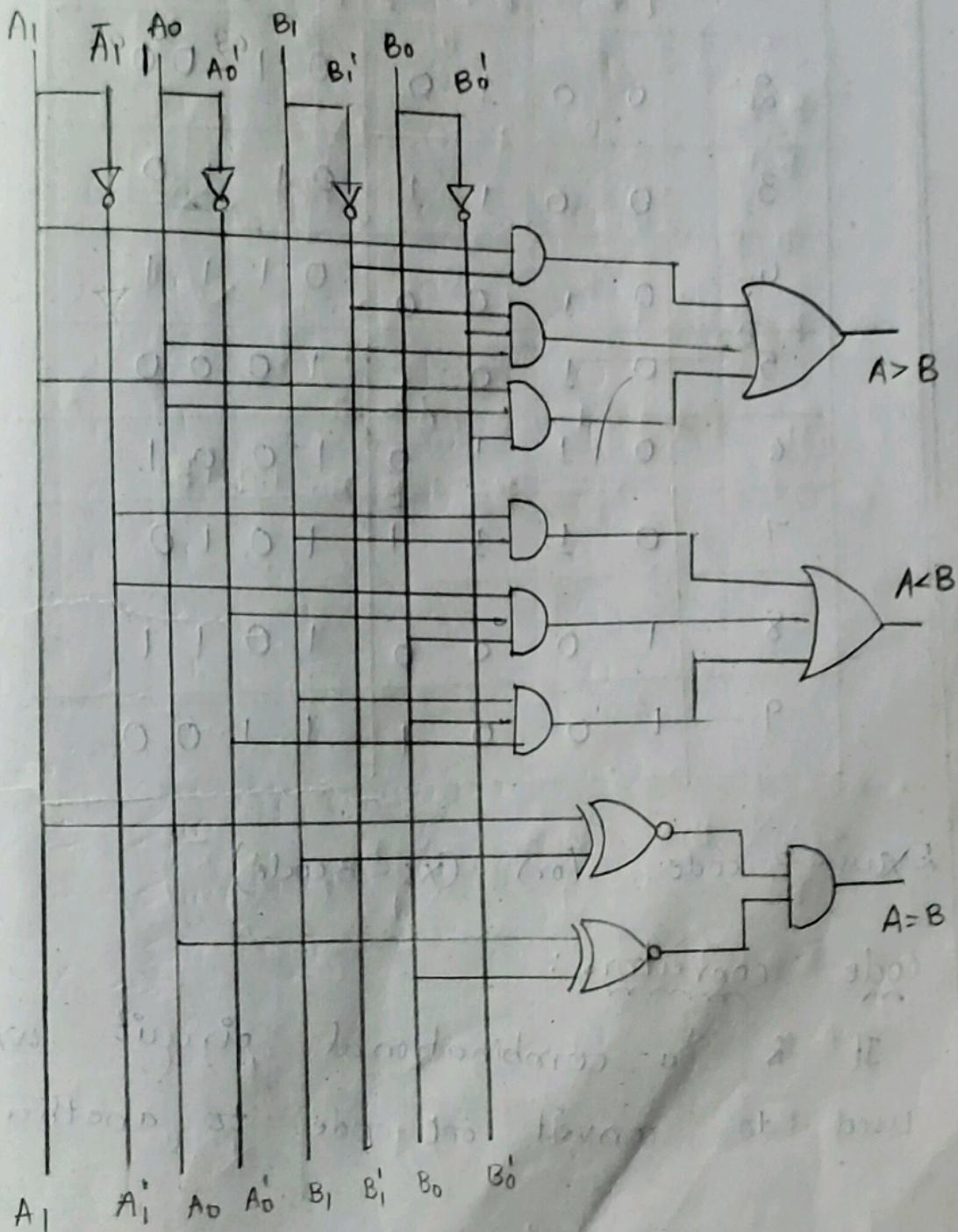
K-map : $(A = B) = E$

		$B_1 B_0$	$\bar{B}_1 \bar{B}_0$	$\bar{B}_1 B_0$	$B_1 B_0$	$B_1 \bar{B}_0$
		0	1	2	3	4
$A_1 A_0$	1	0	1	0	1	0
$\bar{A}_1 A_0$	0	1	0	1	0	1
$A_1 A_0$	1	0	1	0	1	0
$A_1 \bar{A}_0$	0	1	0	1	0	1

Result :

Equation

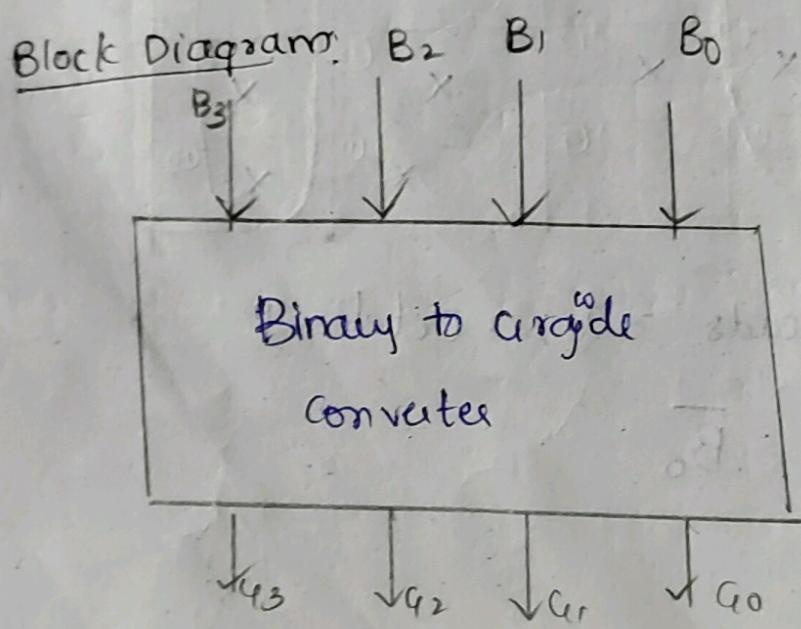
$$\begin{aligned} A &= B ; E = \bar{A}_1 \bar{A}_0 \bar{B}_1 \bar{B}_0 + \bar{A}_1 A_0 \bar{B}_1 B_0 + A_1 A_0 B_1 B_0 + \\ &= A_0 \bar{B}_0 [\bar{A}_1 \bar{B}_1 + A_1 B_1] + A_0 B_0 [\bar{A}_1 \bar{B}_1 + A_1 B_1] \\ &= \bar{A}_0 \bar{B}_0 [A_1 \oplus B_1] + A_0 B_0 [A_1 \oplus B_1] \\ &= A_1 \oplus B_1 [\bar{A}_0 \bar{B}_0 + A_0 B_0] \\ &= (A_1 \oplus B_1) (A_0 \oplus B_0) \end{aligned}$$



2. Design a 4-bit Binary to Gray code converter.

Binary to Gray code converter

The code which converts binary to gray
is known as Binary to Gray code converter.



Truth Table:

dec	B ₃	B ₂	B ₁	B ₀	G ₃	G ₂	G ₁	G ₀
0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	1
2	0	0	1	0	0	0	1	1
3	0	0	1	1	0	0	1	0
4	0	1	0	0	0	1	1	0
5	0	1	0	1	0	1	1	1
6	0	1	1	0	0	1	0	1
7	0	1	1	1	0	1	0	0
8	1	0	0	0	1	1	0	0
9	1	0	0	1	1	1	0	1
10	1	0	1	0	1	1	1	1
11	1	0	1	1	1	1	1	0
12	1	1	0	0	1	0	1	0
13	1	1	0	1	1	0	1	1
14	1	1	1	0	1	0	0	1
15	1	1	1	1	1	0	0	0

Equation:

$$G_3 = \sum m(8, 9, 10, 11, 12, 13, 14, 15)$$

$$G_2 = \sum m(4, 5, 6, 7, 8, 9, 10, 11)$$

$$G_1 = \sum m(2, 3, 4, 5, 10, 11, 12, 13)$$

$$G_0 = \sum m(1, 2, 5, 6, 9, 10, 13, 14)$$



K-map for G₂:

		B ₁ , B ₀	B ₀ , B ₂		
		0	1	0	1
		0	1	0	1
		0	1	0	1
		1	1	1	1
		1	1	1	1
		1	1	1	1

K-map for G₂: $\Sigma m(4, 15, 6, 7, 8, 9, 10, 11)$

		B ₁ , B ₀	B ₁ , B ₀	B ₀ , B ₂	B ₀ , B ₂		
		0	1	0	1	0	1
		0	1	0	1	0	1
		0	1	0	1	0	1
		1	1	1	1	1	1
		1	1	1	1	1	1
		1	1	1	1	1	1

Result: Quad: 2

Eqn: $B_2 \bar{B}_3 + \bar{B}_2 B_3 = B_2 \oplus B_3$

K-map for G₁: $\Sigma m(2, 3, 4, 5, 10, 11, 12, 13)$

		B ₁ , B ₀	B ₁ , B ₀	B ₀ , B ₂	B ₀ , B ₂		
		0	1	0	1	0	1
		0	1	0	1	0	1
		0	1	0	1	0	1
		1	1	1	1	1	1
		1	1	1	1	1	1
		1	1	1	1	1	1

K-map for G₀: $\Sigma m(1, 2, 5, 6, 9, 10, 13, 14)$



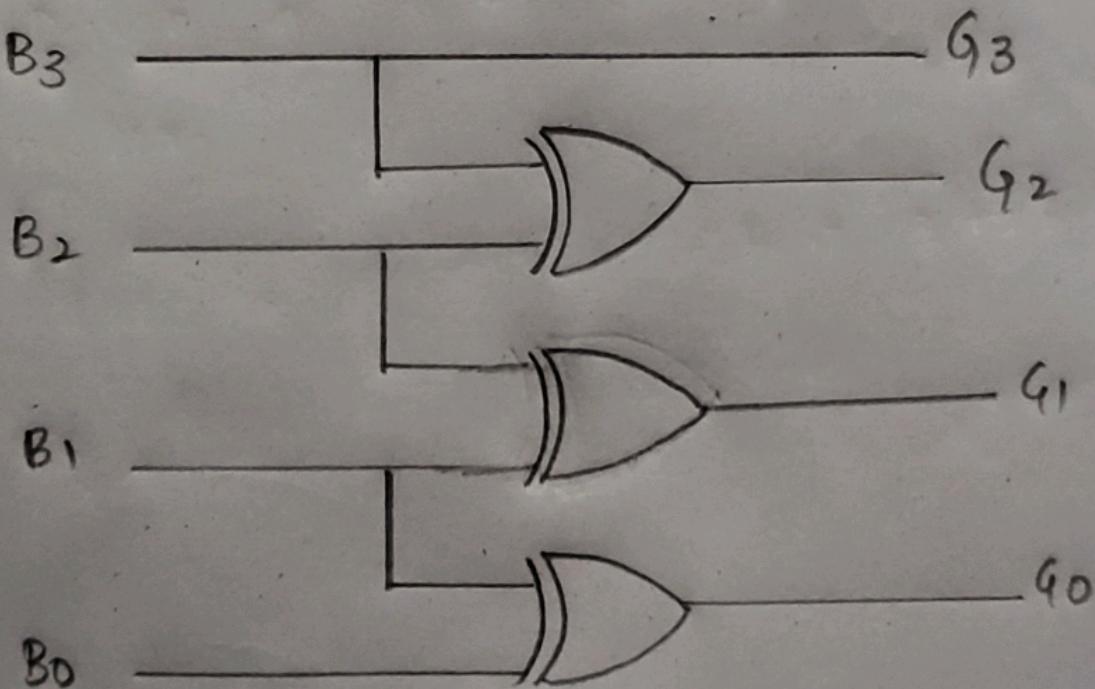
$B_3 B_2$	$B_1 B_0$	$\bar{B}_1 \bar{B}_0$	$\bar{B}_1 B_0$	$B_1 B_0$	$B_1 \bar{B}_0$
$B_3 B_L$	0	1	1	0	1
$B_3 B_2$	4	1	5	7	1
$B_3 B_2$	6	1	13	15	1
$B_3 B_2$	18	1	9	11	1

Result : Two Quads

Equation : $G_D = \bar{B}_1 B_0 + B_1 \bar{B}_0$

$$G_D = B_1 \oplus B_0$$

Logic Diagram:



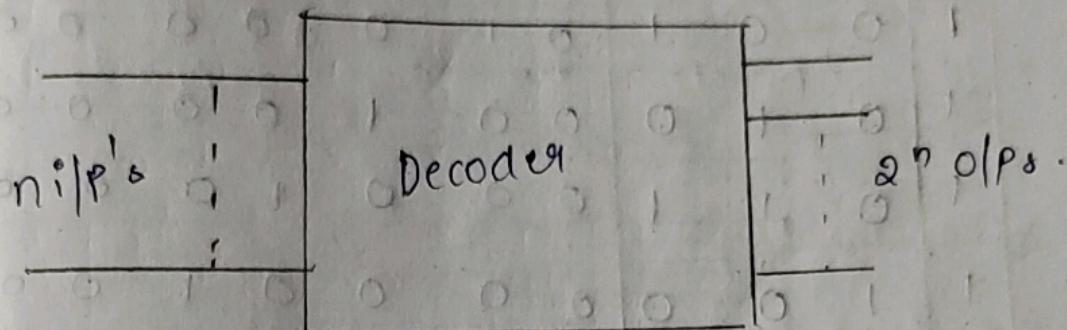
3. What is Decoder ? Construct 3 to 8 Decoder
using logic gates & truth table.

Decoder:

It is a combinational circuits which has n inputs and 2^n outputs.

Depending upon the input, one of the outputs will be high.

Block Diagram:



Ex 2×2^2 Decoder = 2×4

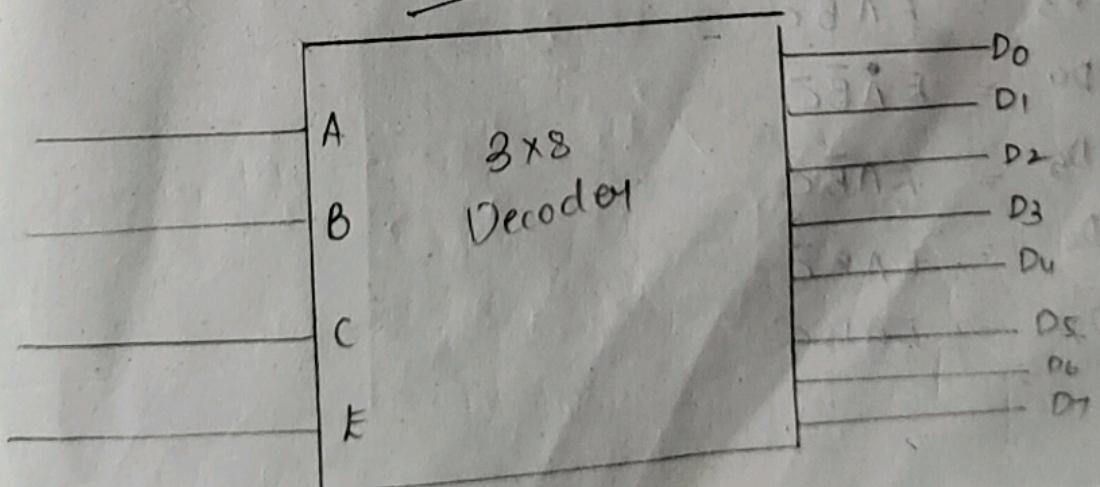
3×2^3 Decoder = 3×8

4×2^4 Decoder = 4×16 .

Decoder:

3x8 Decoder:
The no. of inputs are 3, the no. of outputs = 8.

Block diagram:



Depending upon the 3 inputs, one of the outputs will be high.

Truth Table:

E	A	B	C	D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇
0	*	*	*	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0	0	0
1	0	0	1	0	1	0	0	0	0	0	0
1	0	1	0	0	0	1	0	0	0	0	0
1	0	1	1	0	0	0	1	0	0	0	0
1	1	0	0	0	0	0	0	1	0	0	0
1	1	0	1	0	0	0	0	0	1	0	0
1	1	1	0	0	0	0	0	0	0	0	1
1	1	1	1	0	0	0	0	0	0	0	1

Equations:

$$D_0 = E\bar{A}\bar{B}\bar{C}$$

$$D_1 = E\bar{A}\bar{B}C$$

$$D_2 = EA\bar{B}\bar{C}$$

$$D_3 = EA\bar{B}C$$

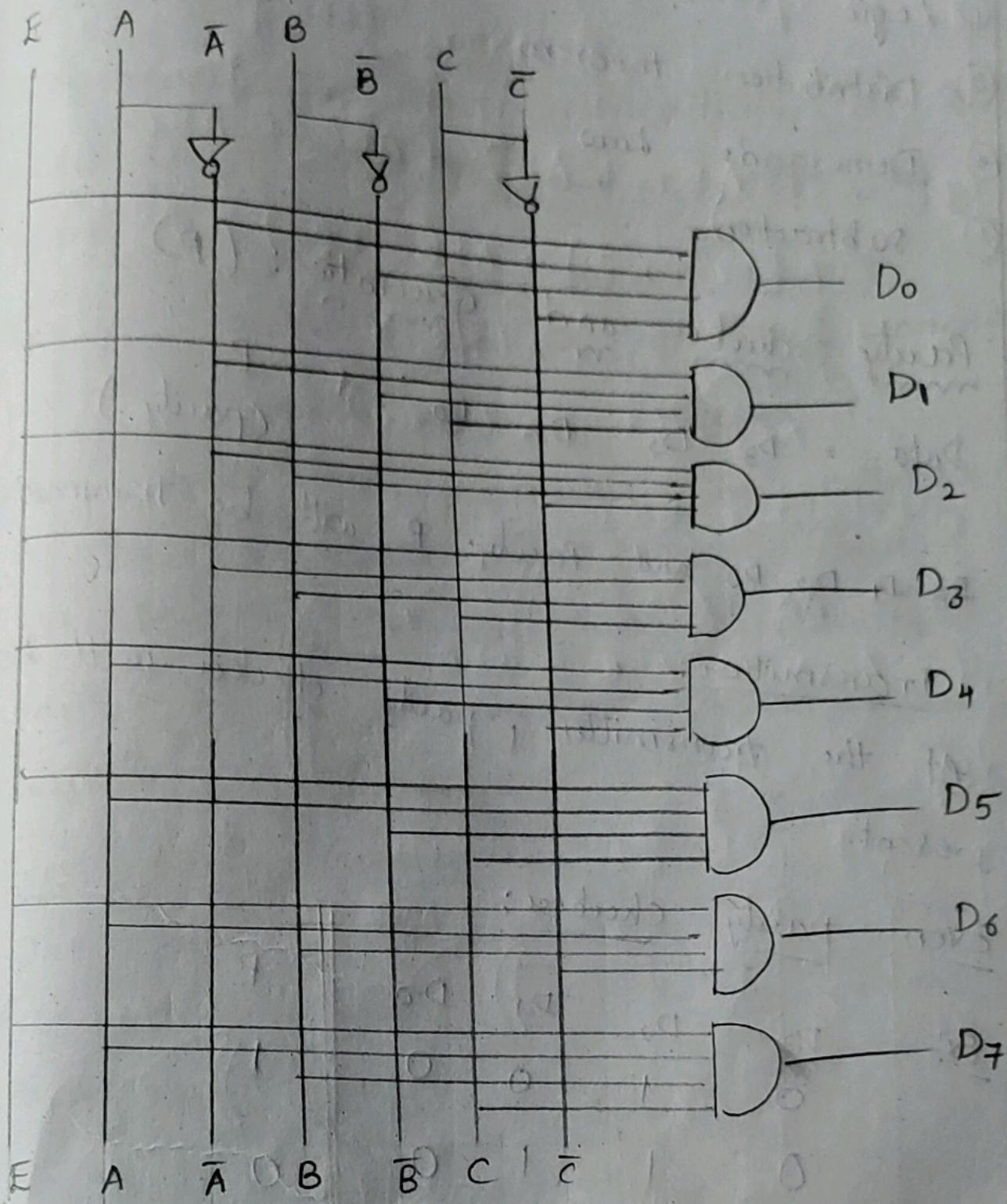
$$D_4 = E\bar{A}B\bar{C}$$

$$D_5 = EA\bar{B}C$$

$$D_6 = EAB\bar{C}$$

$$D_7 = EABC$$

logic diagram:



UNIT - III. (1M)

1. Write the Boolean expression for Difference and Borrow of full subtractor.

A : (i) Boolean expression for Difference of full subtractor

$$\Rightarrow A \oplus B \oplus C_{in}$$

(ii) Boolean expression for Borrow of full subtractor

$$\Rightarrow \bar{A}B + \bar{A}B_{in} + BB_{in}$$

2. Write the Truth-table of Half Adder.

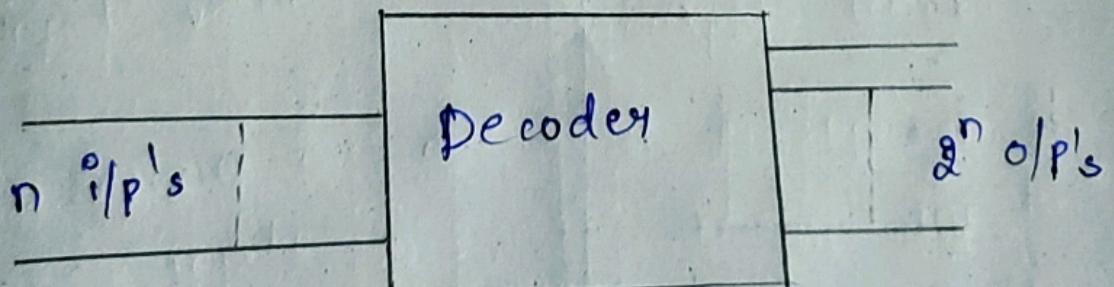
SJ:

A	B	sum	carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

3. Define Decoder and draw its Block diagram.

A) Decoder: It is a combinational circuit which has n inputs and 2^n outputs.

Block diagram



4. What is Priority Encoder?

A: A priority encoder is a logic circuit that response to just one input in accordance with our priority system which will make simultaneously high.

5. What is Comparator?

A) Digital comparator is the combinational circuit which is used to compare 2 bits

3M

1. Write the truth table of full subtractor.

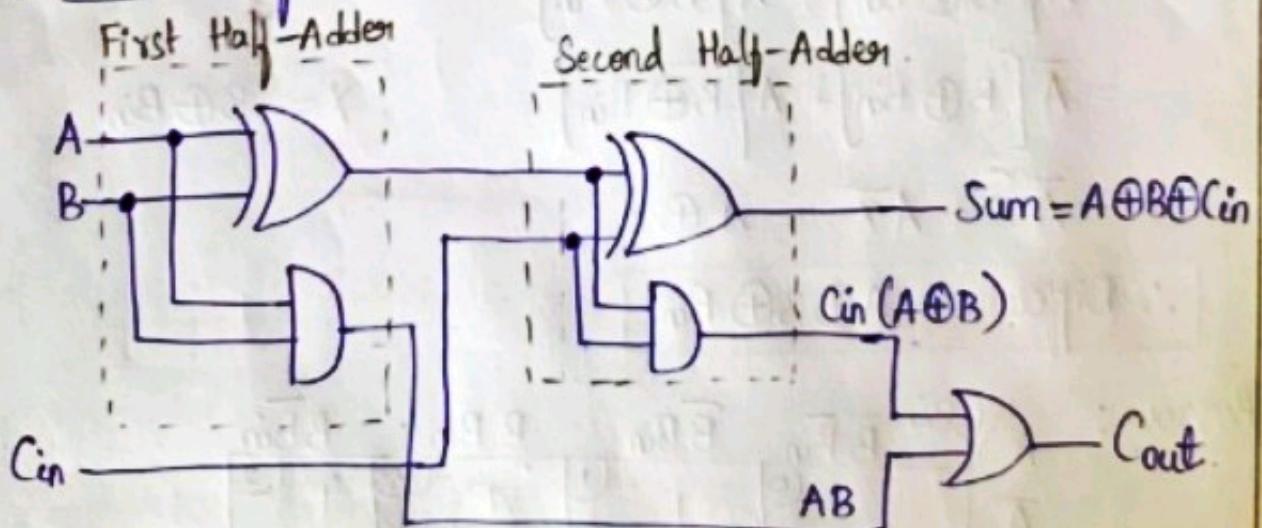
A: Truth Table of full subtractor.

dec	A	B	B _b	D	Bout
0	0	0	0	0	0
1	0	0	1	1	1
2	0	1	0	1	1
3	0	1	1	0	1
4	1	0	0	1	0
5	1	0	1	0	0
6	1	1	0	0	0
7	1	1	1	1	1

Q. Draw the circuit of full Adder using two
Half Adders.

* Full Adder Using Two Half Adders:-

- A full adder can also be implemented with two half-adders and one OR gate.



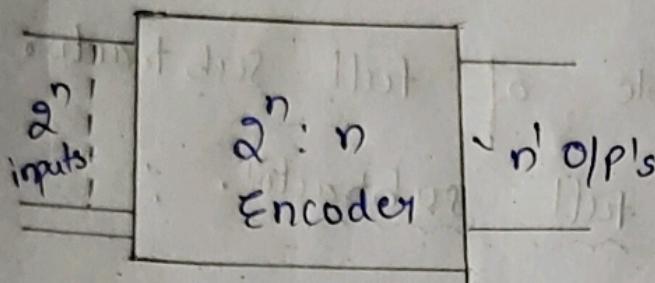
Implementation of A Full-Adder with Two Half-Adders and One OR Gate

3. Compare Encoder and Mux.

A:

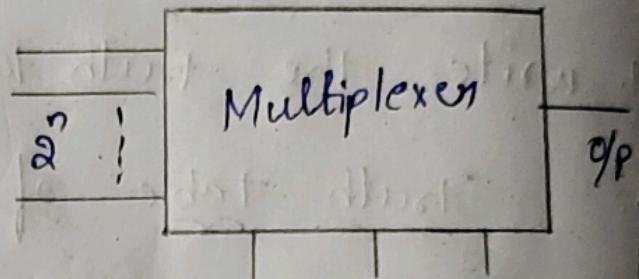
Encoder

1. Block diagram



Mux

Block diagram



2. In encoders, the output lines generate the binary code, corresponding to the input value.

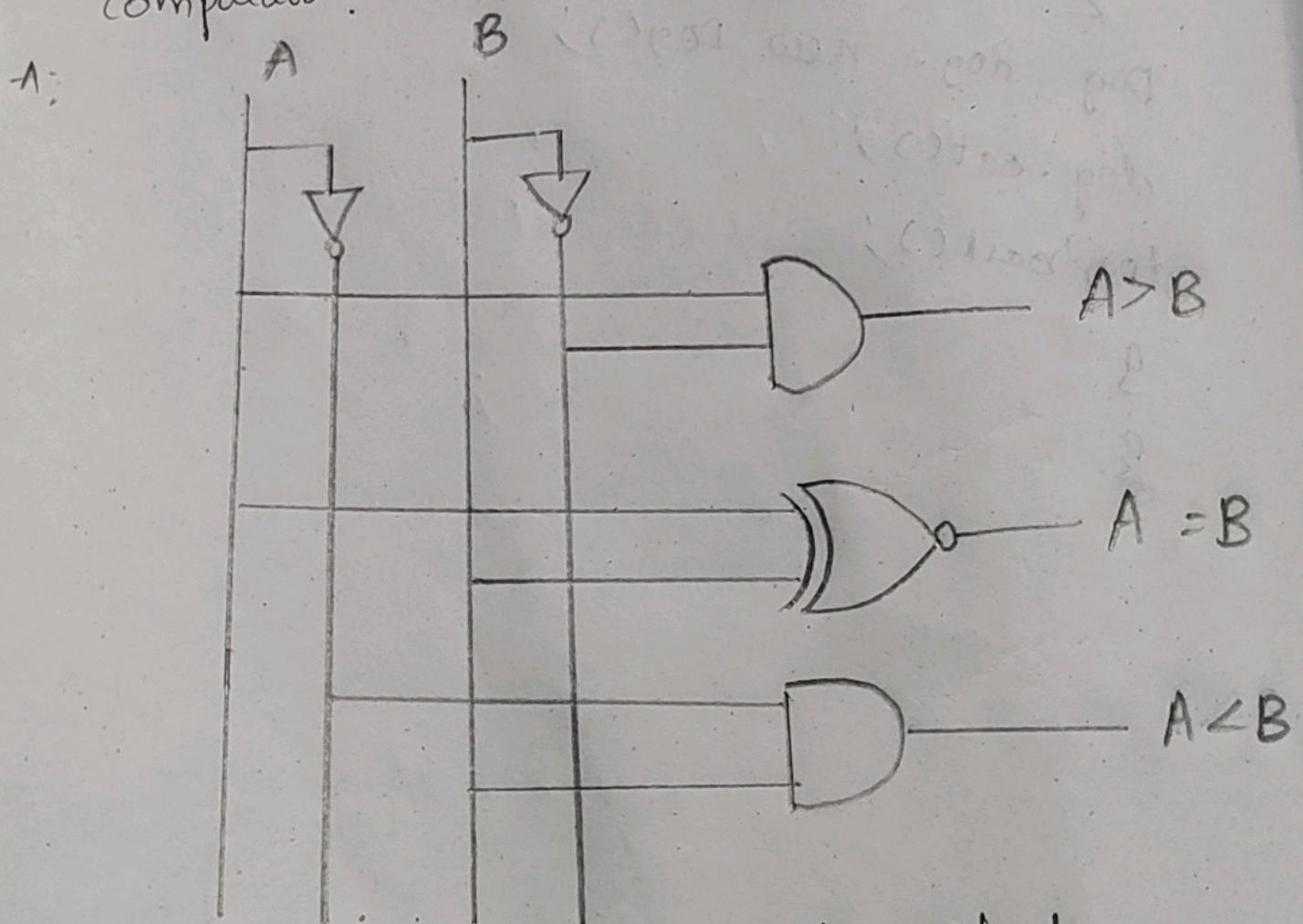
3. Encoder is a many inputs to many output devices

Multiplexer is many to one.

2. In multiplexer selector input determines which input line is selected and routed to single output lines.

3. Multiplexer is a many inputs to one output device

4. Draw the circuit of 1-bit Magnitude
comparator?



logic circuit of 1-bit Magnitude
comparator.

Truth Table :

A	B	$A = B$	$A \leq B$	$A > B$
0	0	1	0	0
0	1	0	1	0
1	0	0	0	1
1	1	1	0	0

Equations :

$$1) A \leq B = A'B$$

$$2) (A = B) = A'B' + AB = A \oplus B$$

$$\boxed{A = B = (A \oplus B)'}$$

$$3) A > B = AB'$$

5. Compare Decoder and Demux.

A:

Decoder	Demux
1. A decoder has n input lines & max of 2^n output lines	1. A Demux has single input, n selection lines and max of 2^n outputs
2. <u>Block diagram</u>	2. <u>Block Diagram</u> 2^n O/Ps \Rightarrow $n=1$ $2^1 = 2$ = 2 output lines $2^{n-1} = 1$ select line

Block diagram of Decoder:

```
graph LR; Decoder[Decoder] --- n_in["n O/Ps"]; Decoder --- n_out["2^n O/Ps"];
```

Block diagram of Demux:

```
graph LR; Demux[Demux] --- S_in["S"]; Demux --- I_in["I"]; Demux --- Y1["Y1"]; Demux --- Y2["Y2"];
```

3. Decoder is inverse of encoder

3. Demux is inverse of Multiplexer (mux)

4. Decoder is used to detect bits, encoding of data.

4. Demux is used in switching, data distribution

5. Decoder has no select lines

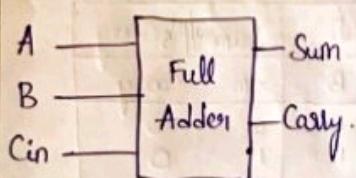
5. Demux contains select lines.

5M

1. Explain the operation of full adder with neat circuit diagram?

2) Full Adder :- It is a combinational circuit which performs addition operation on three bits (A, B, C_{in}) i.e. two are significant bits and one is the previous carry and gives the output as Sum and Carry.

Block Diagram:



Truth Table:

A	B	Cin	Sum	Carry
0	0	0	0	0
1	0	0	1	0
2	0	1	0	0
3	0	1	1	0
4	1	0	0	1
5	1	0	1	0
6	1	1	0	0
7	1	1	1	1

Equation:

$$\text{Sum} = \sum m(1, 2, 4, 7)$$

$$\text{Carry} = \sum m(3, 5, 6, 7)$$

K-Map:

Sum:		$B\bar{C}_{in}\bar{B}\bar{C}_{in}$	$\bar{B}C_{in}$	$B\bar{C}_{in}$	$\bar{B}\bar{C}_{in}$
		0	1	2	3
A		0	1	0	1
A		1	0	1	0
A		0	1	0	1

$$\begin{aligned} \text{Sum} &= \bar{A}\bar{B}\bar{C}_{in} + \bar{A}B\bar{C}_{in} + A\bar{B}\bar{C}_{in} + ABC_{in} \\ &= \bar{A}[\bar{B}\bar{C}_{in} + B\bar{C}_{in}] + A[\bar{B}\bar{C}_{in} + BC_{in}] \\ &= \bar{A}(B \oplus C_{in}) + A(B \odot C_{in}) \\ &= \bar{A}(B \oplus C_{in}) + A(\bar{B} \oplus \bar{C}_{in}) \end{aligned}$$

(2)

Let $B \oplus C = X$, then the Sum becomes.

$$\text{Sum} = \bar{A}X + A\bar{X}$$

$$= A \oplus X \quad (\text{put the value of } X)$$

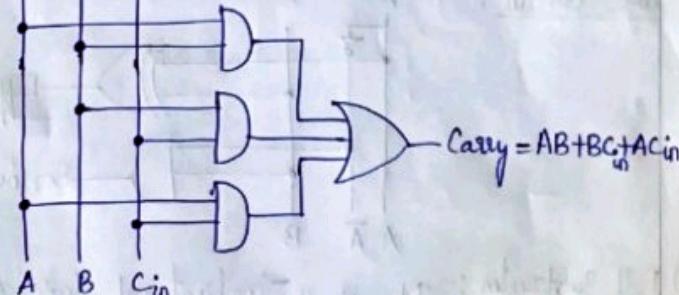
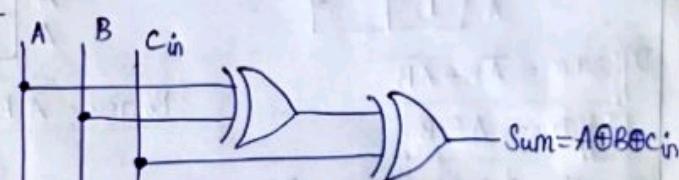
$$\text{Sum} = A \oplus B \oplus C_{in}$$

Carry:		BC	$\bar{B}C$	$\bar{B}\bar{C}$	$B\bar{C}$
		0	1	2	3
A		0	1	1	0
A		0	1	1	0
A		1	0	0	1

Result : Parity = 3

$$\text{Carry} = AB + BC_{in} + AC_{in}$$

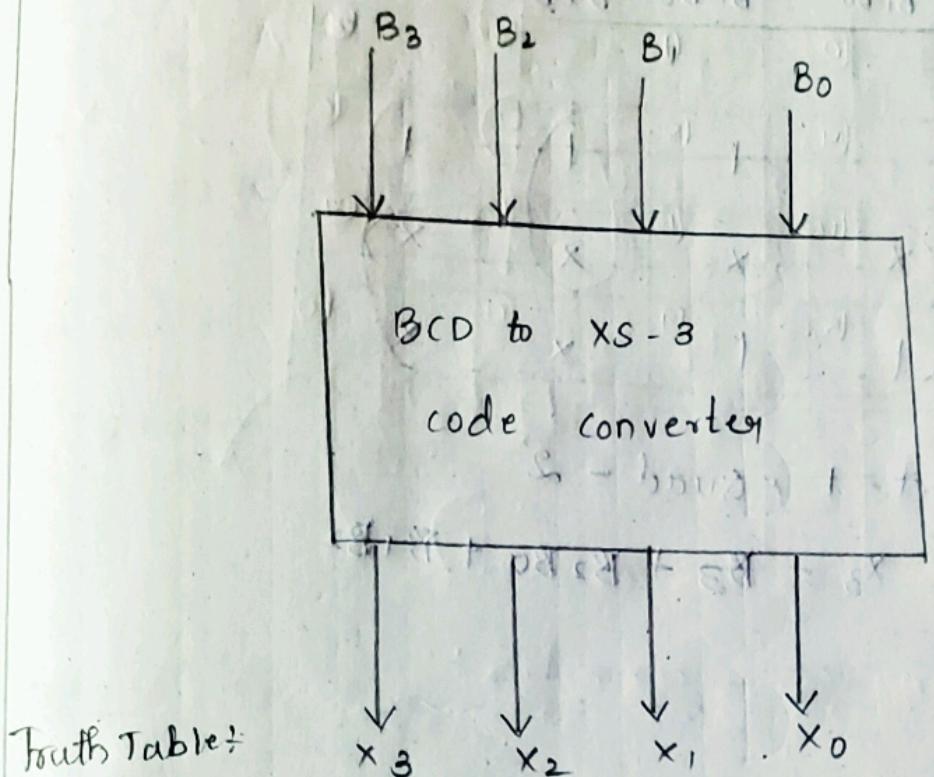
Logic Circuit:



2. Design a 4-bit BCD to Excess-3 code converter.

1. BCD to XS-3 Code converter

we are taking BCD code and it is converted into XS-3 code.



Truth Table:

dec	B ₃	B ₂	B ₁	B ₀	X ₃	X ₂	X ₁	X ₀
0	0	0	0	0	0	0	1	1
1	0	0	0	1	0	1	0	0
2	0	0	1	0	0	1	0	1
3	0	0	1	1	0	1	1	0
4	0	1	0	0	0	1	1	1
5	0	1	0	1	1	0	0	0
6	0	1	1	0	1	0	0	1
7	0	1	1	1	1	0	1	1
8	1	0	0	0	1	1	0	0
9	1	0	0	1	1	1	0	0

Equations:

$$x_3 = \sum m(5, 6, 7, 8, 9) + d(10, 11, 12, 13, 14, 15)$$

$$x_2 = \sum m(0, 1, 2, 3, 4, 9) + d(10, 11, 12, 13, 14, 15)$$

$$x_1 = \sum m(0, 3, 4, 7, 8) + d(10, 11, 12, 13, 14, 15)$$

$$x_0 = \sum m(0, 2, 4, 6, 8) + d(10, 11, 12, 13, 14, 15)$$

K-map for $x_3 =$

$\bar{B}_3 \bar{B}_2$	$B_1 \bar{B}_0$	$B_1 B_0$	$\bar{B}_1 B_0$	$B_1 B_0$
$\bar{B}_3 B_2$	0	1	1	2
$B_3 \bar{B}_2$	4	15	7	16
$B_3 B_2$	12	13	15	14
$\bar{B}_3 B_2$	18	9	11	10

Result: Octet - 1, Quad - 2

$$\text{Equation: } x_3 = B_3 + B_2 \bar{B}_0 + B_1 B_2$$

K-map for $x_2 =$

$\bar{B}_3 \bar{B}_2$	$\bar{B}_1 \bar{B}_0$	$\bar{B}_1 B_0$	$B_1 \bar{B}_0$	$B_1 B_0$
$\bar{B}_3 B_2$	0	1	1	2
$B_3 \bar{B}_2$	14	15	17	16
$B_3 B_2$	12	13	15	14
$\bar{B}_3 \bar{B}_2$	18	9	11	10

Result: Octet - 1, Quad - 2

$$\text{Equation: } x_2 = B_2 \bar{B}_1 \bar{B}_0 + \bar{B}_2 B_0 + \bar{B}_2 B_1$$

K-map for $x_1 =$

$\bar{B}_3 \bar{B}_2$	$\bar{B}_1 \bar{B}_0$	$\bar{B}_1 B_0$	$B_1 \bar{B}_0$	$B_1 B_0$
$\bar{B}_3 B_2$	1	0	1	2
$B_3 \bar{B}_2$	1	4	15	16
$B_3 B_2$	X	12	13	14
$\bar{B}_3 \bar{B}_2$	1	8	9	10

Result: Quads - 2,

$$\text{Equation: } \bar{B}_1 \bar{B}_0 + B_1 B_0$$

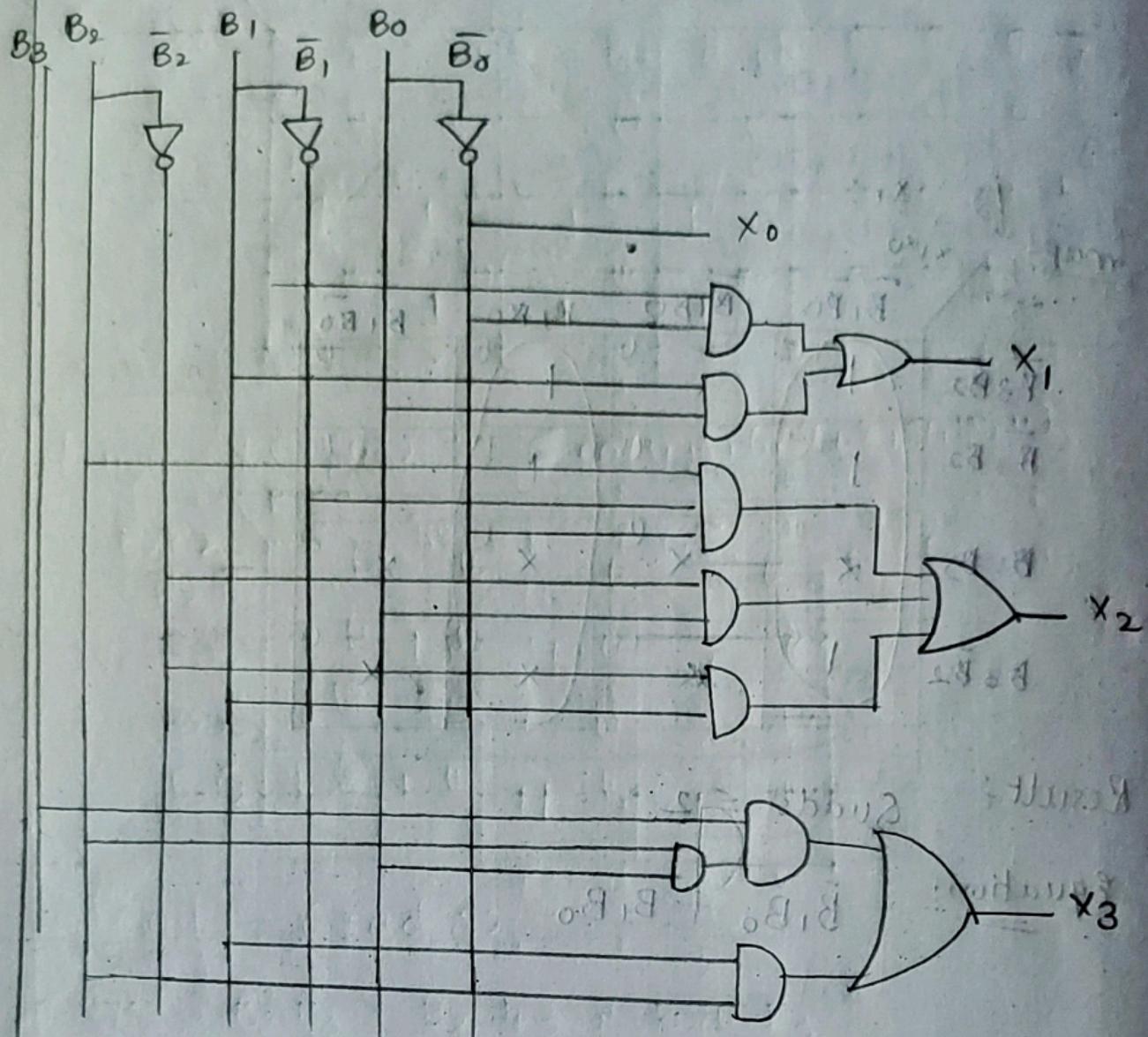
K-map for X_0 :

$B_1 B_0$	$\bar{B}_1 B_0$	$\bar{B}_1 \bar{B}_0$	$B_1 \bar{B}_0$	$B_1 \bar{B}_0$
$\bar{B}_2 B_3$	1 (0)	0 (1)	1 (2)	0 (3)
$\bar{B}_2 \bar{B}_3$	1 (4)	0 (5)	1 (6)	0 (7)
$B_2 B_3$	X (8)	X (9)	X (10)	X (11)
$B_2 \bar{B}_3$	1 (12)	0 (13)	X (14)	X (15)

Result = \bar{B}_0 Octet = 1

Equation : \bar{B}_0

Logic Diagram of 4 to 8 Decoder + OR



3. What is comparator? Design 1-bit comparator.

Digital Comparator:

Digital comparator is the combinational circuit which is used to compare 2 bits.

The operations are:

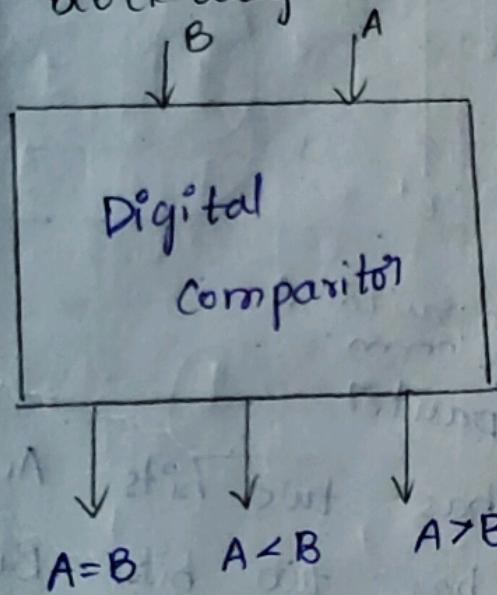
$$A > B$$

$$A < B$$

$$A = B$$

One-bit Comparator:

Block diagram:



Truth Table:

A	B	$A > B$	$A < B$	$A = B$
0	0	0	0	1
1	0	1	0	0
0	1	0	1	0
1	1	0	0	1

Equation:

$$A > B : \Sigma m(2) = A\bar{B}$$

$$A < B : \Sigma m(1) = \bar{A}B$$

$$A = B : \Sigma m(0, 3) = \bar{A}\bar{B} + AB = A \oplus B$$

Logic circuit:

