Unit - IV

1 marks Questions

1. Define Flip-flop.

Ans. Flipflop is the basic building block of sequential circuit. It is one-bit storage Element. flipflop is controlled by Edge triggered clock.

2. List the types of Shift Registers.

Ans. The types of Shift Register are :-

1. serial in - Serial out Shift Register
2. serial in - parallel out Shift Register
3. parallel in - parallel out Shift Register
4. parallel in - serial out Shift Register

3. What is a sequential Circuit? Give Examples.

Ans. sequential circuits are the circuits. when the present output depends upon the present input and previous output.

Example :-

1. Counters
2. Shift Registers

4. Give the applications of Flip-flop?

Ans. 1. It is used as a basic building block in sequential circuits such as counters and Registers.
2. It can be used as a Memory element.

5. what is a Shift Register?

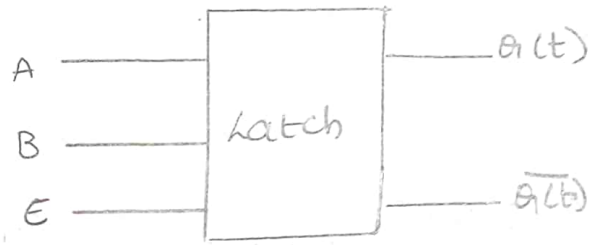
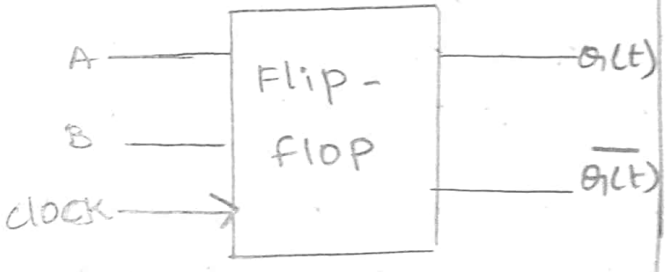
Ans2. This type of shifting bits in the register Gives rise to group of registers are called shift register

1. The Binary information in the register can be moved from one stage to another stage within the register.

3 marks Questions :-

1. Compare Latch and flipflop.

Ans.

Latch	flip-flop.
1. Latch is basic building block of sequential circuit. It is one bit storage Element.	1. flip-flop is basic building block of sequential circuit. It is one bit storage element.
2. Latch is controlled by level triggered clock ie Enable Signal.	2. flip-flop controlled by Edge triggered clock.
3. Latch output responds to Input's until active high (or) active low is maintained on clock.	3. flip-flop o/p responds to i/p's only on specified +ve (or) -ve Edge of the clock.
4. 	

2. write the characteristic tables for D FlipFlop and TFlipflop

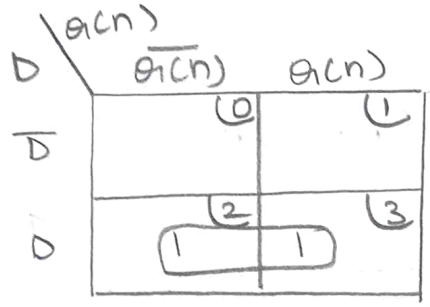
Ans. Characteristic table for D flipflop :-

	D	Q(n)	Q(n+1)
0	0	0	0
1	0	1	0
2	1	0	1
3	1	1	1

External input = D
present state = $Q_1(n)$
Next state = $Q_1(n+1)$

Equation :-

$Q_1(n+1) = \Sigma m(2,3)$ (K-map)



characteristic Equation :-

$\boxed{Q_1(n+1) = D}$

b) Characteristic table for T Flipflop :-

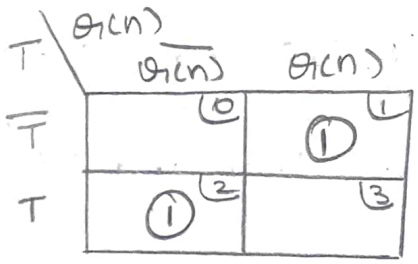
External input = T
present state = $Q_1(n)$
Next state = $Q_1(n+1)$

	T	$Q_1(n)$	$Q_1(n+1)$	
No change	0	0	0	0
	0	1	1	1
Toggle	1	0	1	2
	1	1	0	3

Equation :-

$Q_1(n+1) = \Sigma m(1,2)$

K-map :-



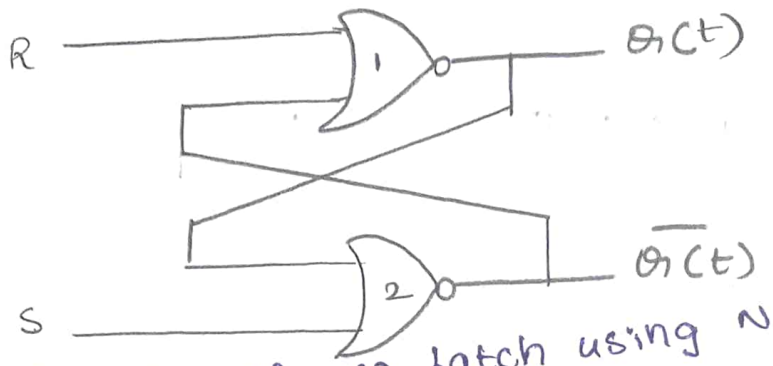
characteristic Equation :-

$\boxed{\therefore Q_1(n+1) = \bar{T} Q_1(n) + T \overline{Q_1(n)}}$

3. Bricfly discuss about SR Latch using NOR Gate.

Ans. Basic SR Latch using NOR Gate :-

i)

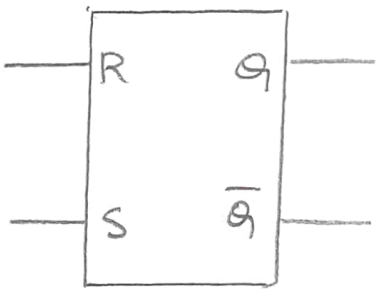


Circuit diagram of SR Latch using NOR gates

Truth table (NOR Gate) :-

A	B	$\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

ii) Block diagram :-



iii) Truth table :-

S	R	Q(t)	$\overline{Q(t)}$	state of operation
0	0	1/0	0/1	No change
0	1	0	1	Reset
1	0	1	0	set
1	1	0	0	Invalid state.

4. Give the Excitation tables for JK Flip flop and T flip flop.

Ans. The Excitation table for JK Flipflop :- It specifies the External Input's based on the given state Q(n) and Q(n+1)

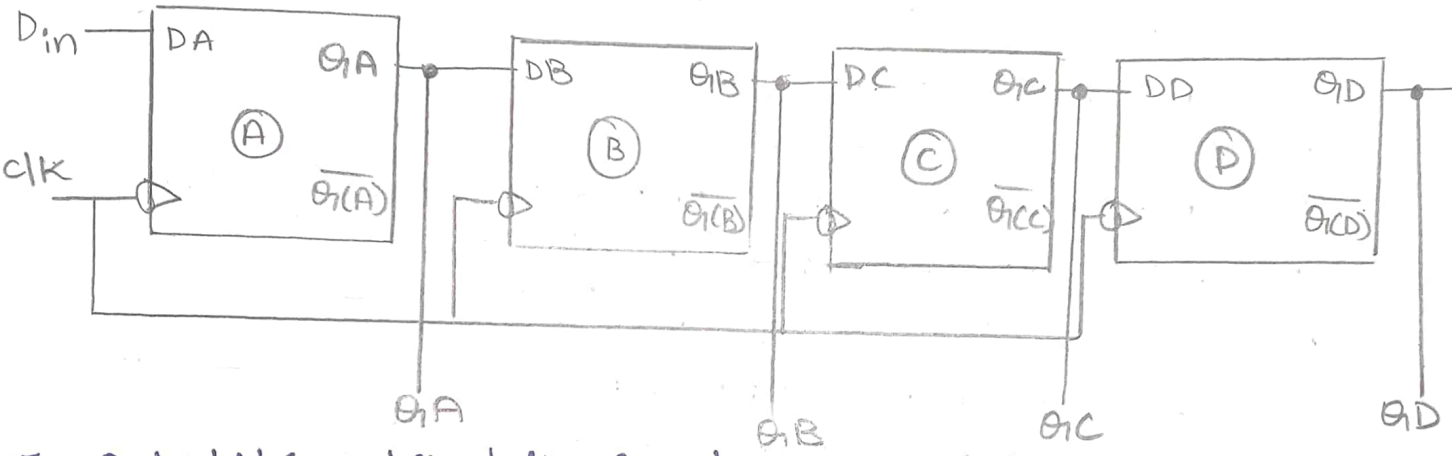
Inputs		Outputs	
Q(n)	Q(n+1)	J	k
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

Excitation table for T Flipflop :- It specifies the external inputs based on the present state $Q_1(n)$ and next state $Q(n+1)$

present State $Q_1(n)$	Next State $Q_1(n+1)$	External input T
0	0	0
0	1	1
1	0	1
1	1	0

5. Explain about serial-In-parallel-out shift Register?

Ans.



The Data bits entered in Serial in into the Register but the output is taken parallel.
Once the data is stored each bit appears on its respective output line and all bits are available simultaneously.

5 marks

1. Explain the operation of JK Flip-flop with truth table.

Ans. Operation :-

1. when clock is not ~~Equal~~ applied :-

since there is no clock signal, the outputs of both the AND Gates are Logic 0. Then S=0, R=0 case for NOR Latch which results is "No change".

2. When clock signal is applied :-

Case a):- J=0, K=0, clock = ↑

The output of AND gates are Logic 0. Then S=0, R=0 case for NOR Latch which results in "No change".

Case b):- J=0, K=1, clock = ↑

AND Gate 2 is disabled. So these is no way to set the flipflop we assume previous output $Q_1=1$. AND Gate 1 output is Logic 1 i.e R=1.

It results in "Reset" state.

Case c):- J=1, K=0, clock = ↑

AND Gate 1 is disabled. So there is no way to Reset the flipflop we assume previous o/p.

$\overline{Q_1}=1$. the output of AND gate 2 is Logic 1.

S=1. The result is "set".

Case d):- J=1, K=1, clock = ↑

Assume $\overline{Q_1}=0$: If $\overline{Q_1}=0 \Rightarrow Q_1=1$

K=1, $Q_1=1$ then output of AND gate 1 is Logic 1.

R=1. The o/p from the NOR gate is $Q_1=0$

Assume $\overline{Q_1}=1$: If $\overline{Q_1}=1 \Rightarrow Q_1=0$

J=1, $\overline{Q_1}=1$ the o/p of AND gate 2 is Logic 1

S=1. The o/p from NOR gate is $\overline{Q_1}=0$

∴ J=1, K=1, the o/p of flipflop toggles on the application of clock pulse. Hence the state of operation is "Toggle".

Truth table :-

clock	J	K	Q_1	$\overline{Q_1}$	State of operation
0	x	x	Q_0	$\overline{Q_0}$	No change
↑	0	0	Q_0	$\overline{Q_0}$	No change
↑	0	1	0	1	Reset
↑	1	0	1	0	Set
↑	1	1	$\overline{Q_0}$	Q_0	Toggle

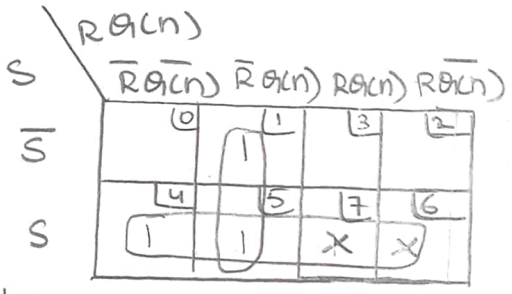
2. Convert a D Flipflop to SR Flipflop

Ans. Truth table :-

dec	i/p's		P.S	N.S	External i/p
	S	R	$Q_1(n)$	$Q_1(n+1)$	D
0	0	0	0	0	0
1	0	0	1	1	1
2	0	1	0	0	0
3	0	1	1	0	0
4	1	0	0	1	1
5	1	0	1	1	1
6	1	1	0	x	x
7	1	1	1	x	x

K-map :-

$D = \Sigma m(1,4,5) + \Sigma d(6,7)$

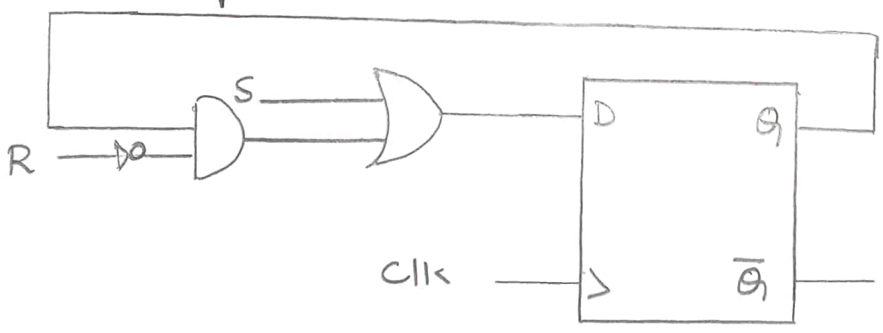


Result :-

Quad = 1, pair = 1

$D = S + \bar{R} Q_1(n)$

Logic diagram :-



3. What is a counter? Give the difference between synchronous counter and Asynchronous Counter.

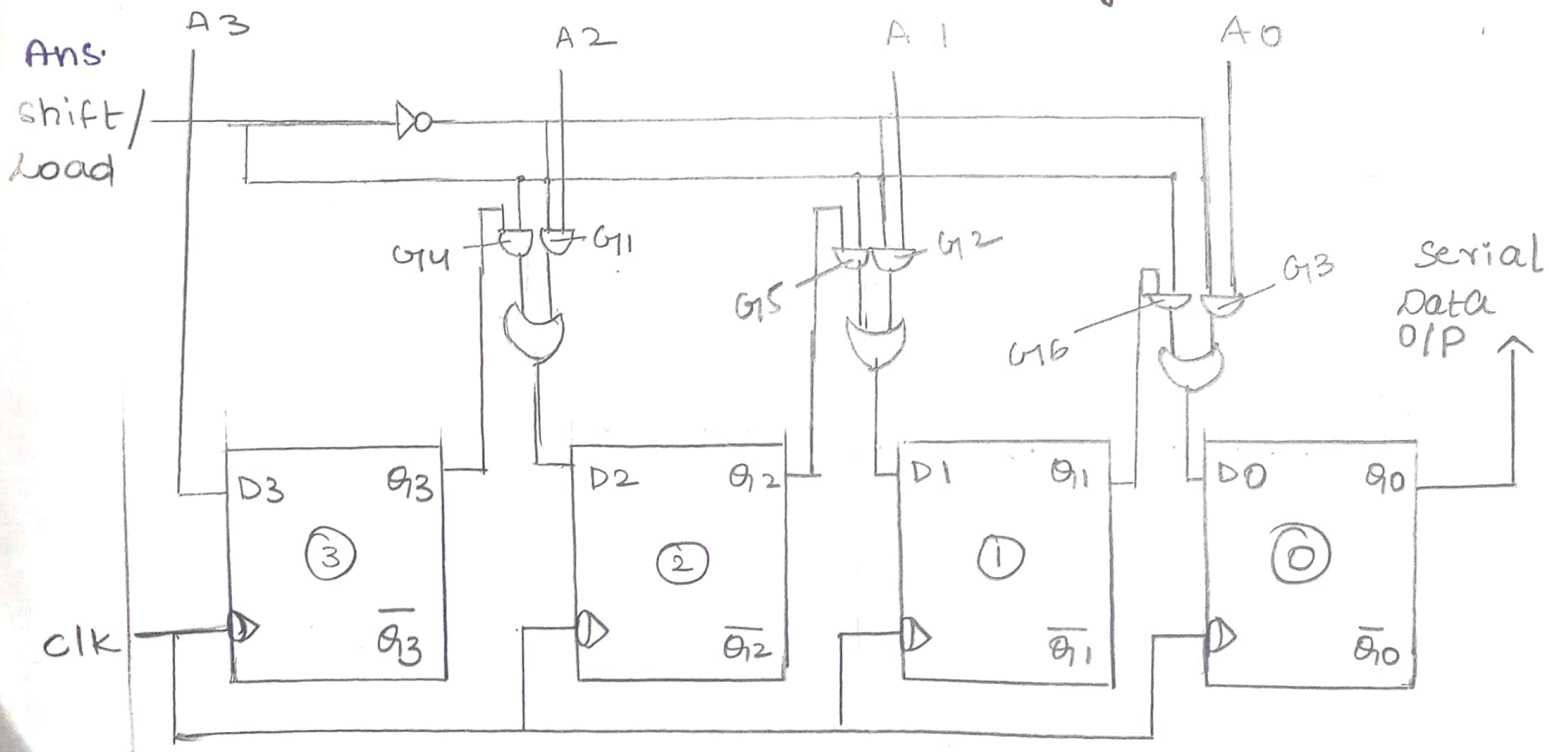
Ans. Counter :- Counter is a sequential circuit which is capable of counting the no. of clock pulse arrived at its clock

The difference b/w synchronous and Asynchronous

synchronous counter	Asynchronous counter.
1. All the flip-flops are clocked simultaneously.	1. All the flip-flops are not clocked simultaneously.
2. In this type, there is no connection b/w o/p of first flip-flop and clock input of next flip-flop.	2. In this type of counter, flip-flops are connected in such a way that o/p of first flip-flop drives the next Flip-Flop.
3. Design involves complex logic circuits as no. of states increases.	3. The logic circuit is very simple even for more no. of stages.
4. There is no propogation delay. Hence they are high speed counters	4. There is propogation delay Hence they are low speed counters.

4. Explain parallel-In-serial-out shift Register.

Ans:



Parallel-In serial-out shift Register

Explanation:-

→ In this type the bits are Entered in parallel i.e simultaneously into their respective stages on parallel lines.

→ A 4-bit parallel-in serial out register is shown in the circuit.

→ There are 4 Input lines i.e A3, A2, A1, A0 for entering data in parallel into ø the register SHIFT/LOAD is low, gates G1, G2, G3 are Enabled, allowing each input data bit to be applied to 'D' input of its respective flip-flop.

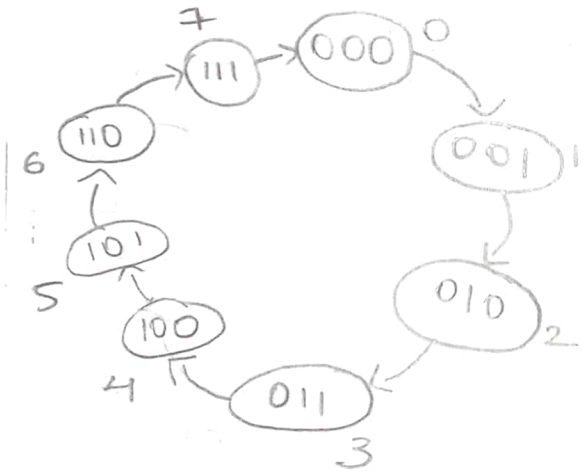
→ When clock pulse is applied, the flip-flop bit D=1 will be "SET" and those which D=0 will be "RESET"

5. Design a 3-Bit Binary counter using T Flip Flop.

Ans. Step 1:- The no. of flipflops required are 3

Step 2:- The type of flipflop used here is T-FlipFlop

State diagram:-



Step 3:-

The Excitation table of Tflip-flop

Q(n)	Q(n+1)	T
0	0	0
0	1	1
1	0	1
1	1	0

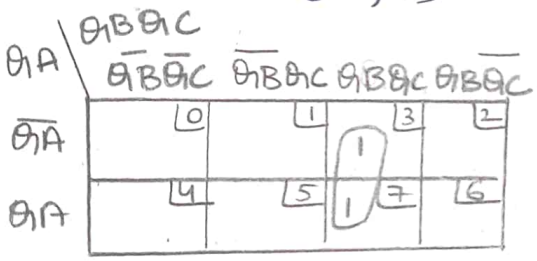
Truth table :-

	Present State			Next State			Flip-Flop Input		
	Q_A	Q_B	Q_C	Q_{A+1}	Q_{B+1}	Q_{C+1}	TA	TB	TC
0	0	0	0	0	0	1	0	0	1
1	0	0	1	0	1	0	0	1	1
2	0	1	0	0	1	1	0	0	1
3	0	1	1	1	0	0	1	1	1
4	1	0	0	1	0	1	0	0	1
5	1	0	1	1	1	0	0	1	1
6	1	1	0	1	1	1	0	0	1
7	1	1	1	0	0	0	1	1	1

Step :- 4

K-map Simplification :-

For $TA = \Sigma m(3,7)$



Result :-

Pair : 1

Equi :- $Q_B Q_C$

$\therefore TA = Q_B Q_C$

For $TB = \Sigma m(1,3,5,7)$

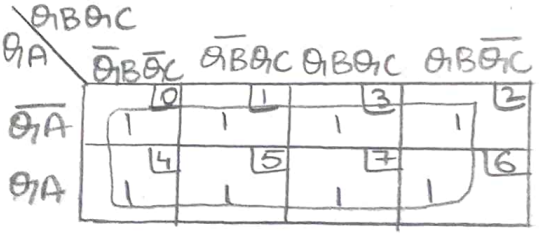
Result :-

Quadil

Equi :- Q_C

$\therefore TB = Q_C$

For $TC = \Sigma m(0,1,2,3,4,5,6,7)$



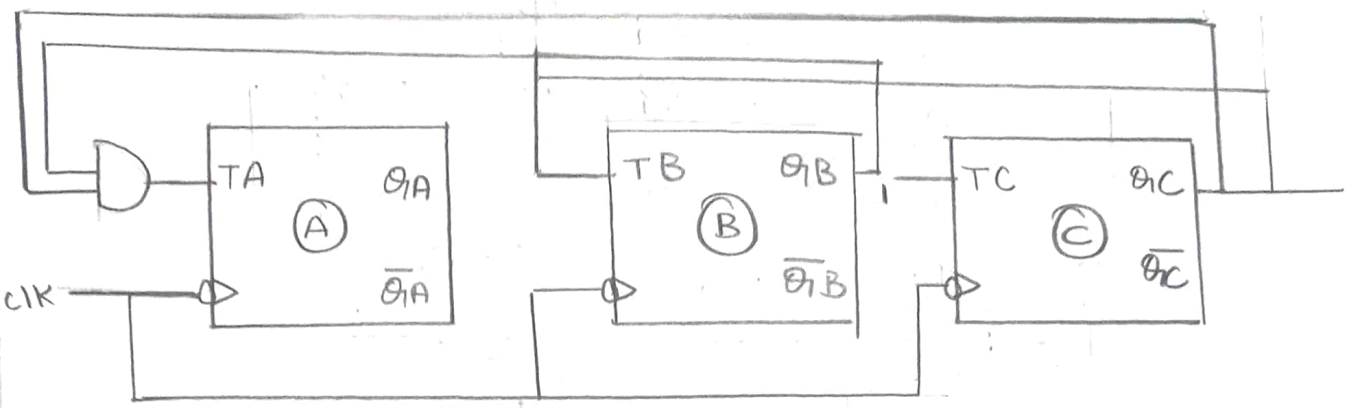
Result :-

Octet : 1

Equi :- 1

$\therefore TC = 1$

Logic diagram :-



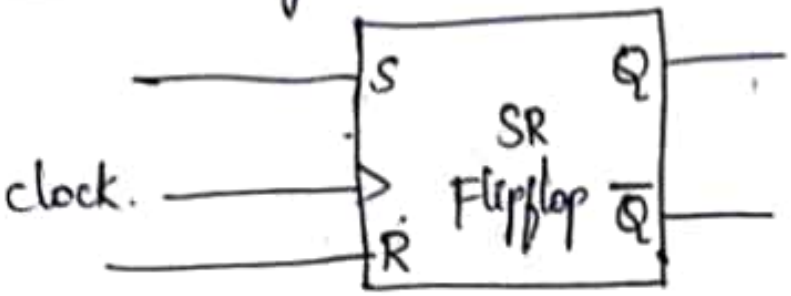
10 marks Questions :-

1. Explain the operation of clocked SR Flip-flop

1). SR Flipflop :-

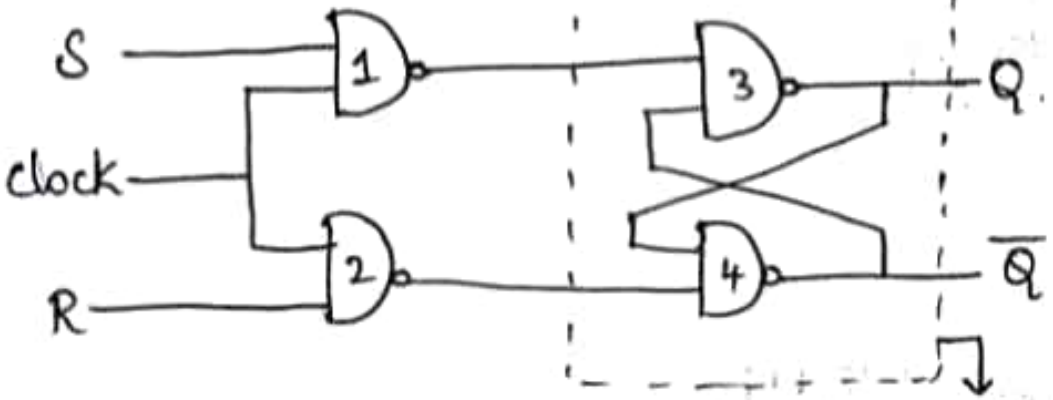
- The inputs are S and R. The outputs are Q and $\overline{Q}$.
- The flipflop is controlled by Positive edge triggered clock.
- The circuit output responds to the S and R inputs, only at the positive edge of the clock pulse.

* Block Diagram :-



Inputs = S, R
outputs = Q, $\overline{Q}$

* Circuit Diagram :-



SR Latch Using NAND gates

* Operation :

1). When clock Signal is not given :-

Since the clock signal is not present, the inputs to NAND gate 1 and NAND gate 2 are Logic 0. The outputs are Logic 1. The input to the SR Latch

using NAND gates are Logic 1. It results in "No change".

2). When clock signal is given :-

Case a): S=0, R=0, clock = ↑

The output of NAND gate 1 and NAND gate 2 are Logic 1. The inputs of SR latch are Logic 1. It results in "No change".

Case b): S=0, R=1, clock = ↑

The output of NAND gate 1 and NAND gate 2 are 1 and 0. The inputs of SR latch are 1 and 0. It results in "Reset".

Case c): S=1, R=0, clock = ↑

The output of NAND gate 1 and NAND gate 2 are 0 and 1. The inputs of SR latch are 0 and 1. It results in "Set".

Case d): S=1, R=1, clock = ↑

The output of NAND gate 1 and NAND gate 2 are 0 and 0. The inputs of SR latch are 0 and 0. It results in "Invalid State".

* Truth Table :

Clock	S	R	Q	$\overline{Q}$	State
0	x	x	1/0	0/1	No change
↑	0	0	1/0	0/1	No change
↑	0	1	0	1	Reset
↑	1	0	1	0	Set
↑	1	1	1	1	Invalid State

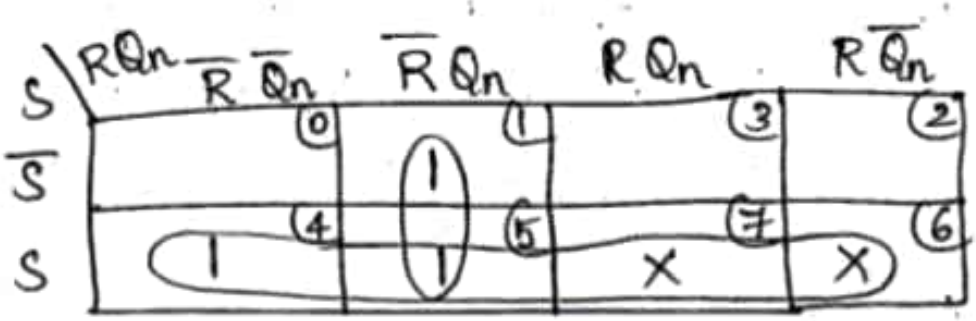
* Characteristic Table : Based on the external inputs i.e S and R and present state Q(n), we get the next state Q(n+1) which is specified in a table.

	External Inputs		Present state	Next state
	S	R	Q_n	Q_{n+1}
No change	0	0	0	0
	0	0	1	1 → 1
Reset	0	1	0	0
	0	1	1	0
Set	1	0	0	1 → 4
	1	0	1	1 → 5
Invalid	1	1	0	X → 6
	1	1	1	X → 7

* Characteristic Equation : It specifies the next state Q(n+1) interms of present state Q(n) and external inputs S and R.

$$Q_{n+1} = \sum m(1,4,5) + \sum d(6,7)$$

K-Map :



$$\boxed{Q_{n+1} = S + \bar{R} Q_n}$$

Result : Pairs = 1
Quad = 1

2. Explain the operation of universal shift Register with ane diagram.

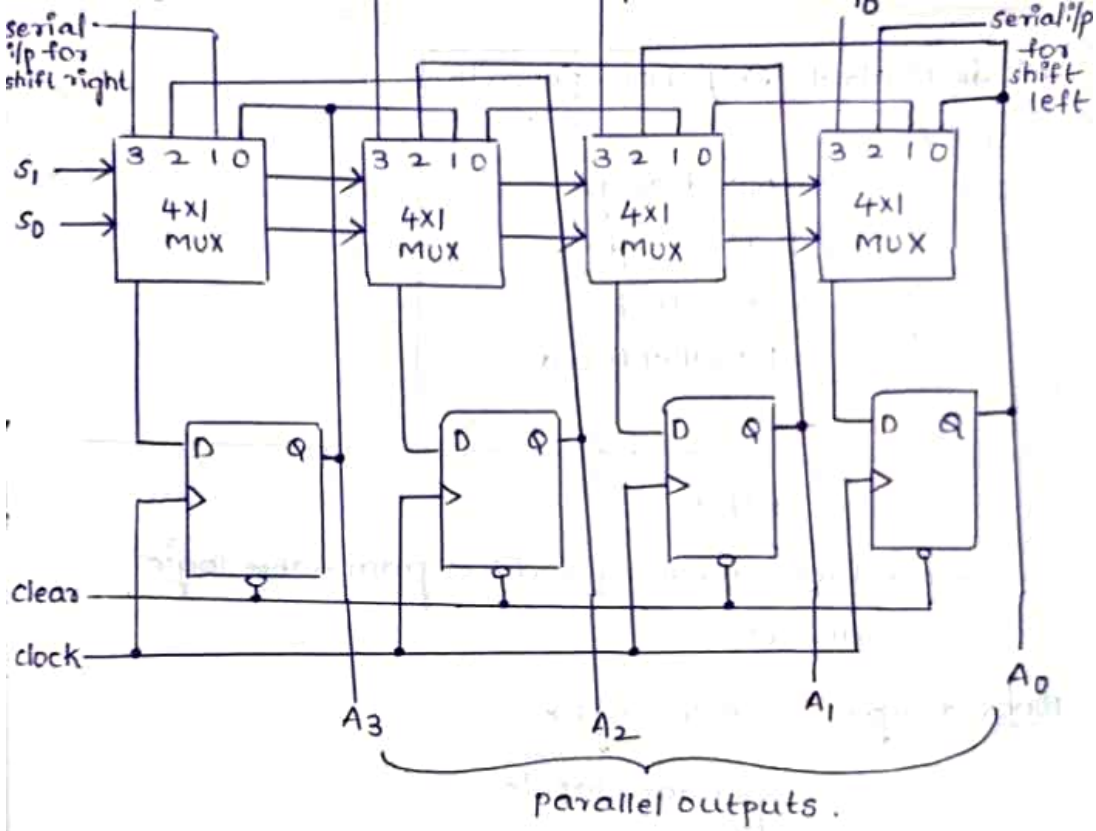
Ans: A Register capable of shifting in one direction only is a unidirectional shift register.

If the register is capable of shifting in both directions. then it is called a bidirectional shift register.

If the register has both shifts and parallel load capabil es it is referred to as universal shift register.

A universal shift register is a Bidirectional register, whc inputs can be either in serial form or in parallel for and whose output also can be either in serial or in pa llel form.

It consists of four flipflops and four multiplexers th four multiplexers have two common selection inputs S_1 So and they select appropriate input for D-flipflop.



→ When $S_1, S_0 = 00$, input '0' is selected and the present value of the register is applied to the d inputs of the flipflop. This results no change in the register value.

→ When $S_1 S_0 = 01$, the input '1' is selected and the circuit connections are such that it operates as a right shift register.

→ When $S_1 S_0 = 10$, the input '2' is selected and the circuit connections are such that it operates as a left shift register.

→ When $S_1 S_0 = 11$, the input '3' is selected the binary information on parallel input lines is transferred into the register simultaneously and it is a parallel load register.

Truthtable :→

Mode control		Register operation
S_1	S_0	
0	0	No change
0	1	shift right
1	0	Shift left
1	1	parallel load.

3. Design of a MOD-5 synchronous up counter using JK Flipflop. Draw the logic diagram.

Ans: Step 1:- Determine the no. of Flipflops.

The no. of flip flops are

$2^n \geq N$

Given $N = 5 \Rightarrow 2^n \geq 5$

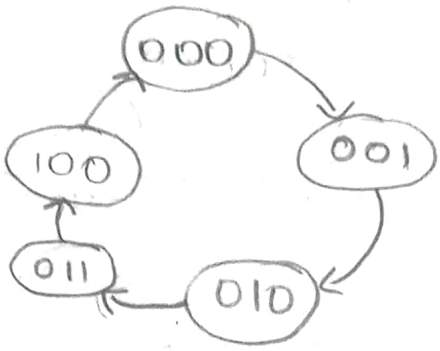
if $n = 3 \Rightarrow 2^3 \geq 5$

$\Rightarrow 8 \geq 5$

$\therefore$ 3 Flip-Flops are required.

step 2: The type of flipflop choosed in JK flipflop

State Diagram :-



step 3:- The Excitation table of JK flip-flop is

Q(n)	Q(n+1)	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

Determine the Excitation table for the Counter.

Present state			Next states			Flip Flop I/P's					
Q_A	Q_B	Q_C	Q_{A+1}	Q_{B+1}	Q_{C+1}	JA	KA	JB	KB	JC	KC
0	0	0	0	0	1	0	x	0	x	1	x
0	0	1	0	1	0	0	x	1	x	x	1
0	1	0	0	1	1	0	x	x	0	1	x
0	1	1	1	0	0	1	x	x	1	x	1
1	0	0	0	0	0	x	1	0	x	0	x
1	0	1	x	x	x	x	x	x	x	x	x
1	1	0	x	x	x	x	x	x	x	x	x
1	1	1	x	x	x	x	x	x	x	x	x

step 4:-

K-map :-

$JA = \Sigma m(3) + \Sigma d(4,5,6,7)$

$KA = \Sigma m(4) + \Sigma d(0,1,2,3,5,6,7)$

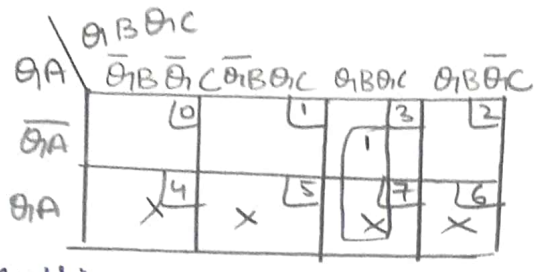
$JB = \Sigma m(1) + \Sigma d(2,3,5,6,7)$

$KB = \Sigma m(3) + \Sigma d(0,1,4,5,6,7)$

$JC = \Sigma m(0,2) + \Sigma d(1,3,5,6,7)$

$KC = \Sigma m(1,3) + \Sigma d(0,2,4,5,6,7)$

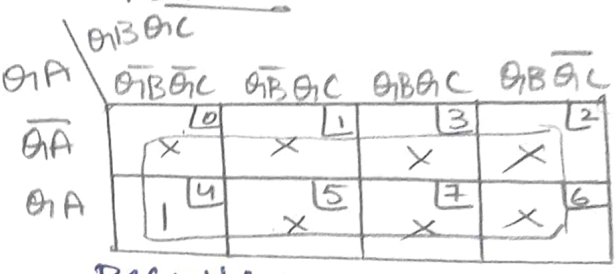
K-map simplification :- FOR JA :-



Result :-
Pair : 1
Equ : $Q_1B\,\overline{Q_1C}$

$\boxed{JA = Q_1B\,\overline{Q_1C}}$

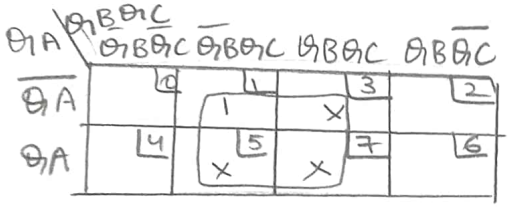
FOR KA :-



Result :-
Octet :- 1
Equ :- 1

$\boxed{KA = 1}$

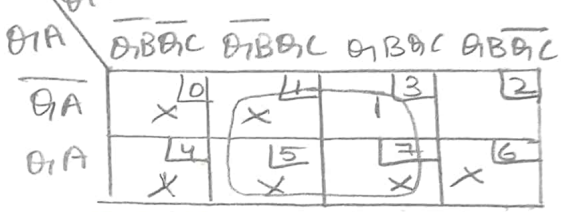
FOR JB :-



Result :-
Quad : 1
Equ :- Q_1C

$\boxed{JB = Q_1C}$

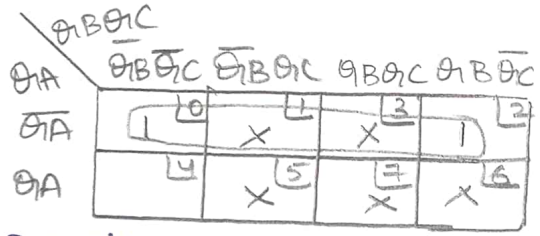
FOR KB :-



Result :-
Quad : 1
Equ :- Q_1C

$\boxed{KB = Q_1C}$

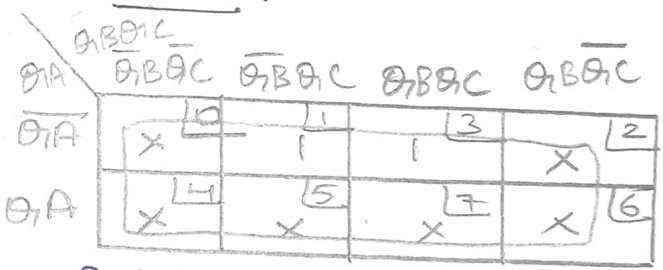
FOR JC :-



Result :-
Quad : 1
Equ :- $\overline{Q_1A}$

$\therefore JC = \overline{Q_1A}$

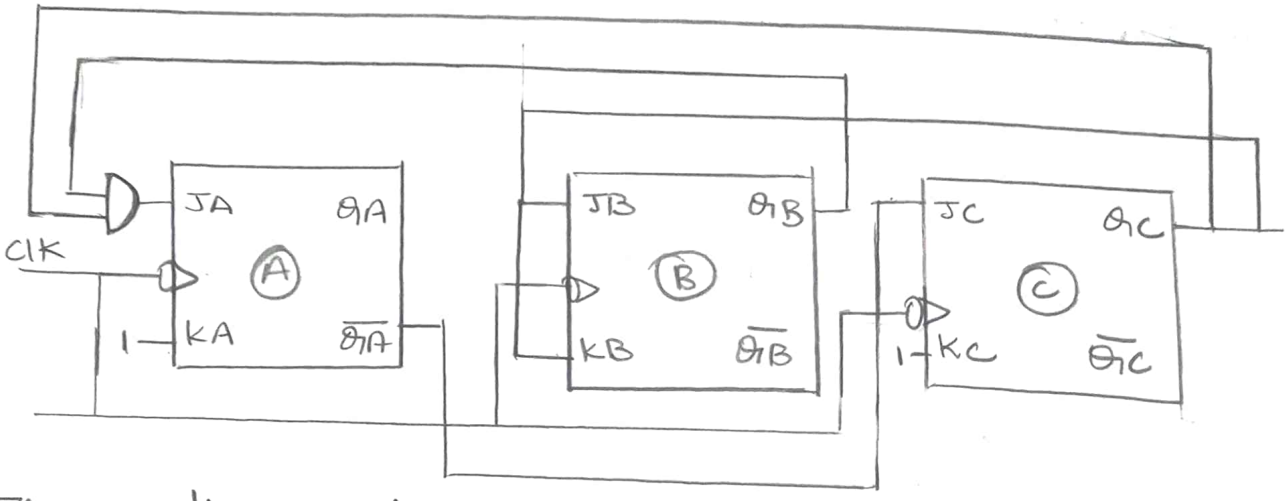
FOR KC :-



Result :-
Octet : 1
Equ :- 1

$\therefore KC = 1$

Logic diagram:-



Timing diagram:-