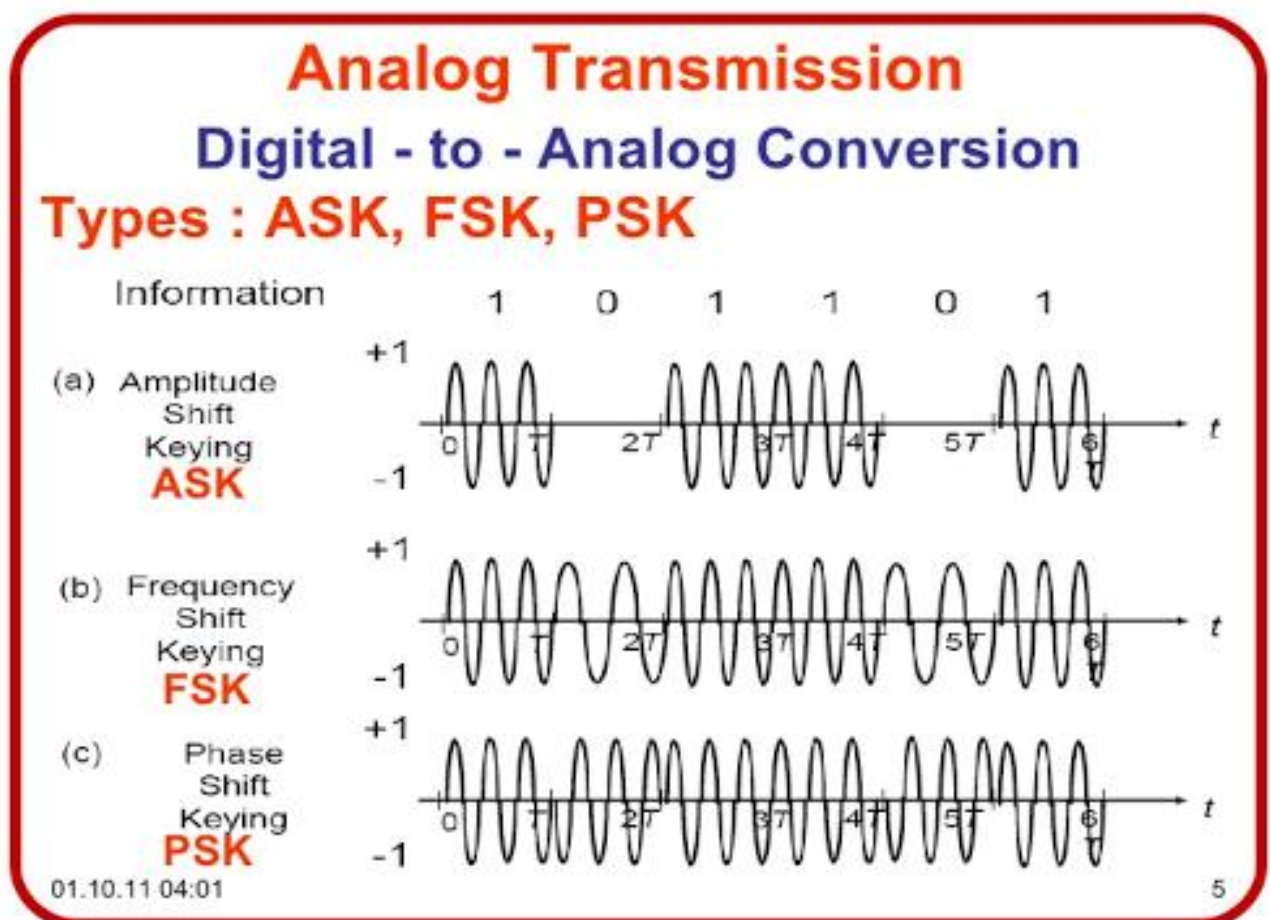


## DIGITAL MODULATION TECHNIQUES

In passband data transmission, the digital data modulates high frequency sinusoidal carrier. Hence they are called digital CW modulation techniques. These techniques are suitable for transmission over long distances.

The digital data can modulate the phase, frequency or amplitude of the carrier signal. This gives rise to three basic techniques.

- 1) Amplitude Shift keying(ASK) : In this technique, the digital data modulates the amplitude of the carrier.
- 2) Frequency Shift keying(FSK) : In this technique, the digital data modulates the frequency of the carrier.
- 3) Phase Shift keying(PSK) : In this technique, the digital data modulates the phase of the carrier.



### **Types of Reception of Passband Transmission:**

There are two types of methods for detection of passband signals.

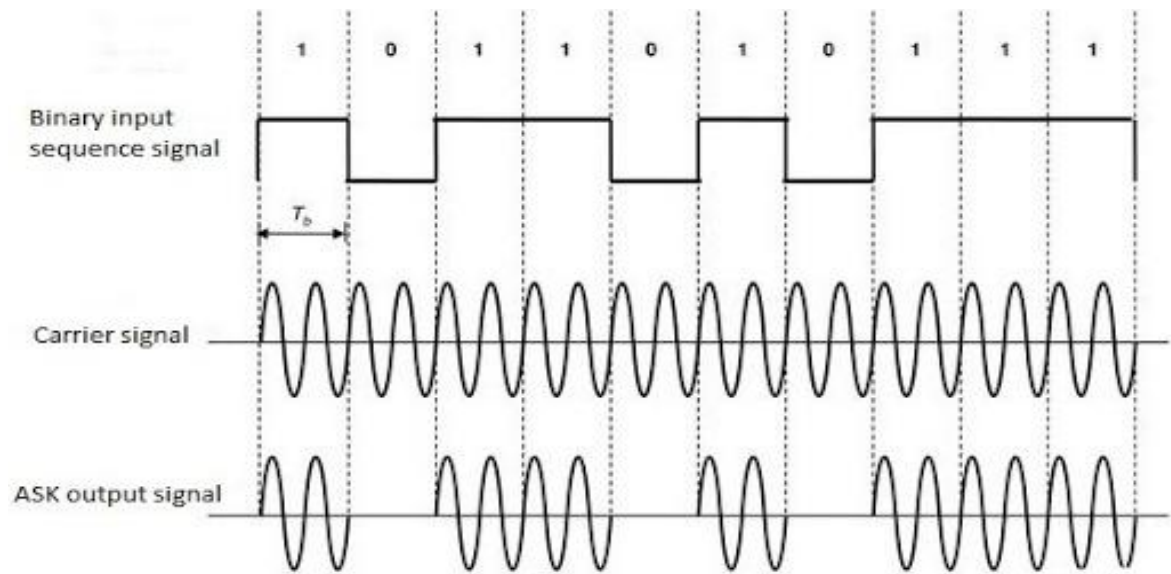
1. Coherent (Synchronous ) detection: In this method, the local carrier generated at the receiver is phase locked with the carrier at the transmitter. Hence it is also called synchronous detection.
2. Non Coherent (Envelope ) detection: In this method, the receiver carrier need not be phase locked with the transmitter carrier. Hence it is also called envelope detection. This detection is simple but it has higher probability of error.

### **AMPLITUDE SHIFT KEYING(ASK)**

In digital communication, different modulation techniques are used to transmit data or message to receiver over a communication channel . One such technique is Amplitude Shift Keying (ASK). It is a modulation technique that alters the amplitude of a carrier signal to transmit the information over channel. It is a modulation scheme having wide range of application in real world which includes radio, television, and digital data transmission.

Amplitude Shift Keying (ASK) is a type of Amplitude Modulation which represents the binary data in the form of variations in the amplitude of the carrier signal.

Following is the diagram for ASK modulated waveform along with its input.



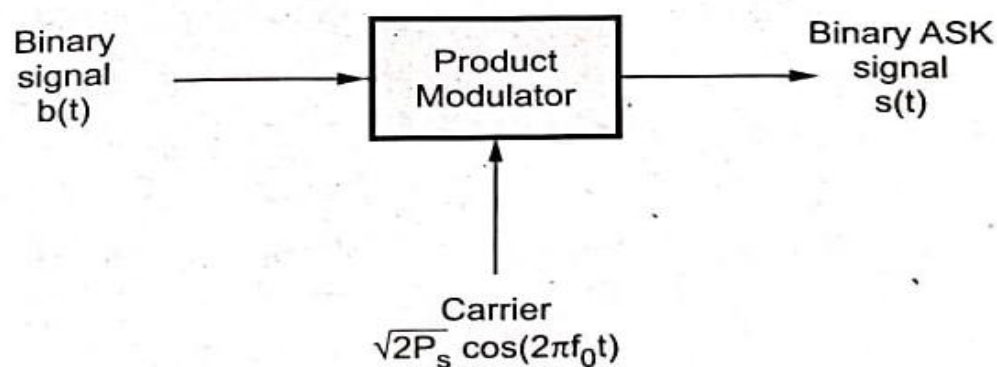
The ASK waveform can be represented as

$$s(t) = \sqrt{2P_s} \cos(2\pi f_0 t) \quad (\text{To transmit '1'})$$

$$= 0 \quad (\text{To transmit '0'})$$

### ASK GENERATION

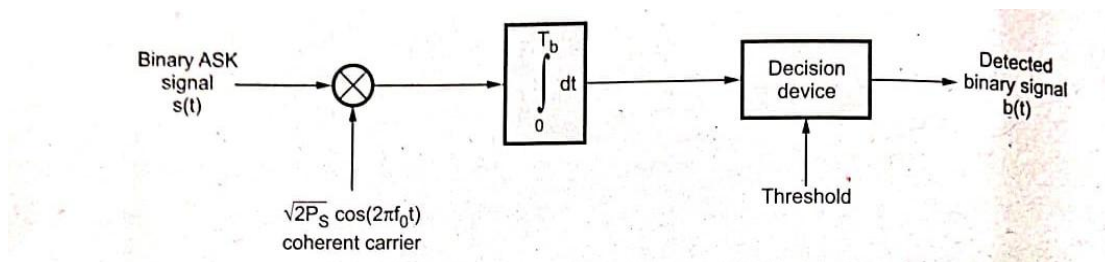
The ASK generator is shown in fig below:



The input binary sequence signal is applied to the product modulator. The product modulator amplitude modulates the sinusoidal carrier. It passes the carrier when input bit is '1'. It blocks the carrier (i.e. zero output) when input bit is '0'.

### ASK DETECTOR

The block diagram of Coherent ASK Detector is shown in fig below:

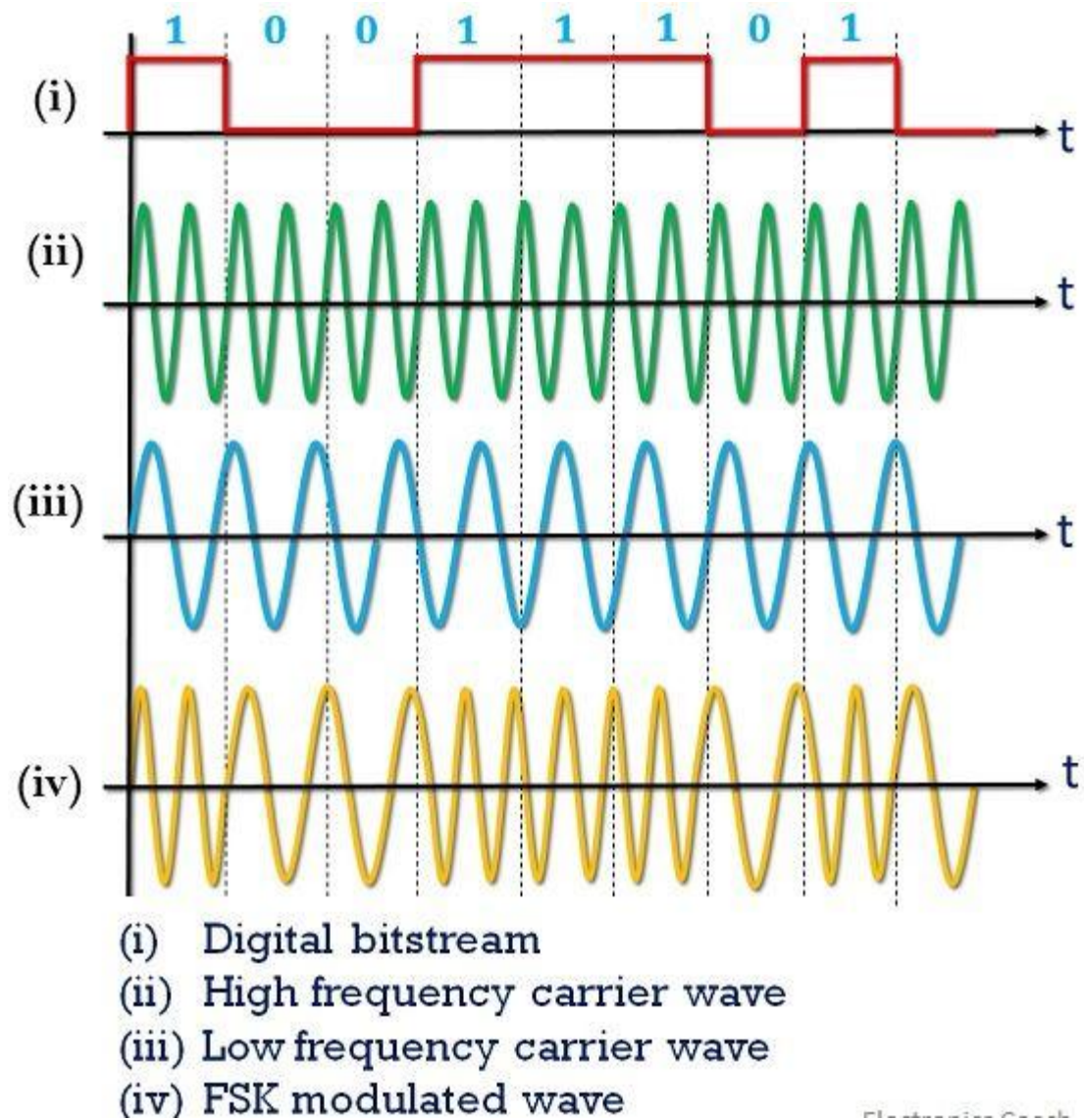


The ASK signal is applied to the correlator consisting of multiplier and an integrator. The locally generated coherent carrier is applied to the multiplier. The output of multiplier is integrated one bit period. The decision device takes the decision at the end of every bit period. It compares the output of integrator with the threshold. Decision is taken in favour of '1' when threshold is exceeded. Decision is taken as '0' if threshold is not exceeded.

### **BINARY FREQUENCY SHIFT KEYING**

The frequency of the output signal will be either high or low, depending upon the input data applied.

Frequency Shift Keying (FSK) is the digital modulation technique in which the frequency of the carrier signal varies according to the discrete digital changes. FSK is a scheme of frequency modulation.



If  $b(t)=1$ ,  $s_H(t)=\sqrt{2P_S}\cos(2\Pi f_0 + \Omega)t$

If  $b(t)=0$ ,  $s_L(t)=\sqrt{2P_S}\cos(2\Pi f_0 - \Omega)t$

Thus there is increase or decrease in frequency by  $\Omega$ . Let us use the following conversion table to combine above two FSK equations.

$b(t)$ Input	$d(t)$	$P_H(t)$	$P_L(t)$
1	+1 V	+1 V	0 V
0	-1 V	0 V	+1 V

Thus, we can write the above two equations combinely as

$$s(t) = \sqrt{2P_s} \cos(2\pi f_0 + d(t)\Omega)t$$

When symbol '1' is to be transmitted, the carrier frequency will be

$$f_0 + \frac{\Omega}{2\pi}$$

When symbol '0' is to be transmitted, the carrier frequency will be

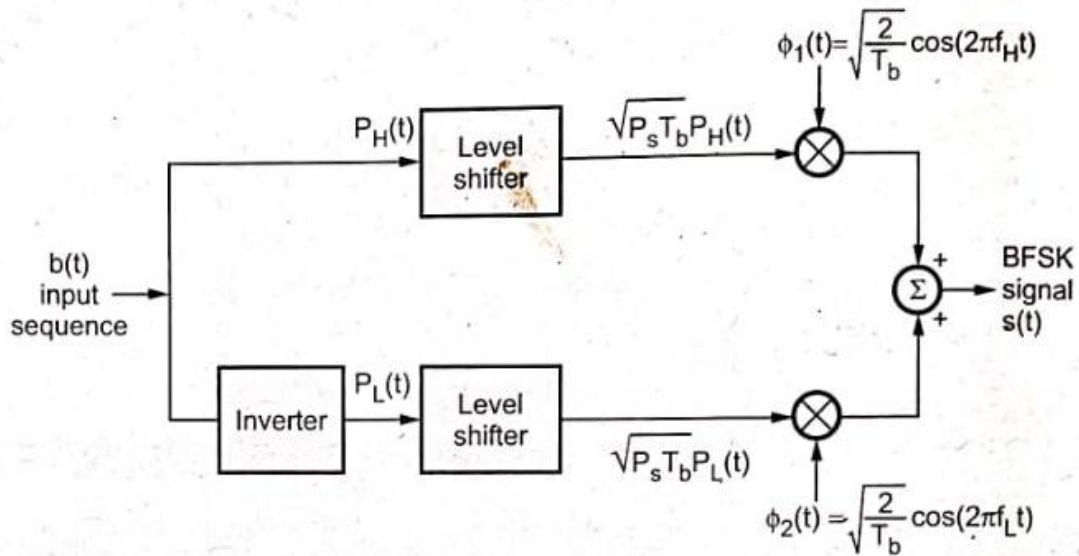
$$f_0 - \frac{\Omega}{2\pi}$$

$$f_H = f_0 + \frac{\Omega}{2\pi} \quad \text{for symbol '1'}$$

$$f_L = f_0 - \frac{\Omega}{2\pi} \quad \text{for symbol '0'}$$

### **BFSK TRANSMITTER**

From the table we observe that  $P_H(t)$  is same as  $b(t)$  and  $P_L(t)$  is the inverted version of  $b(t)$ . The block diagram of FSK Transmitter is shown below

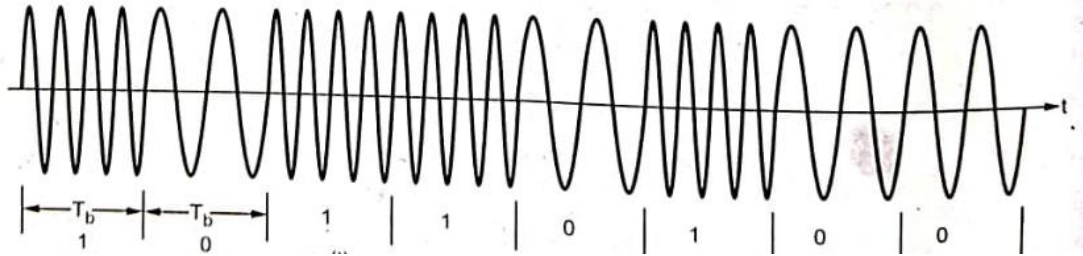


We know that input sequence  $b(t)$  is same as  $P_H(t)$ . An inverter is added after  $b(t)$  to get  $P_L(t)$ .  $P_H(t)$  and  $P_L(t)$  are unipolar signals. The level shifter converts the '+1' level to  $\sqrt{P_s T_b}$ . Zero level is unaffected. Thus the output of the level shifters will be either  $\sqrt{P_s T_b}$  (if '+1') or zero (if input is zero). Further there are product modulators after level shifter. The two



carrier signals  $\Phi_1(t)$  and  $\Phi_2(t)$  are used. In one bit period of input signal (i.e.  $T_b$ ),  $\Phi_1(t)$  or  $\Phi_2(t)$  have integral number of cycles.

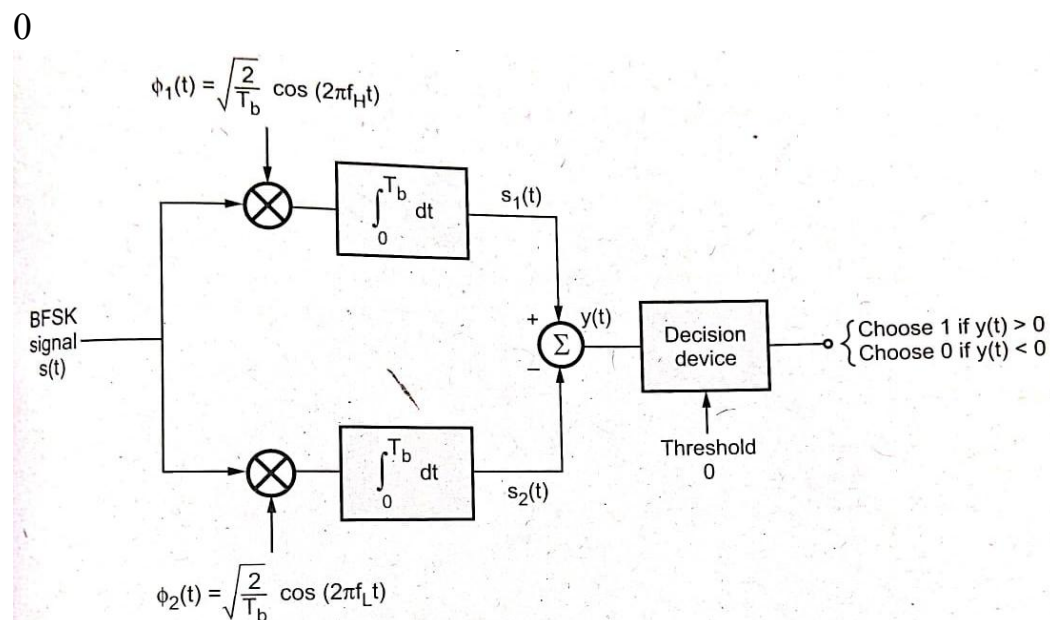
Therefore the modulated signal has continuous phase. Such BFSK signal is shown in Fig. 6.7.2. The adder then adds the two signals.



Here note that outputs from both the multipliers are not possible at a time. This is because  $P_H(t)$  and  $P_L(t)$  are complementary to each other. Therefore if  $P_H(t) = 1$ , then output will be only due to upper modulator and lower modulator output will be zero (since  $P_L(t) = 0$ ).

### **BFSK RECEIVER**

The following shows the block diagram of coherent BFSK receiver.



There are two correlators for two frequencies of FSK signal. These correlators are supplied with locally generated carriers  $\Phi_1(t)$  and  $\Phi_2(t)$ . If the transmitted frequency is  $f_H$ , then output  $s_1(t)$  will be higher than  $s_2(t)$ . Hence  $y(t)$  will be greater than zero. The decision device then decides in

favour of binary '1'. If  $s_2(t) > s_1(t)$  then  $y(t) < 0$  and decision device decides in favour of '0'.

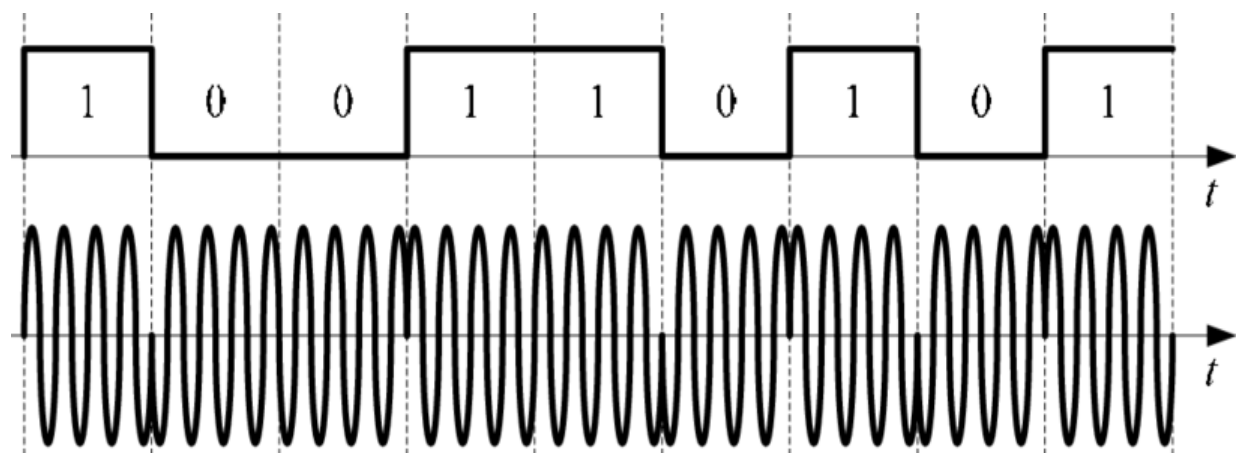
Bandwidth of FSK signal =  $4f_b$  Hz

### **BINARY PHASE SHIFT KEYING**

Binary Phase Shift Keying (BPSK) is a modulation technique employed in communication systems to transmit information via a communication channel. In BPSK the carrier signal is modified by altering its phase by 180 degrees, for each symbol. A phase shift of 180 degrees denotes a binary 0 while no phase shift represents a binary 1. The BPSK modulation process is straightforward and efficient making it suitable for scenarios where the communication channel suffers from noise and interference.

In BPSK the modulation process involves using a sinusoid as the basis function. By adjusting the phase of this sinusoid based on the message bits we can achieve modulation. When transmitting a 1 there is no phase shift, in the carrier signal. However, when transmitting a 0 there is a phase shift of 180 degrees in the carrier signal. This straightforward modulation scheme enables the transmission of data.

#### **BPSK Waveform:**





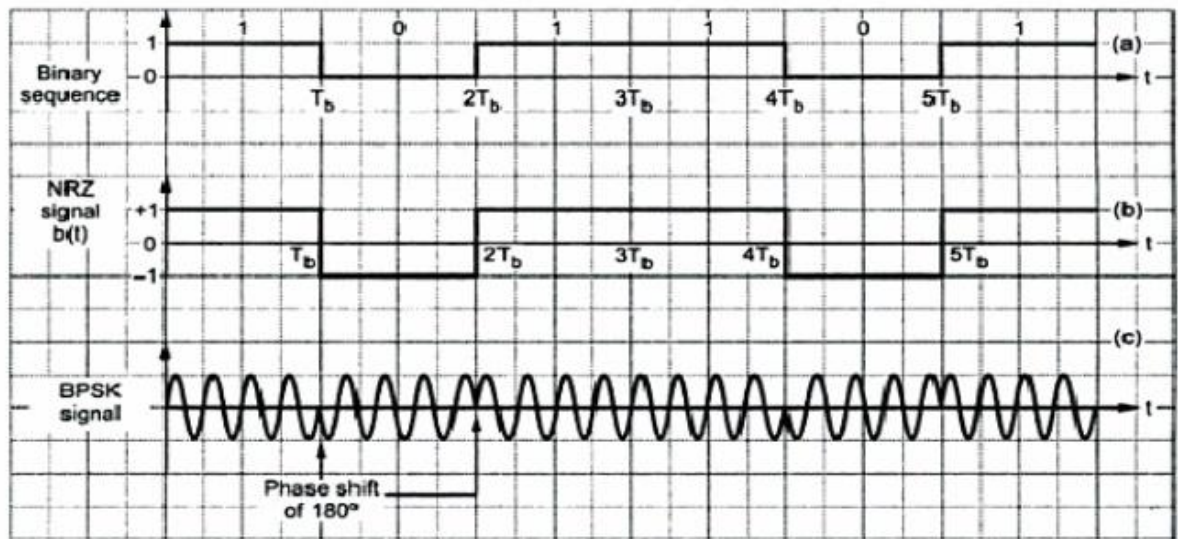


Fig. 4.2.1 (a) Binary sequence  
 (b) Its equivalent bipolar signal  $b(t)$   
 (c) BPSK signal

## BPSK Transmitter and Receiver

**BPSK Transmitter:**

## Binary Phase Shift Keying (BPSK)

### Transmitter

In Binary Phase Shift Keying (BPSK), binary symbol '1' and '0' modulate the phase of the carrier.

Let the carrier be

$c(t) = A \cos(2\pi f_c t)$  where 'A' represents the peak value of sinusoidal carrier.

In the standard  $1\Omega$  load resistor, the power dissipated will be,

$$P = \frac{A^2}{2R_L} = \frac{A^2}{2(1)} \quad (\because R_L = 1\Omega)$$

$$\Rightarrow P = \frac{A^2}{2} \Rightarrow A = \sqrt{2P}$$

If bit '1' is to be transmitted then modulated signal is,

$$s(t) = c(t) = A \cos(2\pi f_c t) = \sqrt{2P} \cos(2\pi f_c t)$$

If bit '0' is to be transmitted then the modulated signal is carrier wave which is shifted by  $180^\circ$  i.e.,

$$s(t) = \sqrt{2P} \cos(2\pi f_c t + 180^\circ) = -\sqrt{2P} \cos(2\pi f_c t)$$

We can define the BPSK signal combinely as

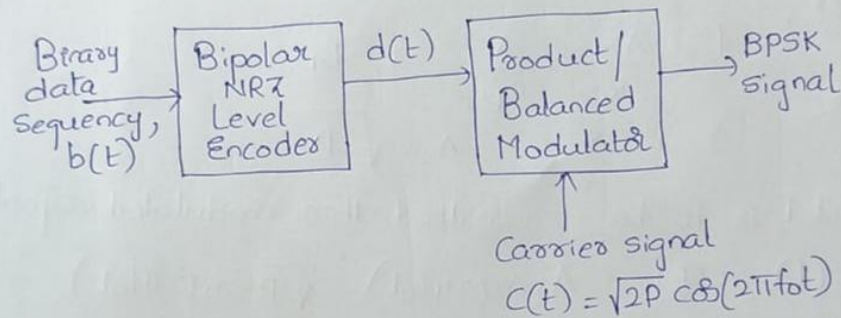
$$\begin{aligned} s(t) &= \pm \sqrt{2P} \cos(2\pi f_c t) \\ &= d(t) \sqrt{2P} \cos(2\pi f_c t) \end{aligned}$$

Here  $d(t) = +1$  when binary '1' is to be transmitted  
 $= -1$  when binary '0' is to be transmitted

The BPSK transmitter comprises of Non Return to Zero (NRZ) level encoder and a product modulator.

The level encoder turns these binary bits into bipolar signals, with '1' represented as +1 and '0' as -1.

as '-1'. This conversion is required for phase modulation. The encoded signal is then supplied to the product modulator. The product modulator multiplies the encoded binary signal with a high frequency carrier signal,  $c(t)$ . Depending upon <sup>the bit number</sup> the phase of carrier maintains  $0^\circ$  & changes to  $180^\circ$  resulting in the BPSK waveform.

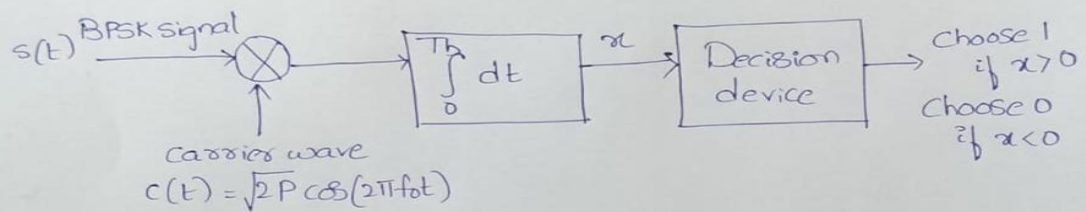


## BPSK Receiver

### BPSK Receiver

The BPSK Receiver recovers the original binary data from the received BPSK signal. The first block which is a multiplier, multiplies the incoming BPSK signal with a locally generated carrier signal that is identical to the one used by the transmitter. The result is then fed to an integrator, which integrates the signal over one bit time and obtains a voltage level that is either positive or negative, depending on whether the received

phase was  $0^\circ$  &  $180^\circ$ . This goes into a decision making device which compares the output to a predefined threshold (typically zero). If the value is larger than zero, it is detected as bit '1', otherwise, it is detected as bit '0'. Thus the original binary data is retrieved.



## QUADRATURE PHASE SHIFT KEYING(QPSK)

**Bit rate** referred as number of bits transmitted per second. It is stored in the memory in one and zero format. Symbol is used to map more than one bits and are used to transmit bits over channel after baseband and carrier modulation. **Symbol rate** is referred as number of symbols transmitted per second. It is also known by "**Baud rate**". The modulated data after modulation is measured in symbols per sec.

In communication systems we know that there are two main resources, i.e. transmission power and the channel bandwidth. The channel bandwidth depends upon the bit rate or signalling rate  $f_b$ . In digital bandpass transmission, a carrier is used for transmission. This carrier is transmitted over a channel.

If two or more bits are combined in some symbols, then the signalling rate is reduced. Therefore the frequency of the carrier required is also reduced. This reduces the transmission channel bandwidth. Thus because of grouping of bits in symbols, the transmission channel bandwidth is reduced.

In quadrature phase shift keying, two successive bits in the data sequence are grouped together. This reduces the bits rate or signalling rate ( $f_b$ ) and hence reduces the bandwidth of the channel. In BPSK we know that when symbol changes the level, the phase of the carrier is changed by  $180^\circ$ .



Since there were only two symbols in BPSK, the phase shift occurs in two levels only.

In QPSK two successive bits are combined. This combination of two bits forms four distinct symbols. When the symbol is changed to next symbol the phase of the carrier is changed by  $90^\circ$  ( $\pi/2$  radians). The following table shows these symbols and their phase shifts.

Sr. No.	Input successive bits		Symbol	Phase shift in carrier
$i = 1$	1 (1 V)	0 (-1 V)	$S_1$	$\pi/4$
$i = 2$	0 (-1 V)	0 (-1 V)	$S_2$	$3\pi/4$
$i = 3$	0 (-1 V)	1 (1 V)	$S_3$	$5\pi/4$
$i = 4$	1 (1 V)	1 (1 V)	$S_4$	$7\pi/4$

Thus as shown in above table, there are 4 symbols and the phase is shifted by  $\pi/2$  for each symbol.

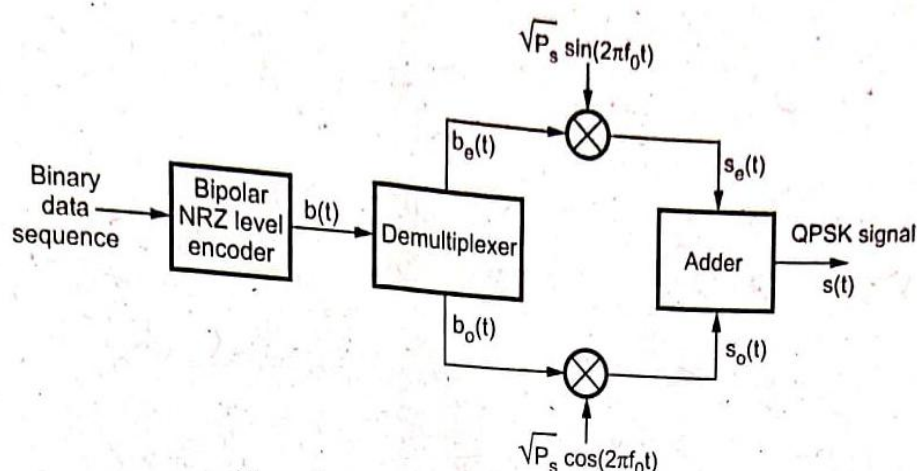
## QPSK TRANSMITTER AND RECEIVER

### Offset QPSK or Staggered QPSK Transmitter

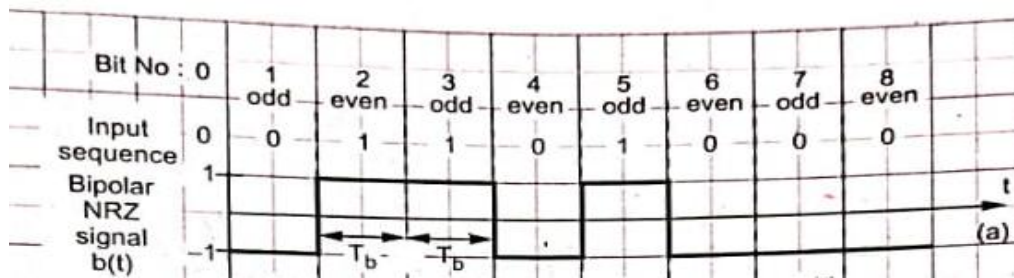
#### Operation and Waveforms

#### Step 1: Input Sequence Converted to NRZ type:

The following figure shows the block diagram of OQPSK transmitter.

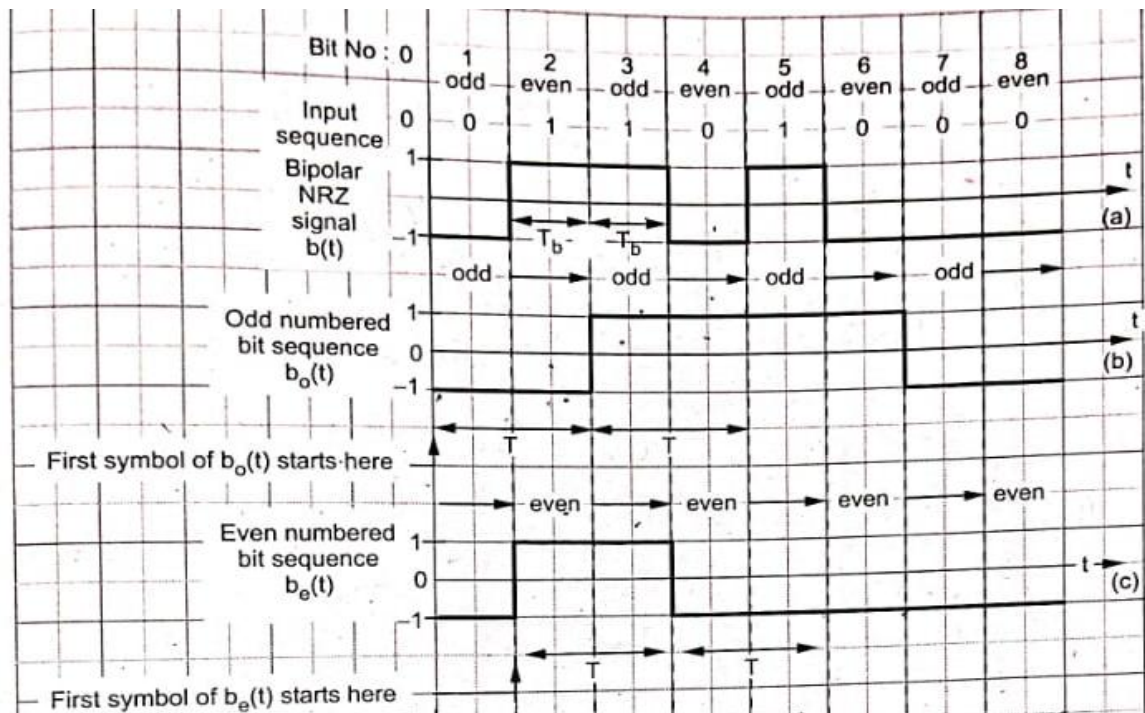


The input binary sequence is first converted to a bipolar NRZ type of signal. This signal is called  $b(t)$ . It represents binary '1' by +1 V and binary '0' by -1 V. This signal is shown in Fig below



## Step 2: Demultiplexing into odd and even numbered sequences

The demultiplexer divides  $b(t)$  into two separate bit streams of the odd numbered and even numbered bits.  $b_e(t)$  represents even numbered sequence and  $b_o(t)$  represents odd numbered sequence. The symbol duration of both of these odd and even numbered sequences is  $2T_b$ . Thus every symbol contains two bits. Fig (b) and (c) shows the waveforms of  $b_e(t)$  and  $b_o(t)$

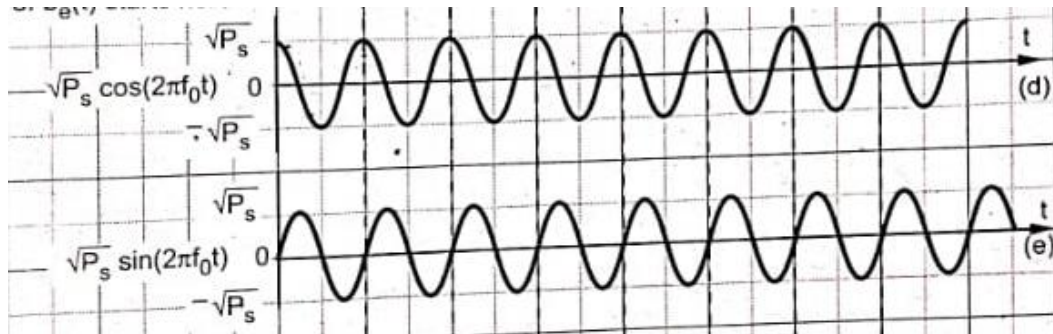


Observe that the first even bit occurs after the first odd bit. Therefore even numbered bit sequence  $b_e(t)$  starts with the delay of one bit period due to first odd bit. Thus first symbol of  $b_e(t)$  is delayed by one bit period ' $T_b$ ' with respect to first symbol of  $b_o(t)$ . This delay of  $T_b$  is called offset. Hence the name offset QPSK is given. This shows that the change in levels of  $b_e(t)$  and  $b_o(t)$  cannot occur at the same time because of offset or staggering.

## Step 3: Modulation of quadrature carriers



The bit stream  $b_0(t)$  modulates the carrier  $\sqrt{P_s}\cos(2\pi f_0 t)$  and  $b_e(t)$  modulates  $\sqrt{P_s}\sin(2\pi f_0 t)$ . These modulators are balanced modulators. The two carriers  $\sqrt{P_s}\cos(2\pi f_0 t)$  and  $\sqrt{P_s}\sin(2\pi f_0 t)$  are shown in fig (d) and (e)



These carriers are also called quadrature carriers. The two modulated signals are

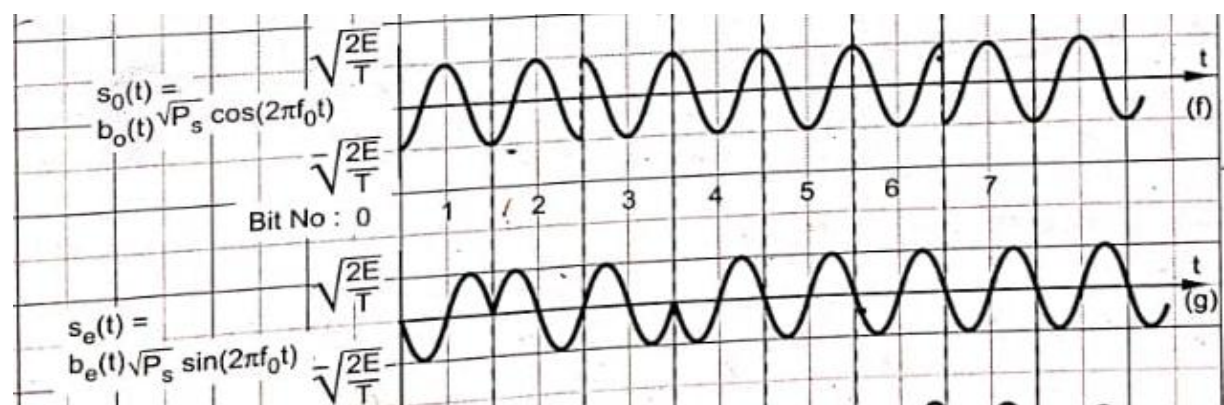
$$s_e(t) = b_e(t) \sqrt{P_s} \sin(2\pi f_0 t)$$

$$s_o(t) = b_o(t) \sqrt{P_s} \cos(2\pi f_0 t)$$

The value of  $b_e(t)$  and  $b_o(t)$  will be +1 V or -1 V. Fig (f) and (g) shows the waveforms of  $s_e(t)$  and  $s_o(t)$ .

$$s_e(t) = b_e(t) \sqrt{P_s} \sin(2\pi f_0 t)$$

$$s_o(t) = b_o(t) \sqrt{P_s} \cos(2\pi f_0 t)$$



a

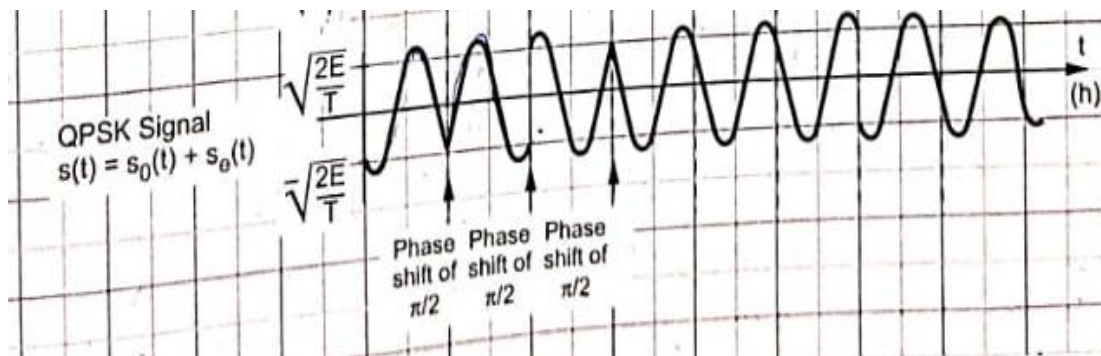
#### Step 4: Addition of modulated carriers

The adder then adds these two signals  $s_e(t)$  and  $s_o(t)$ . The output of the adder is QPSK signal which is shown below and it is given as,

$$s(t) = s_o(t) + s_e(t)$$

$$= b_o(t)\sqrt{P_s}\cos(2\pi f_0 t) + b_e(t)\sqrt{P_s}\sin(2\pi f_0 t)$$

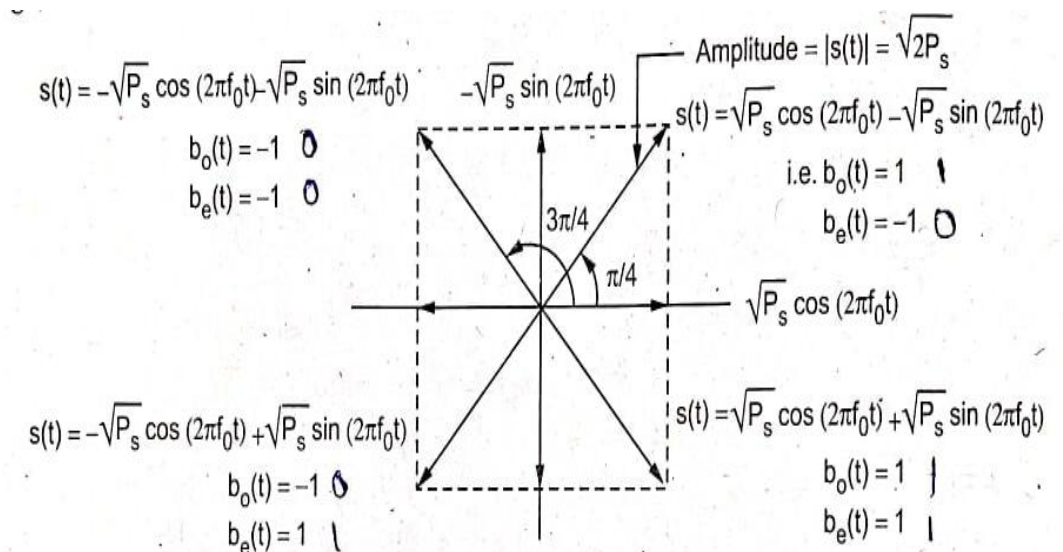
### Step 5: QPSK signal and phase shift



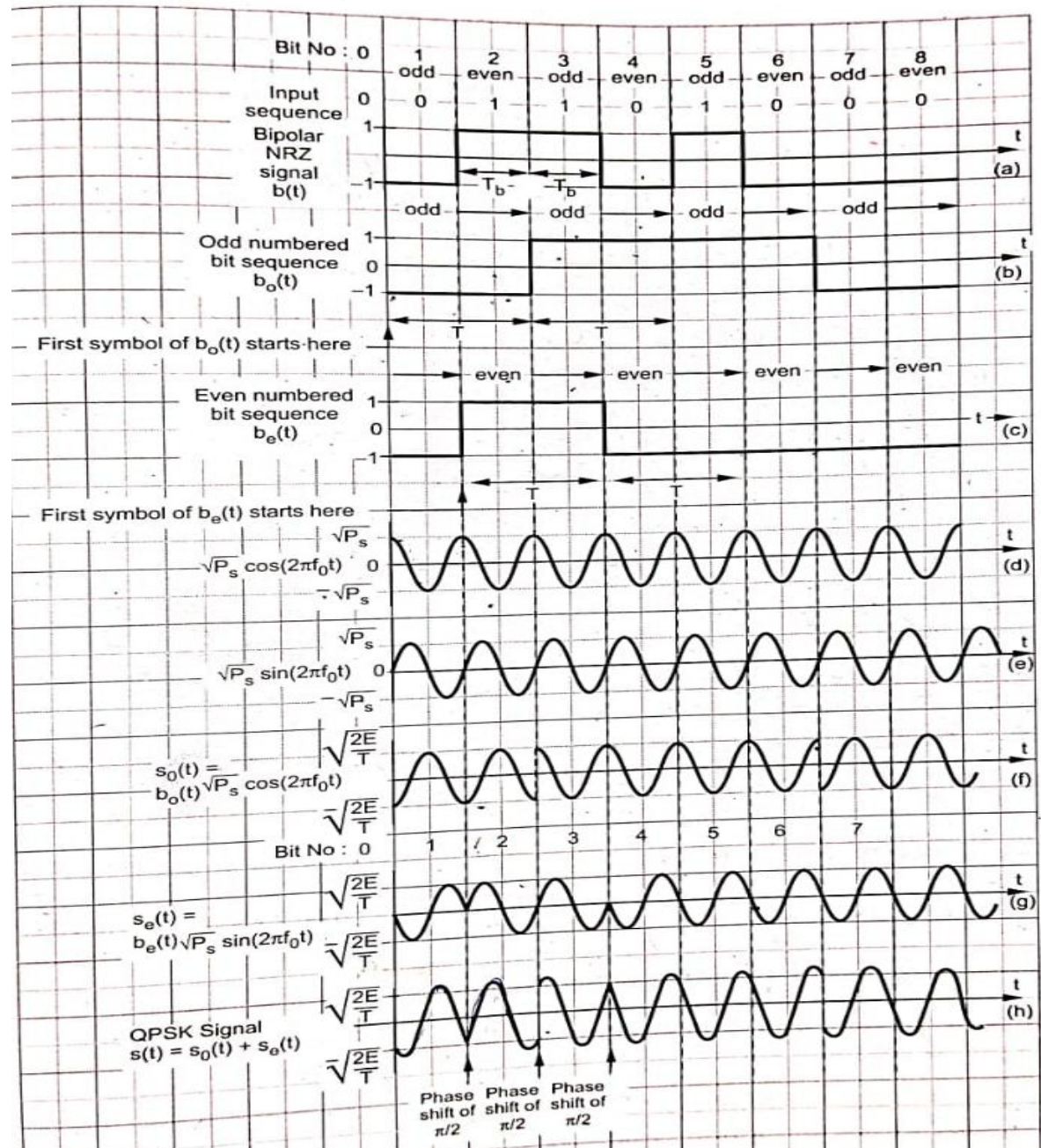
shows the QPSK signal represented by above equation.

In QPSK signal of Fig. (h), if there is any phase change, it occurs at minimum duration of  $T$ . This is because the two signals  $s_e(t)$  and  $s_o(t)$  have an offset of ' $T_b$ '. Because of this offset, the phase shift in QPSK is  $\frac{\pi}{2}$

It is clear from the waveforms that  $b_e(t)$  and  $b_o(t)$  cannot change at the same time because of offset between them. The following fig shows the phasor diagram of QPSK signal of equation  $s(t)$ .



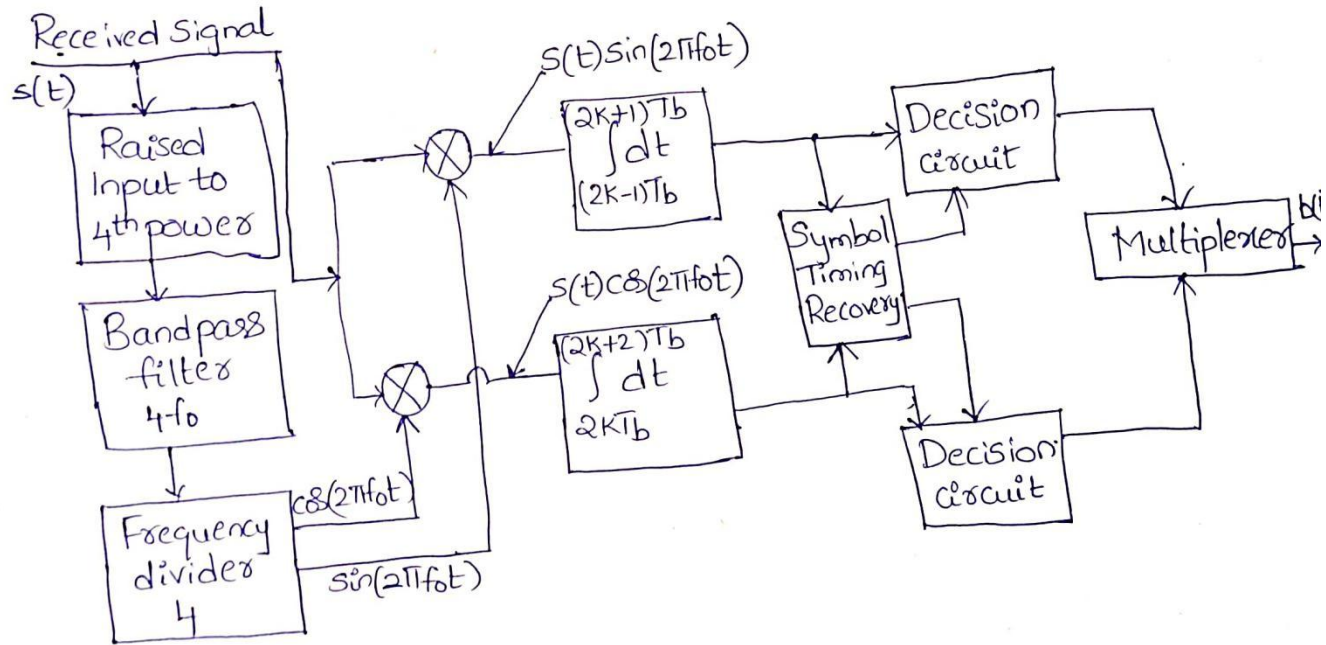
Since  $b_o(t)$  and  $b_e(t)$  cannot change at the same time, the phase change in QPSK signal will be maximum  $\pi/2$ .



## QPSK RECEIVER

The following figure shows the QPSK receiver





### Step 1: Isolation of carrier

The received signal  $s(t)$  is first raised to its 4th power, i.e.  $s^4(t)$ . Then it is passed through a bandpass filter centered around  $4f_0$ . The output of the bandpass filter is a coherent carrier of frequency  $4f_0$ . This is divided by 4 and it gives two coherent quadrature carriers  $\cos(2\pi f_0 t)$  and  $\sin(2\pi f_0 t)$ :

### Step 2: Synchronous detection

These coherent carriers are applied to two synchronous demodulators. These synchronous demodulators consist of multiplier and an integrator.

### Step 3: Integration over two bits interval

The incoming signal is applied to both the multipliers. The integrator integrates the product signal over two bit interval (i.e.  $T_s = 2T_b$ ).

### Step 4: Detection and multiplexing the odd and even bit sequences

The symbol timing recovery circuit recover the clock at the symbol rate or a multiple of symbol rate from the integrated output signal. This clock is required to convert the continuous time received signal into a discrete time sequence of data symbols. At the end of the clock period  $T_s$ , the output value of integrator is taken (sampled). The output values of the two integrators are taken (sampled) at the offset of one bit period  $T_b$ . The decision device detects the bit as bit '1' if the output value exceeds the

decision threshold else the bit is detected as bit '0'. After detection the odd and even sequences are combined by the multiplexer.

### To show the output of integrator depends upon respective bit sequence

Let us consider the product signal at the output of upper multiplier

Let's consider the product signal at the output of upper multiplier.

$$s(t) \sin(2\pi f_0 t) = b_o(t) \sqrt{P_s} \cos(2\pi f_0 t) \sin(2\pi f_0 t) + b_e(t) \sqrt{P_s} \sin^2(2\pi f_0 t)$$

This signal is integrated by the upper integrator in Fig. 6.5.4.

$$\begin{aligned} \therefore \int_{(2k-1)T_b}^{(2k+1)T_b} s(t) \sin(2\pi f_0 t) dt &= b_o(t) \sqrt{P_s} \int_{(2k-1)T_b}^{(2k+1)T_b} \cos(2\pi f_0 t) \sin(2\pi f_0 t) dt \\ &\quad + b_e(t) \sqrt{P_s} \int_{(2k-1)T_b}^{(2k+1)T_b} \sin^2(2\pi f_0 t) dt \end{aligned}$$

Since  $\frac{1}{2} \sin(2x) = \sin x \cdot \cos x$

and  $\sin^2(x) = \frac{1}{2} [1 - \cos(2x)]$

Using the above two trigonometric identities in the above equation,

$$\begin{aligned} \int_{(2k-1)T_b}^{(2k+1)T_b} s(t) \sin(2\pi f_0 t) dt &= \frac{b_o(t) \sqrt{P_s}}{2} \int_{(2k-1)T_b}^{(2k+1)T_b} \sin 4\pi f_0 t dt + \frac{b_e(t) \sqrt{P_s}}{2} \int_{(2k-1)T_b}^{(2k+1)T_b} 1 \cdot \\ &\quad - \frac{b_e(t) \sqrt{P_s}}{2} \int_{(2k-1)T_b}^{(2k+1)T_b} \cos 4\pi f_0 t dt \end{aligned}$$

In the above equation, the first and third integration terms involves integral sinusoidal carriers over two bit period. They have full (integral number of) cycle two bit period and hence integration will be zero.

$$\begin{aligned} \int_{(2k-1)T_b}^{(2k+1)T_b} s(t) \sin(2\pi f_0 t) dt &= \frac{b_e(t) \sqrt{P_s}}{2} [t]_{(2k-1)T_b}^{(2k+1)T_b} = \frac{b_e(t) \sqrt{P_s}}{2} \times 2T_b \\ &= b_e(t) \sqrt{P_s} T_b \end{aligned}$$

Thus the upper integrator responds to even sequence only. Similarly we can obtain the output of lower integrator as  $b_o(t) \sqrt{P_s} T_b$