1 mark

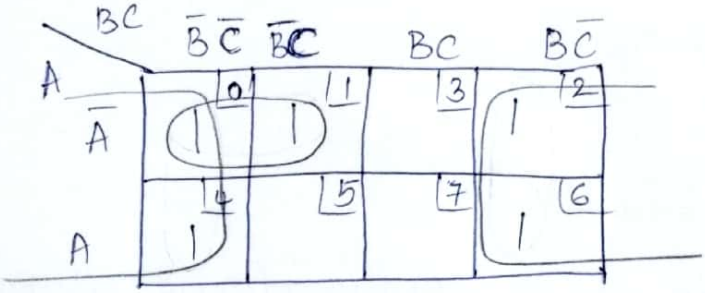
1) (a) Minterm :- It is a product term in which all the variables must exist either in the normal form or compliment form (SOP form)

Ex:- $f(A,B,C) = AB + \underbrace{ABC}_{\text{minterm}} + \bar{B}\bar{C}$

Maxterm :- It is a sum term in which all the variables must exist either in the normal for or compliment form (POS form)

Ex:- $f(A,B,C) = (\bar{A}+B)\cdot\underbrace{(A+B+C)}_{\text{max term}}\cdot(A+\bar{B}+\bar{C})$

(b) $F(x,y,z) = \Sigma m(0,1,2,4,6)$ using K-map



Group 1: Pair : $\bar{A}\bar{B}$

Group 2: Quad : $\bar{C}$

$= \bar{A}\bar{B} + \bar{C}$

(c)

Multiplexer

- The circuit which accepts multiple inputs but presents only one output.
- Works with principle many to one
- Ex :- 2x1 Mux, 8x1 Mux

Demultiplexer

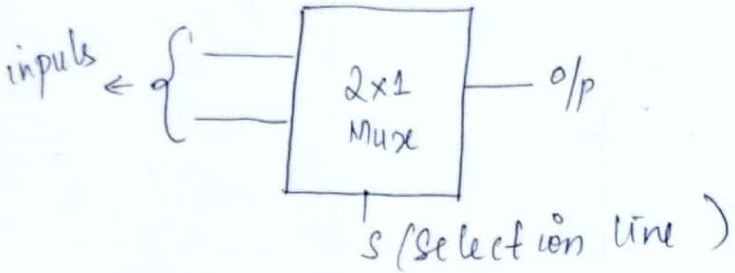
- The circuit which accepts only one input but presents multiple outputs.
- Works with principle one to many
- Ex :- 1x2 Demux, 1x8 Demux.

d) Combinational circuits:-

They consist of 'n' input lines, 'm' output lines and these 'm' output lines depend only on the present 'n' input lines and not on the previous lines.

Ex:- Mux, Demux etc.

e) 2x1 Mux.



A 2x1 Multiplexer is a combinational logic circuit that has only two inputs and 1 output and 1 selection line.

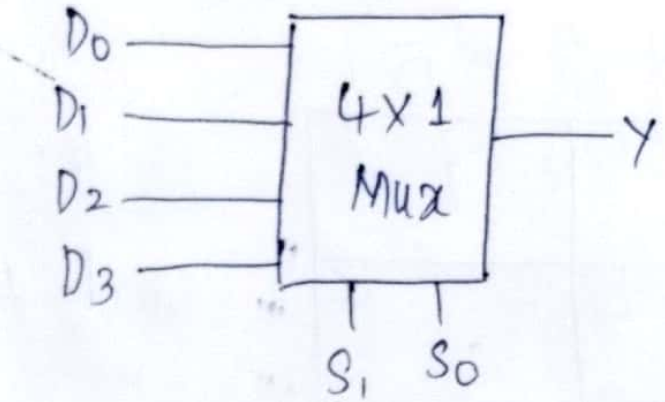
$= A + BC'$

$\therefore$ ~~Absorption law~~

b) Design a 4x1 Multiplexer. 3MARKS (3).

Sol The number of input lines are four and there will be one output and two Select lines

· Block Diagram

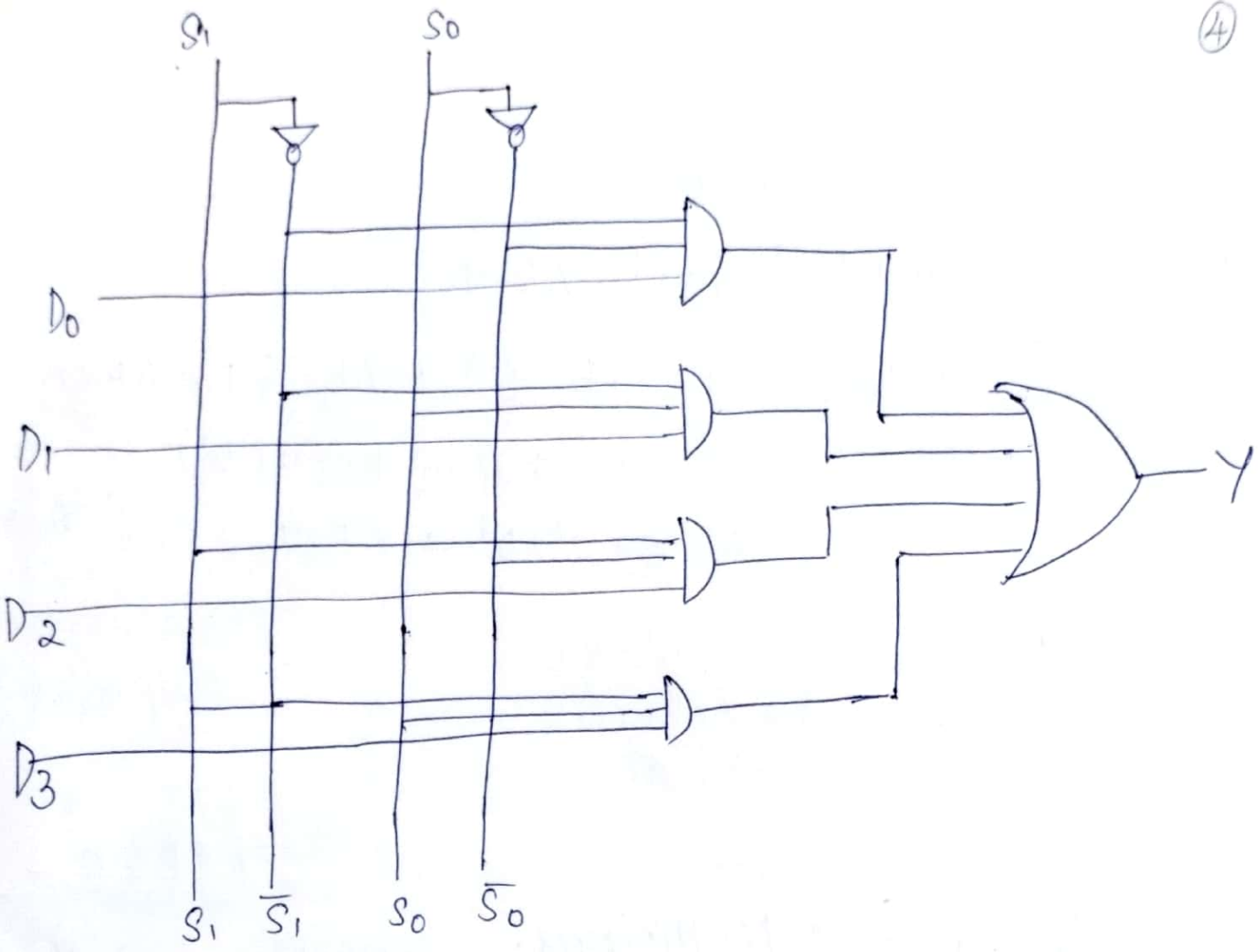


Truth Table

S_1	S_0	Y
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3

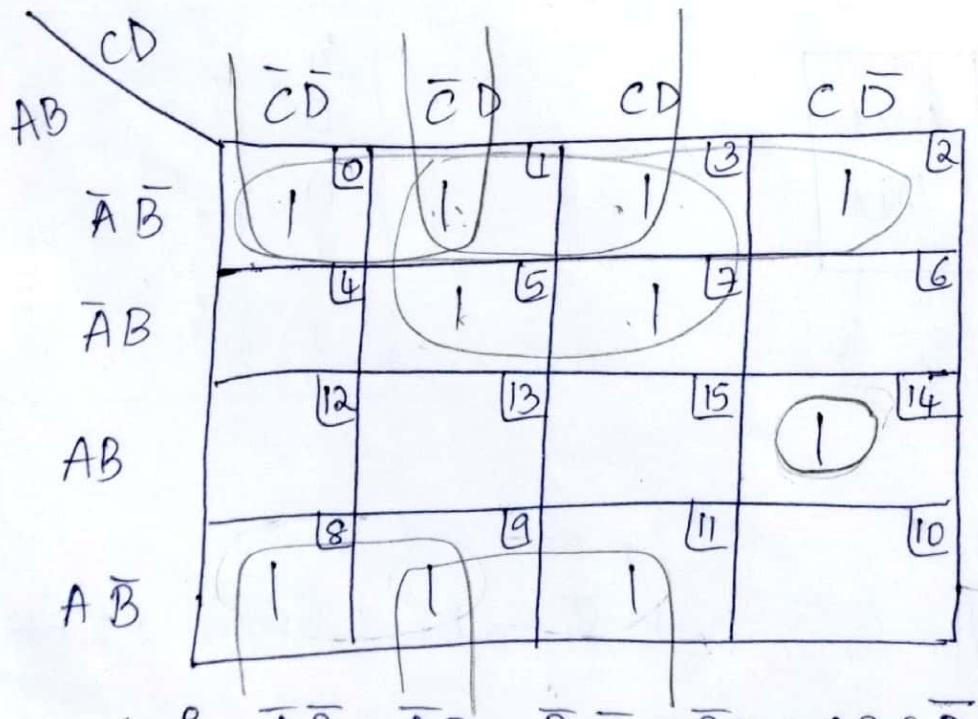
· Equation :-

$$Y = \bar{S}_1 \bar{S}_0 D_0 + \bar{S}_1 S_0 D_1 + S_1 \bar{S}_0 D_2 + S_1 S_0 D_3$$



c) Solve the below four variable logic function using K-map $f(A,B,C,D) = \Sigma m\,(0,1,2,3,5,7,8,9,11,14)$

Sol



Result:

Quad = 4

$\therefore f = \bar{A}\bar{B} + \bar{A}D + \bar{B}\bar{C} + \bar{B}D + ABC\bar{D}$

Group 1: (0,1,3,2) ⇒ $\bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}D + \bar{A}\bar{B}CD + \bar{A}\bar{B}C\bar{D} = \bar{A}\bar{B}$

Group 2: (1,3,5,7) ⇒ $\bar{A}\bar{B}\bar{C}D + \bar{A}\bar{B}CD + \bar{A}B\bar{C}D + \bar{A}BCD = \bar{A}D$.

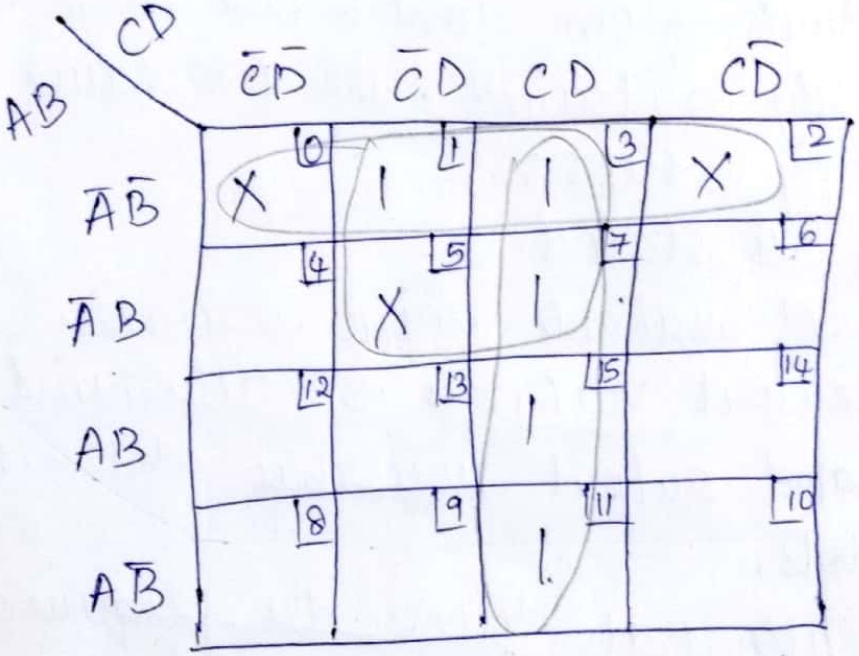
Group 3: (0,1,8,9) ⇒ $\bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}D + A\bar{B}\bar{C}\bar{D} + A\bar{B}\bar{C}D = \bar{B}\bar{C}$.

Group 4: (1,3,9,11) ⇒ $\bar{A}\bar{B}CD + \bar{A}\bar{B}CD + A\bar{B}\bar{C}D + A\bar{B}CD = \bar{B}D$.

d) Simplify the following Boolean expression using k-map and implement it with AOI logic gates.

$f(a,b,c) = \Sigma m(1,3,7,11,15) + d(0,2,5)$

Sol



Group :-1

$\bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}B\bar{C}D + \bar{A}\bar{B}CD + \bar{A}\bar{B}C\bar{D}$

$= \bar{A}\bar{B}$

Group :2

$\bar{A}\bar{B}\bar{C}D + \bar{A}\bar{B}CD + \bar{A}B\bar{C}D + \bar{A}BCD$

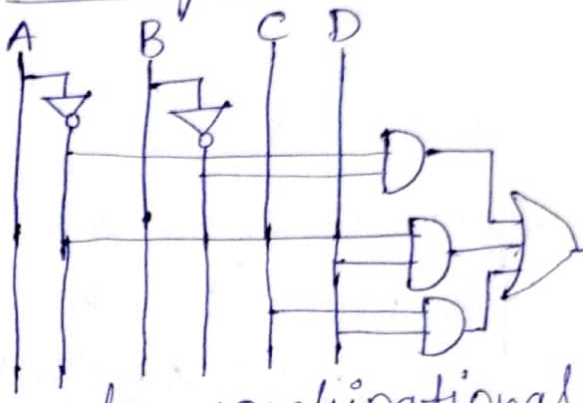
$= \bar{A}D$

Group-3

$\bar{A}\bar{B}CD + \bar{A}BCD + ABCD + A\bar{B}CD$

$= CD.$

AOI logic



$\Rightarrow \bar{A}\bar{B} + \bar{A}D + CD = Y$

$= \bar{A}(\bar{B}+D) + CD$

(e) Explain the design procedure for combinational logic circuits.

Sol The design of combinational circuits starts from the verbal discription of the problem and ends in a logic circuit diagram or a set of Boolean functions from which the logic diagram can be easily obtained. The procedure involves the following steps:

1) The problem is stated.
2) The number of available input variables and required output variables is determined
3) The input and output variables are assigned letter symbols.
4) The truth table that defines the required relationship between inputs and outputs is derived.
5) The simplified Boolean function for each output is obtained.
6) The logic diagram is drawn

a). Obtain the standard SOP of $A + BC' + ABD' + ABCD$

Let $f = A + BC' + ABD' + ABCD$.

First Term: A

$= A(B+B')(C+C')(D+D')$

$= (AB + AB')[CD + CD' + C'D + C'D']$

$= ABCD + ABCD' + ABC'D + ABC'D' + AB'CD +$
$AB'CD' + AB'C'D + AB'C'D'$

(15) (14) (13) (12) (11) (10) (9) (8)

Second Term: $\Rightarrow BC'$

$= (A+A')B \cdot C'(D+D')$

$= [AB + A'B][C'D + C'D']$

$= ABC'D + ABC'D' + A'BC'D + A'BC'D'$

(13) (12) (5) (4)

Third Term: ABD'

$= AB(C+C')D'$

$= A \cdot B[CD' + C'D']$

$= ABCD' + ABC'D'$

(14) (12)

Fourth Term: $ABCD$

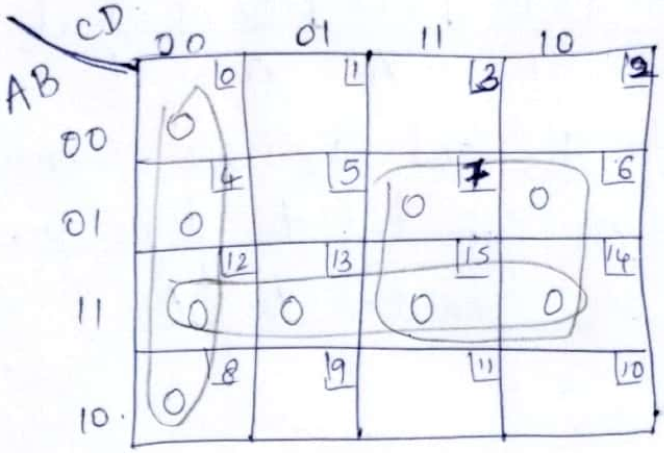
(15)

$$SOP = \sum m(4, 5, 8, 9, 10, 11, 12, 13, 14, 15)$$

5 Marks

3) a) Simplify the following expression using k-map and realise using NOR gates $f = \Pi M(0,4,6,7,8,12,13,14,15)$.

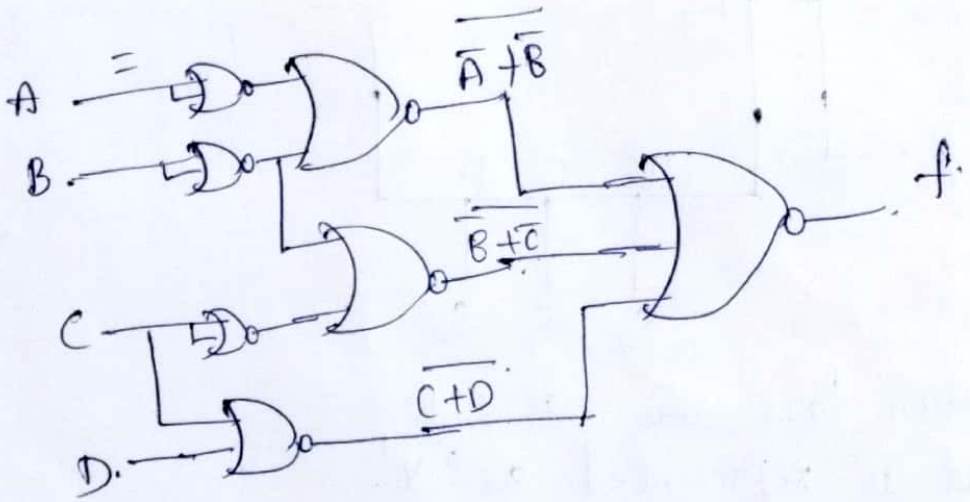
Sol $f = \Pi M(0,4,6,7,8,12,13,14,15)$



$$f = (C+D)(\bar{A}+\bar{B})(\bar{B}+\bar{C})$$

$$\bar{f} = \overline{(C+D)(\bar{A}+\bar{B})(\bar{B}+\bar{C})}$$

$$= \overline{\overline{C+D} + \overline{\bar{A}+\bar{B}} + \overline{\bar{B}+\bar{C}}}$$



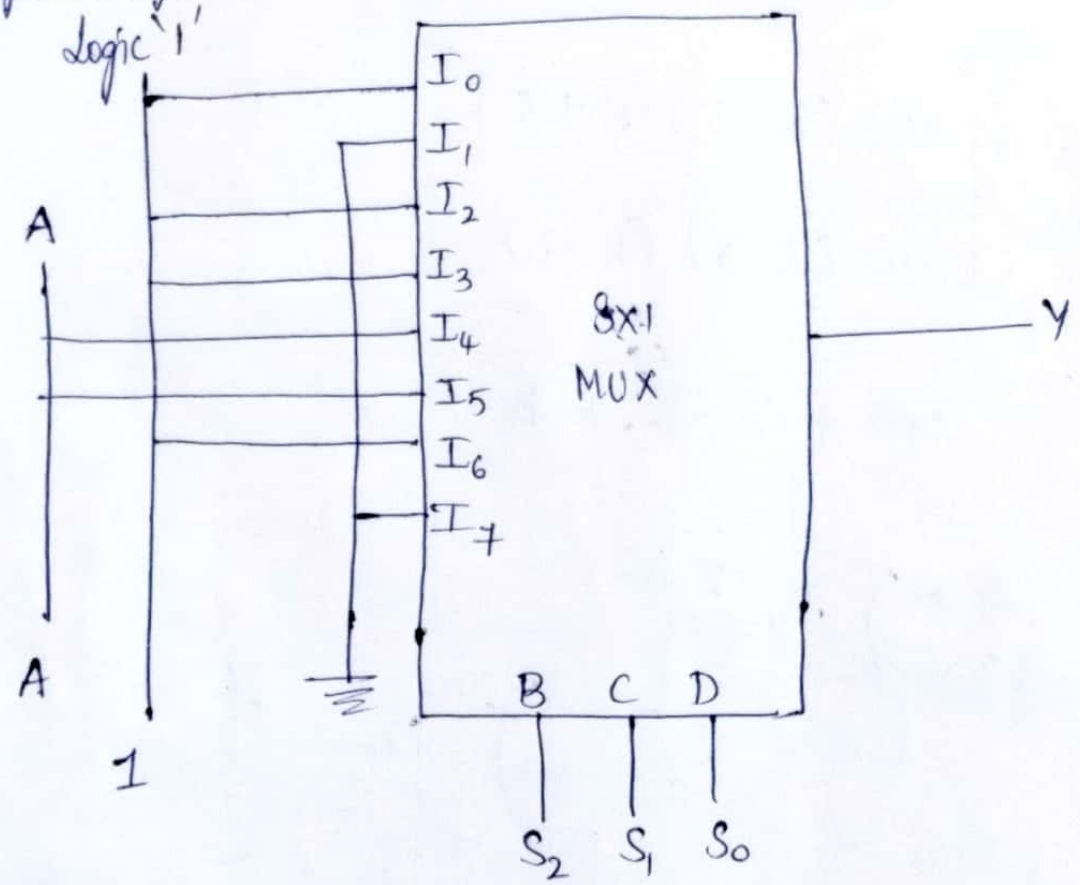
b) Implement the following boolean function with 8:1 multiplexer $F(A,B,C,D) = \Sigma m(0,2,6,10,11,12,13) + d(3,8,14)$ (9)

i) Implementation Table :-

	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7
$\bar{A}$	1 (0)	(1)	1 (2)	X (3)	(4)	(5)	1 (6)	(7)
A	X (8)	(9)	1 (10)	1 (11)	1 (12)	1 (13)	X (14)	(15)
	1	0	1	1	A	A	1	0

1) The inputs I_0, I_2, I_3 and I_6 are connected to 1.
2) The inputs I_1, I_7 are connected to logic 0.
3) The inputs I_4, I_5 are connected to A.

ii) Logic Diagram :-

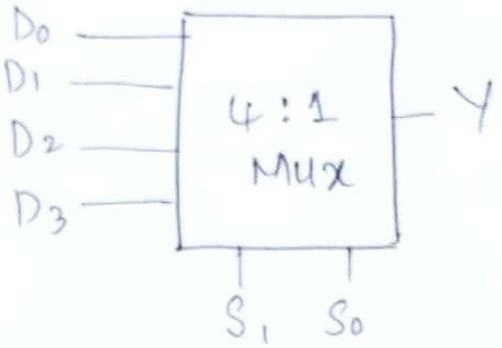


1) The Selection lines are B, C, D.
2) The output is represented as 'Y'.

(c) Construct 4:1 Mux using logic gates and Truth Table (10)

Ans) The number of input lines are four and they will two select lines and one output line.

Block Diagram

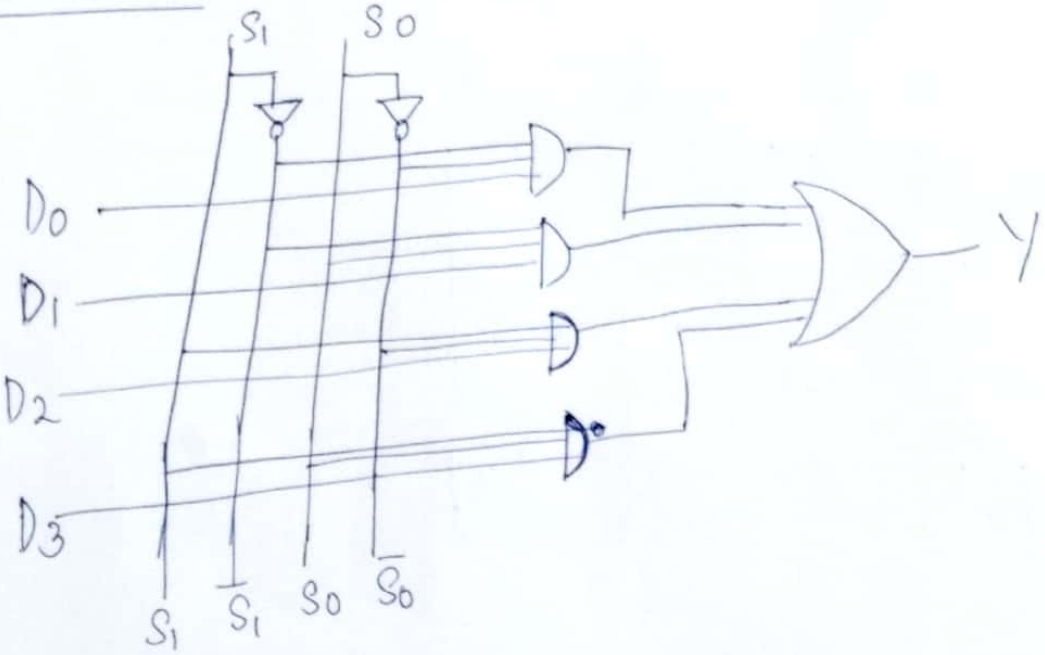


Truth Table

S_1	S_0	Y
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3

Equation :- $\bar{S}_1 \bar{S}_0 D_0 + \bar{S}_1 S_0 D_1 + S_1 \bar{S}_0 D_2 + S_1 S_0 D_3$

Logic circuit



Operation :-

i) If $S_1 = 0, S_0 = 0$ Gate 1 is active ∴ Output D_0

ii) If $S_1 = 0, S_0 = 1$ Gate 2 is active ∴ Output D_1

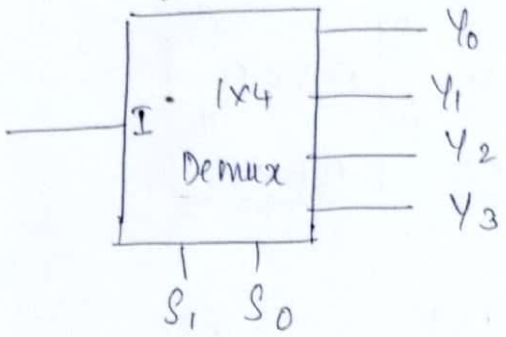
iii) If $S_1 = 1, S_0 = 0$ Gate 3 is active ∴ Output D_2

iv) If $S_1 = 1, S_0 = 1$ Gate 4 is active ∴ Output D_3

e) Construct 1:4 Demux using logic gates and truth table. (11)

Ans) It has one input and four outputs. The number of select lines are two

Block Diagram



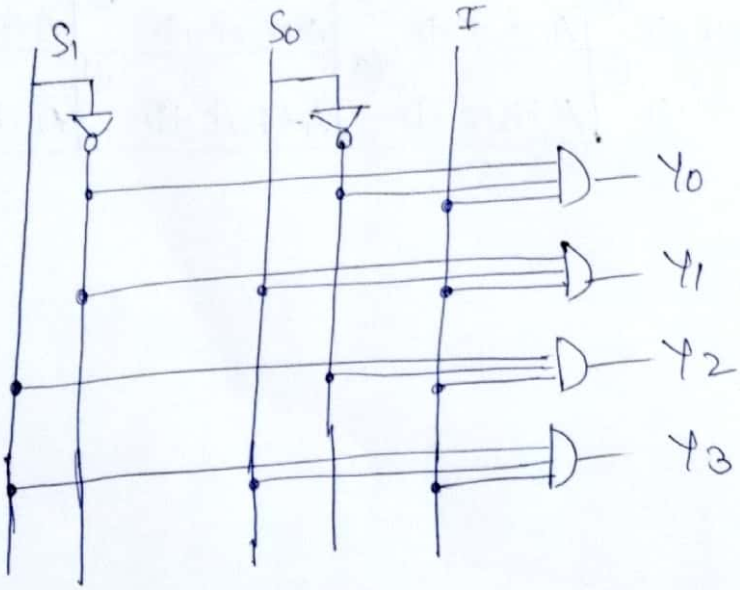
Truth Table

S_1	S_0	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	I
0	1	0	0	I	0
1	0	0	I	0	0
1	1	I	0	0	0

Equation :- $Y_0 = \bar{S}_1 \bar{S}_0 I$, $Y_1 = \bar{S}_1 S_0 I$

$Y_2 = S_1 \bar{S}_0 I$, $Y_3 = S_1 S_0 I$

Cicuit :-



Operation :-

i) When $S_1 = 0$, $S_0 = 0$, only AND gate 1 is active, $\boxed{Y_0 = I}$

ii) When $S_1 = 0$, $S_0 = 1$, only AND gate 2 is active, $\boxed{Y_1 = I}$

iii) When $S_1 = 1$, $S_0 = 0$, only AND gate 3 is active, $\boxed{Y_2 = I}$

iv) When $S_1 = 1$, $S_0 = 1$, only AND gate 4 is active, $\boxed{Y_3 = I}$

d) Interpret Minterm and Maxterm for Four Variables used K-Map.

(i). Minterms :-

AB \ CD	00 $\bar{C}\bar{D}$	01 $\bar{C}D$	11 CD	10 $C\bar{D}$
00 $\bar{A}\bar{B}$	(0) $\bar{A}\bar{B}\bar{C}\bar{D}$	(1) $\bar{A}\bar{B}\bar{C}D$	(3) $\bar{A}\bar{B}CD$	(2) $\bar{A}\bar{B}C\bar{D}$
01 $\bar{A}B$	(4) $\bar{A}B\bar{C}\bar{D}$	(5) $\bar{A}B\bar{C}D$	(7) $\bar{A}BCD$	(6) $\bar{A}BC\bar{D}$
11 AB	(12) $AB\bar{C}\bar{D}$	(13) $AB\bar{C}D$	(15) $ABCD$	(14) $ABC\bar{D}$
10 $A\bar{B}$	(8) $A\bar{B}\bar{C}\bar{D}$	(9) $A\bar{B}\bar{C}D$	(11) $A\bar{B}CD$	(10) $A\bar{B}C\bar{D}$

(ii). Maxterms :-

AB \ CD	00 $C+D$	01 $C+\bar{D}$	11 $\bar{C}+\bar{D}$	10 $\bar{C}+D$
00 $A+B$	(0) $(A+B+C+D)$	(1) $(A+B+C+\bar{D})$	(3) $(A+B+\bar{C}+\bar{D})$	(2) $(A+B+\bar{C}+D)$
01 $A+\bar{B}$	(4) $A+\bar{B}+C+D$	(5) $A+\bar{B}+C+\bar{D}$	(7) $A+\bar{B}+\bar{C}+\bar{D}$	(6) $A+\bar{B}+\bar{C}+D$
11 $\bar{A}+\bar{B}$	(12) $\bar{A}+\bar{B}+C+D$	(13) $\bar{A}+\bar{B}+C+\bar{D}$	(15) $\bar{A}+\bar{B}+\bar{C}+\bar{D}$	(14) $\bar{A}+\bar{B}+\bar{C}+D$
10 $\bar{A}+B$	(8) $\bar{A}+B+C+D$	(9) $\bar{A}+B+C+\bar{D}$	(11) $\bar{A}+B+\bar{C}+\bar{D}$	(10) $\bar{A}+B+\bar{C}+D$.

4) A (i) Implement the following Boolean function using 8:1 Multiplexer (10 Marks) (13)

$$F(A,B,C,D) = \Sigma m\,(0,2,6,10,11,12,13) + d\,(3,8,14)$$

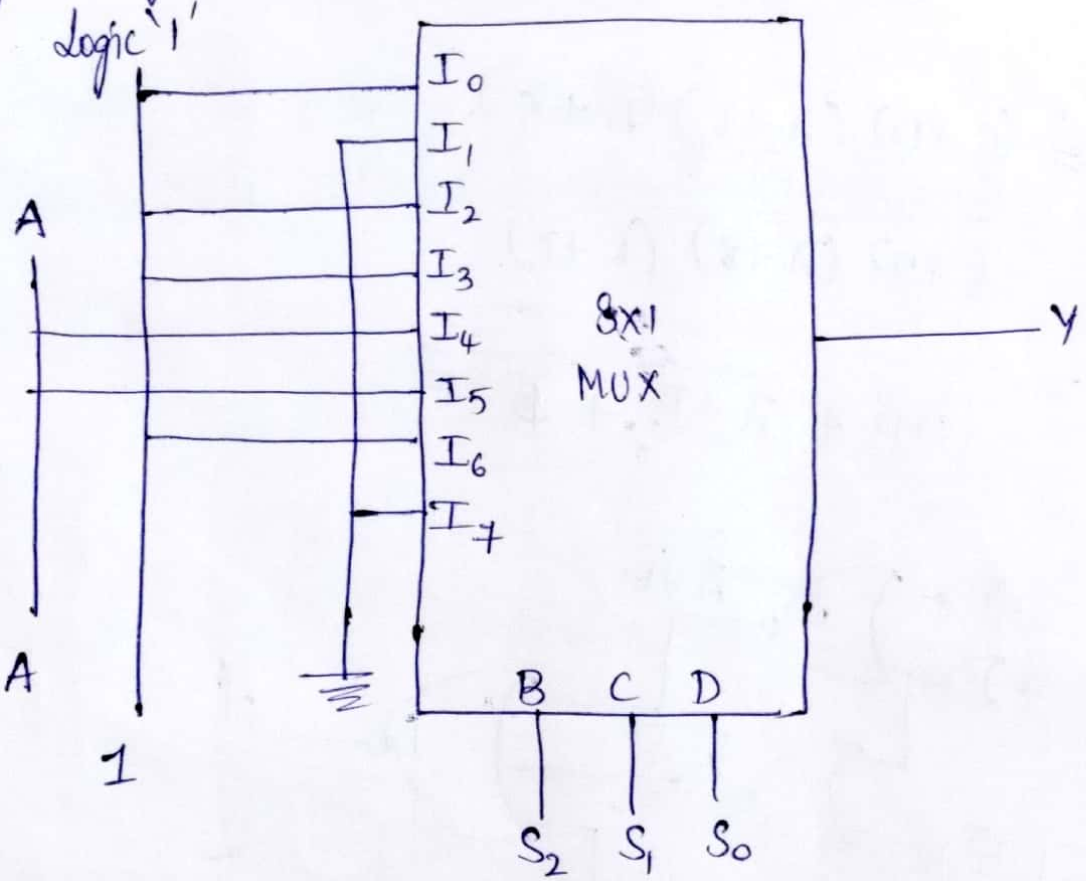
b) Implement the following boolean function with 8:1 multiplexer $F(A,B,C,D) = \Sigma m(0,2,6,10,11,12,13) + d(3,8,14)$ (9)

i). Implementation Table :-

	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7
$\bar{A}$	(0) 1	(1)	(2) 1	(3) X	(4)	(5)	(6) 1	(7)
A	(8) X	(9)	(10) 1	(11) 1	(12) 1	(13) 1	(14) X	(15)
	1	0	1	1	A	A	1	0

1). The inputs I_0, I_2, I_3 and I_6 are connected to 1.
2). The inputs I_1, I_7 are connected to logic 0.
3). The inputs I_4, I_5 are connected to A.

ii). Logic Diagram :-



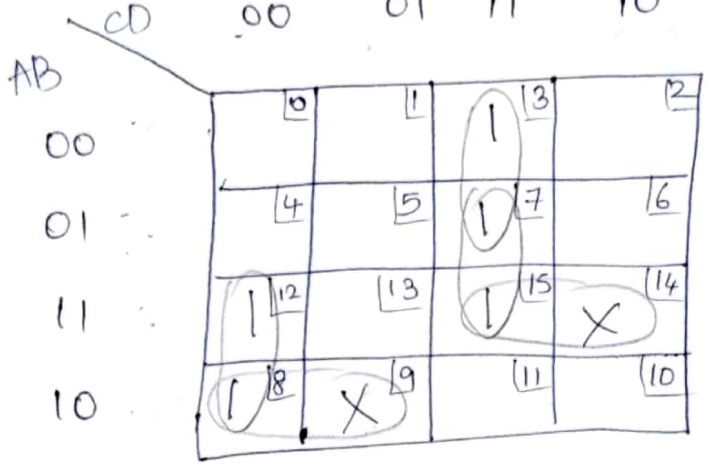
1). The selection lines are B, C, D.
2). The output is represented as 'Y'.

4.b) i). Simplify the following function

$f(A, B, C, D) = \Pi(3, 7, 8, 12, 15) + \Pi d(9, 14)$.

1) Simplify the following function

$F(A,B,C,D) = \Pi(3,7,8,12,15) + \Pi d(9,14)$



Result :-

Pair : 5

~~Group 1~~ :-

~~$\bar{A}\bar{B}CD + \bar{A}BCD$~~

~~$= \bar{A}CD$~~

~~Group 2 :-~~

~~$A\bar{B}CD + ABCD$~~

~~$= BCD$~~

~~Group 3 :-~~

~~$ABCD + ABC\bar{D}$~~

~~$= ABC$~~

~~Group 4 :-~~

~~$AB\bar{C}\bar{D} + A\bar{B}\bar{C}\bar{D}$~~

~~$= A\bar{C}\bar{D}$~~

~~Group 5 :-~~

~~$AB\bar{C}\bar{D} + A\bar{B}\bar{C}\bar{D}$~~

~~$= A\bar{B}\bar{C}$~~

Group 1 : $\bar{A}+C+D$

Group 2 : $\bar{A}+B+C$

Group 3 :- $A+\bar{C}+\bar{D}$

Group 4 : $B+\bar{C}+\bar{D}$

Group 5 :- $\bar{A}+\bar{B}+C$

$f = (\bar{A}+C+D)(\bar{A}+B+C)(A+\bar{C}+\bar{D})$
$(\bar{A}+\bar{B}+C)(B+\bar{C}+\bar{D})$

~~$\Rightarrow \bar{A}CD + BCD + ABC + A\bar{C}\bar{D} + A\bar{B}\bar{C}$~~

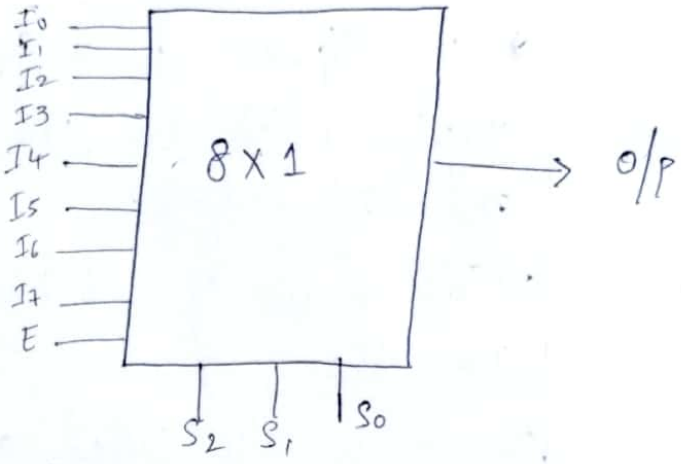
(b) Compare multiplexer and Demultiplexer. (15)

Multiplexer	Demultiplexer
1). Multiplexer is a Combinational Circuit which has 2^n inputs and One output.	1). Demultiplexer is a Combinational circuit which has One input and 2^n outputs.
2) The number of Selection lines are n.	2) The number of selection lines are n.
3). It is also called as Many to One.	3). It is also called as One to Many.
4). It is used as a 'Data Selector'.	4). It is used as a 'Data Distributor.'
5). Examples: 2X1 MUX, 4X1 MUX, 8X1 MUX ---	5) Examples :- 1X2 Demux, 1X4 Demux, 1X8 Demux ---

(C) Construct 8:1 Mux using logic gates and truth table

Block Diagram

(16)

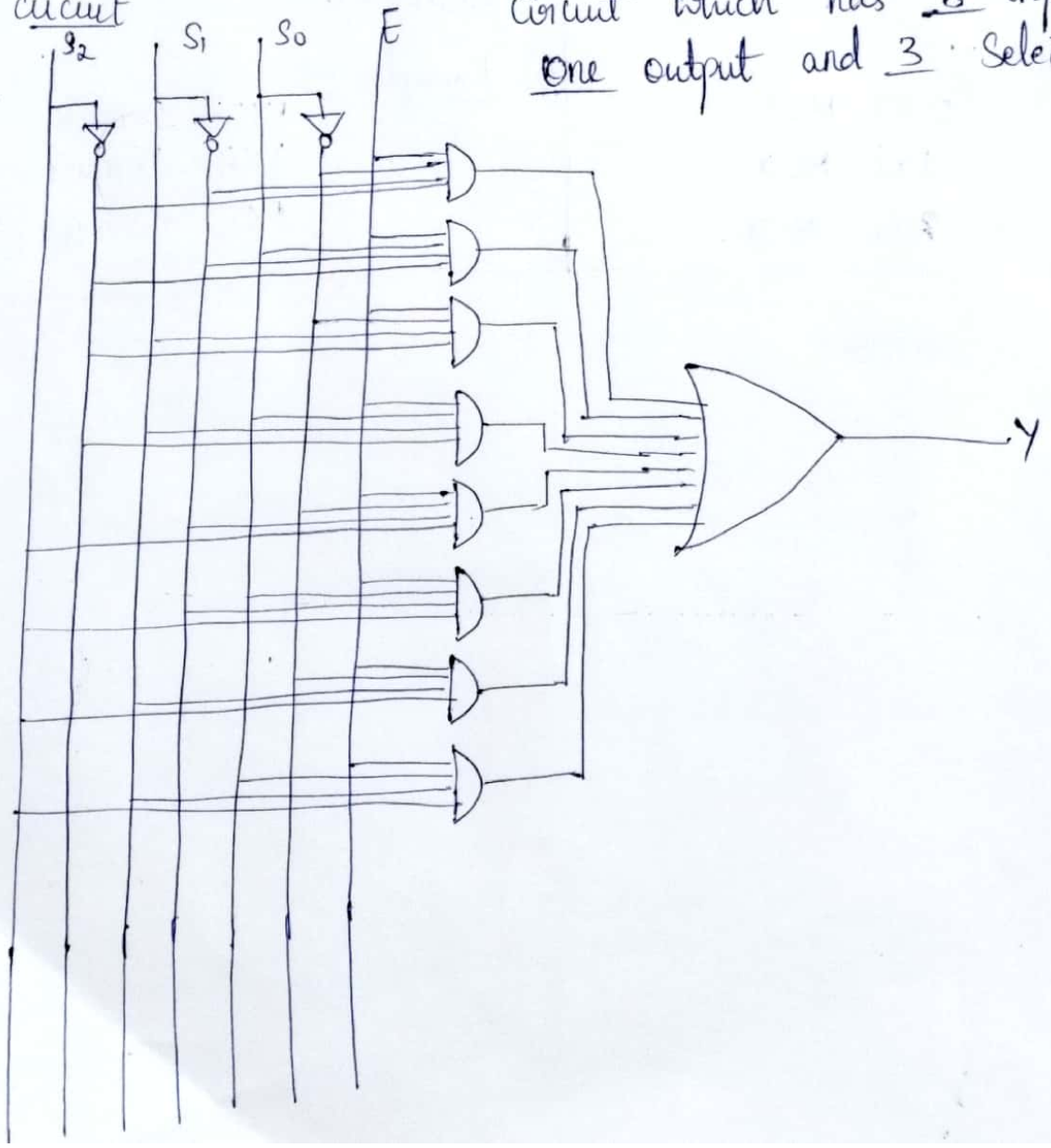


E	S_2	S_1	S_0	Y
0	x	x	x	
1	0	0	0	$I_0 E \bar{S_2} \bar{S_1} \bar{S_0}$
1	0	0	1	$I_1 E \bar{S_2} \bar{S_1} S_0$
1	0	1	0	$I_2 E \bar{S_2} S_1 \bar{S_0}$
1	0	1	1	$I_3 E \bar{S_2} S_1 S_0$
1	1	0	0	$I_4 E S_2 \bar{S_1} \bar{S_0}$
1	1	0	1	$I_5 E S_2 \bar{S_1} S_0$
1	1	1	0	$I_6 E S_2 S_1 \bar{S_0}$
1	1	1	1	$I_7 E S_2 S_1 S_0$

→ 8 inputs
→ 1 output
→ 3 select lines

Definition: Multiplexer is a Combinational Circuit which has 8 inputs and one output and 3 Selection lines.

Logic circuit



Truth Table :-

E	S_2	S_1	S_0	Y
0	x	x	x	0
1	0	0	0	I_0
1	0	0	1	I_1
1	0	1	0	I_2
1	0	1	1	I_3
1	1	0	0	I_4
1	1	0	1	I_5
1	1	1	0	I_6
1	1	1	1	I_7

Equation :

$$Y = E\bar{S_2}\bar{S_1}\bar{S_0}I_0 + E S_2 S_1 \bar{S_0} I_1 + E\bar{S_2} S_1 \bar{S_0} I_2 + E\bar{S_2} S_1 S_0 I_3 + E S_2 \bar{S_1}\bar{S_0} I_4 + E S_2 \bar{S_1} S_0 I_5 + E S_2 S_1 \bar{S_0} I_6 + E S_2 S_1 S_0 I_7$$

Theory :

1) When $S_2=0, S_1=0, S_0=0 \Rightarrow$ Output, $Y = I_0$
2) When $S_2=0, S_1=0, S_0=1 \Rightarrow$ output $Y = I_1$
3) When $S_2=0, S_1=1, S_0=0 \Rightarrow$ output $Y = I_2$
4) When $S_2=0, S_1=1, S_0=1 \Rightarrow$ output $Y = I_3$
5) When $S_2=1, S_1=0, S_0=0 \Rightarrow$ output $Y = I_4$.
6) When $S_2=1, S_1=0, S_0=1 \Rightarrow$ output $Y = I_5$
7) When $S_2=1, S_1=1, S_0=0 \Rightarrow$ output $Y = I_6$
8) When $S_2=1, S_1=1, S_0=1 \Rightarrow$ output $Y = I_7$.