St. Peter's Engineering College (Autonomous)	Dept.	:	CSM, CSC, CSD

Dullapally (P), Medchal, Hyderabad – 500100.

MID – II EXAMINATION – NOVEMBER 2024

Academic Year 2024-25

Subject Code	:	AS22- 04ES07	Subject	:	DIGITAL ELECTRONICS			
Class/Section	:	B. Tech. (A)	Year	:	II	Semester	:	I
Duration	:	120 Min	Max. Marks	:	30	Date:	:	

BLOOMS LEVEL					
Remember	L1	Understand	L2	Apply	L3
Analyze	L4	Evaluate	L5	Create	L6

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PART – A (10x1M = 10M)

Note: Answer all Questions. Each Question carries equal marks.

Q. No		Question (s)	Marks	BL	CO
		UNIT - IV			
1	**a)**	Define Flip-flop.	1M	L1	C212.5
	b)	List the types of Shift Registers.	1M	L1	C212.5
	c)	Compare Latch and flip flop.	1M	L1	C212.5
	d)	Write the Characteristic Tables for D Flipflop and T flipflop.	1M	L1	C212.5
		UNIT – V			
	e)	Define PLA.	1M	L1	C212.6
	f)	How is the memory size specified.	1M	L1	C212.6
	g)	Define ROM. What are the Classifications of the ROM?	1M	L1	C212.6
	h)	Explain the Block Diagram of the Memory.	1M	L2	C212.6
		UNIT – III			
	i)	What is a Comparator?	1M	L1	C212.4
	j)	What is a Parity Generator?	1M	L1	C212.4

PART – B (20M)

Q. No		Question (s)	Marks	BL	CO
		UNIT - IV			
2	**a)**	Explain the operation of JK Flip-Flop with truth table.	4M	L2	C212.5
	b)	Convert a D Flip Flop to SR Flip Flop.	4M	L3	C212.5
		OR			
3	**a)**	Explain the operation of Universal shift register with a neat diagram.	4M	L3	C212.5

	b)	Compare combinational and sequential circuits.	**4M**	L3	C212.5
		UNIT – V			

4	a)	Write a short note on
		    i) EPROM
		   ii) EEPROM
			4M	L1	C212.6

	b)	Differentiate between RAM and ROM.	**4M**	L2	C212.6
		OR			
5	a)	Implement the following Boolean function using PAL withfour inputs and also write the PAL programming table. F1(A,B,C,D)= Σ m(1,2,8,12,13) F2(A,B,C,D)= Σ m(0,2,3,4,5,6,7,8,10,11,15)	**4M**	L4	C212.6
	b)	Differentiate Static and Dynamic RAM.	**4M**	L2	C212.6
		UNIT – III			
6		Design a 4-bit BCD to Excess-3 code converter.	**4M**	L4	C212.4
		OR			
7		Explain 2-bit Magnitude comparator with neat logicdiagram.	**4M**	L2	C212.4

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St. Peter's Engineering College (Autonomous)

Dullapally (P), Medchal, Hyderabad – 500100.

MID – II EXAMINATION – NOVEMBER 2024

Dept.	**:**		
Academic Year 2024-25			

Subject Code	**:**	**AS22- 04ES07**	**Subject**	**:**	**DIGITAL ELECTRONICS**		
Class/Section	**:**	**B. Tech. (A)**	**Year**	**:**	**II**	**Semester :**	**I**
Duration	**:**	**120 Min**	**Max. Marks**	**:**	**30**	**Date:**	**:**

BLOOMS LEVEL					
Remember	L1	Understand	L2	Apply	L3
Analyze	L4	Evaluate	L5	Create	L6

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PART – A (10x1M = 10M)
Note: Answer all Questions. Each Question carries equal marks.

Q. No		Question (s)	Marks	BL	CO
		UNIT - IV			
1	**a)**	What is a Sequential circuit? Give Examples.	**1M**	L1	C212.5
	b)	Give the applications of Flip-Flop.	**1M**	L1	C212.5
	c)	Write the truth table of SR Latch using NOR.	**1M**	L2	C212.5
	d)	Give the Excitation Tables for JK Flipflop.	**1M**	L2	C212.5
		UNIT – V			
	e)	What are the advantages of PLDs over fixed function IC's.	**1M**	L1	C212.6
	f)	State the advantages of FPGA.	**1M**	L1	C212.6
	g)	Write about Programmable Logic Devices.	**1M**	L1	C212.6
	h)	What is FPGA?	**1M**	L1	C212.6
		UNIT – III			
	i)	Draw the block diagram of 3x8 Decoder.	**1M**	L1	C212.4
	j)	What is a Priority Encoder?	**1M**	L1	C212.4

PART – B (20M)

Q. No		Question (s)	Marks	BL	CO
		UNIT - IV			
2	**a)**	What is a Counter? Give the differences betweenSynchronous Counter and Asynchronous Counter.	**4M**	L2	C212.5
	b)	Explain Parallel-In-Serial-Out Shift Register.	**4M**	L3	C212.5
		OR			
3	**a)**	Explain the operation of clocked SR flip-flop.	**4M**	L2	C212.5

	b)	Convert a T Flip Flop to SR Flip Flop.	4M	L3	C212.5
		UNIT – V			
4	a)	Implement the following function using a PAL F(A,B,C,D) = Σm (0, 1,2, 3, 4, 5,7, 10, 11,12, 13, 14, 15).	4M	L4	C212.6
	b)	Write the comparison between PROM, PLA, and PAL?	4M	L2	C212.6
		OR			
5	a)	Implement the following Boolean function using PAL withfour inputs and also write the PAL programming table. F1(A,B,C,D)= Σ m(1,2,8,12,13) F2(A,B,C,D)= Σ m(0,2,3,4,5,6,7,8,10,11,15)	4M	L4	C212.6
	b)	Differentiate Static and Dynamic RAM.	4M	L1	C212.6
		UNIT – III			
6		What is Encoder? Construct 4 to 2 Encoder Using Logic Gates and truth table.	4M	L3	C212.4
		OR			
7		Design a 4-bit Binary to Gary Code Converter.	4M	L2	C212.4

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St. Peter's Engineering College (Autonomous) Dullapally (P), Medchal, Hyderabad – 500100. MID – II EXAMINATION – NOVEMBER 2024	Dept. :	
	Academic Year 2024-25	

Subject Code	:	AS22- 04ES07	Subject	:	**DIGITAL ELECTRONICS**				
Class/Section	:	B. Tech. (A)	Year	:	II		Semester	:	I
Duration	:	120 Min	Max. Marks	:	30	Date:		:	

BLOOMS LEVEL						
Remember	L1	Understand	L2	Apply		L3
Analyze	L4	Evaluate	L5	Create		L6

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PART – A (10x1M = 10M)
Note: Answer all Questions. Each Question carries equal marks.

Q. No		Question (s)	Marks	BL	CO
		UNIT - IV			
1	a)	What is a Shift register?	1M	L1	C212.5
	b)	Explain about Serial-In-Parallel-Out Shift Register.	1M	L2	C212.5
	c)	Give the Excitation Tables for JK Flipflop.	1M	L2	C212.5
	d)	Write the truth table of SR Latch using NAND.	1M	L2	C212.5
		UNIT – V			
	e)	Define PROM.	1M	L1	C212.6
	f)	Explain Dynamic RAM.	1M	L2	C212.6
	g)	Define ROM. What are the Classifications of the ROM?	1M	L1	C212.6
	h)	Define PAL.	1M	L1	C212.6
		UNIT – III			
	i)	Define Decoder and draw its block diagram.	1M	L1	C212.4
	j)	Compare Encoder and Mux.	1M	L2	C212.4

PART – B (20M)

Q. No		Question (s)	Marks	BL	CO
		UNIT - IV			
2	a)	Explain the operation of clocked SR flip-flop.	4M	L4	C212.5
	b)	Compare combinational and sequential circuits.	4M	L2	C212.5
		OR			
3	a)	Design of a MOD-5 Synchronous up counter Using JK Flipflop. Draw the Logic Diagram.	4M	L4	C212.5
	b)	Explain the operation of Serial in Serial Out Shift Register.	4M	L2	C212.5
		UNIT – V			
4	a)	Realize the BCD to EXCESS-3 code converter using PROM.	4M	L3	C212.6

	b)	Differentiate between RAM and ROM.	**4M**	L2	C212.6
		OR			
5	**a)**	Design 3 bit binary to Gray Code converter using PLA?	**4M**	L4	C212.6
	b)	Differentiate Static and Dynamic RAM.	**4M**	L2	C212.6
		UNIT – III			
6		What is Decoder? Construct 2 to 4 Decoder Using LogicGates and truth table.	**4M**	L3	C212.4
		OR			
7		Design a 4-bit Gray to Binary Code Converter	**4M**	L3	C212.4

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