Integrated Electronic Circuits LAB -1

RTL – GDSII Exercise:

Design of MOD5 Counter using Verilog and Synthesis using Encounter tool.

Abhinav Bhattacharya

EEY217501

Path to project: **/afs/iitd.ac.in/user/e/ee/eey217501/rtl_synthesis**

Design and verification using Verilog HDL language in Xilinx ISE

1) Behavioural Level Verilog Code

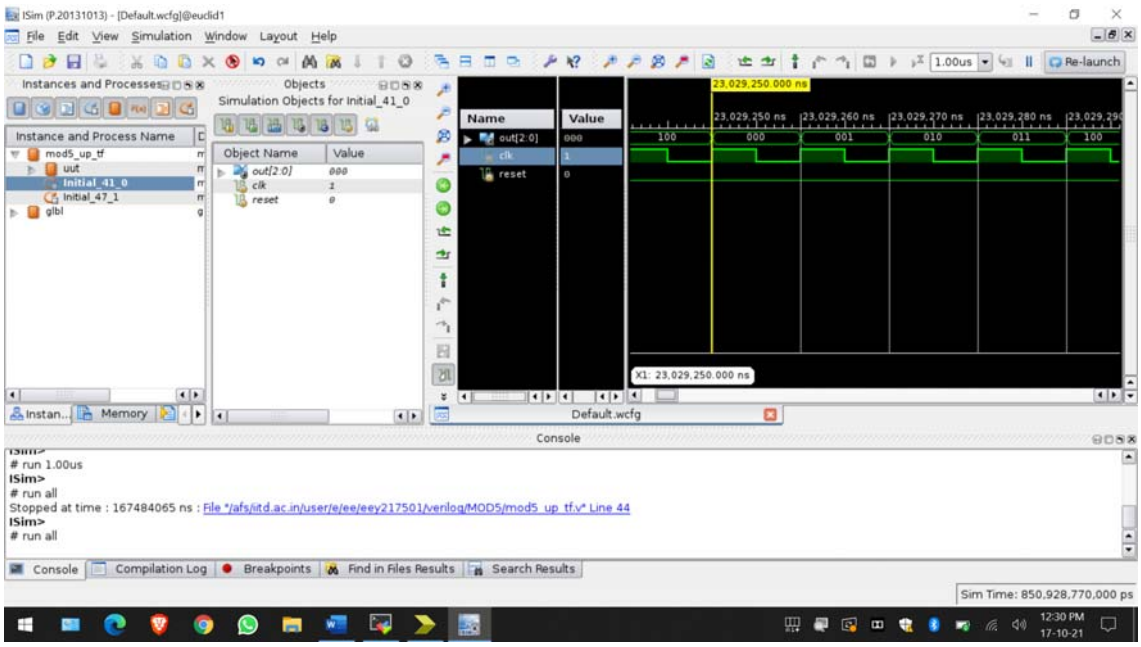
```
`timescale 1ns / 1ps
module mod5_up(out, clk, reset
   );
output [2:0] out;
input clk, reset;

reg [2:0] out;

always @(posedge clk)
if(reset)
begin
 out<= 2'b0;
end

else if(out<4)
 begin
 out<= out+1;
 end

else
 begin
 out<=2'b0;
 end

endmodule
```

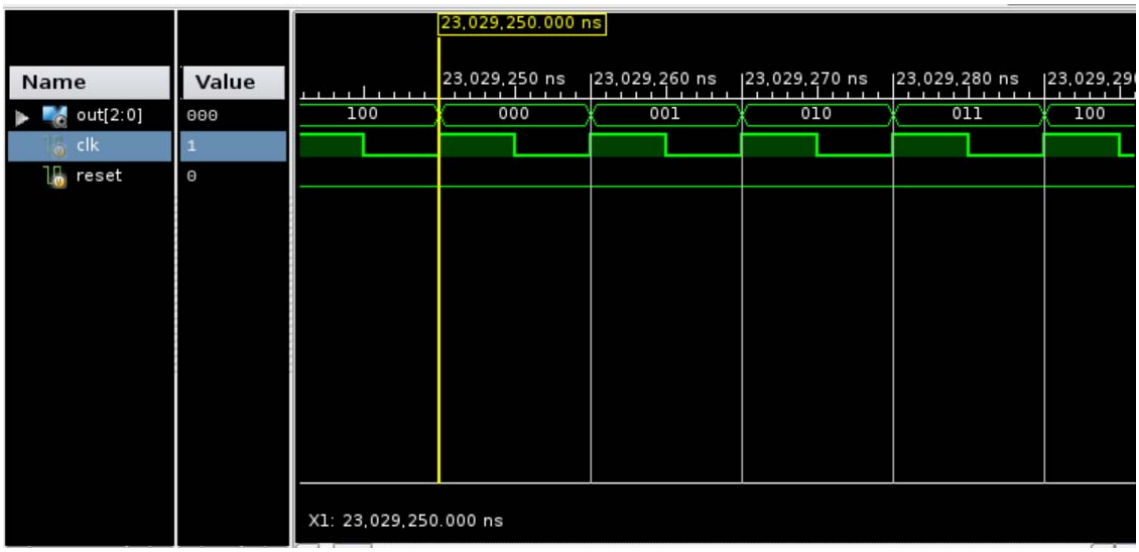
2) Test Bench:

```
`timescale 1ns / 1ps

////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date:   12:46:01 10/09/2021
// Design Name:   mod5_up
// Module Name:
/afs/iitd.ac.in/user/e/ee/eey217501/verilog/MOD5/mod5_up_tf.v
// Project Name:  MOD5
// Target Device:
// Tool versions:
// Description:
//
// Verilog Test Fixture created by ISE for module: mod5_up
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
////////////////////////////////////////////////////////////////////////////////

module mod5_up_tf;

	// Inputs
	reg clk;
	reg reset;

	// Outputs
	wire [2:0] out;

	// Instantiate the Unit Under Test (UUT)
	mod5_up uut (
		.out(out),
		.clk(clk),
		.reset(reset)
	);

	initial begin
		// Initialize Inputs
		clk = 1'b1;
```

```
        forever #5 clk=~clk;
    end

    initial begin
    reset = 1; #10;
    reset = 0; #30;
    end

endmodule
```

3) Test Bench output waveform





Generation of Gate-level synthesizable netlist using Genus

1) TCL script for initialization:

Open ▾ rc_script.tcl ~/rtl_synthesis Save

```
set search_path "/afs/iitd.ac.in/service/tools/public/asiclib/umcoa/L65/libraries/UMC65LLSC/synopsys/ccs"
set_attribute lib_search_path "/afs/iitd.ac.in/service/tools/public/asiclib/umcoa/L65/libraries/UMC65LLSC/synopsys/ccs/"
set_attribute hdl_search_path "./rtl/mod5_up.v"
set_attribute library "uk65lscllmvbbr_100c25_tc_ccs.lib"
set mylist [get_attribute init_hdl_search_path]
read_hdl -v2001 $mylist
elaborate
check_design -unresolved
read_sdc ./constraints_top.sdc
synthesize -to_mapped -effort high
write_hdl > ./output/mod5_counter_netlist.v
write_sdc > ./output/sdc_mod5_output.sdc
```

2) SDC constraints file for clock specifications

Open ▾ constraints_top.sdc ~/rtl_synthesis

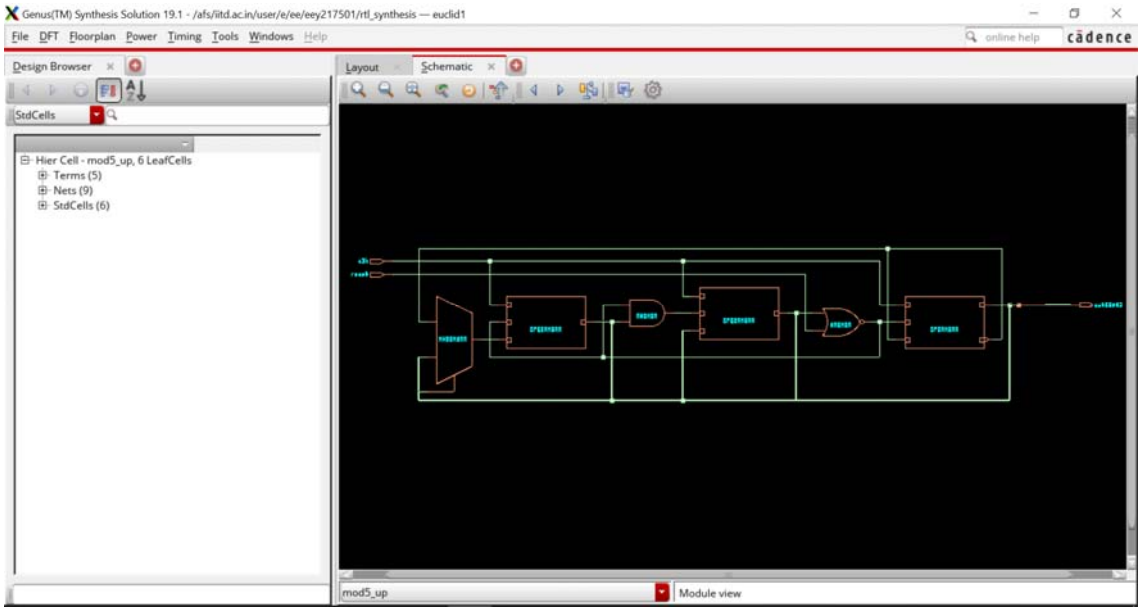
```
create_clock -name clk -period 10 -waveform {0 5} [get_ports "clk"]
set_clock_transistion -rise 0.1 [get_clocks "clk"]
set_clock_transistion -fall 0.1 [get_clocks "clk"]
set_clock_uncertainity 0.1 [get_ports "clk"]
set_input_delay -max 1.0 [get_ports "reset"] -clock [get_clocks "clk"]
set_output_delay -max 1.0 [get_ports "out"] -clock [get_clocks "clk"]
```

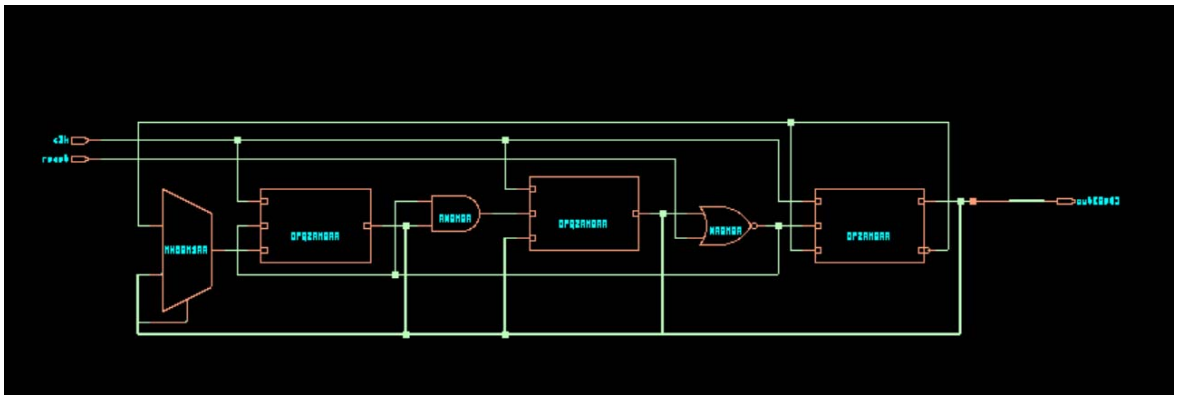
OUTPUT FILES GENERATED BY GENUS

1) Gate-level netlist

Open ▾ mod5_counter_netlist.v ~/rtl_synthesis/output

```
// Generated by Cadence Genus(TM) Synthesis Solution 19.12-s121_1
// Generated on: Oct 14 2021 12:46:02 IST (Oct 14 2021 07:16:02 UTC)

// Verification Directory fv/mod5_up

module mod5_up(out, clk, reset);
  input clk, reset;
  output [2:0] out;
  wire clk, reset;
  wire [2:0] out;
  wire n_0, n_1, n_2, n_3;
  DFQZRM2RA \out_reg[2] (.CK (clk), .D (n_0), .RB (out[0]), .Q
       (out[2]));
  DFQZRM2RA \out_reg[1] (.CK (clk), .D (n_3), .RB (n_2), .Q (out[1]));
  MXB2M1RA g145(.A (n_1), .B (out[0]), .S (out[1]), .Z (n_2));
  AN2M2R g144(.A (n_3), .B (out[1]), .Z (n_0));
  NR2M2R g146(.A (out[2]), .B (reset), .Z (n_3));
  DFZRM2RA \out_reg[0] (.CK (clk), .D (n_3), .RB (n_1), .Q (out[0]),
       .QB (n_1));
endmodule
```





2) Output SDC constraints file

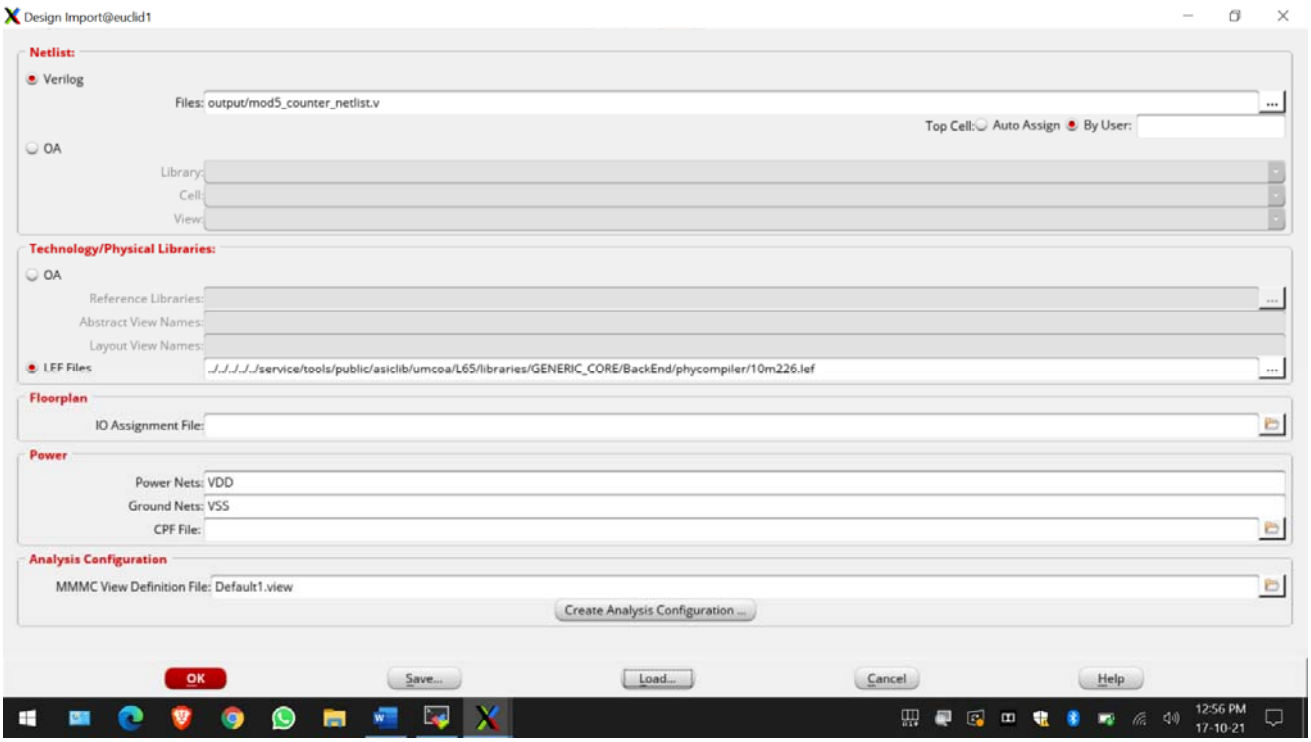
Open

sdc_mod5_output.sdc
~/rtl_synthesis/output

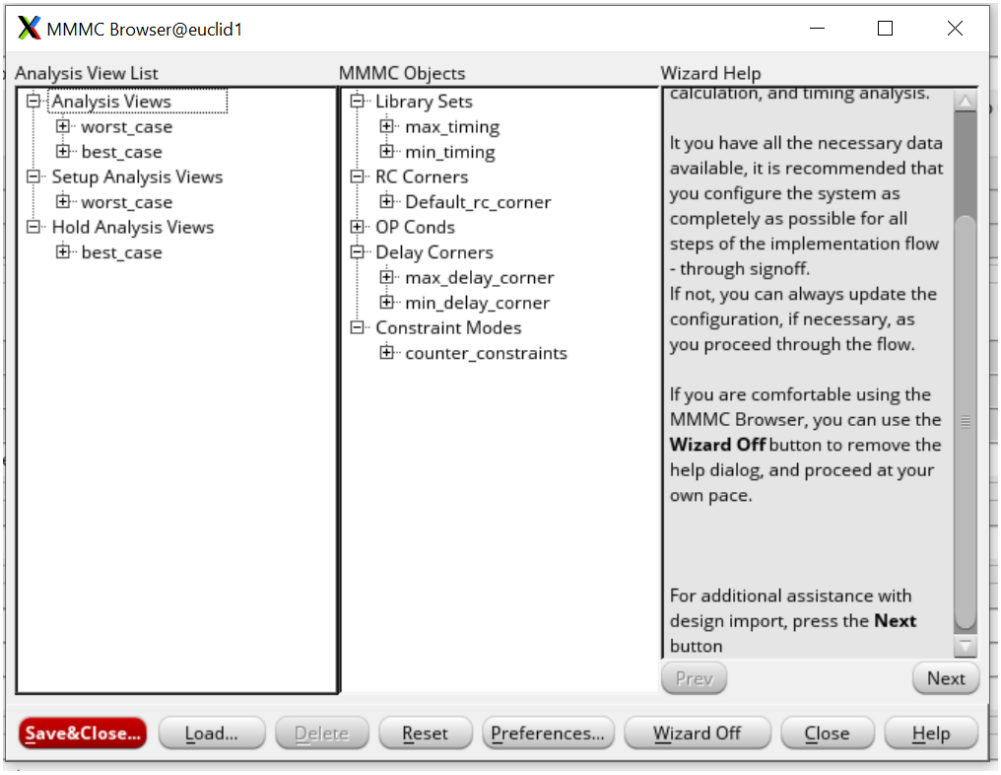
```
# ####################################################################

#  Created by Genus(TM) Synthesis Solution 19.12-s121_1 on Sun Oct 17 12:41:32 IST 2021

# ####################################################################

set sdc_version 2.0

set_units -capacitance 1000fF
set_units -time 1000ps

# Set the current design
current_design mod5_up

create_clock -name "clk" -period 10.0 -waveform {0.0 5.0} [get_ports clk]
set_clock_gating_check -setup 0.0
set_input_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports reset]
set_output_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {out[2]}]
set_output_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {out[1]}]
set_output_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {out[0]}]
set_wire_load_mode "top"
```

3) Layout using Cadence Innovus

1) Importing netlist, LEF file and Power nets



2) MMMC Analysis Configuration



Timing Library file path:
/afs/iitd.ac.in/user/e/ee/eey217501/rtl_synthesis/physicalDesign/timing_lib

LEF file and CapTable path:

/afs/iitd.ac.in/user/e/ee/eey217501/rtl_synthesis/physicalDesign/LEF_file

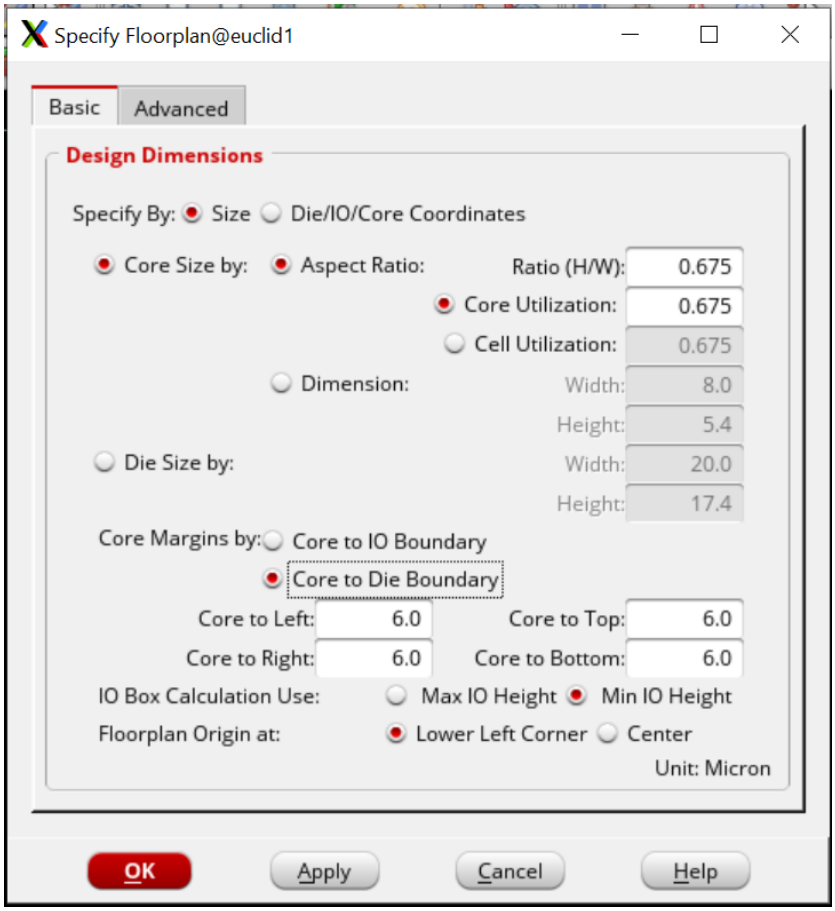
QRC TECH FILE:

/afs/iitd.ac.in/user/e/ee/eey217501/rtl_synthesis/physicalDesign/qrcTechFile.tch

Physical Design

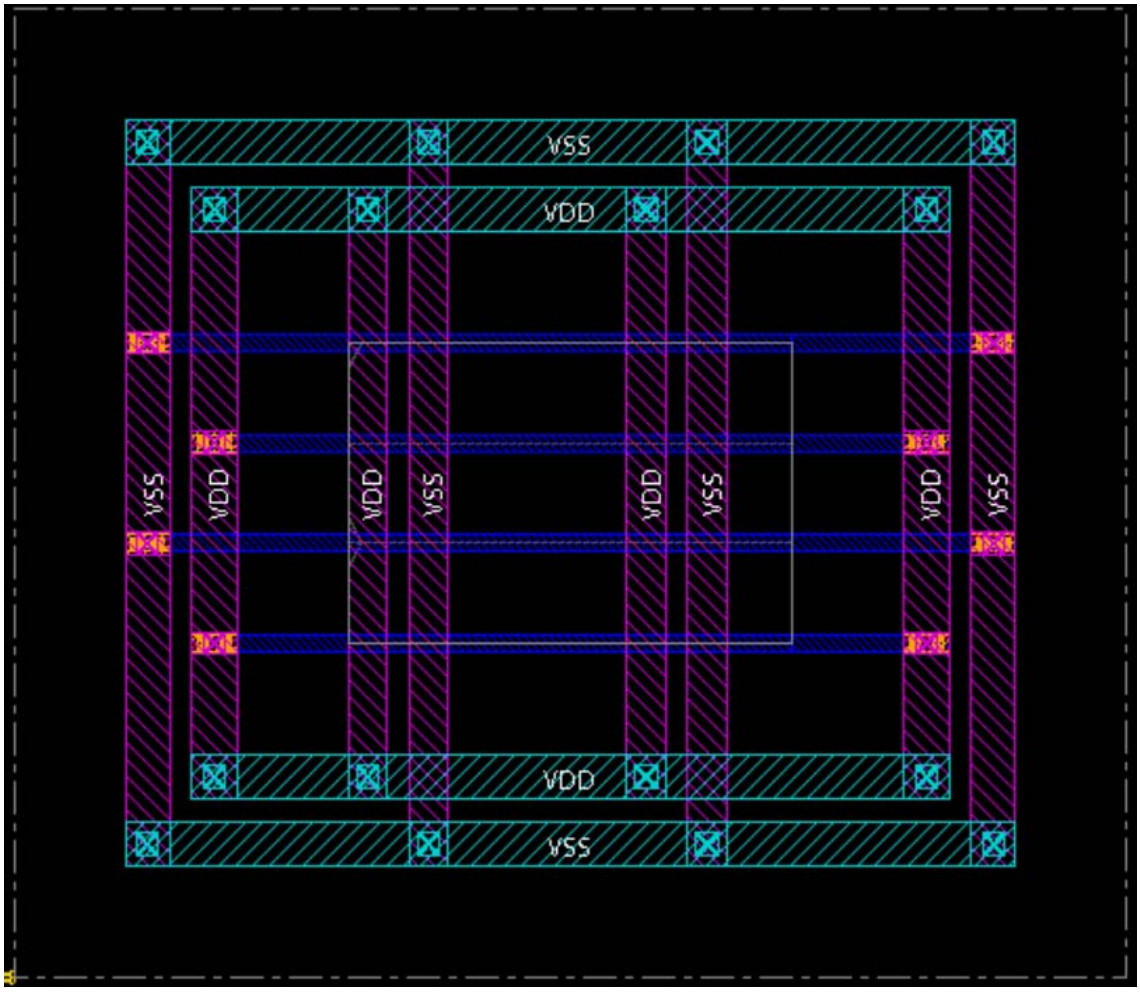
Generating MMMC view

1) Floorplanning



2) Power Planning

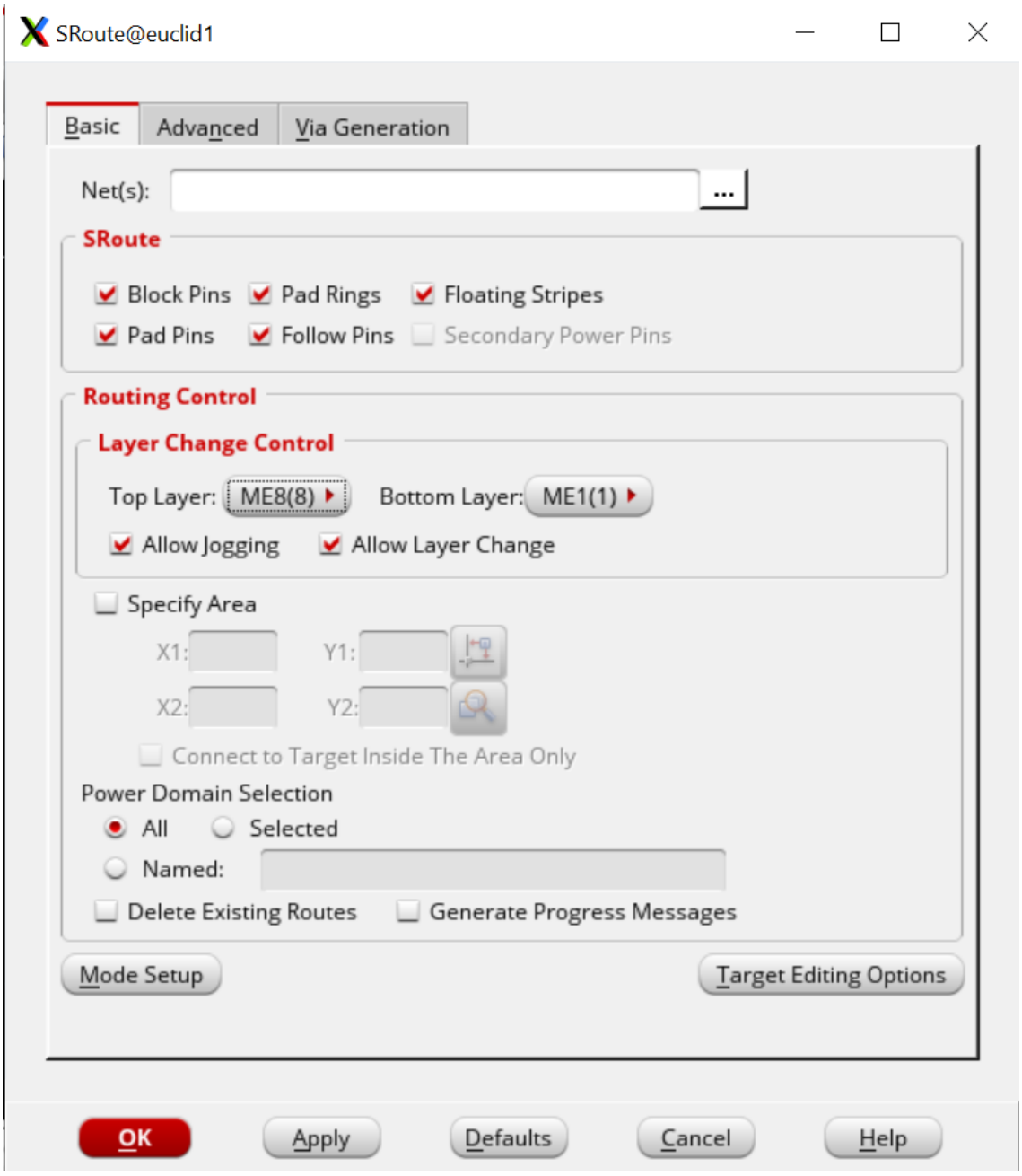
Creating Rings and Stripes for delivering power to standard cells

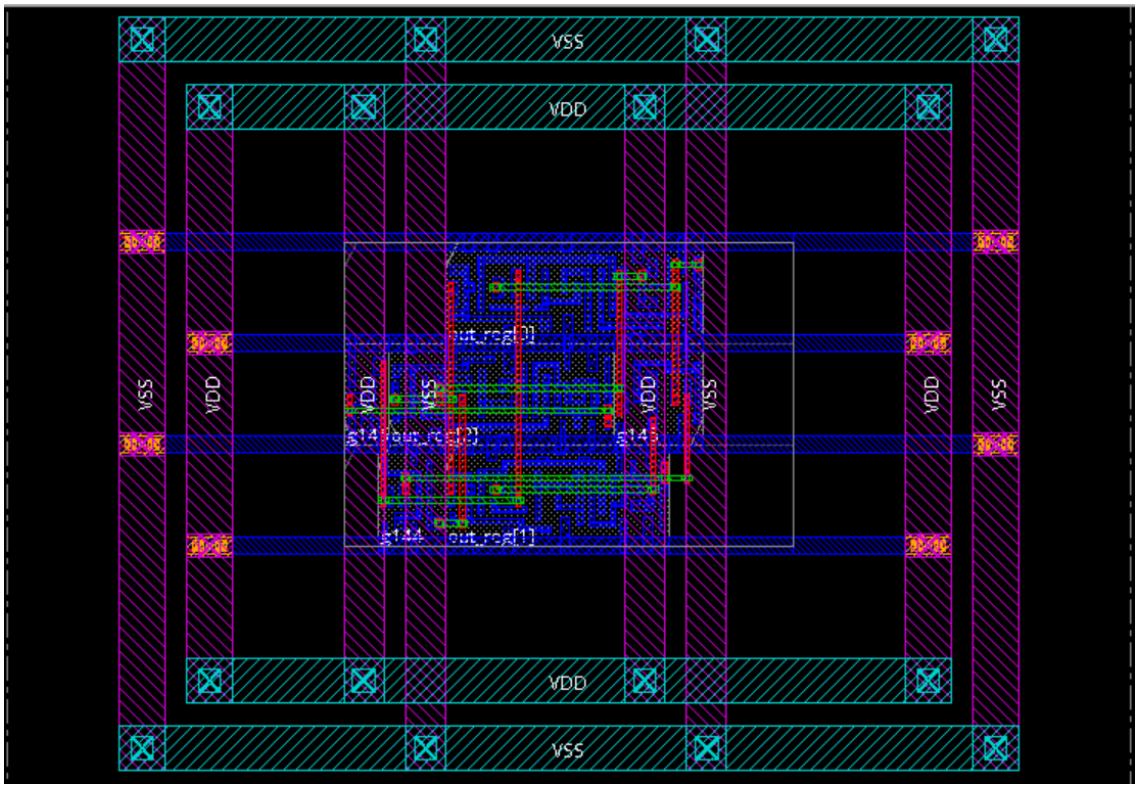


Top-Bottom Power Rail: ME8

Left-Right Power Rails : ME7

3) Standard Cell Placement and auto-routing





PRE-CTS Timing reports:

innovus 1> Setting timing_disable_library_data_to_data_checks to 'true'.
Setting timing_disable_user_data_to_data_checks to 'true'.
Start to check current routing status for nets...
All nets are already routed correctly.
End to check current routing status for nets (mem=1470.3M)
Extraction called for design 'mod5_up' of instances=6 and nets=11 using extraction engine 'preRoute' .
**WARN: (IMPEXT-3530): The process node is not set. Use the command setDesignMode -process <process node> prior to extraction for maximum accuracy and optimal automatic threshold setting.
Type 'man IMPEXT-3530' for more detail.
PreRoute RC Extraction called for design mod5_up.
RC Extraction called in multi-corner(1) mode.
**WARN: (IMPEXT-6166): Capacitance table file(s) without the EXTENDED section is being used for RC extraction. This is not recommended because it results in lower accuracy for clock nets in preRoute extraction and for all nets in postRoute extraction using -

effortLevel low. Regenerate capacitance table file(s) using the generateCapTbl command.
Type 'man IMPEXT-6166' for more detail.
RCMode: PreRoute
    RC Corner Indexes   0
Capacitance Scaling Factor   : 1.00000
Resistance Scaling Factor   : 1.00000
Clock Cap. Scaling Factor   : 1.00000
Clock Res. Scaling Factor   : 1.00000
Shrink Factor   : 1.00000
PreRoute extraction is honoring NDR/Shielding/ExtraSpace for clock nets.
Using capacitance table file ...
Updating RC grid for preRoute extraction ...
Initializing multi-corner resistance tables ...
PreRoute RC Extraction DONE (CPU Time: 0:00:00.0 Real Time: 0:00:00.0 MEM: 1470.258M)
##
######################
Design Stage: PreRoute
Design Name: mod5_up
Design Mode: 90nm
Analysis Mode: MMMC Non-OCV
Parasitics Mode: No SPEF/RCDB
Signoff Settings: SI Off
##
######################
AAE_INFO: 1 threads acquired from CTE.
Calculate delays in Single mode...
Total number of fetched objects 9
AAE_INFO: Total number of nets for which stage creation was skipped for all views 0
End delay calculation. (MEM=1564.71 CPU=0:00:00.0 REAL=0:00:00.0)
*** Done Building Timing Graph (cpu=0:00:00.2 real=0:00:00.0 totSessionCpu=0:01:39 mem=1564.7M)

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timeDesign Summary

Setup views included:
worst_case

Setup mode	all	reg2reg	default
WNS (ns):	8.727	9.554	8.727
TNS (ns):	0.000	0.000	0.000
Violating Paths:	0	0	0
All Paths:	9	6	6

DRVs	Real		Total	
	Nr nets(terms)	Worst Vio	Nr nets(terms)	
max_cap	0 (0)	0.000	0 (0)	
max_tran	0 (0)	0.000	0 (0)	
max_fanout	0 (0)	0	0 (0)	
max_length	0 (0)	0	0 (0)	

Density: 67.500%
Routing Overflow: 0.00% H and 0.00% V

Reported timing to dir timingReports
Total CPU time: 0.28 sec
Total Real time: 0.0 sec
Total Memory Usage: 1509.476562 Mbytes