INTEGRATED ELECTRONIC CIRCUITS LAB

PROGRESS REPORT – TASK 1

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Problem Statement:

Design a mod-5 synchronous counter using JK Flip Flop. Frequency of operation should be 250MHz. Take PMOS width to be 400nm and NMOS width to be 200nm.

Draw a layout for the entire design from scratch and aim for minimum possible area with a rectangular shaped layout with height as 1400nm and width 70um.

Results achieved:

The complete layout for the Mod-5 synchronous counter has been made. Schematic-level simulation at the required clock frequency was achieved using ADE-L tool.

Layout v/s schematic (LVS) and Design Rule Check (DRC) have been cleared for the top-level schematic as well as the instantiated gates.

PEX report generated according to the layout and the parasitic-containing netlist was obtained.

Post Layout simulation done for the JK flip to estimate transient behaviour and maximum frequency of operation

Technology used:

UMC 65nm technology

Library: UMC65LLSC

Model Parameters

1) N_12_LLRVT:
   VDD=1.2V
   Beta0 = 15.9, for W=200nm
   Cgd = 59.9pF
   Cgs = 102.12pF
   Vth = 374.32 mV

2) P_12_LLRVT
   VDD=1.2V
   Beta0 = 17.87 , for W=400nm
   Cgd = 26.144pF
   Cgs = 143pF
   Vth= -311.1 mV

Design of MOD 5 synchronous counter

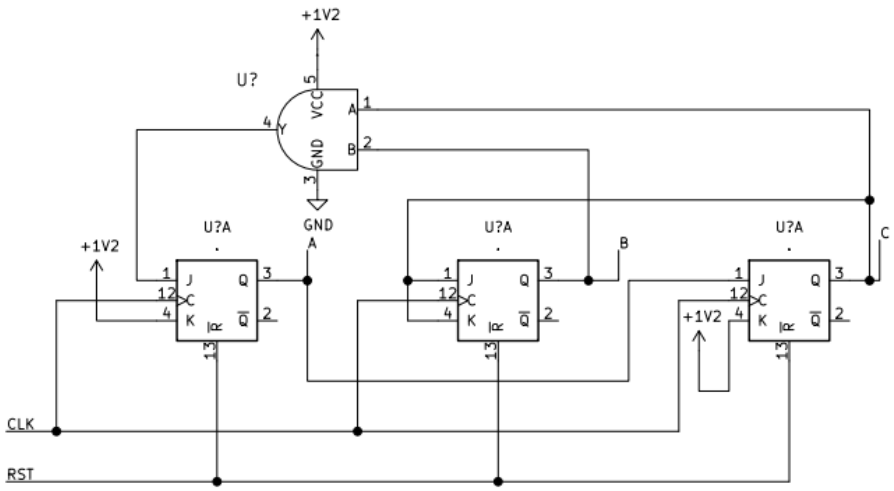


Figure 1: Schematic design of the MOD-5 synchronous counter

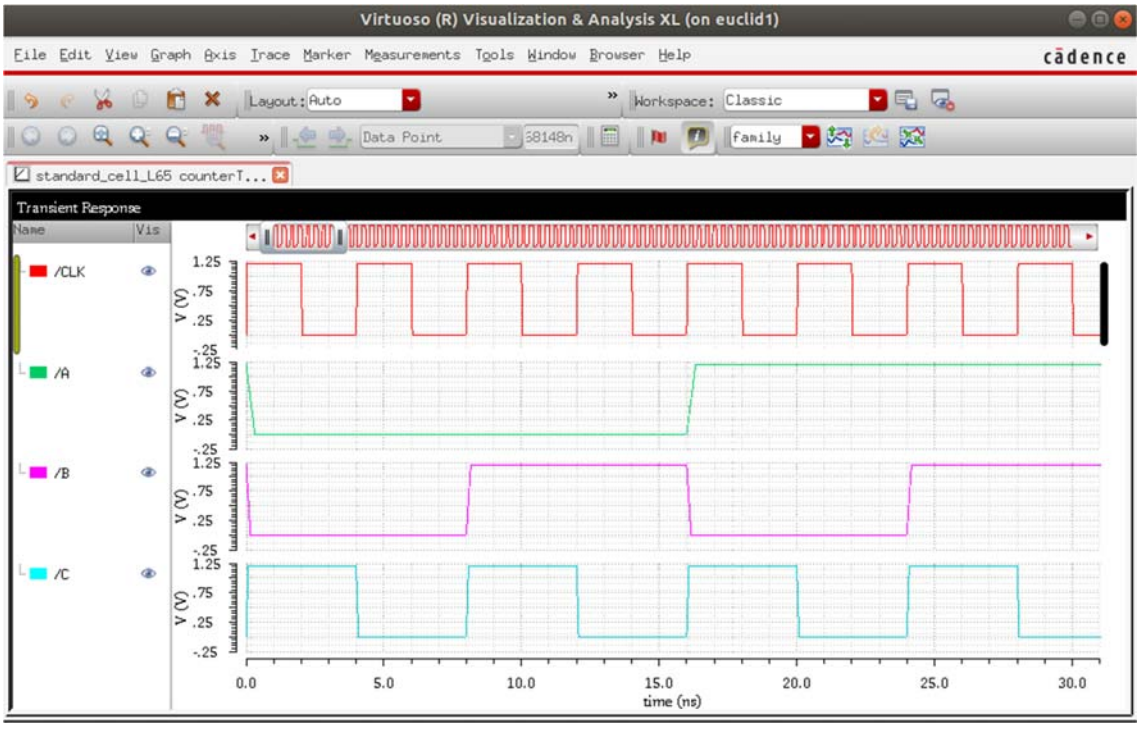


Figure 2: Initial simulation for verification of schematic

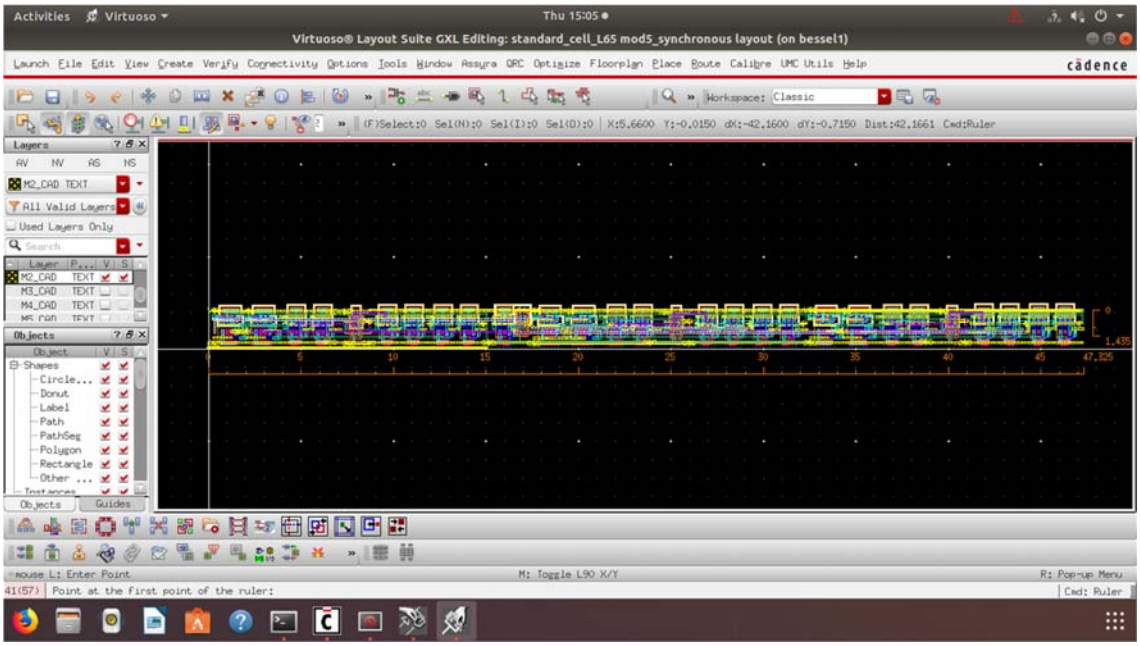


Figure 3: Top-view of overall layout of MOD-5 synchronous counters mad with Master-Slave JK flip flops. Horizontal length is 47.325 micron.

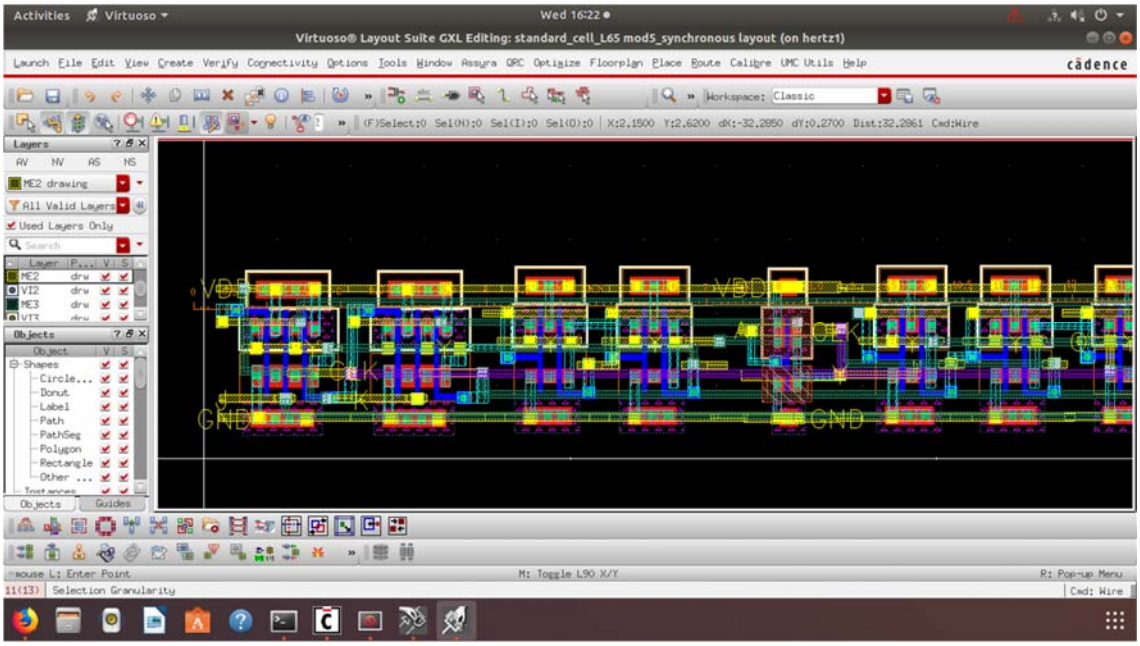


Figure 4: Instantiated gates used in design of mod-5 synchronous counter

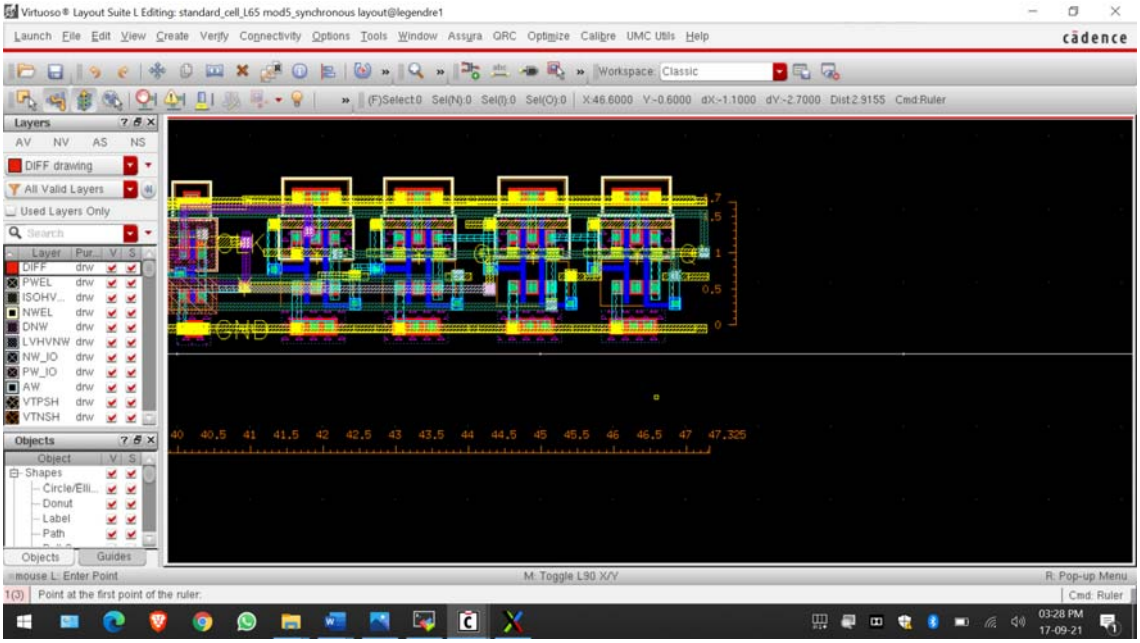


Figure 5: Vertical height: 1.7um

STANDARD JK FLIP FLOP DESIGN AND RACE AROUND CONDITION

For J-K flip-flop, if J=K=1, and if clk=1 for a long period of time, then Q output will toggle as long as CLK is high, which makes the output of the flip-flop unstable or uncertain. This problem is called race around condition in J-K flip-flop. This problem (Race Around Condition) can be avoided by ensuring that the clock input is at logic “1” only for a very short time. This can be achieved using a Master-Slave JK flip flop.

This problem leads to unpredictable results in the operation of the counter.

The initial flip flop designed had the following schematic.

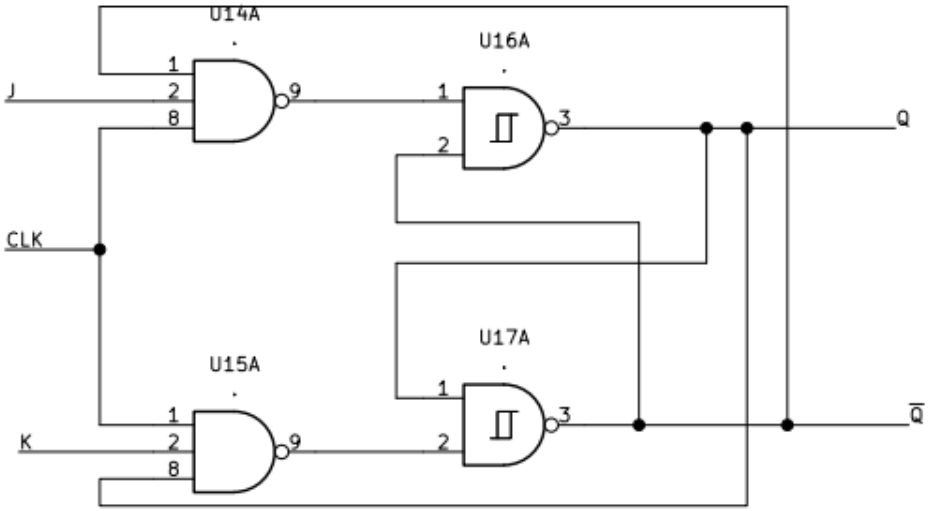


Figure 6: Schematic of simple level-triggered JK flip flop

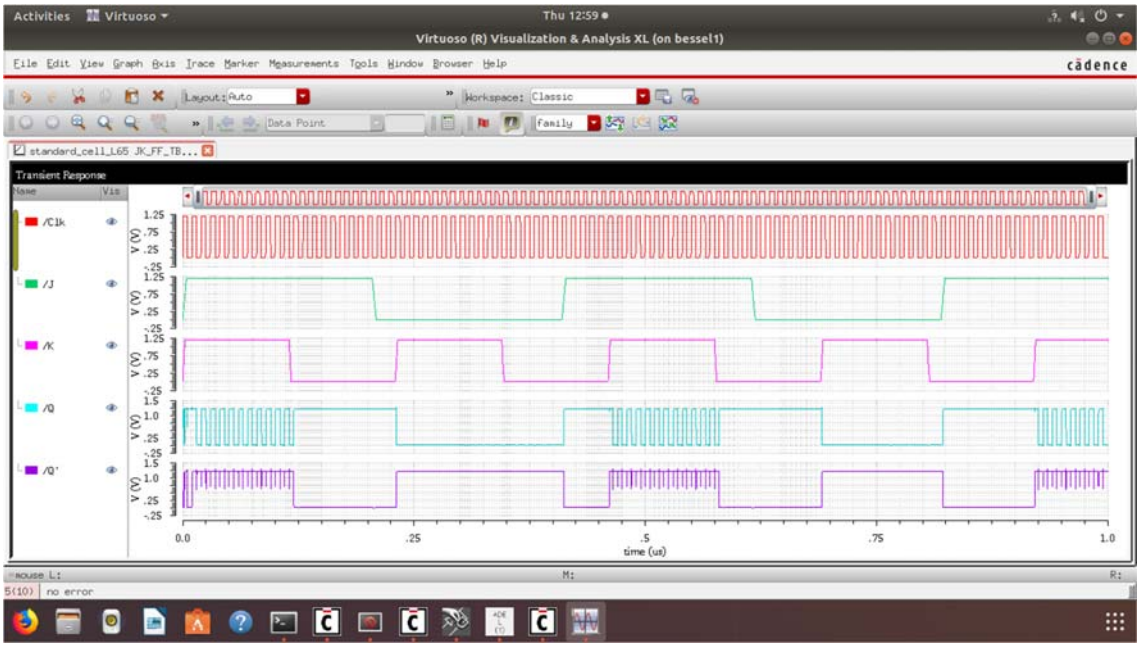


Figure 7: JK Flip Flop Test bench results. With clock frequency at 250MHz output is corrupted in case of J=K=1. Race Around condition is mitigated using master slave latch technique

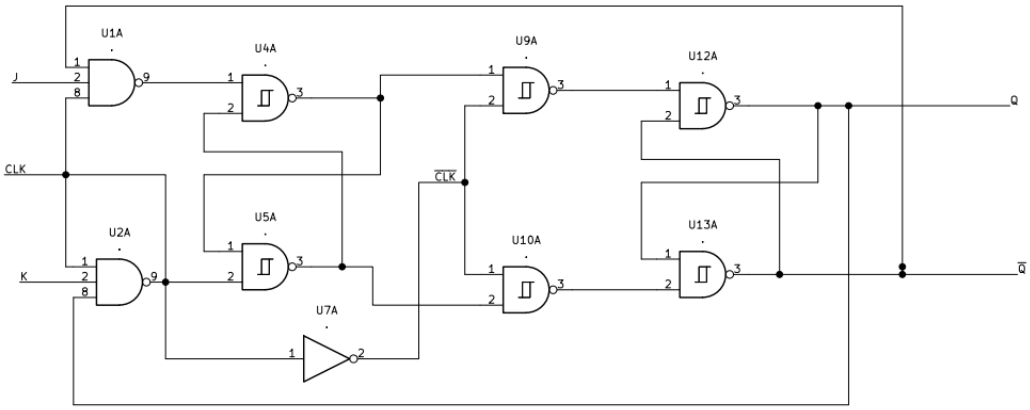


Figure 8: Master-Slave JK flip flop to avoid Race Around when toggle input is applied

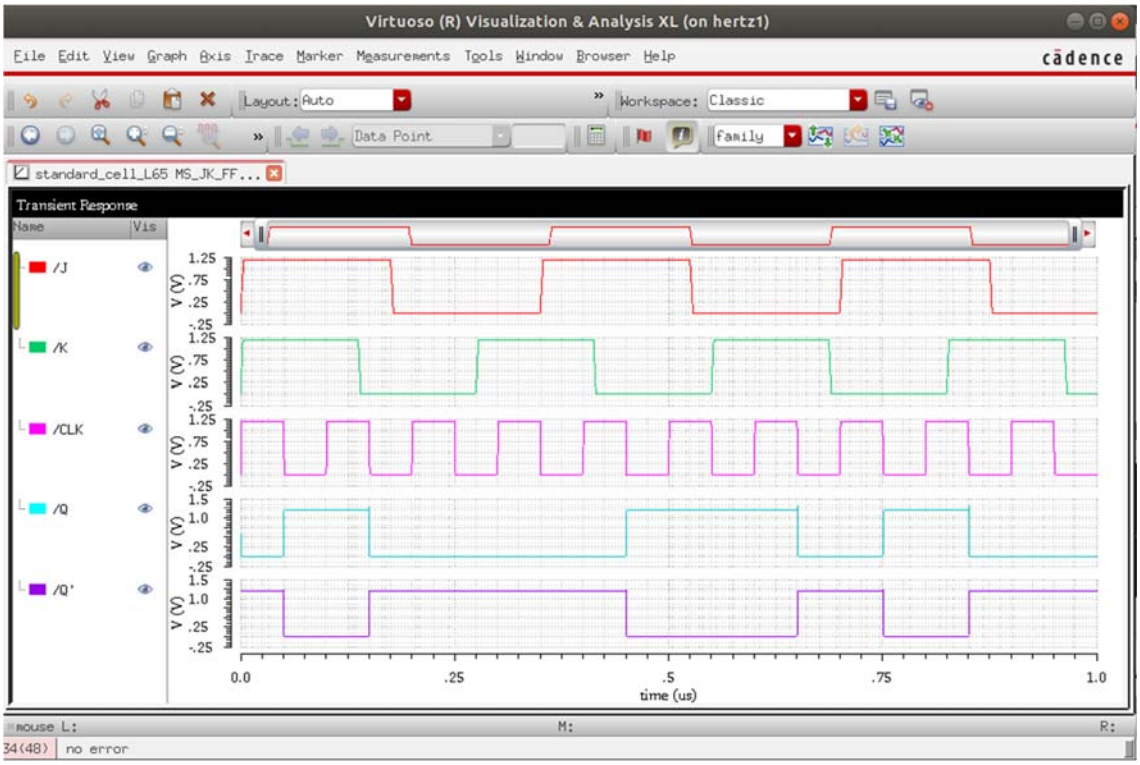


Figure 9: Simulation Results for Master-Slave JK Flop Flop

POST LAYOUT SIMULATION OF JK FLIP FLOP WITH EXTRACTED PARASITICS

After completing the CALIBRE LPE, a PEX netlist is generated and opened in CalibreView.

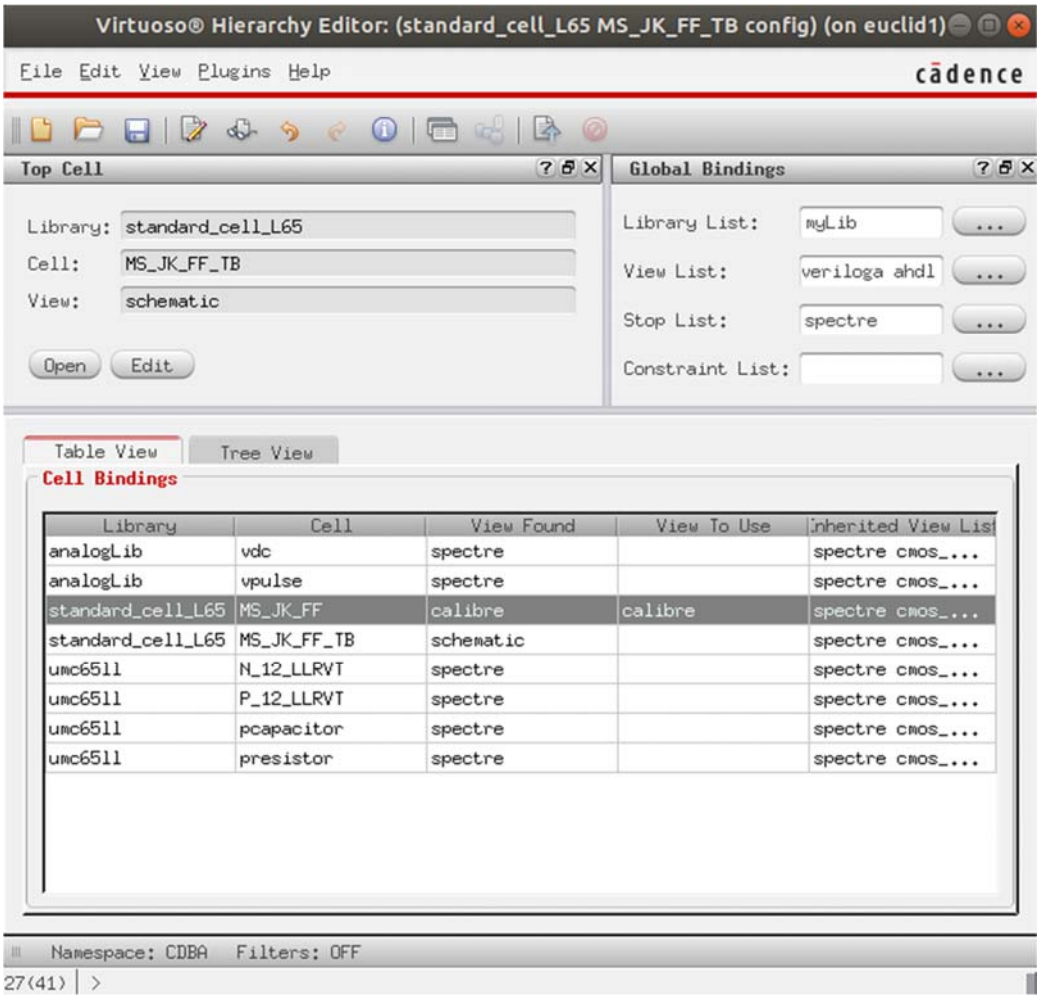


Figure 10: Post layout configuration for simulation using Spectre

Estimation of Clock-to-Q delay:

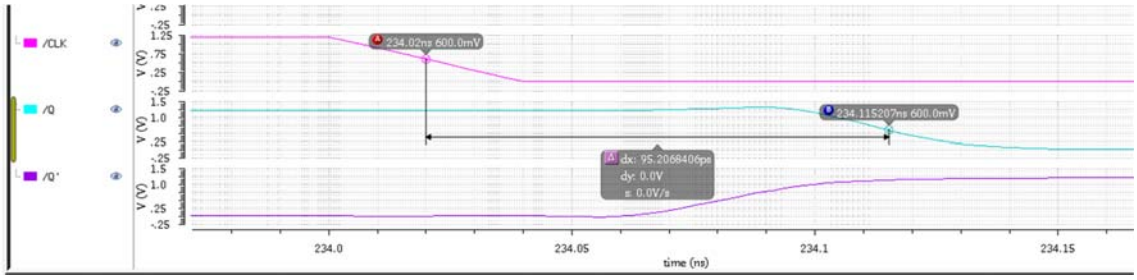


Figure 11: Evaluating CLK-Q time from the ADE-L plot

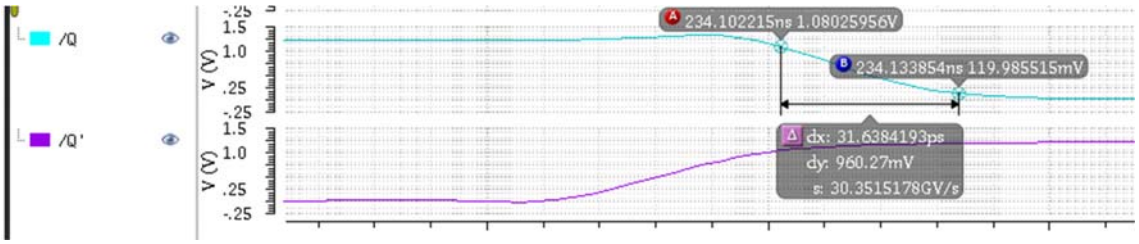


Figure 12: Post layout output fall-time estimation

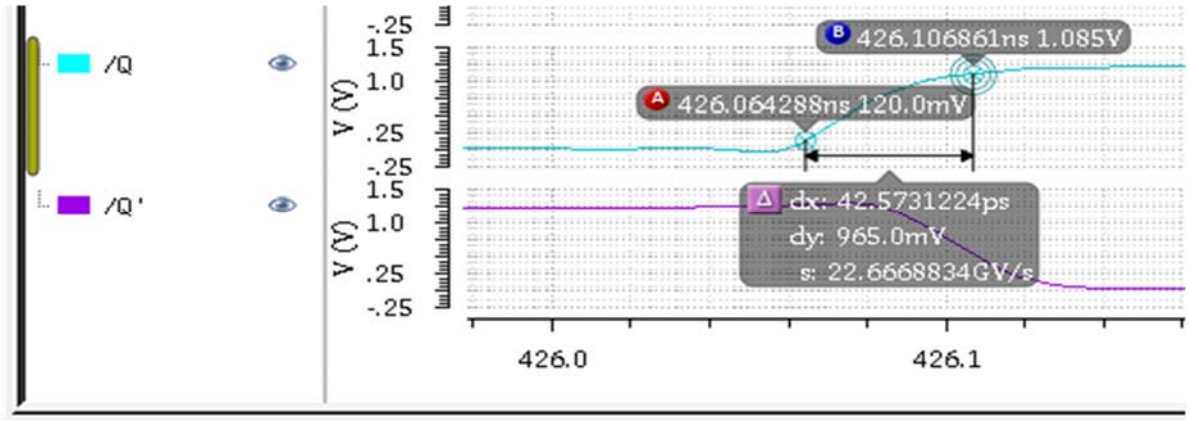


Figure 13: Post layout output rise time estimation

Figure 14: Setup time for JK flip flop with parasitics

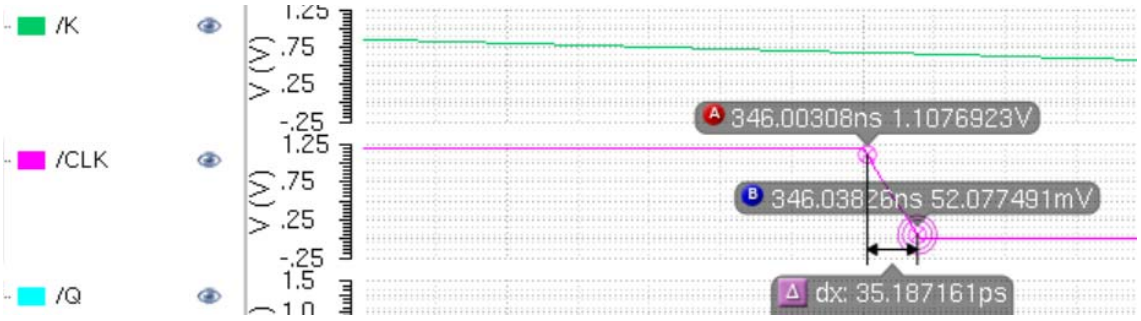


Figure 14: Clock Skew estimation

From figure 11, we find that the propagation delay between the triggering edge (negative) of the clock and the output of the flipflop 'Q' is:

$$T_{\{CLK \to Q\}} = 95.2ps$$

The rise and fall times (delay between 90% of VDD and 10% of VDD) of the output Q are found as shown in figure 12 and 13:

$$T_{rise} = 42.3ps$$

$$T_{fall} = 31.6ps$$

The fall time of the clock is required for estimating the setup and hold time, from figure 14,

$$T_{clkskw} = 35.18ps$$

Now to find maximum frequency of operation, we will use the relation:

$$T_{\{CLK \to Q\}} + T_{setup} + T_{rise} + T_{fall} \leq T_{period}$$

$$T_{period} \geq 2.97ns + 95.2ps + 42.3ps + 31.6ps + 40ps$$

$$f_{clk} \leq \frac{1}{4.661ns}$$

$$f_{clk} \leq 214.5\ MHz$$

Parasitics extraction for interconnects using Calibre LPE (PEX Report)

Configuration used for PEX analysis

```
################################################################
##                                            ##
##          C A L I B R E   S Y S T E M       ##
##                                            ##
##  C I R C U I T   E X T R A C T I O N   R E P O R T  ##
##                                            ##
################################################################
```

REPORT FILE NAME: mod5_synchronous.pex.report.ext
LAYOUT NAME: mod5_synchronous.calibre.db ('mod5_synchronous')
CREATION TIME: Fri Sep 17 11:15:01 2021
CURRENT DIRECTORY: /afs/iitd.ac.in/user/e/ee/eey217501/mod5counter/PEXreport
USER NAME: eey217501
CALIBRE VERSION: v2020.4_34.17 Tue Dec 1 16:11:11 PST 2020

Layout_Net	Source_Net	R_Count	C_Total(F)	CC_Total(F)	C+CC_Total(F)	
VDD	VDD	796	1.53242E-15	9.40800E-15	1.09404E-14	
2	XI3/NET15	36	1.10430E-16	6.21192E-16	7.31622E-16	
C	C	148	5.90236E-16	6.55313E-15	7.14337E-15	
4	NET12	45	1.81194E-16	2.19511E-15	2.37630E-15	
B	B	131	4.50150E-16	5.65274E-15	6.10289E-15	
CLK	CLK	289	1.09954E-15	1.09186E-14	1.20182E-14	
7	NET022	127	4.27988E-16	5.85627E-15	6.28426E-15	
8	NET021	96	2.96259E-16	2.75420E-15	3.05046E-15	
9	NET1	96	3.15511E-16	2.59994E-15	2.91545E-15	
GND	GND	549	1.34142E-15	6.77075E-15	8.11217E-15	
A	A	77	2.93907E-16	2.44240E-15	2.73631E-15	
X4/6	XI3/XI0/NET17	2	2.31160E-19	9.17458E-17	9.19770E-17	
X7/8	XI4/NET29	81	2.65607E-16	2.05092E-15	2.31653E-15	
X7/9	XI4/NET34	70	1.70788E-16	1.63965E-15	1.81044E-15	
X7/10	XI4/NET28	85	2.48383E-16	1.78805E-15	2.03644E-15	
X7/11	XI4/NET32	54	1.50182E-16	1.50397E-15	1.65415E-15	
X7/12	XI4/NET020	57	2.64275E-16	1.23758E-15	1.50186E-15	
X7/13	XI4/NET24	39	1.69020E-16	9.94757E-16	1.16378E-15	
X7/14	XI4/NET33	39	1.59358E-16	9.46333E-16	1.10569E-15	
X7/X6/7	XI4/XI5/NET24	2	1.32510E-19	8.97519E-17	8.98844E-17	$
X7/X6/8	XI4/XI5/NET25	2	1.72219E-19	9.79210E-17	9.80932E-17	$
X7/X7/7	XI4/XI6/NET24	2	2.28777E-19	9.20803E-17	9.23091E-17	$
X7/X7/8	XI4/XI6/NET25	2	6.28996E-19	9.89091E-17	9.95381E-17	$
X7/X8/6	XI4/XI2/NET17	2	4.48563E-19	9.38980E-17	9.43466E-17	$
X7/X9/6	XI4/XI3/NET17	2	5.63944E-19	8.94067E-17	8.99707E-17	$
X7/X10/X4/6	XI4/XI1/XI0/NET17	2	3.16182E-19	8.98851E-17	9.02012E-17	$
X7/X10/X5/6	XI4/XI1/XI1/NET17	2	2.27518E-19	9.00382E-17	9.02658E-17	$
X7/X11/X4/6	XI4/XI0/XI0/NET17	2	2.31160E-19	9.12319E-17	9.14630E-17	$
X8/X11/X4/6	XI5/XI0/XI0/NET17	2	2.31160E-19	9.33739E-17	9.36051E-17	$
X8/X11/X5/6	XI5/XI0/XI1/NET17	2	2.31160E-19	9.28237E-17	9.30549E-17	$
X9/8	XI6/NET29	81	2.65705E-16	1.87085E-15	2.13656E-15	$
X9/9	XI6/NET34	70	1.69428E-16	1.62220E-15	1.79163E-15	$
X9/10	XI6/NET28	85	2.47762E-16	1.74787E-15	1.99563E-15	$

X9/11	XI6/NET32	54	1.57363E-16	1.30926E-15	1.46663E-15	$
X9/12	XI6/NET020	57	2.66434E-16	1.24997E-15	1.51641E-15	$
X9/13	XI6/NET24	39	1.68842E-16	9.85984E-16	1.15483E-15	$
X9/14	XI6/NET33	39	1.53326E-16	9.08239E-16	1.06157E-15	$
X9/X6/7	XI6/XI5/NET24	2	1.92904E-19	9.57440E-17	9.59369E-17	$
X9/X6/8	XI6/XI5/NET25	2	7.05155E-19	1.01262E-16	1.01967E-16	$
X9/X7/7	XI6/XI6/NET24	2	3.82975E-19	9.43659E-17	9.47489E-17	$
X9/X7/8	XI6/XI6/NET25	2	7.99066E-19	1.01253E-16	1.02052E-16	$
X9/X8/6	XI6/XI2/NET17	2	3.54994E-19	9.56559E-17	9.60109E-17	$
X9/X9/6	XI6/XI3/NET17	2	2.21608E-19	9.11581E-17	9.13797E-17	$
X9/X10/X4/6	XI6/XI1/XI0/NET17	2	4.56759E-19	9.11254E-17	9.15822E-17	$
X9/X10/X5/6	XI6/XI1/XI1/NET17	2	3.76559E-19	9.12548E-17	9.16313E-17	$
X9/X11/X4/6	XI6/XI0/XI0/NET17	2	2.09898E-19	8.88154E-17	8.90253E-17	$
X9/X11/X5/6	XI6/XI0/XI1/NET17	2	2.09898E-19	8.82976E-17	8.85075E-17	$

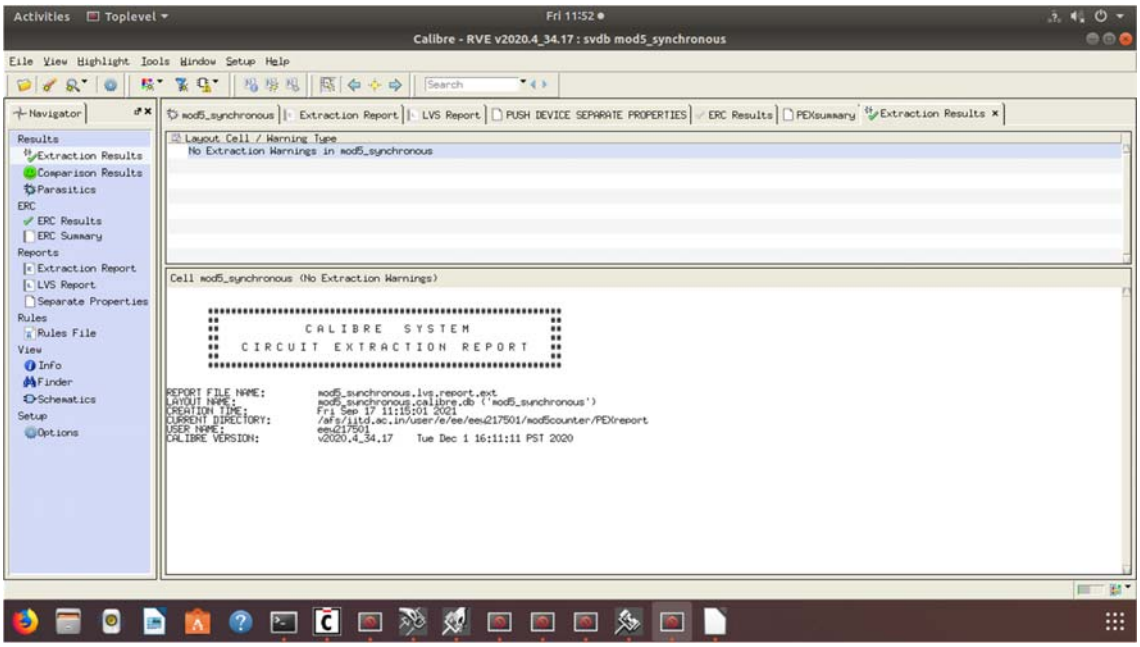


Figure 15: PEX result window

LVS Report for the layout and schematic of MOD-5 counter

eey217501@bessel:~/mod5counter/LVS$ cat mod5_synchronous.lvs.report

```
################################################
##                                            ##
##      C A L I B R E   S Y S T E M           ##
```

```
##                          ##
##        L V S  R E P O R T       ##
##                          ##
##################################################
```

REPORT FILE NAME: mod5_synchronous.lvs.report
LAYOUT NAME: /afs/iitd.ac.in/user/e/ee/eey217501/mod5counter/LVS/mod5_synchronous.sp ('mod5_synchronous')
SOURCE NAME: /afs/iitd.ac.in/user/e/ee/eey217501/mod5counter/LVS/mod5_synchronous.src.net ('mod5_synchronous')
RULE FILE: /afs/iitd.ac.in/user/e/ee/eey217501/mod5counter/LVS/_G-DF-LOGIC_MIXED_MODE65N-LL_LOW_K_CALIBRE-LVS-1.6-P4.txt_
RULE FILE TITLE: UMC Calibre LVS 65nm LOGIC/MIXED MODE Low Leakage Low-K Process
CREATION TIME: Thu Sep 16 14:54:14 2021
CURRENT DIRECTORY: /afs/iitd.ac.in/user/e/ee/eey217501/mod5counter/LVS
USER NAME: eey217501
CALIBRE VERSION: v2020.4_34.17 Tue Dec 1 16:11:11 PST 2020

OVERALL COMPARISON RESULTS

```
   #    ###################    _ _
  #     #          #     *  *
 # #     #   CORRECT    #     |
 ##      #          #    \___/
  #      ###################
```

****
CELL SUMMARY
****

Result	Layout	Source
CORRECT	mod5_synchronous	mod5_synchronous

****
LVS PARAMETERS
****

o LVS Setup:

```
// LVS COMPONENT TYPE PROPERTY
// LVS COMPONENT SUBTYPE PROPERTY
// LVS PIN NAME PROPERTY
LVS POWER NAME "?VCC?" "?VDD?"
```

```
LVS GROUND NAME                    "?GND?" "?VSS?"
LVS CELL SUPPLY                    NO
LVS RECOGNIZE GATES                ALL
// LVS HCELL REPORT
LVS IGNORE PORTS                   NO
LVS CHECK PORT NAMES               YES
LVS IGNORE TRIVIAL NAMED PORTS     NO
LVS BUILTIN DEVICE PIN SWAP        NO
LVS ALL CAPACITOR PINS SWAPPABLE   NO
LVS DISCARD PINS BY DEVICE         NO
LVS SOFT SUBSTRATE PINS            NO
LVS INJECT LOGIC                   NO
LVS EXPAND UNBALANCED CELLS        YES
LVS FLATTEN INSIDE CELL            NO
LVS EXPAND SEED PROMOTIONS         YES
LVS PRESERVE PARAMETERIZED CELLS   NO
LVS GLOBALS ARE PORTS              YES
LVS REVERSE WL                     NO
LVS SPICE PREFER PINS              NO
LVS SPICE SLASH IS SPACE           YES
LVS SPICE ALLOW FLOATING PINS      YES
// LVS SPICE ALLOW INLINE PARAMETERS
LVS SPICE ALLOW UNQUOTED STRINGS   NO
LVS SPICE CONDITIONAL LDD          NO
LVS SPICE CULL PRIMITIVE SUBCIRCUITS   NO
// LVS SPICE EXCLUDE CELL SOURCE
// LVS SPICE EXCLUDE CELL LAYOUT
LVS SPICE IMPLIED MOS AREA         NO
// LVS SPICE MULTIPLIER NAME
LVS SPICE OVERRIDE GLOBALS         NO
LVS SPICE REDEFINE PARAM           NO
LVS SPICE REPLICATE DEVICES        YES
LVS SPICE SCALE X PARAMETERS       NO
LVS SPICE STRICT WL                NO
// LVS SPICE OPTION
LVS STRICT SUBTYPES                NO
LVS EXACT SUBTYPES                 NO
LAYOUT CASE                        NO
SOURCE CASE                        NO
LVS COMPARE CASE                   NO
LVS COMPARE CASE STRICT            NO
LVS DOWNCASE DEVICE                NO
LVS REPORT MAXIMUM                 50
LVS PROPERTY RESOLUTION MAXIMUM    32
// LVS SIGNATURE MAXIMUM
// LVS FILTER UNUSED OPTION
// LVS REPORT OPTION
LVS REPORT UNITS                   YES
// LVS NON USER NAME PORT
// LVS NON USER NAME NET
// LVS NON USER NAME INSTANCE
// LVS IGNORE DEVICE PIN
// LVS PREFER NETS FILTER SOURCE
// LVS PREFER NETS FILTER LAYOUT
LVS PREFER PORT NETS               NO
LVS EXPAND ON ERROR                NO

// Reduction

LVS REDUCE SERIES MOS              NO
```

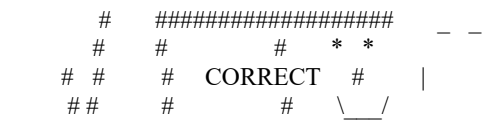
```
LVS REDUCE PARALLEL MOS              YES
LVS REDUCE SEMI SERIES MOS           NO
LVS REDUCE SPLIT GATES               YES
LVS REDUCE PARALLEL BIPOLAR          YES
LVS REDUCE SERIES CAPACITORS         YES
LVS REDUCE PARALLEL CAPACITORS       YES
LVS REDUCE SERIES RESISTORS          YES
LVS REDUCE PARALLEL RESISTORS        YES
LVS REDUCE PARALLEL DIODES           YES

LVS REDUCE  C(MIMCAPS_20F_MM)  PARALLEL NO
LVS REDUCE  C(NCAP_12_LL)  PARALLEL NO
LVS REDUCE  C(PCAP_12_LL)  PARALLEL NO
LVS REDUCE  C(NCAP_25_LL)  PARALLEL NO
LVS REDUCE  C(PCAP_25_LL)  PARALLEL NO
LVS REDUCTION PRIORITY               PARALLEL

LVS SHORT EQUIVALENT NODES           NO

// Trace Property

TRACE PROPERTY  n_12_llrvtrf  lf lf 3
TRACE PROPERTY  n_12_llrvtrf  wf wf 3
TRACE PROPERTY  n_12_llrvtrf  nf nf 0
TRACE PROPERTY  n_12_llrvtrf  con con 0
TRACE PROPERTY  p_12_llrvtrf  lf lf 3
TRACE PROPERTY  p_12_llrvtrf  wf wf 3
TRACE PROPERTY  p_12_llrvtrf  nf nf 0
TRACE PROPERTY  p_12_llrvtrf  con con 0
TRACE PROPERTY  n_bpw_12_llrvtrf  lf lf 3
TRACE PROPERTY  n_bpw_12_llrvtrf  wf wf 3
TRACE PROPERTY  n_bpw_12_llrvtrf  nf nf 0
TRACE PROPERTY  n_bpw_12_llrvtrf  con con 0
TRACE PROPERTY  n_12_llhvtrf  lf lf 3
TRACE PROPERTY  n_12_llhvtrf  wf wf 3
TRACE PROPERTY  n_12_llhvtrf  nf nf 0
TRACE PROPERTY  n_12_llhvtrf  con con 0
TRACE PROPERTY  p_12_llhvtrf  lf lf 3
TRACE PROPERTY  p_12_llhvtrf  wf wf 3
TRACE PROPERTY  p_12_llhvtrf  nf nf 0
TRACE PROPERTY  p_12_llhvtrf  con con 0
TRACE PROPERTY  n_bpw_12_llhvtrf  lf lf 3
TRACE PROPERTY  n_bpw_12_llhvtrf  wf wf 3
TRACE PROPERTY  n_bpw_12_llhvtrf  nf nf 0
TRACE PROPERTY  n_bpw_12_llhvtrf  con con 0
TRACE PROPERTY  n_12_lllvtrf  lf lf 3
TRACE PROPERTY  n_12_lllvtrf  wf wf 3
TRACE PROPERTY  n_12_lllvtrf  nf nf 0
TRACE PROPERTY  n_12_lllvtrf  con con 0
TRACE PROPERTY  p_12_lllvtrf  lf lf 3
TRACE PROPERTY  p_12_lllvtrf  wf wf 3
TRACE PROPERTY  p_12_lllvtrf  nf nf 0
TRACE PROPERTY  p_12_lllvtrf  con con 0
TRACE PROPERTY  n_bpw_12_lllvtrf  lf lf 3
TRACE PROPERTY  n_bpw_12_lllvtrf  wf wf 3
TRACE PROPERTY  n_bpw_12_lllvtrf  nf nf 0
TRACE PROPERTY  n_bpw_12_lllvtrf  con con 0
TRACE PROPERTY  n_25_llrf  lf lf 3
TRACE PROPERTY  n_25_llrf  wf wf 3
TRACE PROPERTY  n_25_llrf  nf nf 0
```

```
TRACE PROPERTY  n_25_llrf  con con 0
TRACE PROPERTY  p_25_llrf  lf lf 3
TRACE PROPERTY  p_25_llrf  wf wf 3
TRACE PROPERTY  p_25_llrf  nf nf 0
TRACE PROPERTY  p_25_llrf  con con 0
TRACE PROPERTY  n_bpw_25_llrf  lf lf 3
TRACE PROPERTY  n_bpw_25_llrf  wf wf 3
TRACE PROPERTY  n_bpw_25_llrf  nf nf 0
TRACE PROPERTY  n_bpw_25_llrf  con con 0
TRACE PROPERTY  r(rsnpo_efuse)  r r 3
TRACE PROPERTY  r(rsppo_efuse)  r r 3
TRACE PROPERTY  rnnpo_nw_llrf  r r 3
TRACE PROPERTY  rnnpo_nw_llrf  l l 3
TRACE PROPERTY  rnnpo_nw_llrf  w w 3
TRACE PROPERTY  rnnpo_llrf  r r 3
TRACE PROPERTY  rnnpo_llrf  l l 3
TRACE PROPERTY  rnnpo_llrf  w w 3
TRACE PROPERTY  rnppo_nw_llrf  r r 3
TRACE PROPERTY  rnppo_nw_llrf  l l 3
TRACE PROPERTY  rnppo_nw_llrf  w w 3
TRACE PROPERTY  rnppo_llrf  r r 3
TRACE PROPERTY  rnppo_llrf  l l 3
TRACE PROPERTY  rnppo_llrf  w w 3
TRACE PROPERTY  rnhr_nw_llrf  r r 3
TRACE PROPERTY  rnhr_nw_llrf  l l 3
TRACE PROPERTY  rnhr_nw_llrf  w w 3
TRACE PROPERTY  rnhr_llrf  r r 3
TRACE PROPERTY  rnhr_llrf  l l 3
TRACE PROPERTY  rnhr_llrf  w w 3
TRACE PROPERTY  r(fuse)  r r 3
TRACE PROPERTY  r(ral)  r r 3
TRACE PROPERTY  varmis_12_llrf  lf lf 3
TRACE PROPERTY  varmis_12_llrf  wf wf 3
TRACE PROPERTY  varmis_12_llrf  nf nf 0
TRACE PROPERTY  varmis_12_llrf  array array 0
TRACE PROPERTY  varmis_25_llrf  lf lf 3
TRACE PROPERTY  varmis_25_llrf  wf wf 3
TRACE PROPERTY  varmis_25_llrf  nf nf 0
TRACE PROPERTY  varmis_25_llrf  array array 0
TRACE PROPERTY  vardiop_llrf  l l 3
TRACE PROPERTY  vardiop_llrf  wp wp 3
TRACE PROPERTY  vardiop_llrf  nf nf 0
TRACE PROPERTY  vardiop_llrf  c c 3
TRACE PROPERTY  d(dionw_ll)  a a 3
TRACE PROPERTY  d(dionw_ll)  p p 3
TRACE PROPERTY  d(diodnw_ll)  a a 3
TRACE PROPERTY  d(diodnw_ll)  p p 3
TRACE PROPERTY  d(diodp_ll)  a a 3
TRACE PROPERTY  d(diodp_ll)  p p 3
TRACE PROPERTY  momcaps_sy_mmkf  nf nf 0
TRACE PROPERTY  momcaps_sy_mmkf  l l 3
TRACE PROPERTY  momcaps_sy_mmkf  nm nm 0
TRACE PROPERTY  momcaps_sy_mmkf  bm bm 0
TRACE PROPERTY  momcaps_as_mmkf  nf nf 0
TRACE PROPERTY  momcaps_as_mmkf  l l 3
TRACE PROPERTY  momcaps_as_mmkf  nm nm 0
TRACE PROPERTY  momcaps_as_mmkf  bm bm 0
TRACE PROPERTY  momcaps_symesh_mmkf  nf nf 0
TRACE PROPERTY  momcaps_symesh_mmkf  mh mh 0
TRACE PROPERTY  momcaps_symesh_mmkf  nm nm 0
```

```
TRACE PROPERTY  momcaps_symesh_mmkf  bm bm 0
TRACE PROPERTY  momcaps_symesh_mmkf  l l 3
TRACE PROPERTY  momcaps_asmesh_mmkf  nf nf 0
TRACE PROPERTY  momcaps_asmesh_mmkf  mh mh 0
TRACE PROPERTY  momcaps_asmesh_mmkf  nm nm 0
TRACE PROPERTY  momcaps_asmesh_mmkf  bm bm 0
TRACE PROPERTY  momcaps_asmesh_mmkf  l l 3
TRACE PROPERTY  momcaps_array_vp3_rfvcl  bm bm 0
TRACE PROPERTY  momcaps_array_vp3_rfvcl  ns ns 0
TRACE PROPERTY  momcaps_array_vp3_rfvcl  nf nf 0
TRACE PROPERTY  momcaps_array_vp3_rfvcl  array array 0
TRACE PROPERTY  momcaps_array_vp3_rfvcl  lf lf 3
TRACE PROPERTY  momcaps_array_vp4_rfvcl  bm bm 0
TRACE PROPERTY  momcaps_array_vp4_rfvcl  ns ns 0
TRACE PROPERTY  momcaps_array_vp4_rfvcl  nf nf 0
TRACE PROPERTY  momcaps_array_vp4_rfvcl  array array 0
TRACE PROPERTY  momcaps_array_vp4_rfvcl  lf lf 3
TRACE PROPERTY  momcaps_array_vp5_rfvcl  bm bm 0
TRACE PROPERTY  momcaps_array_vp5_rfvcl  ns ns 0
TRACE PROPERTY  momcaps_array_vp5_rfvcl  nf nf 0
TRACE PROPERTY  momcaps_array_vp5_rfvcl  array array 0
TRACE PROPERTY  momcaps_array_vp5_rfvcl  lf lf 3
TRACE PROPERTY  momcaps_array_vp5_rfvcl  sh sh 0
TRACE PROPERTY  l_slcr30k_rfvil  s s 3
TRACE PROPERTY  l_slcr30k_rfvil  w w 3
TRACE PROPERTY  l_slcr30k_rfvil  od od 3
TRACE PROPERTY  l_slcr30k_rfvil  nt nt 0
TRACE PROPERTY  l_syct30k_rfvil  nt nt 0
TRACE PROPERTY  l_syct30k_rfvil  s s 3
TRACE PROPERTY  l_syct30k_rfvil  w w 3
TRACE PROPERTY  l_syct30k_rfvil  od od 3
TRACE PROPERTY  l_sy30k_rfvil  nt nt 0
TRACE PROPERTY  l_sy30k_rfvil  s s 3
TRACE PROPERTY  l_sy30k_rfvil  w w 3
TRACE PROPERTY  l_sy30k_rfvil  od od 3
TRACE PROPERTY  l_sqsk_rfvil  nt nt 0
TRACE PROPERTY  l_sqsk_rfvil  s s 3
TRACE PROPERTY  l_sqsk_rfvil  w w 3
TRACE PROPERTY  l_sqsk_rfvil  od od 3
TRACE PROPERTY  l_sqsk_rfvil  ns ns 0
TRACE PROPERTY  l_sqsk_rfvil  bm bm 0
TRACE PROPERTY  mimcaps_20f_nwell_rfkf  l l 3
TRACE PROPERTY  mimcaps_20f_nwell_rfkf  w w 3
TRACE PROPERTY  mimcaps_20f_psub_rfkf  l l 3
TRACE PROPERTY  mimcaps_20f_psub_rfkf  w w 3
TRACE PROPERTY  mimcaps_20f_m1_rfkf  l l 3
TRACE PROPERTY  mimcaps_20f_m1_rfkf  w w 3
TRACE PROPERTY  c(mimcaps_20f_mm)  c c 3
TRACE PROPERTY  l_sq_trans_rfvil  nt_in nt_in 0
TRACE PROPERTY  l_sq_trans_rfvil  nt_out nt_out 0
TRACE PROPERTY  l_sq_trans_rfvil  w w 3
TRACE PROPERTY  l_sq_trans_rfvil  od od 3
TRACE PROPERTY  l_sqctin_trans_rfvil  nt_in nt_in 0
TRACE PROPERTY  l_sqctin_trans_rfvil  nt_out nt_out 0
TRACE PROPERTY  l_sqctin_trans_rfvil  w w 3
TRACE PROPERTY  l_sqctin_trans_rfvil  od od 3
TRACE PROPERTY  l_sqctout_trans_rfvil  nt_in nt_in 0
TRACE PROPERTY  l_sqctout_trans_rfvil  nt_out nt_out 0
TRACE PROPERTY  l_sqctout_trans_rfvil  w w 3
TRACE PROPERTY  l_sqctout_trans_rfvil  od od 3
```

TRACE PROPERTY l_sqctinout_trans_rfvil nt_in nt_in 0
TRACE PROPERTY l_sqctinout_trans_rfvil nt_out nt_out 0
TRACE PROPERTY l_sqctinout_trans_rfvil w w 3
TRACE PROPERTY l_sqctinout_trans_rfvil od od 3
TRACE PROPERTY l_occtout_trans_rfvil nt_in nt_in 0
TRACE PROPERTY l_occtout_trans_rfvil w w 3
TRACE PROPERTY l_occtout_trans_rfvil od od 3
TRACE PROPERTY pad_rf index_layer index_layer 0
TRACE PROPERTY pad_rf index_thick index_thick 0
TRACE PROPERTY pad_rf index_pad index_pad 0

CELL COMPARISON RESULTS (TOP LEVEL)



LAYOUT CELL NAME: mod5_synchronous
SOURCE CELL NAME: mod5_synchronous

INITIAL NUMBERS OF OBJECTS

	Layout	Source	Component Type
Ports:	6	6	
Nets:	63	63	
Instances:	60	60	MN (4 pins)
	60	60	MP (4 pins)
Total Inst:	120	120	

NUMBERS OF OBJECTS AFTER TRANSFORMATION

	Layout	Source	Component Type
Ports:	6	6	
Nets:	32	32	
Instances:	4	4	INV (2 pins)
	19	19	NAND2 (3 pins)
	6	6	NAND3 (4 pins)
Total Inst:	29	29	

****
INFORMATION AND WARNINGS
****

	Matched Layout	Matched Source	Unmatched Layout	Unmatched Source	Component Type
Ports:	6	6	0	0	
Nets:	32	32	0	0	
Instances:	4	4	0	0	INV
	19	19	0	0	NAND2
	6	6	0	0	NAND3
Total Inst:	29	29	0	0	

o Initial Correspondence Points:

Ports: VDD GND C B CLK A

o Voltage Names Matched by Wildcard:

Power Names from Layout:

VDD

Ground Names from Layout:

GND

Power Names from Source:

VDD

Ground Names from Source:

GND

****
SUMMARY
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Total CPU Time: 0 sec
Total Elapsed Time: 1 sec