OAI321- Complex Gate using Domino

Group Number: 17

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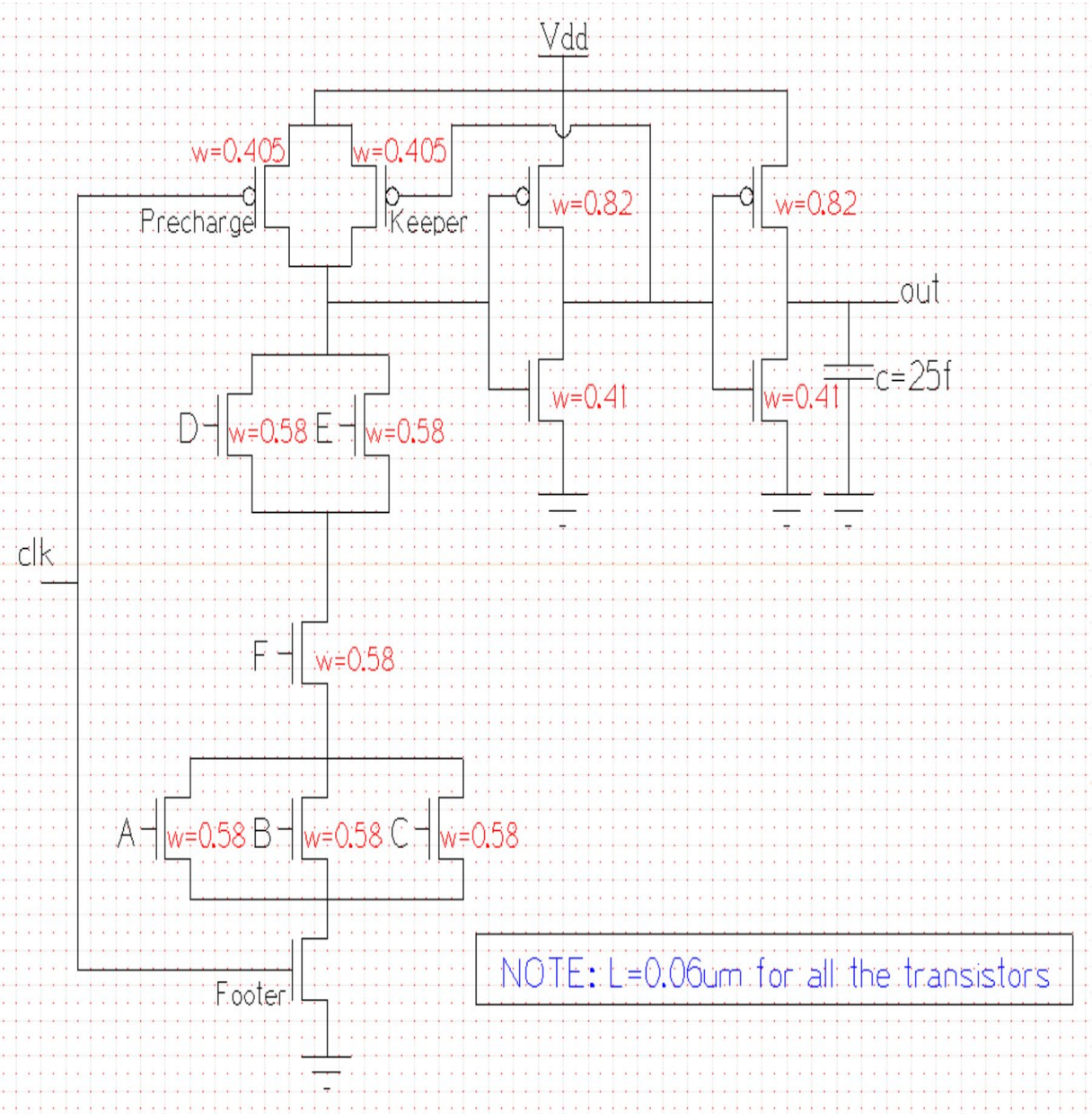
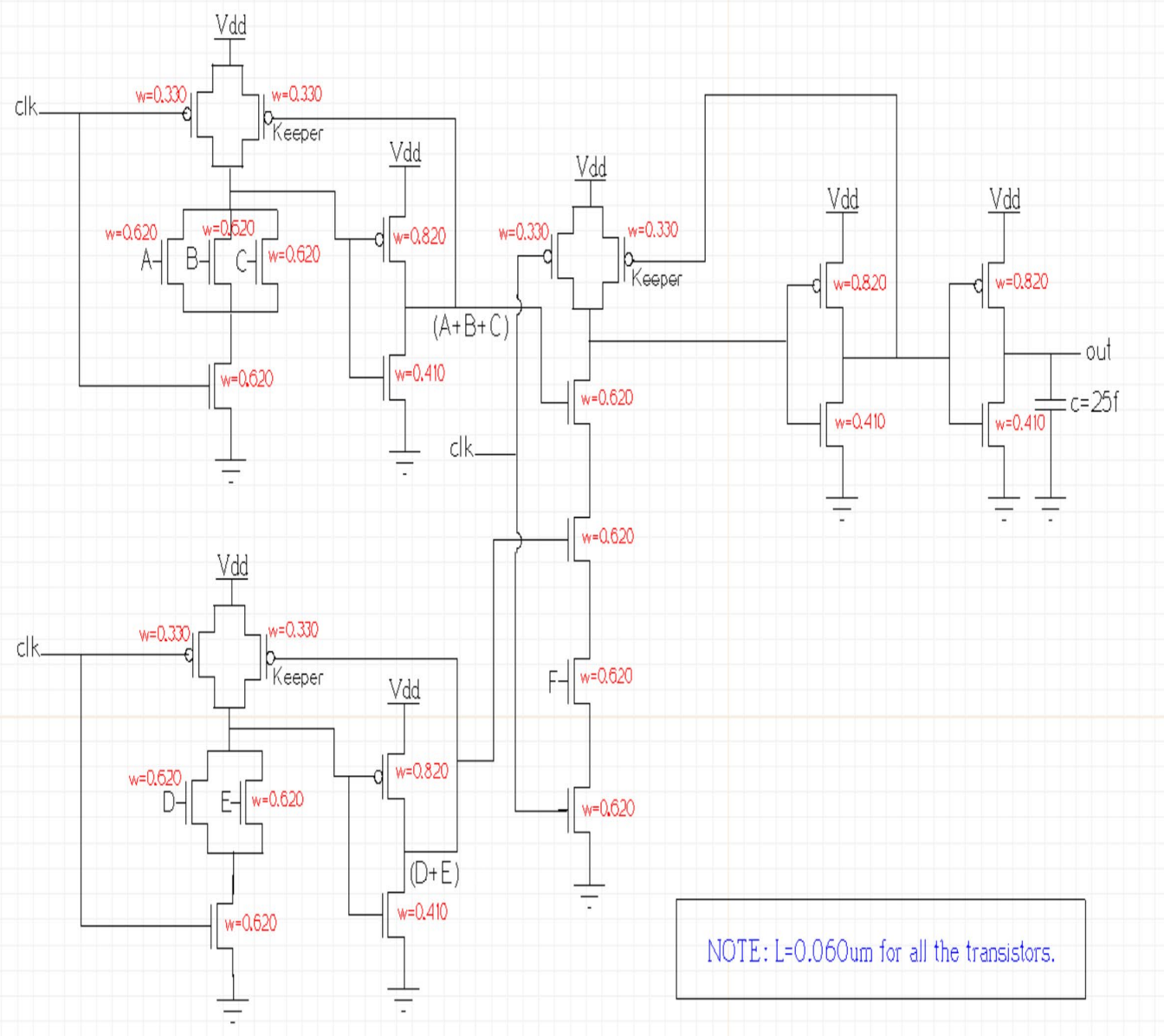
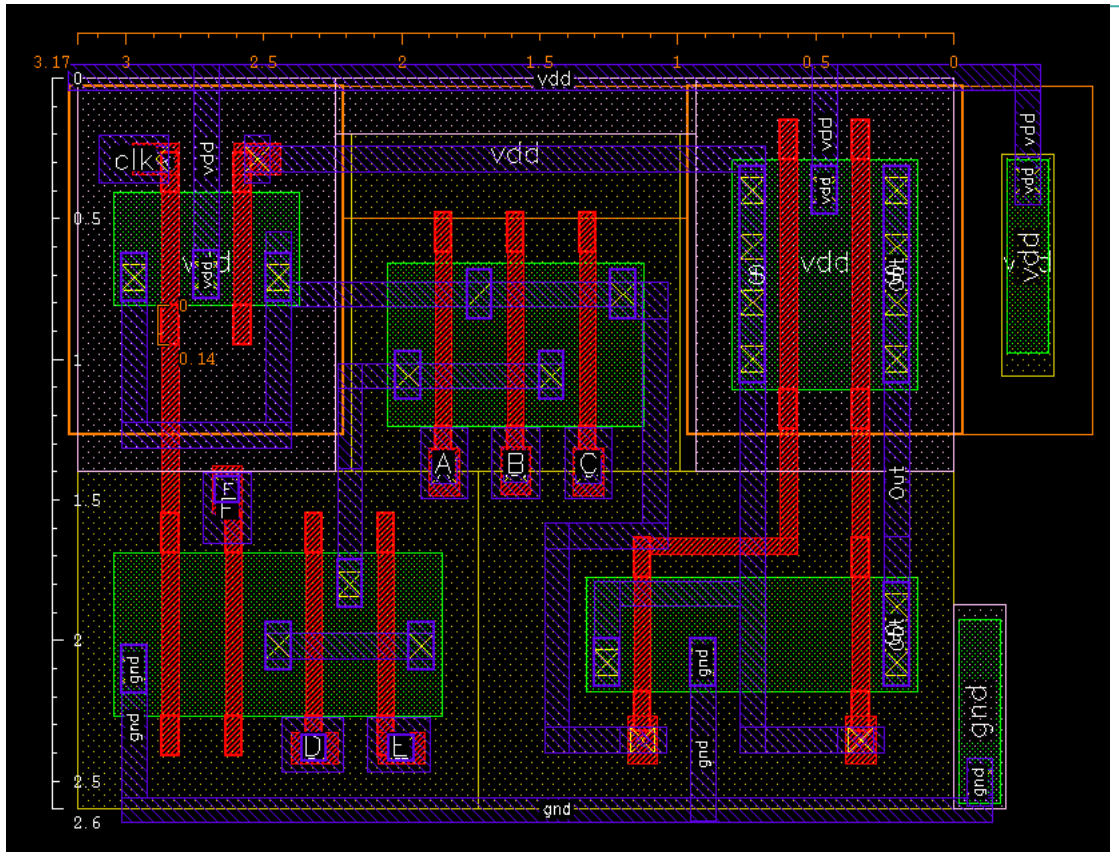
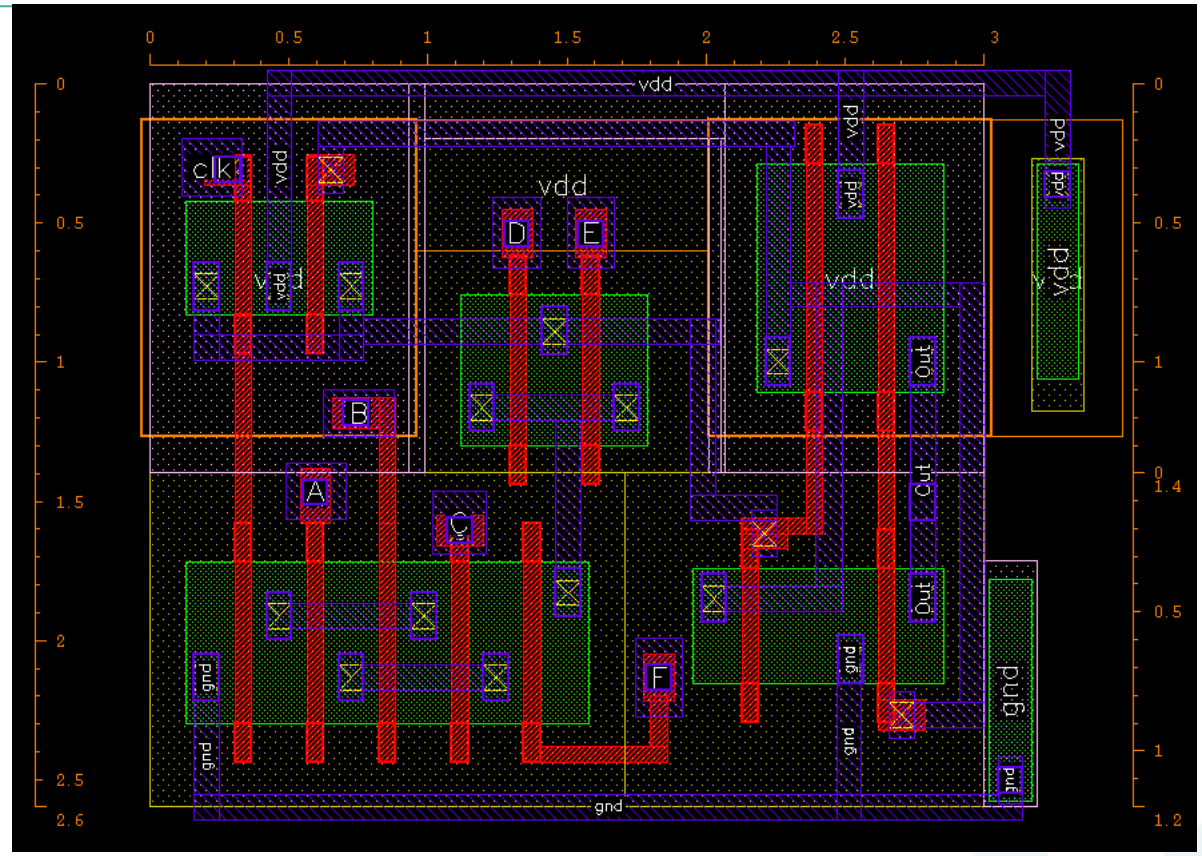
Schematic + Sizing (Complex & Non-Complex Gate(s))





Layout (Complex Gate)





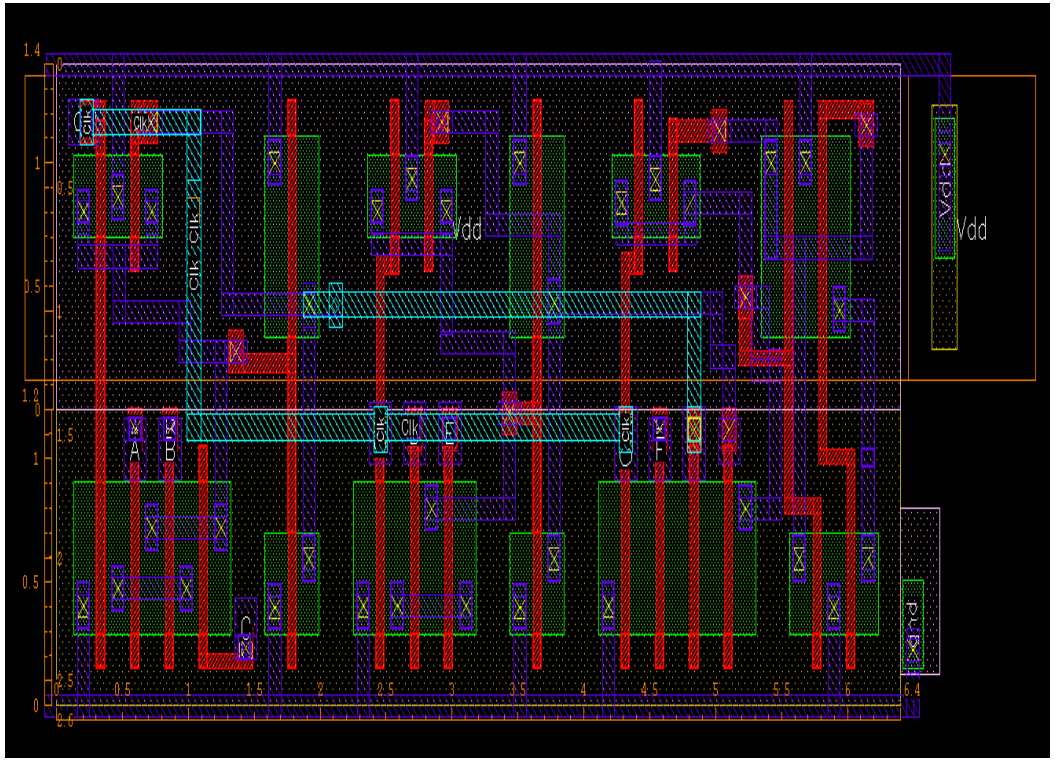
LAYOUT 1

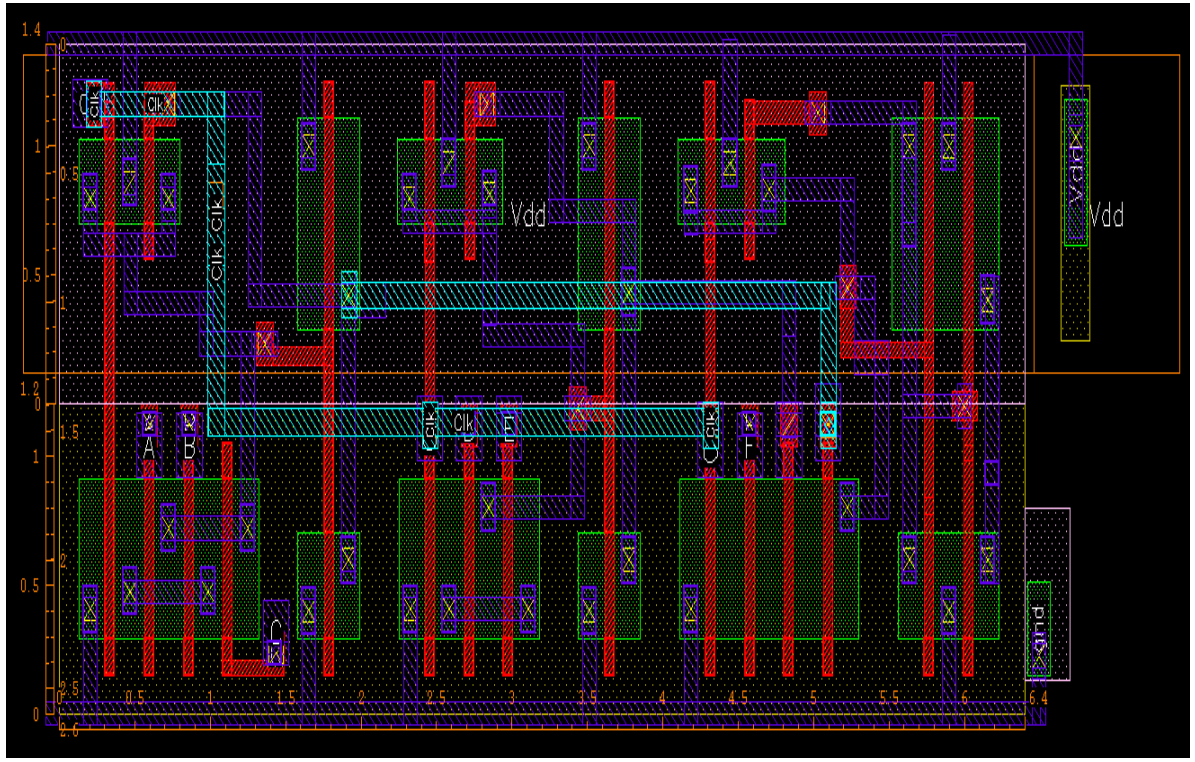
- **AREA** = (3.17*2.6) μm^2 = 8.242 μm^2
- **CHARACTERISTICS** : *More Area , Less Hammerheads, Shared Contacts .*

LAYOUT 2

- **AREA** = (2.6*3) μm^2 = 7.8 μm^2
- **CHARACTERISTICS** : *Less Area , More Hammerheads, Shared Contacts , Dense Layout .*

Layout (Non-Complex Gate)





LAYOUT 1

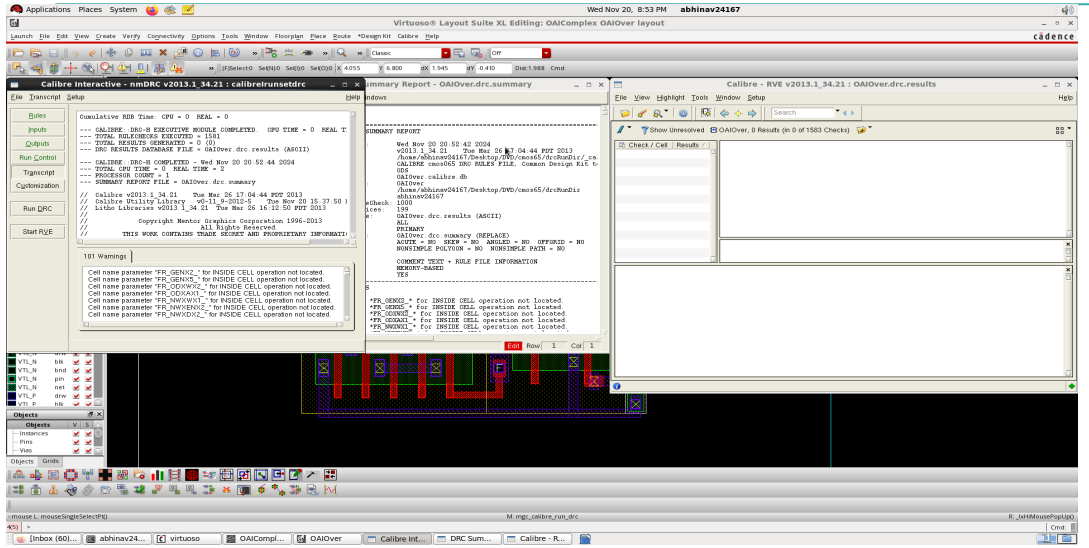
- **AREA** = (2.6*6.4) μm^2 = 16.64 μm^2
- **CHARACTERISTICS**: *More Poly-bending, Higher Poly Resistance, More Hammerheads.*

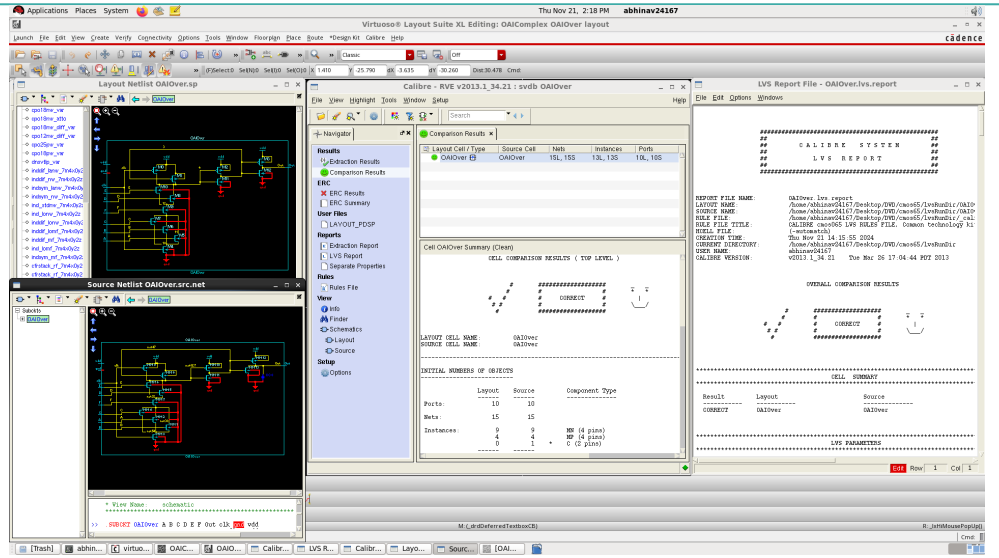
LAYOUT 2

- **AREA** = (2.6*6.4) μm^2 = 16.64 μm^2
- **CHARACTERISTICS**: *Less Poly-bending, Less Poly Resistance, Less Hammerheads.*

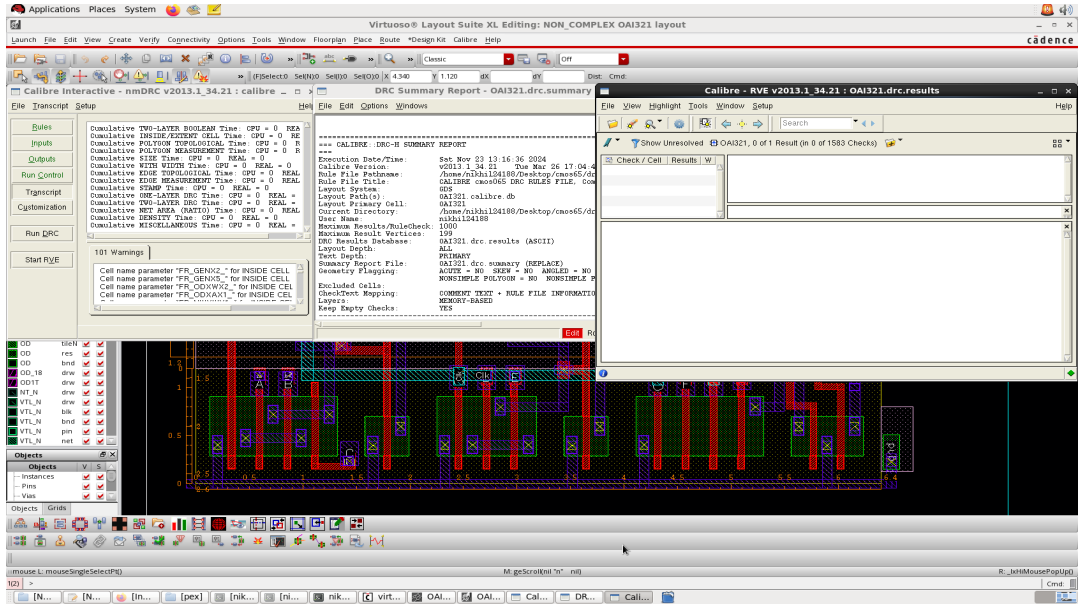
DRC, LVS Report(s) for Complex and Non-Complex Gate(s)

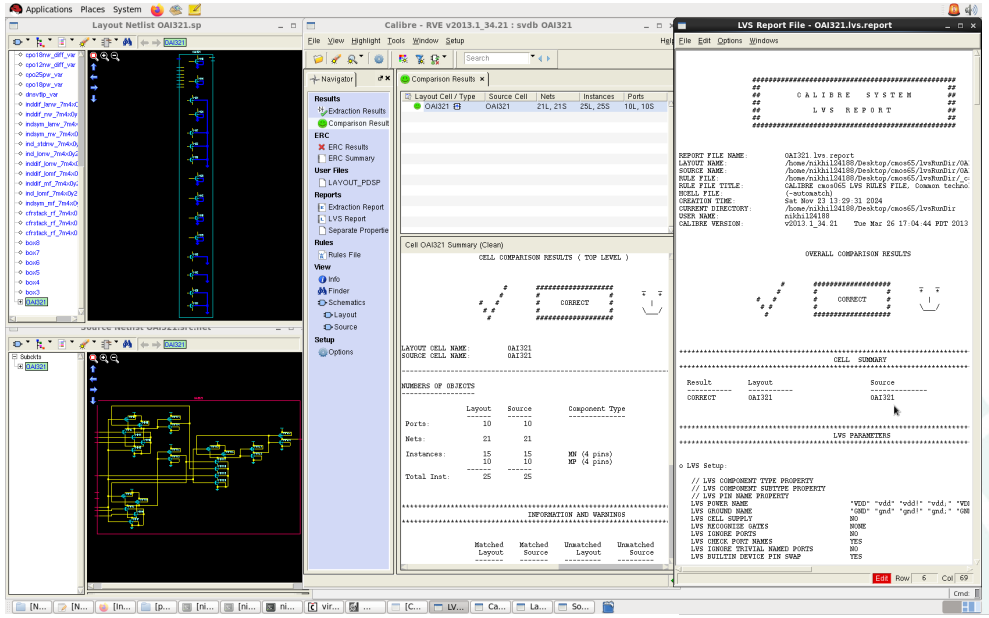
COMPLEX





NON-COMPLEX





Analytical Simulation(s)

COMPLEX	
Contamination Delay	Trise:- Clk 1→0 A,B,C,D,E,F = 0
	Tfall:- Clk 0→1 D,E 0→1 A,B,C,F = 1
Propagation Delay	Trise:- Clk 1 → 0 A,B,C,D,E,F = 1
	Tfall:- Clk 0→1 C 0→1 E,F =1 A,B,D =0

NON-COMPLEX	
Contamination Delay	Trise:- Clk 1→0 A,B,C,D,E,F = 0
	Tfall:- Clk 0→1 A,B,C 0→1 D,E,F = 1
Propagation Delay	Trise:- Clk 1 → 0 A,B,C,D,E,F = 1
	Tfall:- Clk 0→1 F 0→1 E,C =1 A,B,D =0

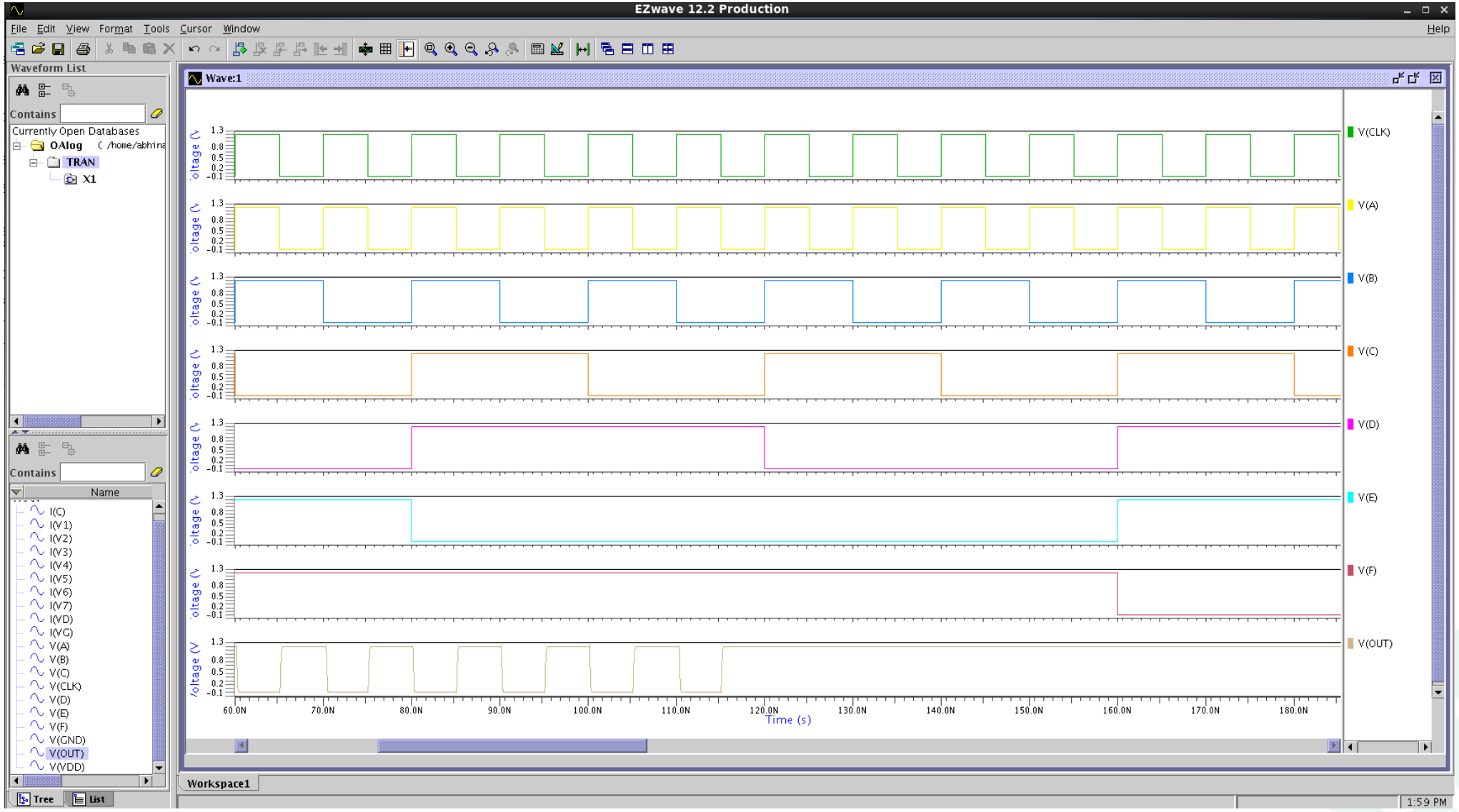
Contamination delay for Complex and Non-Complex Gate(s)

	COMPLEX		NON-COMPLEX	
PVT corner	TCD (Pre-Layout)	TCD (Post-Layout)	TCD (Pre-Layout)	TCD (Post-Layout)
SS,1.08V,125C	0.24433 ns	0.24081 ns	0.43612 ns	0.38908 ns
SS,1.08V,25C	0.22038 ns	0.2192 ns	0.40302 ns	0.36295 ns
SS,1.08V,-40C	0.20198 ns	0.20194 ns	0.37091 ns	0.34094 ns
TT,1.2V,25C	0.16035 ns	0.15954 ns	0.21933 ns	0.21901 ns
FF,1.32V,125C	0.14379 ns	0.14063 ns	0.16514 ns	0.16978 ns
FF,1.32V,-40C	0.10979 ns	0.11079 ns	0.12747 ns	0.13484 ns

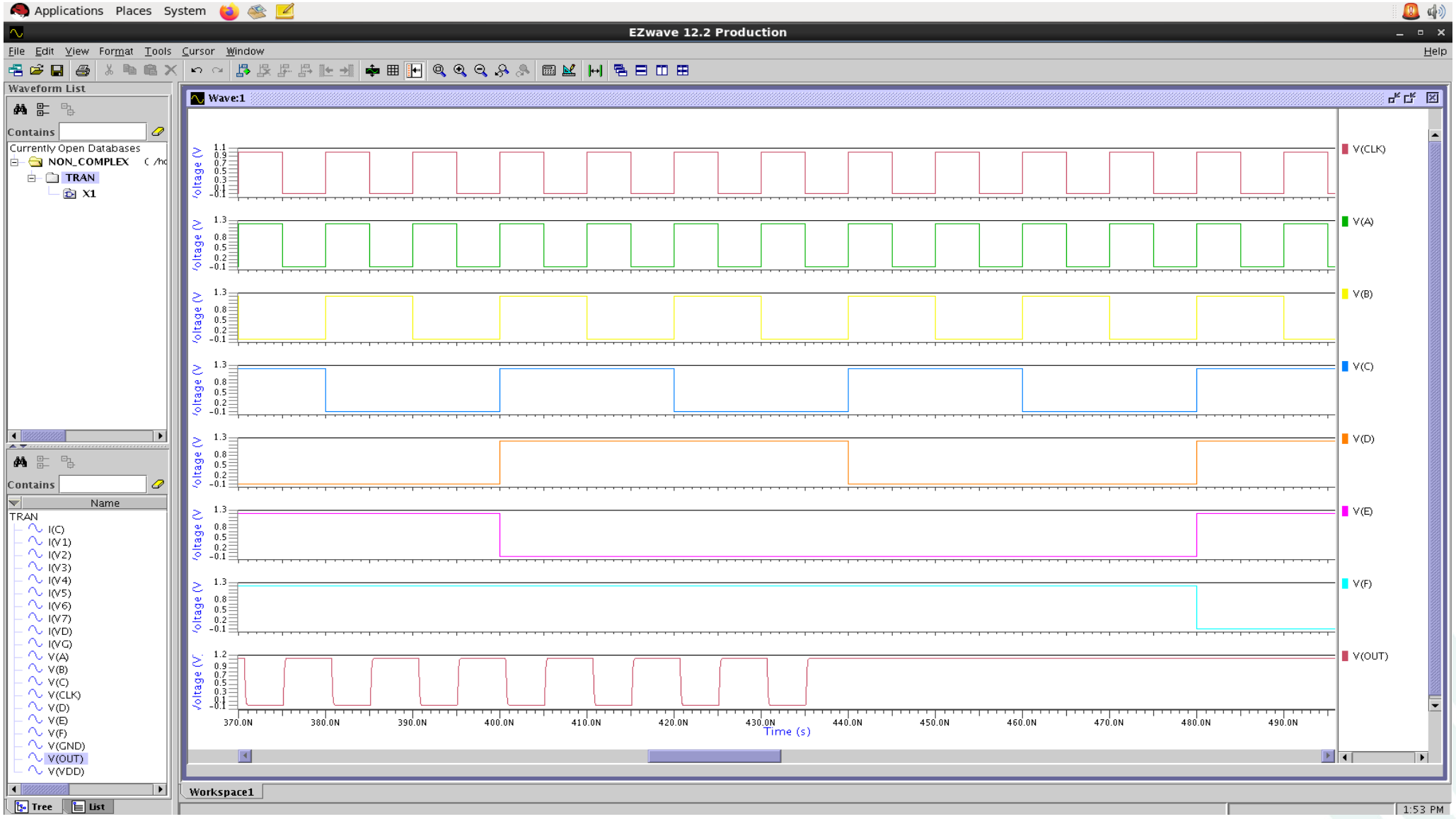
Propagation delay for Complex and Non-Complex Gate

	COMPLEX		NON-COMPLEX	
PVT corner	TPD (Pre-Layout)	TPD (Post-Layout)	TPD (Pre-Layout)	TPD (Post-Layout)
SS,1.08V,125C	0.4421 ns	0.37046 ns	0.44884 ns	0.40075 ns
SS,1.08V,25C	0.37977 ns	0.33217 ns	0.41451 ns	0.37335 ns
SS,1.08V,-40C	0.33835 ns	0.30604 ns	0.38141 ns	0.35037 ns
TT,1.2V,25C	0.1883 ns	0.1592 ns	0.22830 ns	0.22717 ns
FF,1.32V,125C	0.1335 ns	0.1062 ns	0.1739 ns	0.17687 ns
FF,1.32V,-40C	0.09344 ns	0.06218 ns	0.13344 ns	0.14029 ns

Waveforms of Complex Gate



Waveforms of Non-Complex Gate



LEAKAGE CURRENT , STATIC AND DYNAMIC POWER

STATIC POWER IN DIFFERENT STIMULI IN nW

STIMULI (ABCDEF)	COMPLEX	NON-COMPLEX
000000	64.612	317.09
000001	79.796	318.24
000010	76.310	315.40
000011	140.052	371.14
000101	140.052	371.14
000110	76.495	316.66
000111	141.174	364.39
001000	63.767	285.08
001010	104.017	298.46
001011	136.488	328.39
001111	138.283	327.88
010000	63.767	285.08
010001	148.579	299.41
010100	104.017	298.46
010101	137.662	323.60
010110	105.630	301.14
010111	134.600	326.22
011000	63.419	283.81
011001	150.031	299.48
011010	104.115	298.55
011011	138.903	328.20
011101	141.306	328.20
011110	105.879	298.95
011111	140.659	327.72
111001	150.559	285.64
110001	150.031	301.56

POWER AND CURRENT IN COMPLEX GATE

PARAMETER	PVT CONDITION	STIMULI	PRE – LAYOUT	POST – LAYOUT
DYNAMIC POWER (WORST CASE)	TT , 1.2V, 25C	101101	6.8136 µW	6.625 µW
STATIC POWER (WORST CASE)	FF, 1.32V, 125C	111001	150.559 nW	160.762 nW
LEAKAGE CURRENT (WORST CASE)	FF, 1.32V , 125C	111001	114.06 nA	121.79 nA

POWER AND CURRENT IN NON-COMPLEX GATE

PARAMETER	PVT CONDITION	STIMULI	PRE – LAYOUT	POST – LAYOUT
DYNAMIC POWER (WORST CASE)	TT , 1.2V, 25C	001011	9.0709 µW	9.0495 µW
STATIC POWER (WORST CASE)	FF, 1.32V, 125C	000101	371.14 nW	391.81 nW
LEAKAGE CURRENT (WORST CASE)	FF, 1.32V , 125C	000101	264.25 nA	296.83 nA

Work Distribution

- Schematic – Abhinav, Mayank
- Complex Layout - Abhinav
- Non complex layout – Mayank, Nikhil
- Eldo simulation – Nikhil , Abhinav, Devansh
- Xcircuit – Devansh
- Tables and presentation- Devansh, Nikhil, Mayank


THANK YOU