Lab 4-Classwork Part 2

19-02-2020 CS 254-Digital Logic Design Lab 14:00-16:55

The following digital circuits must be designed using VHDL, and simulated and tested using Quartus.

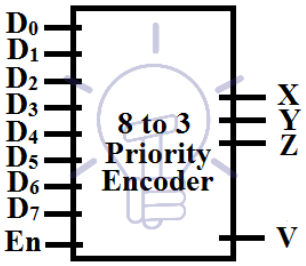
Q4. (5marks) Design a 2-bit Grey to BCD converter using Decoder and Demultiplexers only (Use Demultiplexers to make the basic gates required)

Grey Code(G_1G_o)	BCD(ABCD)
00	0000
01	0001
11	0010
10	0011

The trace file format for the design is as follows:

G_1G_0 ABCD

BONUS(5marks) Design a 8:3 Priority encoder using two 4:2 Priority encoders and Demultiplexers only (Use Demultiplexers to make the basic gates required)



Input									Output			
En	**D_0**	**D_1**	**D_2**	**D_3**	**D_4**	**D_5**	**D_6**	**D_7**	**X**	**Y**	**Z**	**V**
0	X	X	X	X	X	X	X	X	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0	1
1	X	1	0	0	0	0	0	0	0	0	1	1
1	X	X	1	0	0	0	0	0	0	1	0	1
1	X	X	X	1	0	0	0	0	0	1	1	1
1	X	X	X	X	1	0	0	0	1	0	0	1
1	X	X	X	X	X	1	0	0	1	1	0	1
1	X	X	X	X	X	X	1	0	1	0	1	1
1	X	X	X	X	X	X	X	1	1	1	1	1

The trace file format for the design is as follows:

$EnD_0D_1D_2D_3D_4D_5D_6D_7$ XYZV