Lab 3

12-02-2020 CS 254-Digital Logic Design Lab 14:00-16:55

The following digital circuits must be designed using VHDL, and simulated and tested using Quartus.

Q1. (5marks) Design an 8-bit Carry-Look-Ahead (CLA) adder (signed adder). The inputs are in 2's complement form.

Carry generation: $P_i = A_i$ **XOR** B_i
Carry propagate: $G_i = A_i$ **AND** B_i
Sum output: $S_i = P_i$ **XOR** C_i
Carry output: $C_{i+1} = G_i$ **OR** (P_i **AND** C_i)
where, A_i and B_i are the 8-bit input.

The trace file format for the design is as follows:

$A_{7-0}B_{7-0}$ Z_{8-0}

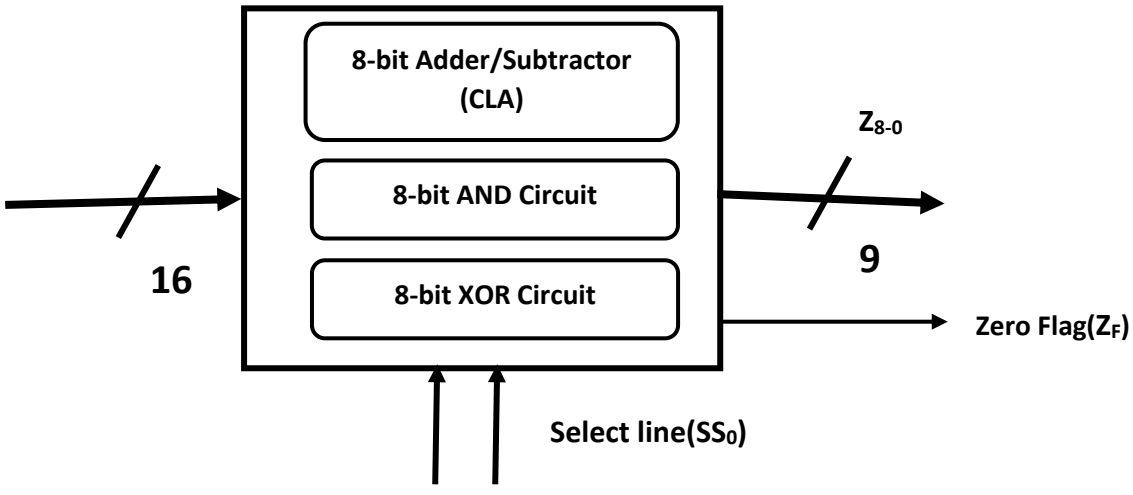
Q2. (5marks) Design an 8-bit arithmetic circuit which should have:

1. 8-bit adder-subtractor unit (use CLA)
2. 8-bit AND logic function unit
3. 8-bit XOR logic function unit

Inputs	Select line(S_1S_0)	Function	Output	
A_{7-0}, B_{7-0}	00	Adder	Z_{8-0}	Z_F
A_{7-0}, B_{7-0}	01	Subtractor	Z_{8-0}	Z_F
A_{7-0}, B_{7-0}	10	AND	Z_{7-0}(Z_8 = 0)	Z_F
A_{7-0}, B_{7-0}	11	XOR	Z_{7-0}(Z_8 = 0)	Z_F

The trace file format for the design is as follows:

$A_{7-0}B_{7-0}$ S_1S_0 Z_{8-0} Z_F



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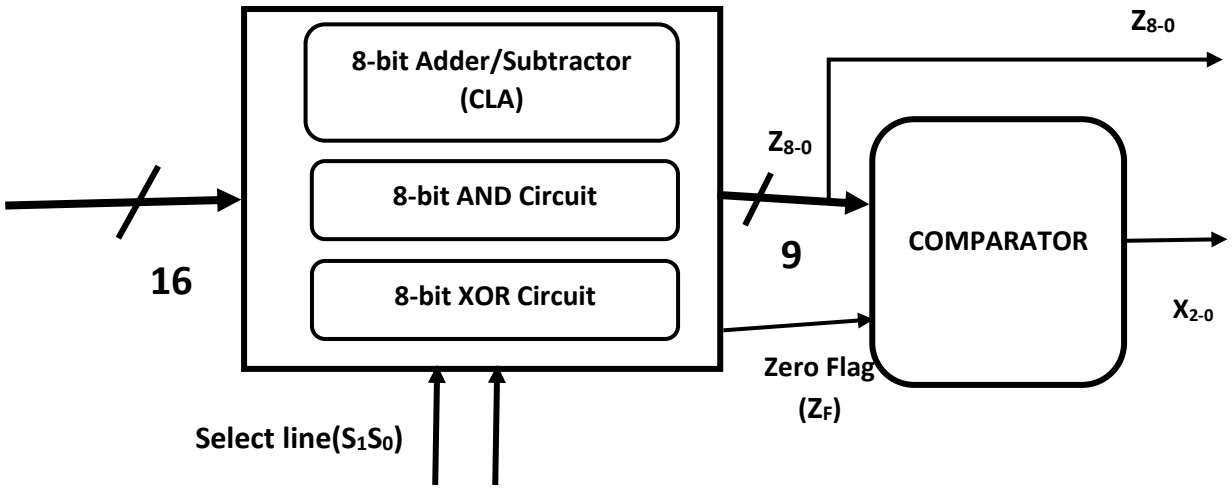
BONUS Question(5marks):

Design an 8-bit arithmetic circuit which should have:

1. 8-bit adder-subtractor unit (use CLA)
2. 8-bit AND logic function unit
3. 8-bit XOR logic function unit

Inputs	Select line(S_1S_0)	Function	Output
A_{7-0}, B_{7-0}	00	Adder	Z_{8-0}, X_{2-0}
A_{7-0}, B_{7-0}	01	Subtractor	Z_{8-0}, X_{2-0}
A_{7-0}, B_{7-0}	10	AND	Z_{8-0}, X_{2-0}
A_{7-0}, B_{7-0}	11	XOR	Z_{8-0}, X_{2-0}



The input of the comparator is the output of the ALU designed in Q2. The output truth table of the comparator is shown below.

The trace file format for the design is as follows:

$A_{7-0}B_{7-0}\,S_1S_0 \quad Z_{8-0}\,X_{2-0}$

Inputs	Condition	Output(X_{2-0})
A_{7-0}, B_{7-0}	**$A_{7-0} > B_{7-0}$**	**100**
A_{7-0}, B_{7-0}	**$A_{7-0} < B_{7-0}$**	**001**
A_{7-0}, B_{7-0}	**$A_{7-0} = B_{7-0}$**	**010**