



The ModelSim - INTEL FPGA STARTER EDITION 10.5b interface shows the Objects window, Processes (Active) window, and Transcript window. The Objects window lists the following objects:

Name	Value	Kind	Mode
input_vector	00	Signal Inter...	
output_vector	00001	Signal Inter...	
number_of_inputs	2	Cons... Inter...	
number_of_outputs	5	Cons... Inter...	

The Processes (Active) window shows the following processes:

Name	Type (filtered)	State	Order	Parent Path	Class Info

The Transcript window shows the following text:

```
# vaim -t lps -L altera -L lpm -L sgate -L altera_nf -L altera_nsim -L cyclonev -L rtl_work -L work -voptargs="+acc" Testbench
# vaim -t lps -L altera -L lpm -L sgate -L altera_nf -L altera_nsim -L cyclonev -L rtl_work -L work -voptargs="+acc" Testbench
# Start time: 12:08:24 on Mar 07,2020
# Loading std.standard
# Loading std.textio(body)
# Loading ieee.std_logic_1164(body)
# Loading work.testbench(behavior)
# Loading work.upcounter(arc)
#
# add wave *
# view structure
# .main_pane.structure.interior.cs.body.struct
# view signals
# .main_pane.objects.interior.cs.body.tree
# run -all
# ** Note: SUCCESS, all tests passed.
# Time: 864 ns Iteration: 0 Instance: /testbench
```

Now: 864 ns Delta: 1 sim:/testbench

