Lab 5-Homework

04-03-2020 CS 254-Digital Logic Design Lab 14:00-16:55

The following digital circuits must be designed using VHDL, and simulated and tested using Quartus.

The code for FSM should contain **three processes**:

1. First, to define the state transition logic

eg:
```
p1: process (clk,reset)
    begin
        if (reset = '1') then
            state <= no_carry;
        elsif (clk'event and clk = '1') then
            state <= next_state;
        end if;
    end process;
```

2. Second, for next states logic
3. Third, for output logic

All the code from hereon which contains FSM should be written in above format, strictly.

Q1. Design a 4-bit up-counter which counts from 0-15 and then goes back to 0 and so on, every clock event. The counter goes to 0 when reset input is applied.

This has been explained in the CS-226 class.

Trace file Format:

Reset_Clock Done_Value[3:0] MaskBits

An example trace file for 2-bit counter is attached below for reference:

```
Reset_Clock   Done_Value(1)_Value(0)  MaskBits

00 000 000
10 000 111
01 001 111
00 001 111
01 010 111
00 010 111
01 111 111
00 111 111
01 000 111
00 000 111
01 001 111
```