Report for Lab-3 Classwork

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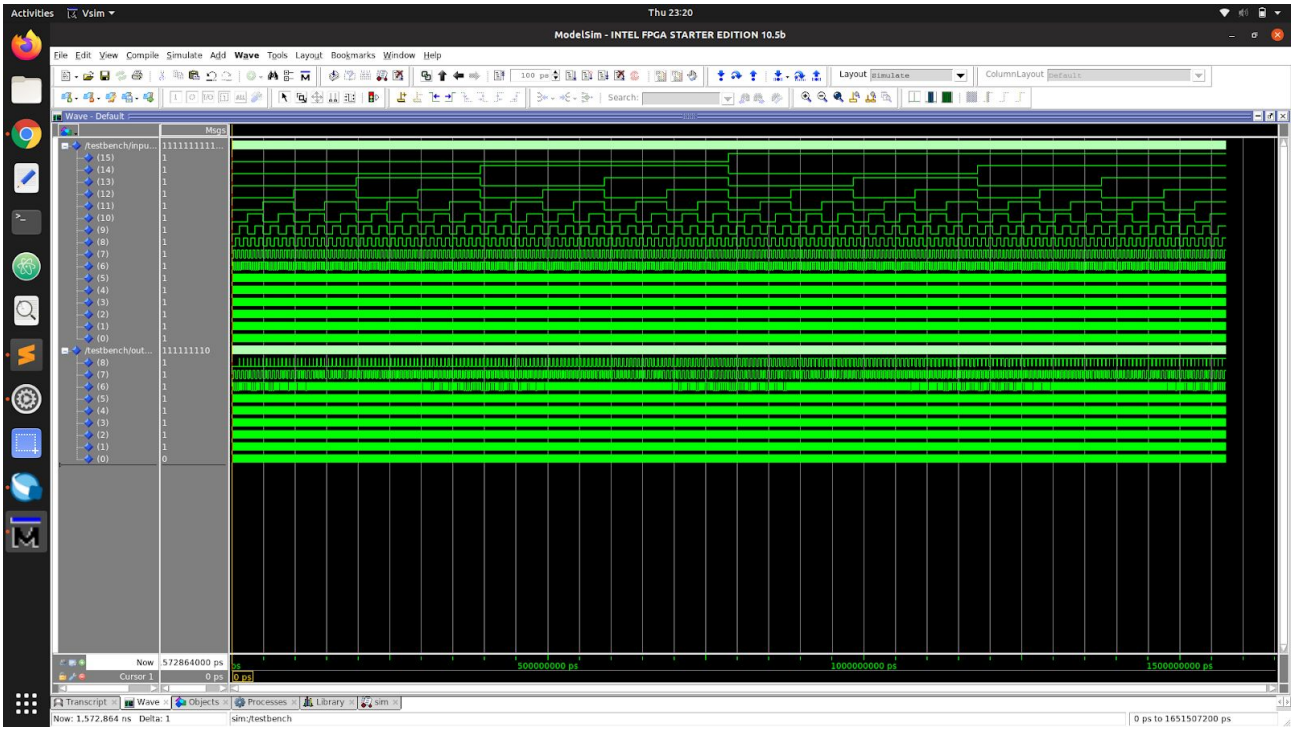
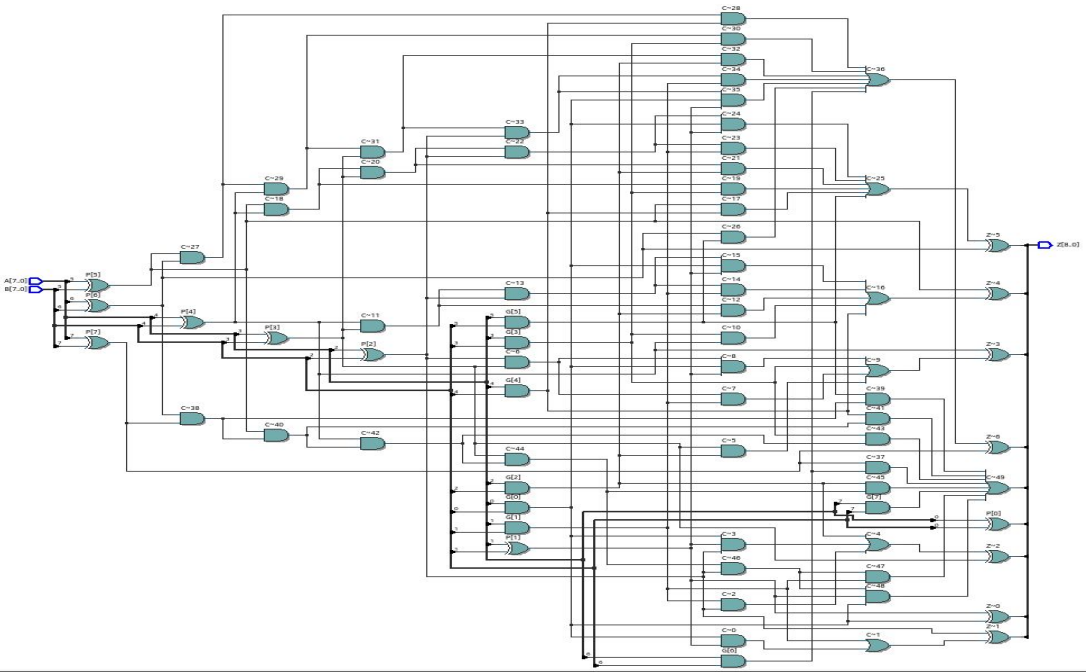
Carry-Look-Ahead Adder

```
#
# vcom -93 -work work {/home/bargav07/lab3/claa/Testbench.vhdl}
# Model Technology ModelSim - Intel FPGA Edition vcom 10.5b Compiler 2016.10 Oct  5 2016
# Start time: 23:19:02 on Feb 13,2020
# vcom -reportprogress 300 -93 -work work /home/bargav07/lab3/claa/Testbench.vhdl
# -- Loading package STANDARD
# -- Loading package TEXTIO
# -- Loading package std_logic_1164
# -- Compiling entity Testbench
# -- Compiling architecture Behave of Testbench
# End time: 23:19:02 on Feb 13,2020, Elapsed time: 0:00:00
# Errors: 0, Warnings: 0
#
# vsim -t 1ps -L altera -L lpm -L sgate -L altera_mf -L altera_lnsim -L cyclonev -L rtl_work -L work -voptargs="+acc"  Testbench
# vsim -t 1ps -L altera -L lpm -L sgate -L altera_mf -L altera_lnsim -L cyclonev -L rtl_work -L work -voptargs=""+acc"" Testbench
# Start time: 23:19:02 on Feb 13,2020
# Loading std.standard
# Loading std.textio(body)
# Loading ieee.std_logic_1164(body)
# Loading work.testbench(behave)
# Loading work.claa(struct)
#
# add wave *
# view structure
# .main_pane.structure.interior.cs.body.struct
# view signals
# .main_pane.objects.interior.cs.body.tree
# run -all
# ** Warning: (vsim-3116) Problem reading symbols from linux-gate.so.1 : can not open ELF file.
# ** Note: SUCCESS, all tests passed.
#    Time: 1572864 ns  Iteration: 0  Instance: /testbench
#
# stdin: <EOF>

VSIM 2>
```



CLA adder RTL Block Diagram

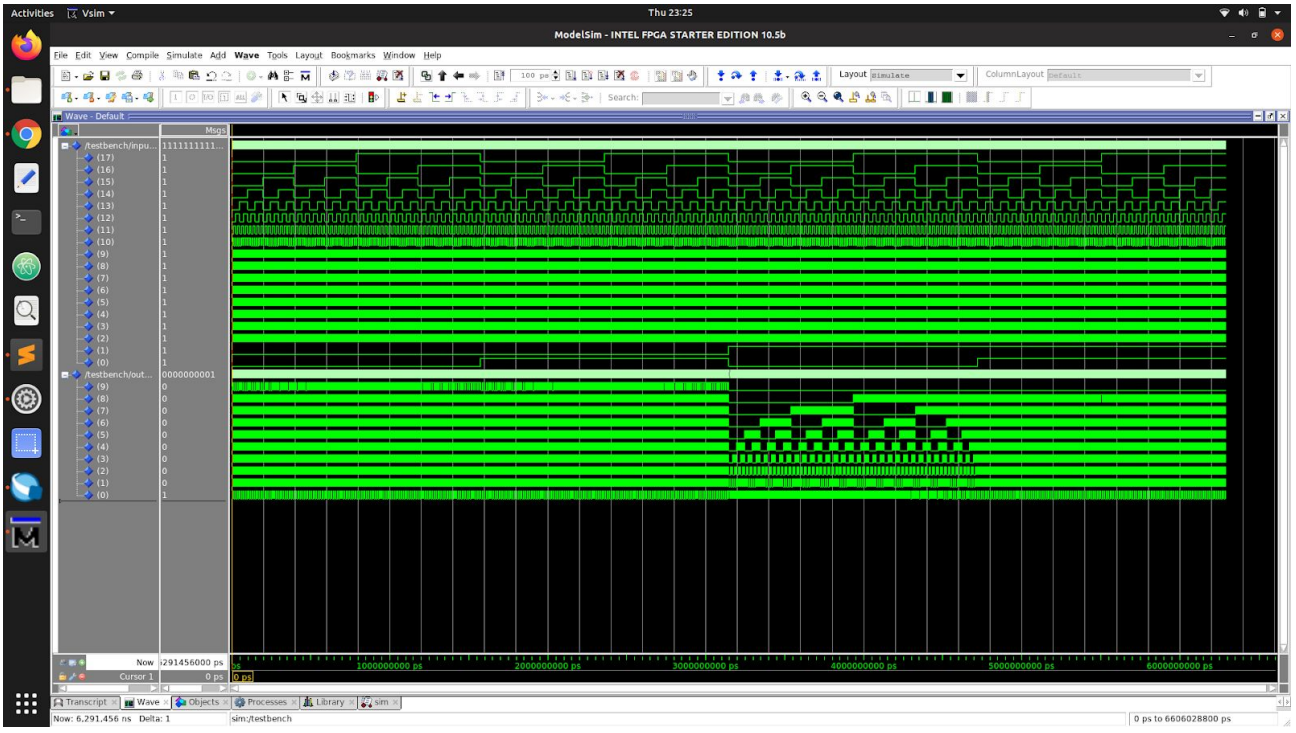


Q2

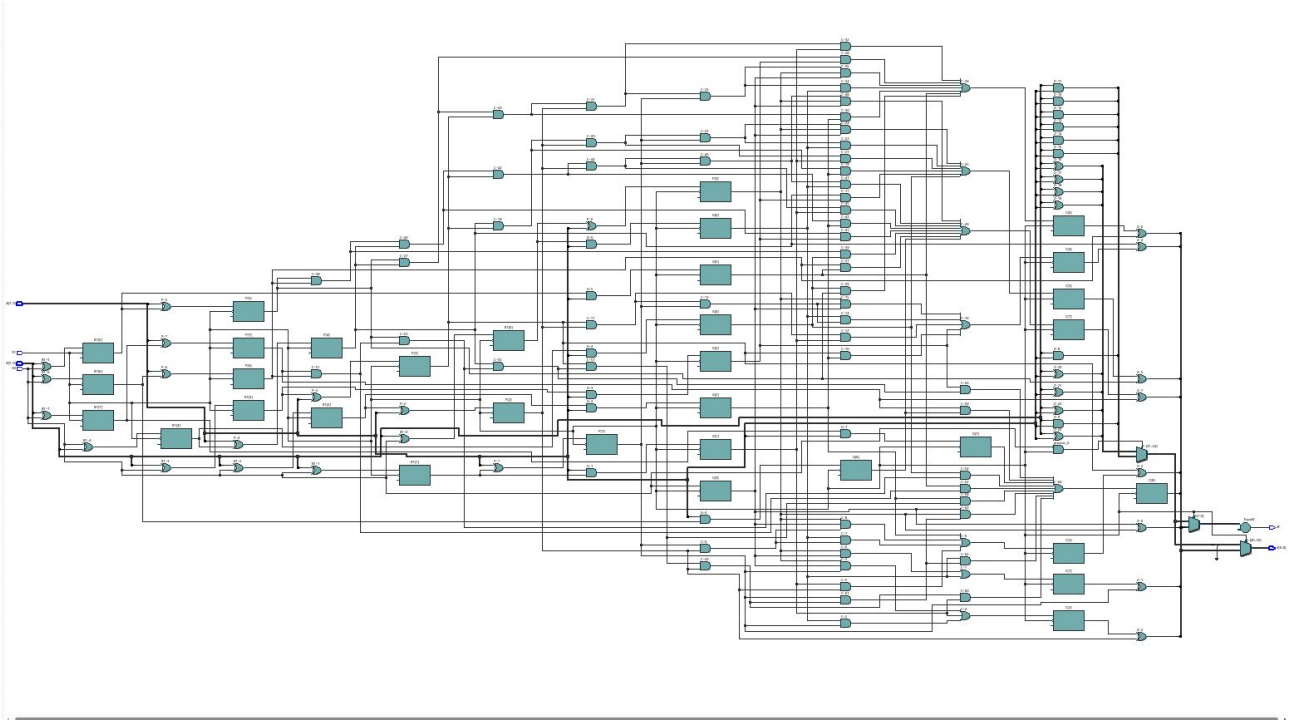
Transcript

```
vcom -93 -work work {/home/bargav07/lab3/alu/Testbench.vhd1}
Model Technology ModelSim - Intel FPGA Edition vcom 10.5b Compiler 2016.10 Oct  5 2016
Start time: 23:24:58 on Feb 13,2020
vcom -reportprogress 300 -93 -work work /home/bargav07/lab3/alu/Testbench.vhd1
-- Loading package STANDARD
-- Loading package TEXTIO
-- Loading package std_logic_1164
-- Compiling entity Testbench
-- Compiling architecture Behave of Testbench
End time: 23:24:58 on Feb 13,2020, Elapsed time: 0:00:00
Errors: 0, Warnings: 0

vsim -t 1ps -L altera -L lpm -L sgate -L altera_mf -L altera_lnsim -L cyclonev -L rtl_work -L work -voptargs="+acc"  Testbench
vsim -t 1ps -L altera -L lpm -L sgate -L altera_mf -L altera_lnsim -L cyclonev -L rtl_work -L work -voptargs=""+acc"" Testbench
Start time: 23:24:58 on Feb 13,2020
Loading std.standard
Loading std.textio(body)
Loading ieee.std_logic_1164(body)
Loading work.testbench(behave)
Loading work.alu(struct)

add wave *
view structure
.main_pane.structure.interior.cs.body.struct
view signals
.main_pane.objects.interior.cs.body.tree
run -all
** Warning: (vsim-3116) Problem reading symbols from linux-gate.so.1 : can not open ELF file.
** Note: SUCCESS, all tests passed.
   Time: 6291456 ns  Iteration: 0  Instance: /testbench

stdin: <EOF>

SIM 2>
```

Simulation



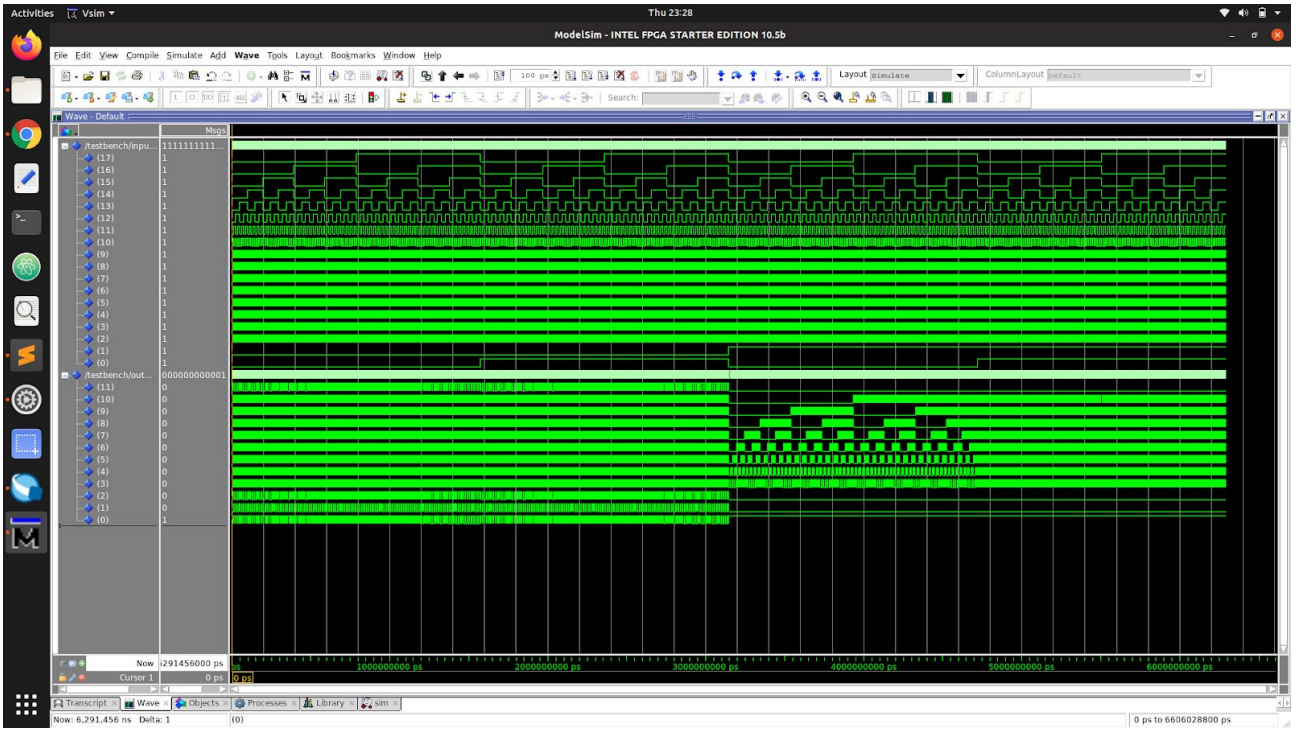
RTL Block Diagram



Q3
Transcript

```
vcom -93 -work work {/home/bargav07/lab3/comp/Testbench.vhdl}
Model Technology ModelSim - Intel FPGA Edition vcom 10.5b Compiler 2016.10 Oct  5 2016
Start time: 23:27:08 on Feb 13,2020
vcom -reportprogress 300 -93 -work work /home/bargav07/lab3/comp/Testbench.vhdl
-- Loading package STANDARD
-- Loading package TEXTIO
-- Loading package std_logic_1164
-- Compiling entity Testbench
-- Compiling architecture Behave of Testbench
End time: 23:27:08 on Feb 13,2020, Elapsed time: 0:00:00
Errors: 0, Warnings: 0

vsim -t 1ps -L altera -L lpm -L sgate -L altera_mf -L altera_lnsim -L cyclonev -L rtl_work -L work -voptargs="+acc"  Testbench
vsim -t 1ps -L altera -L lpm -L sgate -L altera_mf -L altera_lnsim -L cyclonev -L rtl_work -L work -voptargs=""+acc"" Testbench
Start time: 23:27:08 on Feb 13,2020
Loading std.standard
Loading std.textio(body)
Loading ieee.std_logic_1164(body)
Loading work.testbench(behave)
Loading work.comp(struct)

add wave *
view structure
.main_pane.structure.interior.cs.body.struct
view signals
.main_pane.objects.interior.cs.body.tree
run -all
** Warning: (vsim-3116) Problem reading symbols from linux-gate.so.1 : can not open ELF file.
** Note: SUCCESS, all tests passed.
   Time: 6291456 ns  Iteration: 0  Instance: /testbench

stdin: <EOF>
VSIM 2>
```

Simulation



RTL Block Diagram