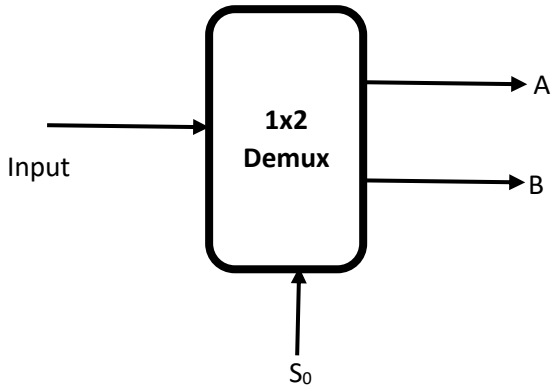
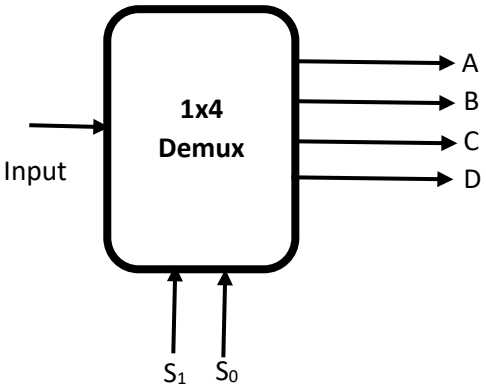
Lab 4-Classwork Part 1

19-02-2020 CS 254-Digital Logic Design Lab 14:00-16:55

The following digital circuits must be designed using VHDL, and simulated and tested using Quartus.

Q1. (10marks) Design a 1x2 Demultiplexer and a 1x4 Demultiplexer.





Input	S_0	AB
0	0	00
1	0	01
0	1	00
1	1	10

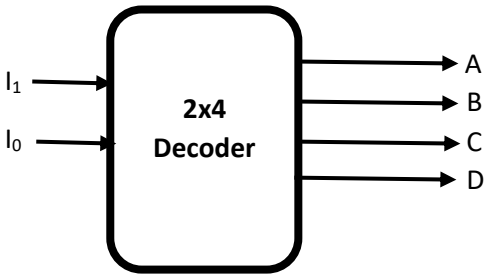
Input	S_1	S_0	ABCD
0	0	0	0000
1	0	0	0001
0	0	1	0000
1	0	1	0010
0	1	0	0000
1	1	0	0100
0	1	1	0000
1	1	1	1000

The trace file format for the design is as follows:

Input S_0 AB | Input S_1S_0 ABCD

Q2. (5marks) Design a 2x4 Decoder.

I_1	I_0	A	B	C	D
0	0	1	1	1	0
0	1	1	1	0	1
1	0	1	0	1	1
1	1	0	1	1	1

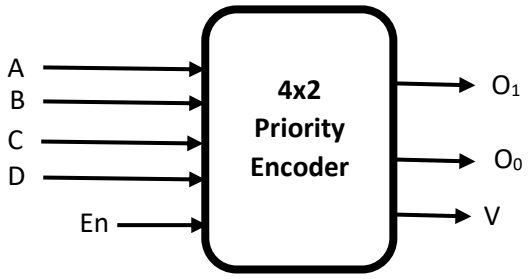


The trace file format for the design is as follows:

I_1I_0 ABCD

Q3. (5marks) Design a 4x2 Priority encoder.

En	A	B	C	D	O_1	O_0	V
0	x	x	x	x	x	x	0
1	0	0	0	0	x	x	0
1	0	0	0	1	0	0	1
1	0	0	1	x	0	1	1
1	0	1	x	x	1	0	1
1	1	x	x	x	1	1	1



The trace file format for the design is as follows:

EnABCD O_1O_0V