MAC Unit ILA

CASEST

हैदराबाद विश्वविद्यालय
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Lab Report No. 2

MV—: Digital VLSI System Design Lab

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1 | Introduction

1.1 | Objective

MAC unit implementation and verification using ILA.

2 | Code

2.1 | MAC unit

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 03/04/2024 05:28:36 PM
// Design Name:
// Module Name: mac
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////

module mac_unit (
    input clk,
    input rst,
    input [3:0] a,
    input [3:0] b,
    output reg [7:0] accum_out
);


always @(posedge clk or posedge rst)
    begin
        if(rst)
            begin
                accum_out=0;
            end
         else
            begin
                accum_out<=accum_out+a*b;
            end
    end
endmodule
```

2.2 | Testbench

```
`timescale 1ns / 1ps
```

```
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 03/04/2024 05:28:36 PM
// Design Name:
// Module Name: tb_mac
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module tb_mac_unit;

    reg clk;
    reg rst;
    reg [8:0] a;
    reg [8:0] b;
    wire [31:0] accum_out;

    mac_unit uut (
        .clk(clk),
        .rst(rst),
        .a(a),
        .b(b),
        .accum_out(accum_out)
    );

    initial begin
        clk=0;
        forever #10 clk = ~clk;
    end



    initial begin
        rst = 1;
        #10 rst =0;

        a = 8'd17;b=8'd5;
        #20 a = 8'd2;b=8'd6;
        #20 a = 8'd5;b=8'd8;

        #100 $finish;
    end

endmodule
```

2.3 | Result

MAC unit was simulated successfully and implemented in Zedboard and verified functionality with ILA.

3 | References

A | Appendix A: GitHub Repo

The GitHub repo referenced below contains the Verilog code and testbenches mentioned in this report.
https://github.com/AbhinavM2000/MV401D/