Ring and Johnson Counters

CASEST

हैदराबाद विश्वविद्यालय
University of Hyderabad

Lab Report No. 9

MV407: IC Design Lab-1 (Digital)

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1 | Ring counter

1.1 | Objective

Design RTL for ring counter. Verify its functionality using testbench.

1.2 | Code

1.2.1 | Design

```
1
2  `timescale 1ns / 1ps
3  //////////////////////////////////////////////////////////////////////////////////
4  // Company : CASEST, University of Hyderabad:
5  // Author : Abhinav M
6  //
7  // Create Date: 10/25/2023 02:52:37 PM
8  // Design Name:
9  // Module Name: CB_DFF_async
10 // Project Name:
11 // Target Devices:
12 // Tool Versions:
13 // Description:
14 //
15 // Dependencies:
16 //
17 // Revision:
18 // Revision 0.01 - File Created
19 // Additional Comments:
20 //
21 //////////////////////////////////////////////////////////////////////////////////
22 module ringcounter (out,clk,rst);
23 input clk,rst;
24 output [3:0] out;
25 reg [3:0] q;
26
27 always @(posedge clk) begin
28 if(rst) begin
29  q <= 4'b1000;
30 end
31 else begin
32  q[0] <= q[3];
33  q[1] <= q[0];
34  q[2] <= q[1];
35  q[3] <= q[2];
36 end
37 end
38
39 assign out = q;
40 endmodule
```

1.2.2 | Testbench

```
1
2  `timescale 1ns / 1ps
3  //////////////////////////////////////////////////////////////////////////////////
4  // Company:
5  // Author: Abhinav M
6  //
7  // Create Date: 10/25/2023 03:02:13 PM
8  // Design Name:
9  // Module Name: tb_CB_DFF_sync
10 // Project Name:
11 // Target Devices:
12 // Tool Versions:
13 // Description:
14 //
15 // Dependencies:
16 //
17 // Revision:
18 // Revision 0.01 - File Created
19 // Additional Comments:
20 //
21 //////////////////////////////////////////////////////////////////////////////////
22 module ringcounter_tb ();
23 reg clk,rst;
24 wire [3:0] out;
25
26 ringcounter uut(out,clk,rst);
27
```

```
28  initial begin
29  clk = 0;
30  forever #5 clk = ~clk;
31  end
32
33  initial begin
34  rst = 1'b1;
35  #20 rst = 1'b0;
36  #200 $ finish;
37  end
38  endmodule
```

1.3 | Elaborated design

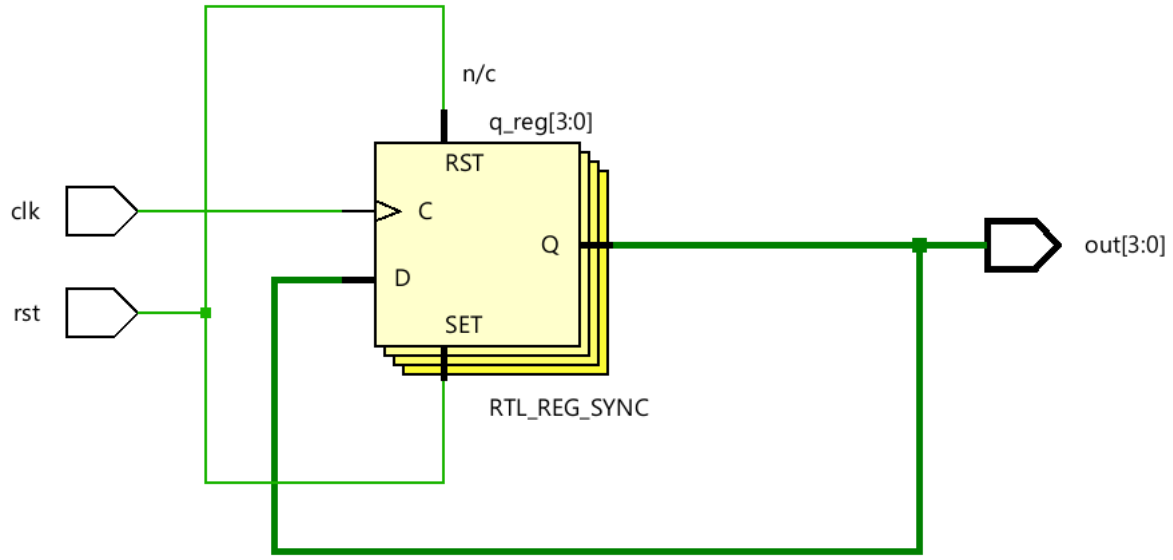

Figure 1.1: Elaborated design

1.4 | Timing diagram

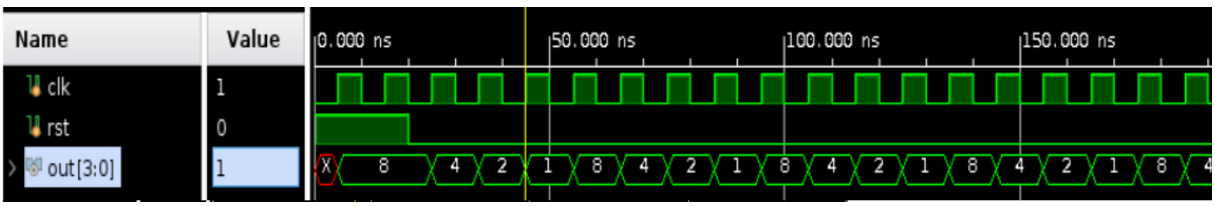

Figure 1.2: Timing diagram

1.5 | Remarks

Circuit was designed and tested successfully, expected functionality was achieved.

2 | Johnson counter

2.1 | Objective

Design RTL for johnson counter. Verify its functionality using testbench.

2.2 | Code

2.2.1 | Design

```
1
2  `timescale 1ns / 1ps
3  //////////////////////////////////////////////////////////////////////////////////
4  // Company : CASEST, University of Hyderabad:
5  // Author : Abhinav M
6  //
7  // Create Date: 10/25/2023 02:52:37 PM
8  // Design Name:
9  // Module Name: CB_DFF_async
10 // Project Name:
11 // Target Devices:
12 // Tool Versions:
13 // Description:
14 //
15 // Dependencies:
16 //
17 // Revision:
18 // Revision 0.01 - File Created
19 // Additional Comments:
20 //
21 //////////////////////////////////////////////////////////////////////////////////
22 module johnsoncounter (out,clk,rst);
23 input clk,rst;
24 output [3:0] out;
25 reg [3:0] q;
26
27 always @(posedge clk) begin
28 if(rst) begin
29  q <= 4'b1000;
30 end
31 else begin
32  q[3] <= q[0];
33  q[2] <= q[3];
34  q[1] <= q[2];
35  q[0] <= q[1];
36 end
37 end
38
39 assign out = q;
40 endmodule
```

2.2.2 | Testbench

```
1
2  `timescale 1ns / 1ps
3  //////////////////////////////////////////////////////////////////////////////////
4  // Company:
5  // Author: Abhinav M
6  //
7  // Create Date: 10/25/2023 03:02:13 PM
8  // Design Name:
9  // Module Name: tb_CB_DFF_sync
10 // Project Name:
11 // Target Devices:
12 // Tool Versions:
13 // Description:
14 //
15 // Dependencies:
16 //
17 // Revision:
18 // Revision 0.01 - File Created
19 // Additional Comments:
20 //
21 //////////////////////////////////////////////////////////////////////////////////
22 module johnsoncounter_tb ();
23 reg clk,rst;
24 wire [3:0] out;
25
26 johnsoncounter uut(out,clk,rst);
27
```

```
28  initial begin
29  clk = 0;
30  forever #5 clk = ~clk;
31  end
32
33  initial begin
34  rst = 1'b1;
35  #20 rst = 1'b0;
36  #200 $ finish;
37  end
38  endmodule
```

2.3 | Elaborated design

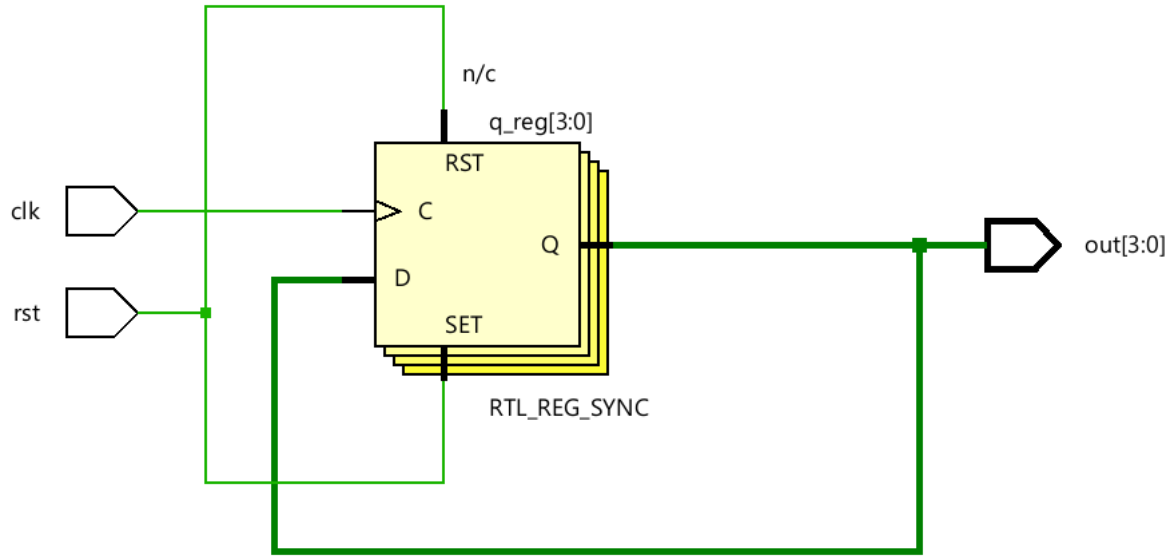

Figure 2.1: Elaborated design

2.4 | Timing diagram

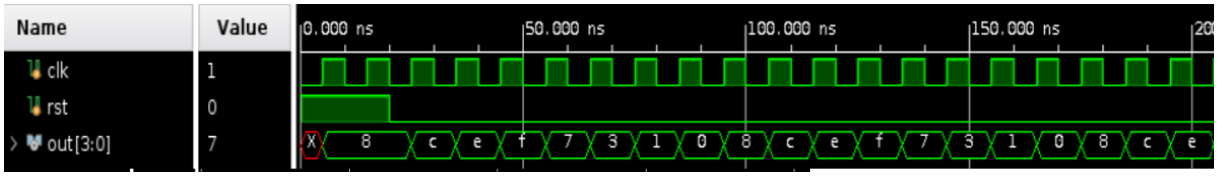

Figure 2.2: Timing diagram

2.5 | Remarks

Circuit was designed and tested successfully, expected functionality was achieved.

3 | References

A | Appendix A: GitHub Repo

The GitHub repo referenced below contains the Verilog code and testbenches mentioned in this report.
https://github.com/AbhinavM2000/MV401D/