1010 Sequence Detector

CASEST

हैदराबाद विश्वविद्यालय
University of Hyderabad

Lab Report No. 7

MV407: IC Design Lab-1 (Digital)

Submitted by:

Full Name	Enrollment No.
Abhinav M	23PMMT11(@uohyd.ac.in)

Lab Instructor: Dr. Bhawna Gomber

Teaching Assistant: Ms. Bhargavi

Center for Advanced Studies in Electronics Science and Technology
University of Hyderabad
Hyderabad, India

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1 | Overlapping 1010 detector (mealy machine)

1.1 | Problem statement

Design a overlapping 1010 sequence detector mealy machine.

1.2 | Block diagram

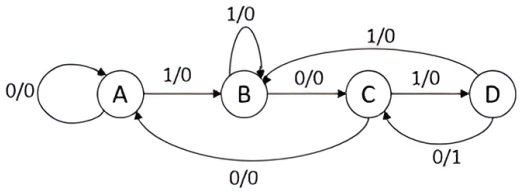

Figure 1.1: State diagram

1.3 | Code

1.3.1 | Design

```
1
2
3   `timescale 1ns / 1ps
4   //////////////////////////////////////////////////////////////////////////////////
5   // Company: CASEST, University of Hyderabad
6   // Author: Abhinav M
7   //
8   // Create Date: 11/22/2023 02:55:51 PM
9   // Design Name:
10  // Module Name: FB_det_1010_mea
11  // Project Name:
12  // Target Devices:
13  // Tool Versions:
14  // Description:
15  //
16  // Dependencies:
17  //
18  // Revision:
19  // Revision 0.01 - File Created
20  // Additional Comments:
21  //
22  //////////////////////////////////////////////////////////////////////////////////
23  module FB_det_1010_mea(input clk,input w,input rst,output reg z);
24      reg [1:0]CS, NS;
25      //wire [1:0]A,B,C,D;
26      //assign A=2'b00;
27      //assign B=2'b01;
28      //assign C=2'b10;
29      //assign D=2'b11;
30  parameter A=2'b00, B=2'b01,C=2'b10,D=2'b11;
31      always@(w,CS)
32          begin
33              case(CS)
34                  A:
35                      begin
36                          if(w==0)
37                              begin
38                                  NS=A;
39                                  z=0;
40                              end
41                          else
42                              begin
43                                  NS=B;
44                                  z=0;
45                              end
46                      end
47                  B:
48                      begin
49                          if(w==0)
50                              begin
51                                  NS=C;
52                                  z=0;
```

```
                            end
                        else
                            begin
                                NS=B;
                                z=0;
                            end
                    end
                C:
                    begin
                        if(w==0)
                            begin
                                NS=A;
                                z=0;
                            end
                        else
                            begin
                                NS=D;
                                z=0;
                            end
                    end
                D:
                    begin
                        if(w==0)
                            begin
                                NS=C;
                                z=1;
                            end
                        else
                            begin
                                NS=B;
                                z=0;
                            end
                    end
            endcase
        end

    always@(posedge clk)  //CS triggered here, w triggered at i/p
        begin
            if(rst==1)
                CS<=A;   //init
            else
                CS<=NS; //NS from prev. clk
        end
endmodule
```

1.3.2 | Testbench

```


`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company: CASEST, University of Hyderabad
// Author: Abhinav M
//
// Create Date: 11/22/2023 03:30:39 PM
// Design Name:
// Module Name: tb_FB_det_1010_mea
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////
module tb_FB_det_1010_mea();
   wire z;
   reg clk,w,rst;
   FB_det_1010_mea uut(clk,w,rst,z);
initial
    begin
        clk=0;
        forever #1 clk = ~clk;
    end
initial
begin
rst=1;#2
rst=0;

w=0;#2
```

```
w=1;#2
w=0;#2
w=1;#2
w=0;#2
// hit
w=1;#2
w=1;#2
w=0;#2
w=0;#2
w=1;#2
w=0;#2
w=1;#2
w=0;#2
// hit

w=0;#2
w=1;#2
w=0;#2
w=1;#2
w=0;#2
// hit
w=1;#2
w=1;#2
w=0;#2
w=0;#2
w=1;#2
w=0;#2
w=1;#2
w=0;#2
// hit

w=0;#2
w=1;#2
w=0;#2
w=1;#2
w=0;#2
// hit
w=1;#2
w=1;#2
w=0;#2
w=0;#2
w=1;#2
w=0;#2
w=1;#2
w=0;#2
// hit

w=0;#2
w=1;#2
w=0;#2
w=1;#2
w=0;#2
// hit
w=1;#2
w=1;#2
w=0;#2
w=0;#2
w=1;#2
w=0;#2
w=1;#2
w=0;#2
// hit

w=0;#2
w=1;#2
w=0;#2
w=1;#2
w=0;#2
// hit
w=1;#2
w=1;#2
w=0;#2
w=0;#2
w=1;#2
w=0;#2
w=1;#2
w=0;#2
// hit
w=0;#2
#50 $finish;
end
endmodule
```

1.4 | Elaborated design

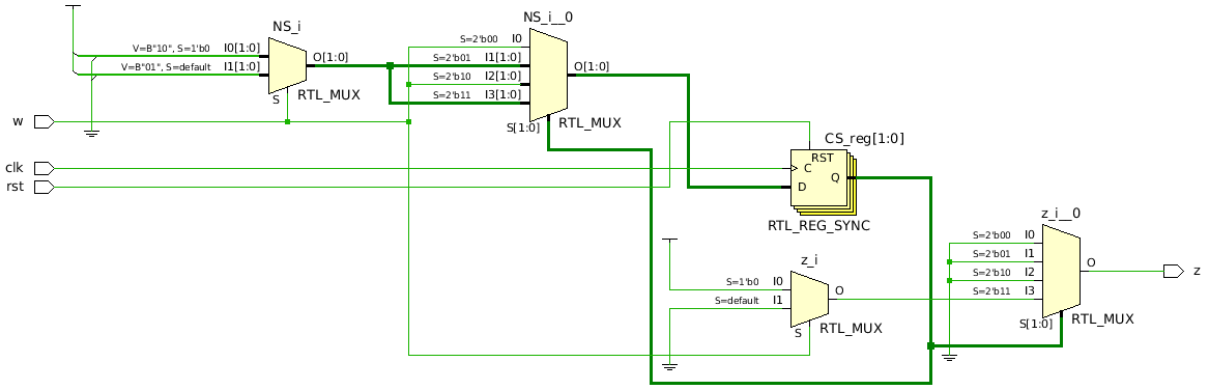

Figure 1.2: Elaborated design.

1.5 | Timing diagram

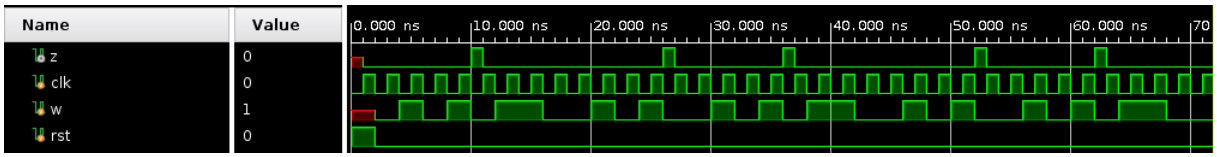

Figure 1.3: Timing diagram.

1.6 | Remarks

Circuit was designed and tested successfully.

2 | References

A | Appendix A: GitHub Repo

The GitHub repo referenced below contains the Verilog code and testbenches mentioned in this report.
https://github.com/AbhinavM2000/MV401D/