Full adder VIO

CASEST

हैदराबाद विश्वविद्यालय
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Lab Report No. 2

MV—: Digital VLSI System Design Lab

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Contents

1 | Introduction

1.1 | Objective

Full adder implementation and verification using VIO.

2 | Code

2.1 | Full adder

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 09/13/2023 02:55:03 PM
// Design Name:
// Module Name: fa
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////

module fa(
    input a,
    input b,
    input c_in,
    output s,
    output c_out
    );




    wire w_1,w_2,w_3,w_4;

    xor x_1(w_1, a,b); //A XOR B
    xor x_2(s, w_1,c_in); // A XOR B XOR C_IN = SUM

    and a_1(w_3,w_1,c_in); // (A XOR B) .C_IN
    and a_2(w_4,a,b); // A.B
    or o_1(c_out,w_3); // // (A XOR B) .C_IN + AB = C_OUT

endmodule
// SUM = A XOR B XOR C_IN | C_OUT = (A XOR B) C_IN + A.B
```

2.2 | Top module

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 01/17/2024 04:25:59 PM
// Design Name:
// Module Name: top_m
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module top_m(
    input clk
    );

    wire probe_in0,probe_in1,probe_out0,probe_out1,probe_out2;

vio_0 vio_test (
  .clk(clk),                // input wire clk
  .probe_in0(probe_in0),    // input wire [0 : 0] probe_in0
  .probe_in1(probe_in1),    // input wire [0 : 0] probe_in1
  .probe_out0(probe_out0),  // output wire [0 : 0] probe_out0
  .probe_out1(probe_out1),  // output wire [0 : 0] probe_out1
  .probe_out2(probe_out2)  // output wire [0 : 0] probe_out2
);
    fa ex1(probe_out0,probe_out1,probe_out2,probe_in1,probe_in0);

endmodule
```

2.3 | Testbench

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 09/13/2023 03:32:44 PM
// Design Name:
// Module Name: test_fa
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
```

```
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module test_fa(

    );
    reg a,b,c_in;
    wire  s,c_out;
    fa uut(a,b,c_in,s,c_out);
    initial
    begin
    #10 a=0;b=0;c_in=0;
    #10 a=0;b=0;c_in=1;
    #10 a=0;b=1;c_in=0;
    #10 a=0;b=1;c_in=1;
    #10 a=1;b=0;c_in=0;
    #10 a=1;b=0;c_in=1;
    #10 a=1;b=1;c_in=0;
    #10 a=1;b=1;c_in=1;

    #10 $finish;
    end

endmodule
```

2.4 | Result

Full adder was simulated successfully and implemented in Zedboard and verified functionality with VIO.

3 | References

A | Appendix A: GitHub Repo

The GitHub repo referenced below contains the Verilog code and testbenches mentioned in this report.
https://github.com/AbhinavM2000/MV401D/