Quiz: Intro and Verilog basics

Draw the schematic of a 4 bit adder, label the schematic. Write a Verilog code in structural level for the labelled schematic design.

```
1  module adder_four_bit(
2  output [3:0]sum,
3  output cout ,
4  input [3:0]a,b);
5
6  wire c1,c2,c3,c4;
7
8  full_3 ad0( .a(a[0]), .b(b[0]),.cin(0), .s(sum[0]), .cout(c1));
9  full_3 ad1( .a(a[1]), .b(b[1]),.cin(c1), .s(sum[1]), .cout(c2));
10 full_3 ad2( .a(a[2]), .b(b[2]),.cin(c2), .s(sum[2]), .cout(c3));
11 full_3 ad3( .a(a[3]), .b(b[3]),.cin(c3), .s(sum[3]), .cout(c4));
12 assign cout= c4;
13 endmodule
14
15 module full_3(a,b,cin,s,cout);
16 input a,b,cin;
17 output s, cout;
18 assign s=a^b^cin;
19 assign cout = (a&b) | (b&cin) | (cin&a);
20 endmodule
21
```