

1010 Sequence Detector

CASEST



हैदराबाद विश्वविद्यालय
University of Hyderabad

Lab Report No. 7

MV407: IC Design Lab-1 (Digital)

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1 | Overlapping 1010 detector (mealy machine)

1.1 | Problem statement

Design a overlapping 1010 sequence detector mealy machine.

1.2 | Block diagram

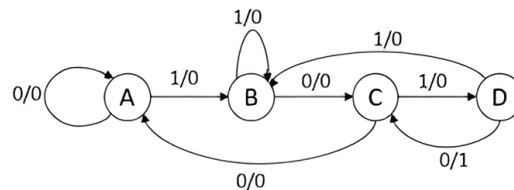


Figure 1.1: State diagram

1.3 | Code

1.3.1 | Design

```
1
2
3 `timescale 1ns / 1ps
4 //////////////////////////////////////////////////////////////////////////////////////////////////////////////////
5 // Company: CASEST, University of Hyderabad
6 // Author: Abhinav M
7 //
8 // Create Date: 11/22/2023 02:55:51 PM
9 // Design Name:
10 // Module Name: FB_det_1010_mea
11 // Project Name:
12 // Target Devices:
13 // Tool Versions:
14 // Description:
15 //
16 // Dependencies:
17 //
18 // Revision:
19 // Revision 0.01 - File Created
20 // Additional Comments:
21 //
22 //////////////////////////////////////////////////////////////////////////////////////////////////////////////////
23 module FB_det_1010_mea(input clk,input w,input rst,output reg z);
24     reg [1:0]CS, NS;
25     //wire [1:0]A,B,C,D;
26     //assign A=2'b00;
27     //assign B=2'b01;
28     //assign C=2'b10;
29     //assign D=2'b11;
30     parameter A=2'b00, B=2'b01,C=2'b10,D=2'b11;
31     always@(w,CS)
32     begin
33         case(CS)
34             A:
35                 begin
36                     if(w==0)
37                         begin
38                             NS=A;
39                             z=0;
40                         end
41                     else
42                         begin
43                             NS=B;
44                             z=0;
45                         end
46                 end
47             B:
48                 begin
49                     if(w==0)
50                         begin
51                             NS=C;
52                             z=0;
```



```
53         end
54     else
55         begin
56             NS=B;
57             z=0;
58         end
59     end
60     C:
61     begin
62         if(w==0)
63             begin
64                 NS=A;
65                 z=0;
66             end
67         else
68             begin
69                 NS=D;
70                 z=0;
71             end
72         end
73     D:
74     begin
75         if(w==0)
76             begin
77                 NS=C;
78                 z=1;
79             end
80         else
81             begin
82                 NS=B;
83                 z=0;
84             end
85         end
86     endcase
87 end
88
89 always@(posedge clk) //CS triggered here, w triggered at i/p
90 begin
91     if(rst==1)
92         CS<=A; //init
93     else
94         CS<=NS; //NS from prev. clk
95     end
96 endmodule
```

1.3.2 Testbench

```
1
2
3 `timescale 1ns / 1ps
4 ///////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////
5 // Company: CASEST, University of Hyderabad
6 // Author: Abhinav M
7 //
8 // Create Date: 11/22/2023 03:30:39 PM
9 // Design Name:
10 // Module Name: tb_FB_det_1010_mea
11 // Project Name:
12 // Target Devices:
13 // Tool Versions:
14 // Description:
15 //
16 // Dependencies:
17 //
18 // Revision:
19 // Revision 0.01 - File Created
20 // Additional Comments:
21 //
22 ///////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////
23 module tb_FB_det_1010_mea();
24     wire z;
25     reg clk,w,rst;
26     FB_det_1010_mea uut(clk,w,rst,z);
27     initial
28     begin
29         clk=0;
30         forever #1 clk = ~clk;
31     end
32     initial
33     begin
34         rst=1;#2
35         rst=0;
36
37         w=0;#2
```



```
38 w=1;#2
39 w=0;#2
40 w=1;#2
41 w=0;#2
42 // hit
43 w=1;#2
44 w=1;#2
45 w=0;#2
46 w=0;#2
47 w=1;#2
48 w=0;#2
49 w=1;#2
50 w=0;#2
51 // hit
52
53 w=0;#2
54 w=1;#2
55 w=0;#2
56 w=1;#2
57 w=0;#2
58 // hit
59 w=1;#2
60 w=1;#2
61 w=0;#2
62 w=0;#2
63 w=1;#2
64 w=0;#2
65 w=1;#2
66 w=0;#2
67 // hit
68
69 w=0;#2
70 w=1;#2
71 w=0;#2
72 w=1;#2
73 w=0;#2
74 // hit
75 w=1;#2
76 w=1;#2
77 w=0;#2
78 w=0;#2
79 w=1;#2
80 w=0;#2
81 w=1;#2
82 w=0;#2
83 // hit
84
85 w=0;#2
86 w=1;#2
87 w=0;#2
88 w=1;#2
89 w=0;#2
90 // hit
91 w=1;#2
92 w=1;#2
93 w=0;#2
94 w=0;#2
95 w=1;#2
96 w=0;#2
97 w=1;#2
98 w=0;#2
99 // hit
100
101 w=0;#2
102 w=1;#2
103 w=0;#2
104 w=1;#2
105 w=0;#2
106 // hit
107 w=1;#2
108 w=1;#2
109 w=0;#2
110 w=0;#2
111 w=1;#2
112 w=0;#2
113 w=1;#2
114 w=0;#2
115 // hit
116 w=0;#2
117 #50 $finish;
118 end
119 endmodule
```

1.4 | Elaborated design

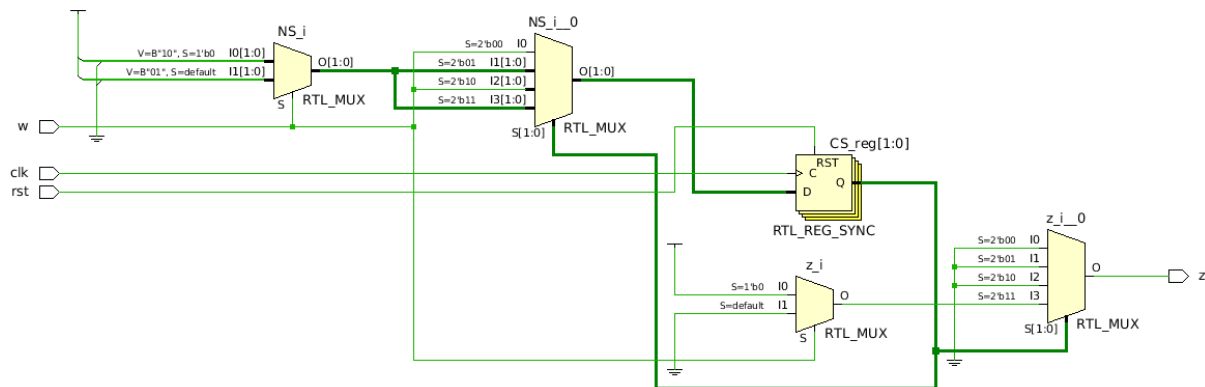


Figure 1.2: Elaborated design.

1.5 | Timing diagram

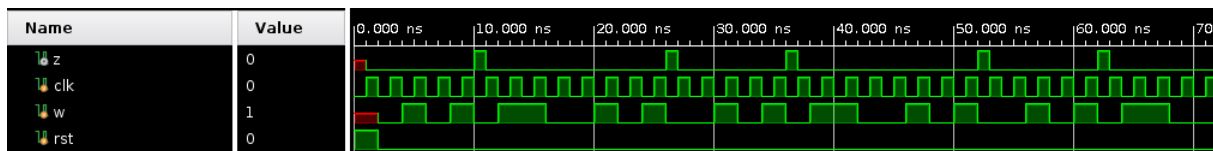


Figure 1.3: Timing diagram.

1.6 | Remarks

Circuit was designed and tested successfully.



2 | References



A | Appendix A: GitHub Repo

The GitHub repo referenced below contains the Verilog code and testbenches mentioned in this report.

<https://github.com/AbhinavM2000/MV401D/>