Dual port RAM VIO

CASEST

हैदराबाद विश्वविद्यालय
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Lab Report No. 2

MV—: Digital VLSI System Design Lab

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1 | Introduction

1.1 | Objective

Dual port RAM implementation and verification using VIO.

2 | Code

2.1 | Dual port RAM

```
‘timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 04/24/2024 06:32:15 AM
// Design Name:
// Module Name: dp_ram
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module d_p_ram(input [7:0] data_a, data_b,input [5:0] addr_a, addr_b,input we_a, we_b, i

 reg [15:0] ram1 [1023:0];

  always @ (posedge clk)
    begin
      if(we_a)
        ram1[addr_a] <= data_a;

    end

  always @ (posedge clk)
    begin
      if(we_b)
        ram1[addr_b] <= data_b;

    end

         assign q_b = ram1[addr_b];
        assign q_a = ram1[addr_a];
endmodule
```

2.2 | Top module

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 04/24/2024 07:20:43 AM
// Design Name:
// Module Name: topww
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module topww(input clk);

    wire [7 : 0] probe_in0;
    wire [7 : 0] probe_in1;
 wire [5 : 0] probe_in2;
   wire [5 : 0] probe_in3;
    wire [0 : 0] probe_in4;
 wire [0 : 0] probe_in5;
  wire [7 : 0] probe_out0;
  wire [7 : 0] probe_out1;







    vio_0 vio_0 (
  .clk(clk),                // input wire clk
  .probe_in0(probe_in0),    // input wire [7 : 0] probe_in0
  .probe_in1(probe_in1),    // input wire [7 : 0] probe_in1
  .probe_in2(probe_in2),    // input wire [5 : 0] probe_in2
  .probe_in3(probe_in3),    // input wire [5 : 0] probe_in3
  .probe_in4(probe_in4),    // input wire [0 : 0] probe_in4
  .probe_in5(probe_in5),    // input wire [0 : 0] probe_in5
  .probe_out0(probe_out0),  // output wire [7 : 0] probe_out0
  .probe_out1(probe_out1)  // output wire [7 : 0] probe_out1
);
d_p_ram(probe_out1,probe_out0,probe_in5,probe_in4,probe_in3,probe_in2,probe_in1,probe_in
endmodule
```

2.3 | Testbench

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
```

```
//
// Create Date: 04/24/2024 06:37:57 AM
// Design Name:
// Module Name: tb_d_p_ram
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module tb_d_p_ram;
  reg [7:0] data_a, data_b;
  reg [5:0] addr_a, addr_b;
  reg we_a, we_b;
  reg clk;
  wire [7:0] q_a, q_b;

  d_p_ram dpr1(
    .data_a(data_a),
    .data_b(data_b),
    .addr_a(addr_a),
    .addr_b(addr_b),
    .we_a(we_a),
    .we_b(we_b),
    .clk(clk),
    .q_a(q_a),
    .q_b(q_b)
  );

  initial
    begin
      clk=1'b1;
------forever #5 clk = ~clk;
----end

--initial
----begin
------data_a = 8'h33;
      addr_a = 6'h01;
------data_b = 8'h44;
      addr_b = 6'h02;
------we_a = 1'b1;
      we_b = 1'b1;

------#10;

------data_a = 8'h55;
      addr_a = 6'h03;
------addr_b = 6'h01;
```

```
        we_b = 1'b0;

      #10;

      addr_a = 6'h02;
        addr_b = 6'h03;
      we_a = 1'b0;

        #10;

    end

  initial
    #40 $stop;

endmodule
```

2.4 | Result

Dual port RAM was simulated successfully and implemented in Zedboard and verified functionality with VIO.

3 | References

A | Appendix A: GitHub Repo

The GitHub repo referenced below contains the Verilog code and testbenches mentioned in this report.
https://github.com/AbhinavM2000/MV401D/