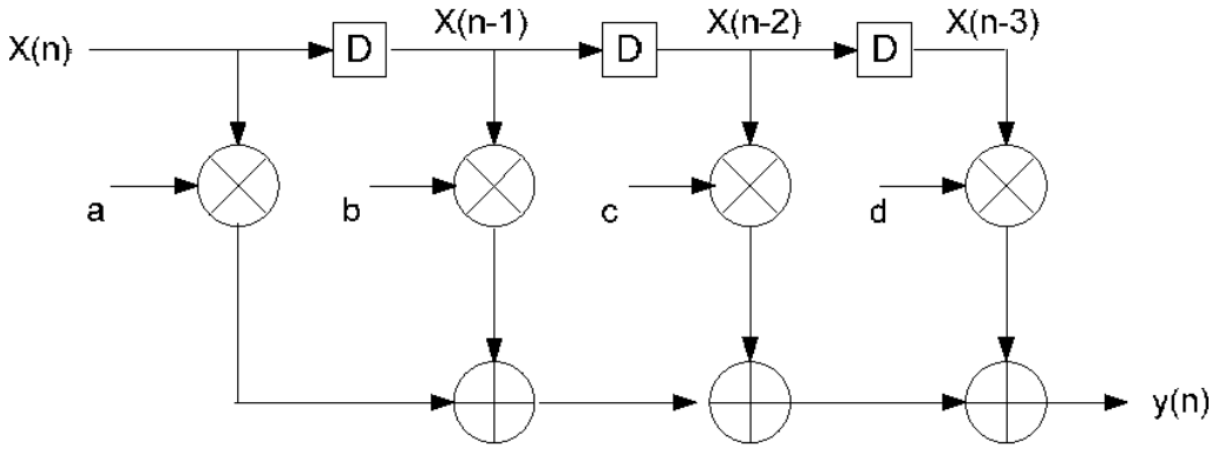
Question

To design a 4- tap FIR filter, report timing, power and utilization.

Logic



Code

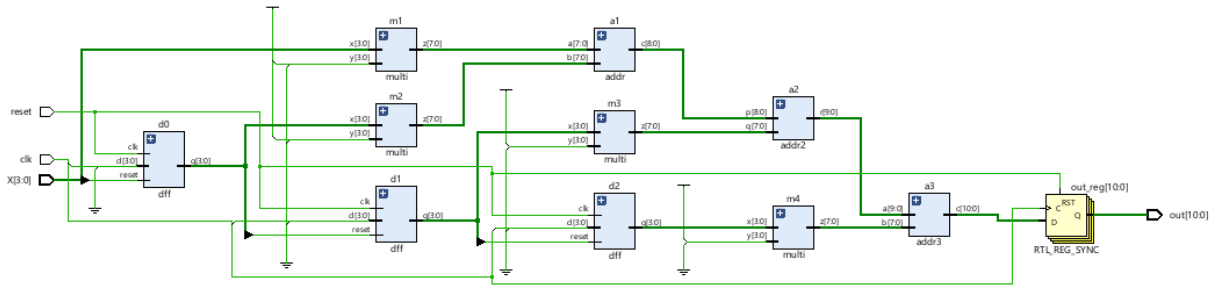
```
module tap_4_fir(
  input [3:0] X,
  input clk,
  input reset,
  output reg [10:0] out
);

  wire [3:0] H0,H1,H2,H3;
  wire [8:0] add_out1;
  wire [9:0] add_out2;
  wire [10:0] add_out3;
  wire [7:0] mul_out1,mul_out2,mul_out3,mul_out4;
  wire [3:0] X_delay1,X_delay2,X_delay3;

  // Giving h coefficient
assign H0 = 4'd1;
  assign H1 = 4'd2;
  assign H2 = 4'd3;
  assign H3 = 4'd4;

  multi m1(X,H0,mul_out1);
  multi m2(X_delay1,H1,mul_out2);
  multi m3(X_delay2,H2,mul_out3);
  multi m4(X_delay3,H3,mul_out4);
  dff d0(clk,reset,X,X_delay1);
  dff d1(clk,reset,X_delay1,X_delay2);
  dff d2(clk,reset,X_delay2,X_delay3);
  addr a1(mul_out1,mul_out2,add_out1);
  addr2 a2(add_out1,mul_out3,add_out2);
 addr3 a3(add_out2,mul_out4,add_out3);

  always @(posedge clk) begin
    if(reset) begin
```

```
      out<= 0;
    end
    else begin
      out <= add_out3;
    end

  end

endmodule


module multi (
  input [3:0] x,
  input [3:0] y,
  output [7:0] z);
  assign z = x*y;
endmodule

module addr (
  input [7:0] a,
  input [7:0] b,
  output [8:0] c);

  assign c = a + b;
endmodule

   module addr2(
   input [8:0] p,
   input [7:0] q,
   output [9:0] r);
   assign r = p + q;
   endmodule

   module addr3(
   input [9:0] a,
   input [7:0] b,
   output [10:0] c );
   assign c = a + b;
   endmodule


module dff (
input clk,
input reset,
  input [3:0] d,
  output reg [3:0] q
);


  always @(posedge clk) begin
    if(reset) begin
      q <= 0;
    end
    else begin
      q <= d;
    end
    end
endmodule
```

Testbench

```
module tb1;
  reg [3:0] X;
  reg clk;
  reg reset;
  wire [10:0] out;

  tap_4_fir uut(X,clk,reset,out);

  initial begin
    clk = 1'b0;
    forever #5 clk = ~clk;
  end


  initial begin
    #5 reset = 1;
    #8 reset = 0;
    X = 4'd1;
    //#5 X = 4'd7;

    #50 $finish;

  end

endmodule
```

Elaboration



Timing (100ns clock)

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	91.522 ns	Worst Hold Slack (WHS):	0.159 ns	Worst Pulse Width Slack (WPWS):	49.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	48	Total Number of Endpoints:	48	Total Number of Endpoints:	21

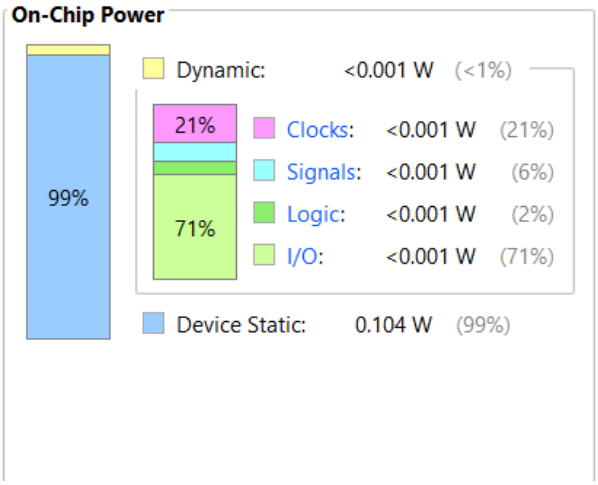
All user specified timing constraints are met.

Power

Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**0.104 W**
Design Power Budget:	**Not Specified**
Process:	typical
Power Budget Margin:	**N/A**
Junction Temperature:	**26.2°C**
Thermal Margin:	58.8°C (4.9 W)
Ambient Temperature:	25.0 °C
Effective ϑJA:	11.5°C/W



Utilization

Resource	Utilization	Available	Utilization %
LUT	7	53200	0.01
FF	9	106400	0.01
IO	17	200	8.50