CASEST

हैदराबाद विश्वविद्यालय
University of Hyderabad

Lab Assignment 3

Digital Signal Processing

Submitted by:

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Contents

Systolic FIR filter

Centre for Advanced Studies in Electronics Science and Technology

Objectives

Design a systolic 4 tap FIR filter

Logic

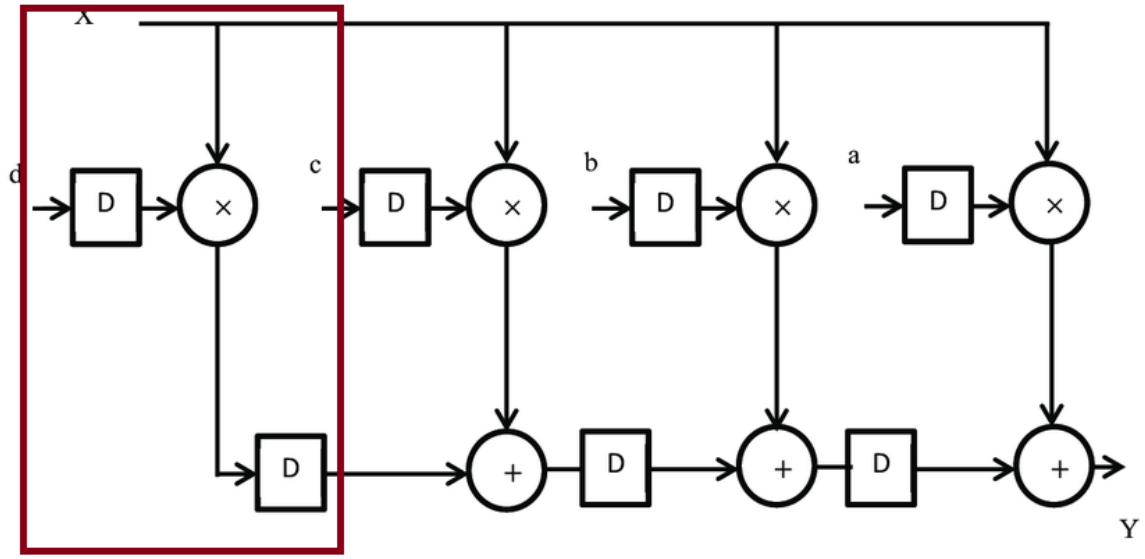


Figure 1 One PE unit is shown in the rectangle, similarly total 4 units.

Code

```
// Delay for coefficients input
module dff_k(
input [3:0] din,
input clk,
input reset,
output reg [3:0] q);

always @(posedge clk) begin
   if(reset) begin
      q <= 0;
   end
   else begin
      q <= din;
   end
end
endmodule

// PE definition
module PE(input [3:0] Xin,
input [3:0] Hin,
input [8:0] Yin,
input reset,
output reg [8:0] Yout,
output reg [3:0] Xout
    );

  always @(Xin,Hin,reset,Yin) begin
    if(reset) begin
      Yout <= 0;
      Xout <= 0;
    end
    else begin
```

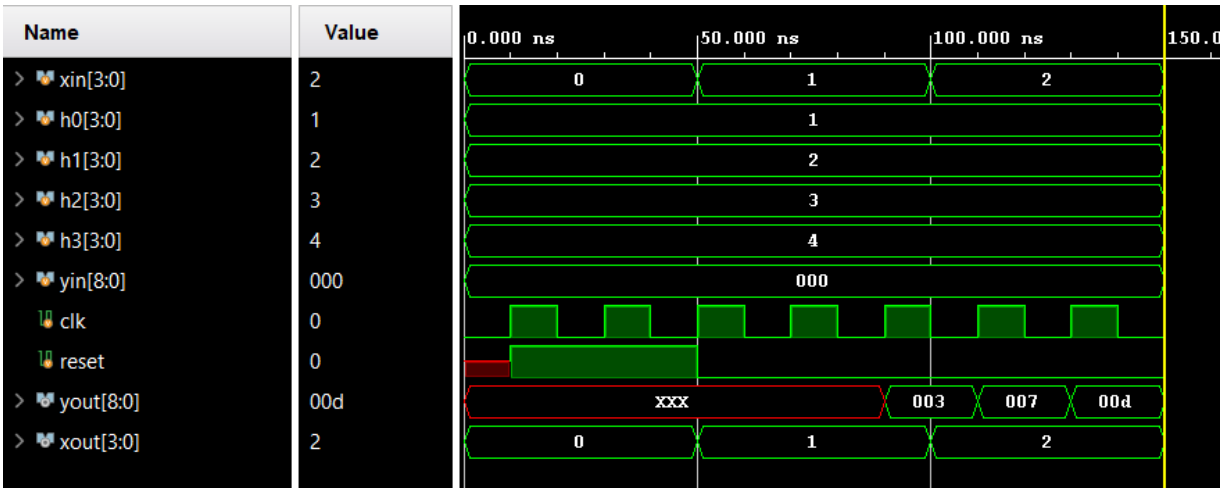
```
     Yout <= (Xin * Hin) + Yin;
     Xout <= Xin;
    end
  end
endmodule


// Delay output <------> adder
module dff_op(
input [8:0] din,
input clk,
input reset,
output reg [8:0] q);

always @(posedge clk) begin
  if(reset) begin
     q <= 0;
  end
  else begin
    q <= din;
  end
end
endmodule

module systlc_fir4(xin,h0,h1,h2,h3,yin,clk,rst,xout,yout);
input [3:0] xin;
input [3:0] h0,h1,h2,h3;
input [8:0] yin;
input clk,rst;
output [3:0] xout;
output [8:0] yout;

wire [8:0] y1,y2,y3,y4,y5,y6,y7;
wire [3:0] x1,x2,x3;
wire [3:0] h_0,h_1,h_2,h_3;


PE p1(.Xin(xin),.Hin(h_0),.Yin(y7),.reset(reset),.Yout(y1),.Xout(x1));
PE p2(.Xin(x1),.Hin(h_1),.Yin(y6),.reset(reset),.Yout(y2),.Xout(x2));
PE p3(.Xin(x2),.Hin(h_2),.Yin(y5),.reset(reset),.Yout(y3),.Xout(x3));
PE p4(.Xin(x3),.Hin(h_3),.Yin(yin),.reset(reset),.Yout(y4),.Xout(xout));


dff_k k1(.din(h0),.clk(clk),.reset(reset),.q(h_0));
dff_k k2(.din(h1),.clk(clk),.reset(reset),.q(h_1));
dff_k k3(.din(h2),.clk(clk),.reset(reset),.q(h_2));
dff_k k4(.din(h3),.clk(clk),.reset(reset),.q(h_3));


dff_op o1(.din(y1),.clk(clk),.reset(reset),.q(yout));
dff_op o2(.din(y2),.clk(clk),.reset(reset),.q(y7));
dff_op o3(.din(y3),.clk(clk),.reset(reset),.q(y6));
dff_op o4(.din(y4),.clk(clk),.reset(reset),.q(y5));
endmodule
```

Test bench

```
module tb();
reg [3:0] xin;
```

```
reg [3:0] h0,h1,h2,h3;
reg [8:0] yin;
reg clk;
reg reset;
wire [8:0] yout;
wire [3:0] xout;

systlc_fir4 uut(xin,h0,h1,h2,h3,yin,clk,reset,xout,yout);

initial begin
  clk = 0;
  forever #10 clk = ~clk;
end

initial begin
   xin = 0;
   h0=1;h1=2;h2=3;h3=4;
  yin = 9'b0;
   #10 reset = 1;
   #40 reset = 0;
   xin = 1;
   #50 xin = 2;
   #50 $finish;
  end

  endmodule
```

Waveform



Elaborated Design

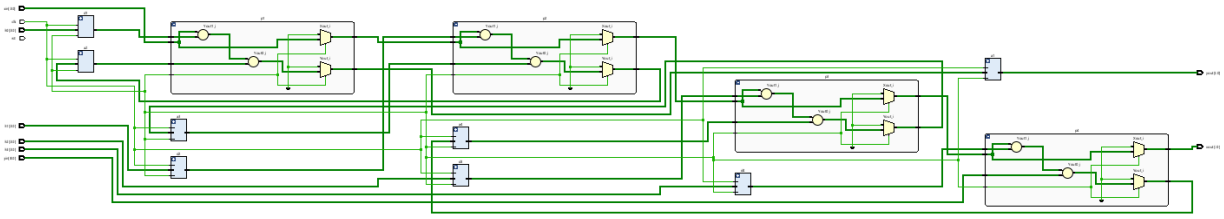


Figure 2 PE elements are seen in the exploded view.

Timing Report

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	91.522 ns	Worst Hold Slack (WHS):	0.249 ns	Worst Pulse Width Slack (WPWS):	49.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	65	Total Number of Endpoints:	65	Total Number of Endpoints:	53

All user specified timing constraints are met.

Figure 3 100ns clock was used

Synthesized Design

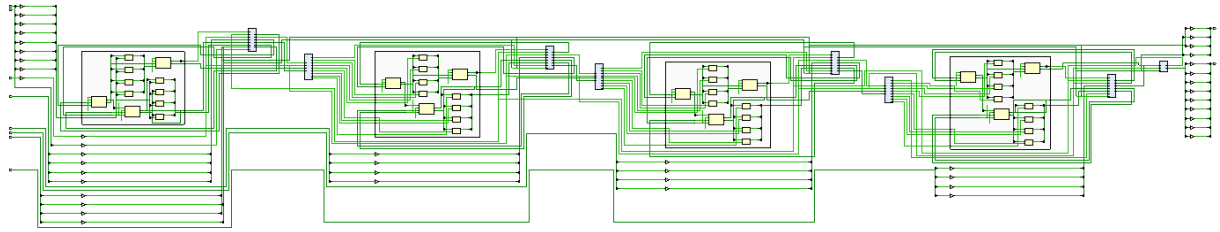
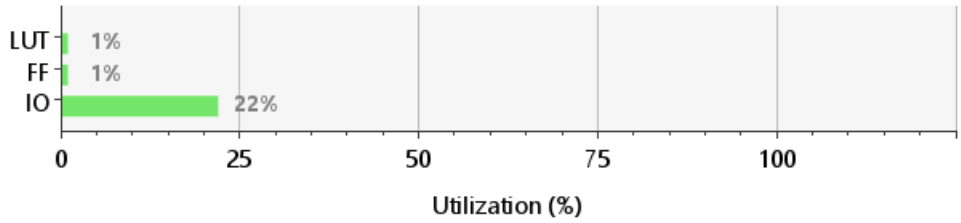


Figure 4 Synthesized PE elements are seen in the exploded view

Utilization

Summary

Resource	Utilization	Available	Utilization %
LUT	97	53200	0.18
FF	52	106400	0.05
IO	43	200	21.50



Power Report

Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**0.103 W**
Design Power Budget:	**Not Specified**
Process:	typical
Power Budget Margin:	**N/A**
Junction Temperature:	**24.1°C**
Thermal Margin:	60.9°C (5.7 W)
Ambient Temperature:	23.0 °C

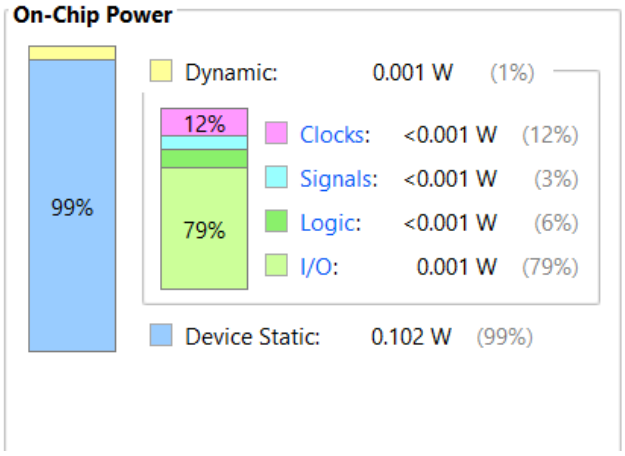


Figure 5 Not accurate without SAIF file