RTL to GDSII for sequence detector

CASEST

हैदराबाद विश्वविद्यालय
University of Hyderabad

Lab Report No. 8

MV407: IC Design Lab-1 (Digital)

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Contents

1 | 011 sequence detector

1.1 | Objective

Demonstrate RTL to GDSII for 011 sequence detector.

1.2 | State diagram

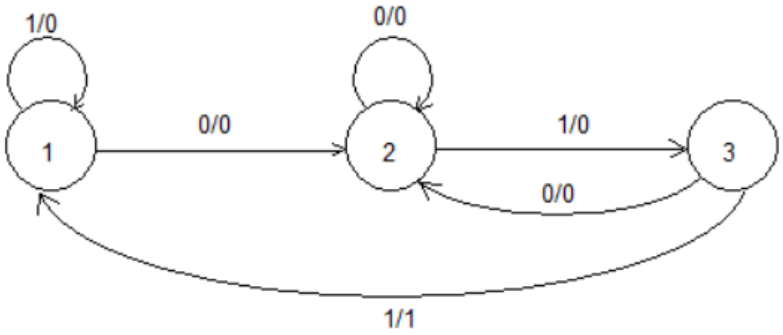


Figure 1.1: State diagram

1.3 | Code

1.3.1 | Design

```
1
2  `timescale 1ns / 1ps
3  //////////////////////////////////////////////////////////////////////////////////
4  // Company : CASEST, University of Hyderabad:
5  // Author : Abhinav M
6  //
7  // Create Date: 11/25/2023 02:52:37 PM
8  // Design Name:
9  // Module Name: 011
10 // Project Name:
11 // Target Devices:
12 // Tool Versions:
13 // Description:
14 //
15 // Dependencies:
16 //
17 // Revision:
18 // Revision 0.01 - File Created
19 // Additional Comments:
20 //
21 //////////////////////////////////////////////////////////////////////////////////
22
23
24
25 `timescale 1ns / 1ps
26 module seq_dec (
27 input in,
28 input clk,
29 input reset,
30 output reg out
31 );
32 Parameter s0= 2 b00 ,s1= 2 b01 ,s2= 2 b10 ;
33 Reg [1:0] cs,ns;
34 always @(posedge clk) begin
35 case(cs)
36 s0:being
37 if(in==0) being
38 ns=s1;
39 out=0;
40 end
41 else begin
42 ns=s0;
43 out=0;
```

```
end
S0 S1 S2
1/1
0/0 1/0
0/1
0/1
1/0
end
s1:being
if(in==0) being
ns=s1;
out=0;
end
else begin
ns=s2;
out=0;
end
end
s2:being
if(in==0) being
ns=s1;
out=0;
end
else begin
ns=s0;
out=1;
end
end
default: out=0;
endcase
always @ (posedge clk or posedge reset) begin
if(reset) cs<= 2 b00 ;
else cs<=ns;
end
endmodule
```

1.3.2 | Testbench

```

`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Author: Abhinav M
//
// Create Date: 11/25/2023 03:02:13 PM
// Design Name:
// Module Name: tb_011
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////
`timescale 1ns / 1ps
module tb();
reg clk,reset,in;
wire out;
seq_dec uut(in,clk,reset,out);
initial begin
clk=0;
forever #5 clk=~clk;
end
initial begin
reset=1; #14;
reset=0;#1;
in=0;#10;
in=1;#10;
in=1;#10;
in=0;#10;
in=1;#10;
in=1;#10;
in=0;#10;
in=0;#10;
in=1;#10;
in=0;#10;
$finish;
end
endmodule
```

1.4 | Elaborated design

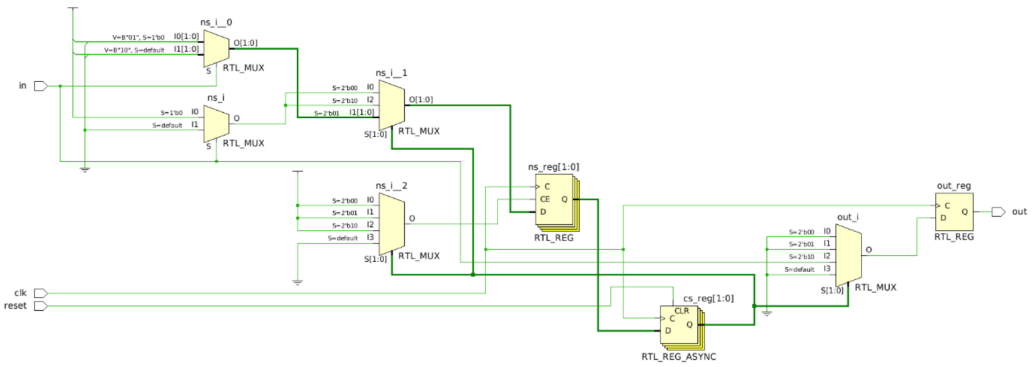


Figure 1.2: Elaborated design.

1.5 | Timing diagram

Figure 1.3: Timing Diagram

1.6 | Post synthesis netlist

```
1
2  module seq_dec(in, clk, reset, out);
3  input in, clk, reset;
4  output out;
5  wire in, clk, reset;
6  wire out;
7  wire [1:0] cs;
8  wire [1:0] ns;
9  wire UNCONNECTED, UNCONNECTED0, n_0, n_1, n_2, n_3, n_4;
10 DFFTRX1 \ns_reg[1] (.CK (clk), .D (cs[0]), .RN (n_4), .Q (ns[1]), .QN
11 (UNCONNECTED));
12 SDFFHQX1 \ns_reg[0] (.CK (clk), .D (ns[0]), .SI (n_3), .SE (n_0), .Q
13 (ns[0]));
14 DFFTRXL out_reg(.CK (clk), .D (cs[1]), .RN (n_2), .Q (out), .QN
15 (UNCONNECTED0));
16 OAI2BB2XL g235__8780(.AON (ns[1]), .A1N (cs[1]), .B0 (cs[1]), .B1
17 (n_3), .Y (n_4));
18 DFFRHQX1 \cs_reg[1] (.RN (n_1), .CK (clk), .D (ns[1]), .Q (cs[1]));
19 NOR2XL g238__4296(.A (cs[0]), .B (n_3), .Y (n_2));
20 DFFRHQX1 \cs_reg[0] (.RN (n_1), .CK (clk), .D (ns[0]), .Q (cs[0]));
21 NAND2XL g239__3772(.A (cs[0]), .B (cs[1]), .Y (n_0));
22 INVXL g240(.A (reset), .Y (n_1));
23 INVXL g241(.A (in), .Y (n_3));
24 endmodule
```

1.7 | SDC

```
set sdc_version 2.0
set_units -capacitance 1000.0fF
set_units -time 1000.0ps
# Set the current design
current_design seq_dec
create_clock -name "clk" -period 10.0 -waveform {0.0 5.0} [get_ports clk]
set_clock_transition 0.1 [get_clocks clk]
set_clock_gating_check -setup 0.0
set_wire_load_mode "enclosed"
set_dont_use [get_lib_cells tsmc18/RF1R1WX2]
set_dont_use [get_lib_cells tsmc18/RF2R1WX2]
set_dont_use [get_lib_cells tsmc18/RFRDX1]
set_dont_use [get_lib_cells tsmc18/RFRDX2]
set_dont_use [get_lib_cells tsmc18/RFRDX4]
set_dont_use [get_lib_cells tsmc18/TIEHI]
set_dont_use [get_lib_cells tsmc18/TIELO]
set_clock_uncertainty -setup 1.0 [get_ports clk]
set_clock_uncertainty -hold 1.0 [get_ports clk]
```

1.8 | Reports

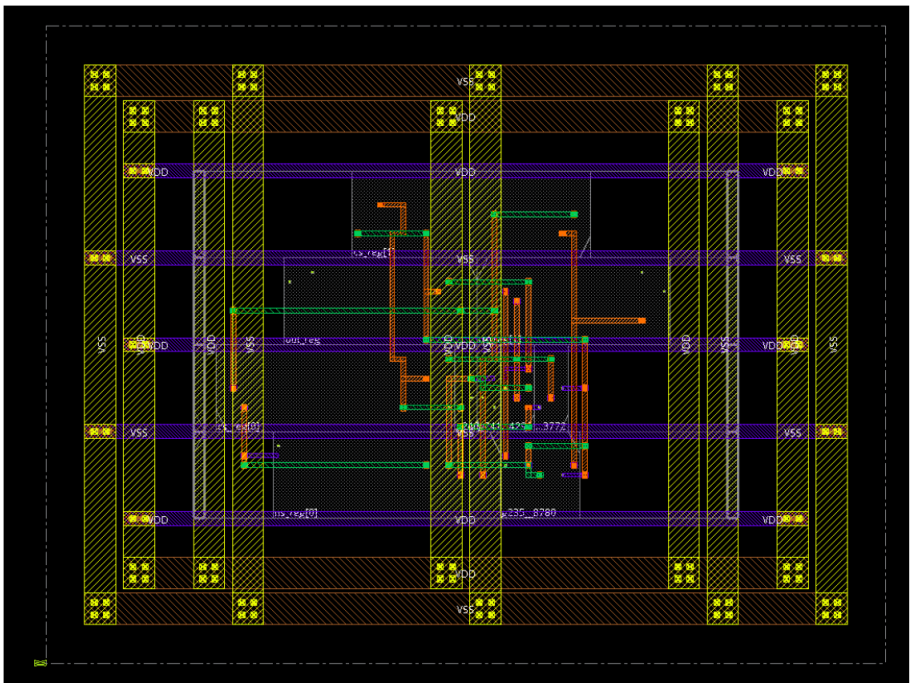
```

 Power:
 Leakage Dynamic Total
Instance Cells Power(nW) Power(nW) Power(nW)
------------------------------------------
seq_dec 10 10.747 46220.515 46231.262
AREA:
Instance Module Cell Count Cell Area Net Area Total Area Wireload
-----------------------------------------------------------------------------
seq_dec 10 375.883 0.000 375.883 <none> (D)
(D) = wireload is default in technology library
Timing:
Path 1: MET (7722 ps) Setup Check with Pin ns_reg[0]/CK->SE
 Group: clk
 Startpoint: (R) cs_reg[1]/CK
 Clock: (R) clk
 Endpoint: (F) ns_reg[0]/SE
 Clock: (R) clk
 Capture Launch
 Clock Edge:+ 10000 0
 Src Latency:+ 0 0
 Net Latency:+ 0 (I) 0 (I)
 Arrival:= 10000 0

 Setup:- 725
 Uncertainty:- 1000
 Required Time:= 8275
 Launch Clock:- 0
 Data Path:- 552
 Slack:= 7722
#-------------------------------------------------------------------------------------------
# Timing Point Flags Arc Edge Cell Fanout Load Trans Delay Arrival Instance
# (fF) (ps) (ps) (ps) Location
#-------------------------------------------------------------------------------------------
 cs_reg[1]/CK - - R (arrival) 5 - 100 - 0 (-,-)
 cs_reg[1]/Q - CK->Q R DFFRHQX1 4 11.3 298 459 459 (-,-)
 g239__3772/Y - B->Y F NAND2XL 1 4.0 112 93 552 (-,-)
 ns_reg[0]/SE <<< - F SDFFHQX1 1 - - 0 552 (-,-)
#-------------------------------------------------------------------------------------------
```

1.9 | Physical Design

```
seq_dec_preCTS:
# Format_clock timeReq slackR/slackF setupR/setupF instName/pinName # cycle(s)
clk(R)->clk(R) 8.272 */7.653 */0.728 ns_reg[0]/SE 1
clk(R)->clk(R) 8.571 */7.949 */0.429 ns_reg[1]/RN 1
clk(R)->clk(R) 8.267 */7.965 */0.733 ns_reg[0]/D 1
clk(R)->clk(R) 8.717 */8.178 */0.283 out_reg/RN 1
@(R)->clk(R) 8.283 */8.204 */0.717 ns_reg[0]/SI 1
clk(R)->clk(R) 8.595 */8.256 */0.405 ns_reg[1]/D 1
clk(R)->clk(R) 8.822 8.317/* 0.178/* out_reg/D 1
clk(R)->clk(R) 8.645 */8.343 */0.355 cs_reg[0]/D 1
clk(R)->clk(R) 8.644 */8.355 */0.356 cs_reg[1]/D 1
@(R)->clk(R) 8.797 8.659/* 0.203/* cs_reg[1]/RN 1
@(R)->clk(R) 8.797 8.659/* 0.203/* cs_reg[0]/RN 1
seq_dec_postCTS:
# Format_clock timeReq slackR/slackF setupR/setupF instName/pinName # cycle(s)
```

```
clk(R)->clk(R) 8.272 */7.653 */0.728 ns_reg[0]/SE 1
clk(R)->clk(R) 8.571 */7.949 */0.429 ns_reg[1]/RN 1
clk(R)->clk(R) 8.267 */7.965 */0.733 ns_reg[0]/D 1
clk(R)->clk(R) 8.717 */8.178 */0.283 out_reg/RN 1
@(R)->clk(R) 8.283 */8.204 */0.717 ns_reg[0]/SI 1
clk(R)->clk(R) 8.595 */8.256 */0.405 ns_reg[1]/D 1
clk(R)->clk(R) 8.822 8.317/* 0.178/* out_reg/D 1
clk(R)->clk(R) 8.645 */8.343 */0.355 cs_reg[0]/D 1
clk(R)->clk(R) 8.644 */8.355 */0.356 cs_reg[1]/D 1
@(R)->clk(R) 8.797 8.659/* 0.203/* cs_reg[1]/RN 1
@(R)->clk(R) 8.797 8.659/* 0.203/* cs_reg[0]/RN 1
```

1.10 | GDSII Layout



1.11 | Remarks

The 011 sequence detector was implemented using 180nm technology from RTL to GDSII.

2 | References

A | Appendix A: GitHub Repo

The GitHub repo referenced below contains the Verilog code and testbenches mentioned in this report.
https://github.com/AbhinavM2000/MV401D/