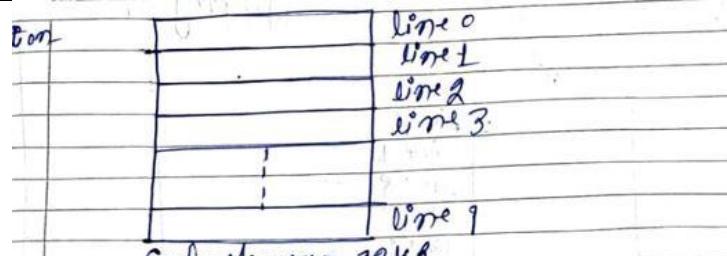


Unit No-04 Question Bank
Paper Code:BCS302
Paper Name: Computer Organization and Architecture

IV	Memory: Basic concept and hierarchy, semiconductor RAM memories, 2D & 2 1/2D memory organization. ROM memories. Cache memories: concept and design issues & performance, address mapping and replacement Auxiliary memories: magnetic disk, magnetic tape and optical disks Virtual memory: concept implementation.	08
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No.	Questions	CO	KL
1.	<p>Consider a machine with a byte addressable main memory of 2^{16} bytes and block size of 8 bytes. Assume that a direct mapped cache consisting of 32 lines used with this machine. How many bits will be there in Tag line, word field of format of main memory addresses ?</p> <p style="text-align: right;"><i>UGC-NET-2020</i></p> <p>Cache Memory = $32 \times 8 = 256$ bytes Main Memory = 2^{16} bytes As we know that [Block size = Line size] Already given data: Block size = 8 bytes So Line size = 8 bytes Main Memory size = 2^{16} bytes Block size = 8 bytes Total no. of blocks = $2^{16} / 8 = 2^{13}$. Line no. → Line no. → Block size. Tag. no. = Total size - (Line no + Block size) = $16 - (5 + 3) = 8$ Tag no. = 3 Tag no., Line no., Block size = 3, 5, 8</p>	<i>CO₄</i>	
2.	<p>Consider a direct mapped cache of size 32 KB with block size 32 bytes. The CPU generate 32-bit address. The number of bits required for cache indexing and Tag bit respectively.</p> <p style="text-align: right;"><i>GATE 2005</i></p>	<i>CO₄</i>	



Cache Memory = 32 kB.

$$\text{Block size} = 32 \text{ bytes} = 2^5$$

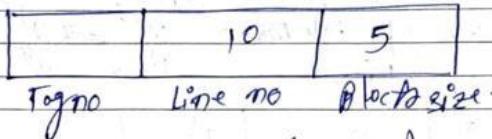
$$\text{Total no. of lines} = \frac{32 \text{ KB}}{32 \text{ B}}$$

$$= 1 \text{ K} = 1024$$

$$= \frac{10}{2}$$

CPU generate logical Address (A) = 32-bit

$$K \quad 32 \rightarrow$$



$$\text{Tag no} = 32 - (10 + 5)$$

$$= 32 - 15$$

$$\text{Tag bit} = 17$$

$$\text{Line bit} = 10$$

$$\text{Block size} = 05$$

3. Write a short note on Magnetic Tape, Magnetic disk and Optical disk.

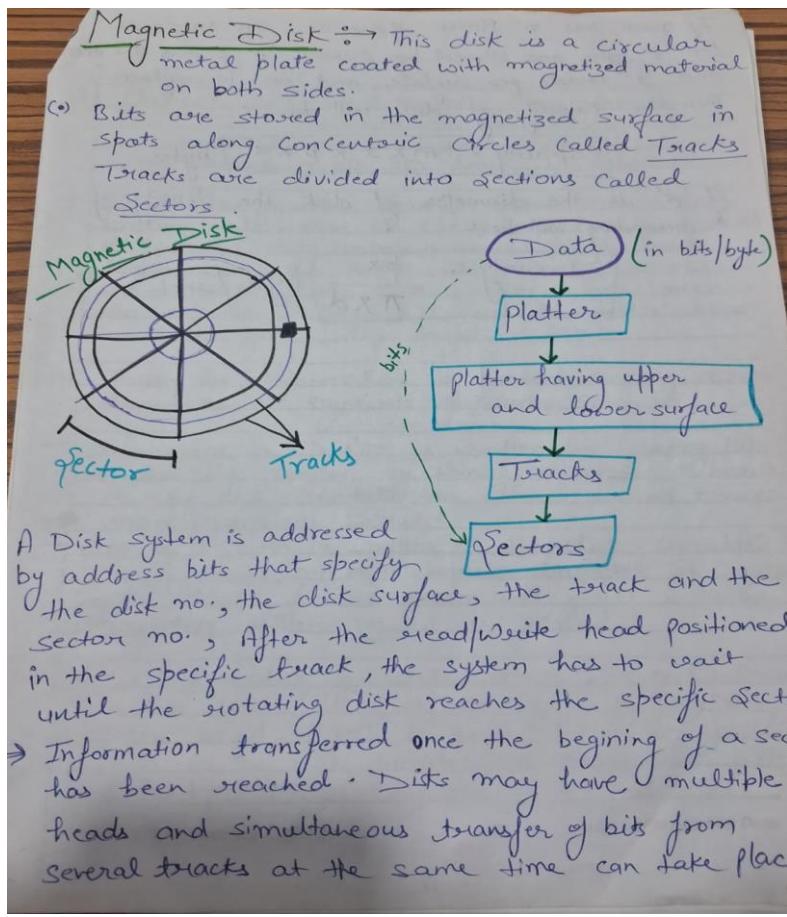
CO_4

1) Magnetic Tapes → This Tape appears similar to the tape used in music Cassettes. It is a plastic Tape with magnetic Coating.

- It comes under Sequentially access and it reads the data line by line.
- It can be stopped, started to move forward or in reverse or can be rewinded.
- This Tape drive consists of two spool on which the tape is wounded. Between these spools, there is a set of nine magnetic heads to read/write the information on the tape.

The nine heads operates independently and records information on nine parallel tracks. A block of data is recorded and then a gap is left and then another block recorded. This gap is called Inter-block Gap (IBG).

- The data on the tape is arranged as block, which can not be accessed. They can only be retrieved sequentially in the same order in which they were written.
- Thus, if desired record is present at the end, earlier records have to be read before it is reached and hence the access time is very high as compared to other devices.
- These are less expensive.



Practical Name: _____ Practical No. _____
 3) Optical Disk → A Magnetic disk, information is recorded in Concentric tracks with simplest constant angular velocity (CAV) system, the number of bits per track is constant.
 → To achieve greater capacity optical disks do not organize information on Concentric tracks. Instead of that, the disk contain a single spiral track beginning near the center and spiraling out to the outer edge of the disk. Sector near the outside of the disk and the Sector near inside the disk, the length is same.
 → Thus the Information is packed evenly across the disk in segments of same size.
 → Information in CD-ROM is written by creating pits on the disk surface by shining a Laser Beam. As the disk rotates the Laser beam traces out a continuous spiral.
 → When a '1' is to be written on the disk, circular pit of around 0.8 micrometer diameter is created by the sharply focused beam and if '0' is to be written often no pit is created.
 → The CD-ROM disk is inserted into a slot of CD-Drive. Then this Drive (disk) is rotated by a motor. A laser head moves 'in' and 'out' to the specified position. As the disk rotates, the head sense pits and land, which is converted to 1's and 0's.
 Sign of Faculty with Date

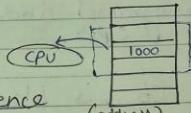
4. Explain the following terms with example.
- Locality of reference
 - Cache write back
 - Cache write through
 - Simultaneous Access

CO₄

Locality of Reference

If CPU has requested one address for memory access, then that particular address or nearby addresses will be accessed soon.

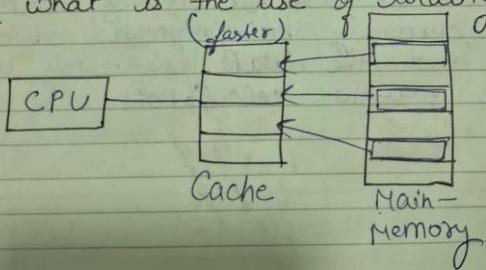
Types



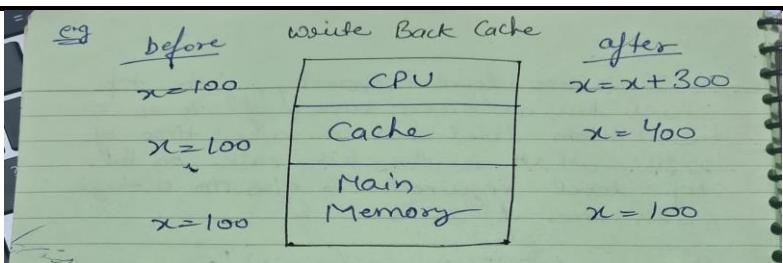
(i) Temporal locality of Reference
(it is based on time). i.e same ^(address) context is referred again.

(ii) Spatial locality of Reference
(based on space). i.e near by addresses will be referred by the CPU.

Q what is the use of locality of reference?

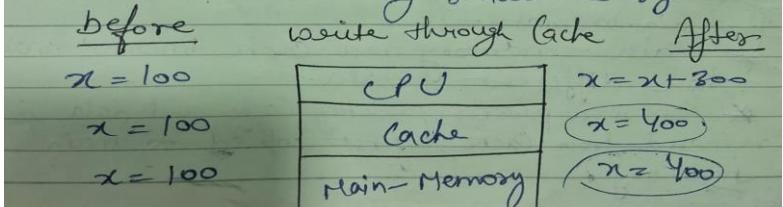


Cache Write back \leftrightarrow To keep data in Cache & main- memory consistent for write operation, write back Cache concept is used.
* when the block written is evicted from Cache, contents of block are written into main- memory.
* Main - memory and cache memory may have different data.
* It is a process of writing Cache and data is removed from Cache, first copied to main memory.



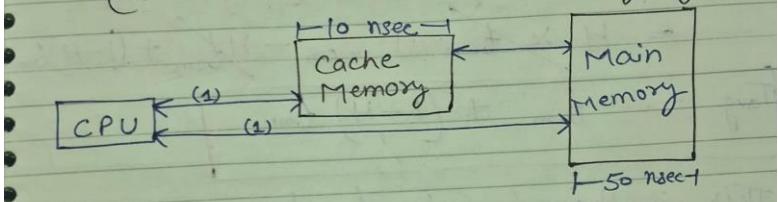
Write through (Cache) \Rightarrow To keep data in Cache & main-memory consistent for write operation, write back cache concept is used.

- * Every write to Cache causes write to main-memory.
- * Main-memory always contains same data as Cache.
- * also, it is a process of writing Cache and main-memory simultaneously.



Types of Cache Access

1. Simultaneous Access (Parallel Access).
2. Hierarchical Access (Serial Access).
(or two-level hierarchical memory organization)



$$T_{avg.} = H * t_{cm} + (1-H)t_{mm}$$

This is the formula for Simultaneously access.

5. Consider a fully associative cache with 8 cache blocks (0-7). The memory block requests are in the order:- 4,3,25,,8,19,6,25,8,16,35,45,22,8,3,16,25,7. If LRU(Least Recent Unit) replacement policy is used. Which cache block will have memory block 7 ?Also calculate the hit ratio and miss ratio.
GATE 2004

CO₄

Solution -	<table border="1"> <tr><td>B0</td><td>4 45</td></tr> <tr><td>B1</td><td>3 22</td></tr> <tr><td>B2</td><td>25</td></tr> <tr><td>B3</td><td>0</td></tr> <tr><td>B4</td><td>19 3</td></tr> <tr><td>B5</td><td>6 \oplus</td></tr> <tr><td>B6</td><td>16</td></tr> <tr><td>B7</td><td>35</td></tr> </table>	B0	4 45	B1	3 22	B2	25	B3	0	B4	19 3	B5	6 \oplus	B6	16	B7	35	- position
B0	4 45																	
B1	3 22																	
B2	25																	
B3	0																	
B4	19 3																	
B5	6 \oplus																	
B6	16																	
B7	35																	
		24 36 41 42 25 48 4 31 41																

Cache Memory with fully associative

Memory block request : LRU Policy H
4, 3, 25, 0; 19, 6, 25, 6, 16, 35, 45, 22, 8, 3, 16, H H

Memory selects 7 in cache block of \oplus (05)

Total hit = 04

Total Miss = 15

Total Memory References = 19

Hit ratio = $\frac{4}{19} = 4 \text{ (91\%)}$

Miss ratio = $\frac{15}{19} = 78.94\%$

6. What are the differences between SRAM & DRAM?

No.	SRAM	DRAM
1.	Made of flip-flops	Made up of capacitors (storage in the form of j. charges)
2.	No refresh required	Periodic refresh is required to keep the content
3.	Faster Read/write	Slower Read/write
4.	Expensive	Less expensive
5.	Used for cache memory implementation	Used for main memory implementation
6.	Low idle power consumption	High idle power consumption
7.	High operational power consumption	Low operational power consumption

CO₄

7. Discuss the Concept of Cache Memory with an example.

CO₃

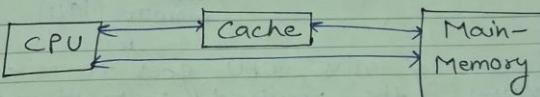
Cache Memory

A very high speed memory called a Cache, it is used to increase the speed of processing by making current programs and data available to the CPU.

- * It is placed between the CPU and the main-memory.
- * The Cache-memory access time is less than the access time of main memory.
- * The Cache is used for storing program segments currently being executed in the CPU and the data frequently used in the present calculations.

Based on locality of reference concept, current demanded localities are kept into a smaller & faster memory called as Cache

- * Use of cache reduces CPU's memory access time.



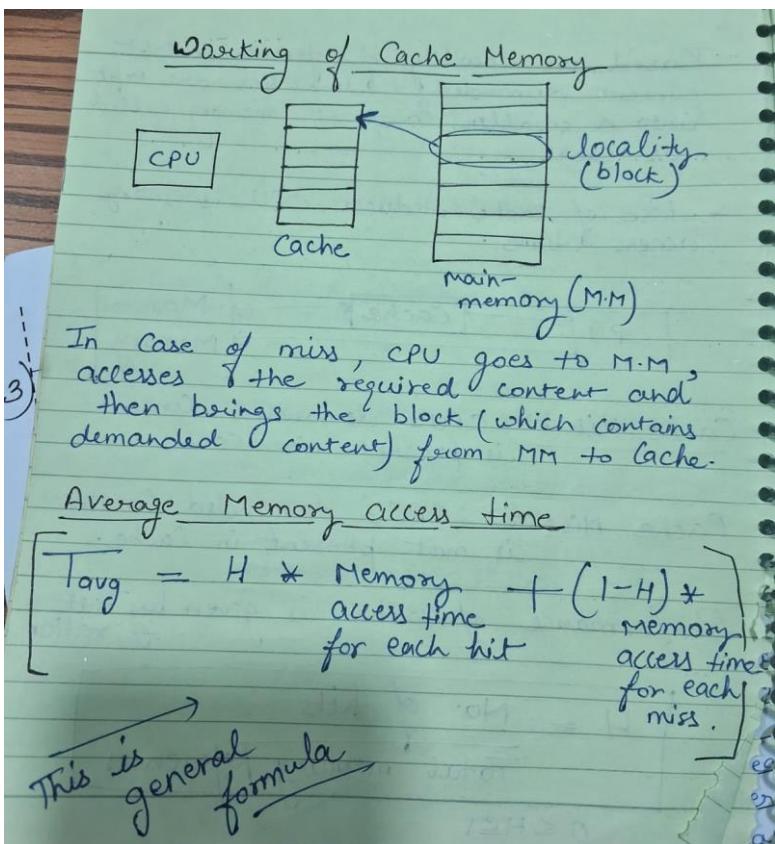
Cache Hit \Rightarrow CPU's demanded Content is present in Cache

Cache Miss \Rightarrow CPU's demanded Content is not present in Cache.

Performance of Cache is given by Hit ratio

$$H = \frac{\text{No. of hits}}{\text{Total memory References}}$$

$$0 \leq H \leq 1$$



Ex CPU referred memory 200 times

Hit = 160 times
Miss = 40 times

Each hit requires = 10 nsec
Each Miss requires = 100 nsec.

Sol'n No. 1
Total hit time = 160×10
= 1600

Total miss time = 40×100
= 4000

Total time = 5600 nsec.

avg. memory access time for 200 times
= 5600

avg. " " " 1 time = $\frac{5600}{200}$
= 28 nsec-

8.	<p>The logical address space in a computer system consisting 8 pages and 1024 words each, mapped into a physical memory of 32 frames. How many bits are there in the physical address and logical address respectively?</p> <p><u>Q</u> Consider a logical address space of 8 Pages and 1024 words each, mapped into a physical (address) memory of 32 frames. How many bits are there in the physical address and logical address respectively?</p> <p><u>Soln</u> Logical address space = 8×1024 Size = $2^3 \times 2^{10} \Rightarrow 2^{13}$</p> <p>there are 13 bits</p> <p>Physical address space size = 32 frames \times Size of 1 Page or 1 frame = 32×1024 = $2^5 \times 2^{10} = 2^{15}$</p> <p>there are 15 bits.</p>	CO_4
9.	<p>Consider a cache consisting of 256 block of 16 words each for a total of 4096 words and assume that the main memory is addressable by a 16 bit addresses and it consist of 4K blocks. How many bits are there in TAG,SET, WORD field for 2-way set associative technique ?</p>	CO_4 <i>AKTU 2020-21</i>

Date _____ / _____ / _____	Mapping	Page No.: _____
<p><u>Solution -</u></p>	<p>Cache Memory = $(4 \times 16 \text{ words}) = 64 \text{ words}$</p> <p>Main Memory = 2^{16} words</p> <p>Total Blocks = $2^{16} \text{ blocks} = 65,536 \text{ words}$</p> <p>size of each block = (16 words)</p> <p>Now:</p> <p>Total no. of sets = $\frac{\text{Total no. of blocks}}{\text{K-way set}} = \frac{2^2 \times 2^{14}}{2^2} = 2^{12}$</p> <p>Total no. of sets = $\frac{128}{2} = 2^7$</p> <p>Total no. of bits = 16</p> <p>Tag no. = $16 - (\text{Set no.} + \text{Block size})$</p> <p>Tag no. = $16 - (7 + 4) = 11$</p> <p>Tag no. = 05</p>	

10. A virtual memory has a page size of 1k words. There are 8 pages and 4 blocks. The associative memory page contains the following entries.

PAGE	BLOCK
0	3
2	1
5	2
7	0

Make a list of virtual addresses (in decimal) that will cause page fault if used by CPU.

CO₄

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Soln Since page size is $1K = 1024$ words

<u>Address Range</u>	<u>Page No.</u>
0 — 1023	(0)
1024 — 2047	(1)
2048 — 3071	(2)
3072 — 4095	(3)
4096 — 5119	(4)
5120 — 6143	(5)
6144 — 7167	(6)
7168 — 8191	(7)

then we can make steing from the given virtual addresses.

page fault occurs for the Page 2,3,5,7

11. A Digital computer has a memory unit of $64 K \times 16$ and a cache memory of $1K$ words. The Cache uses direct mapping with a block size of 4 words.

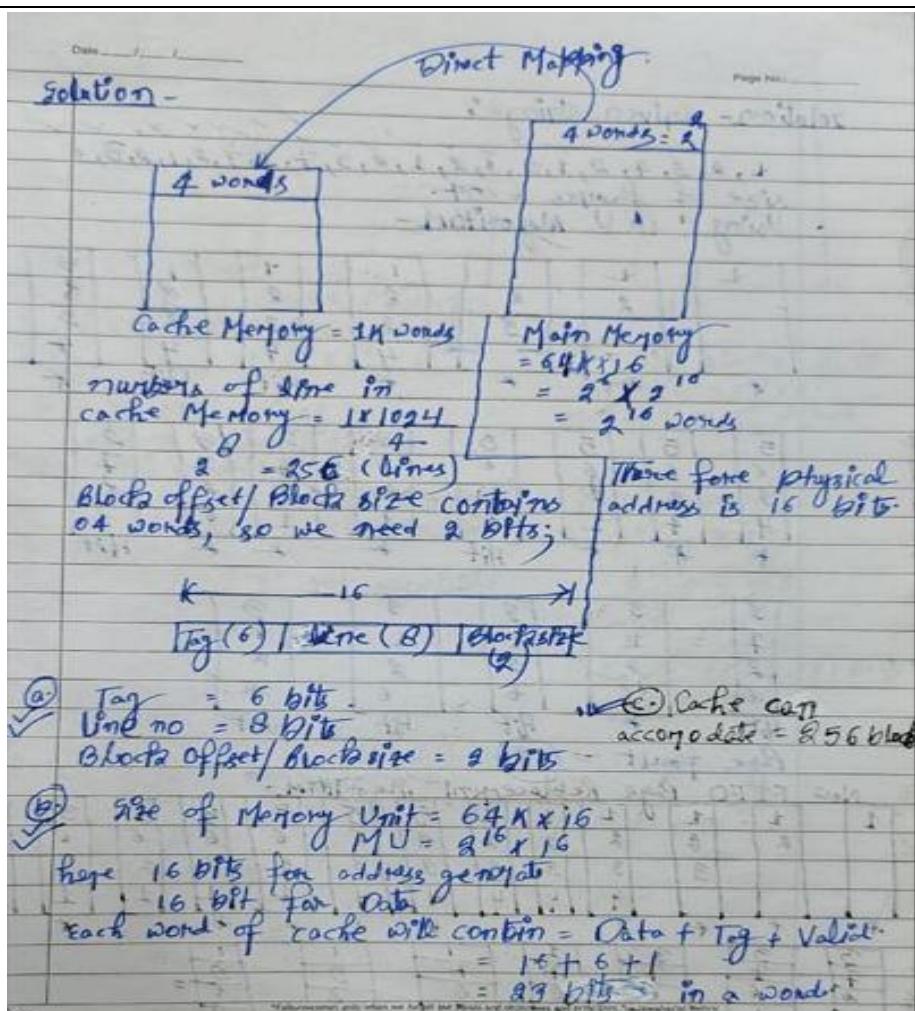
Calculate:

- How many bits are there in the tag, index, block and word fields of the address format.
-
- How many bits are there in each word of cache
- how many blocks can cache accommodate.

AKTU 2021-22

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12. Discuss RAM and 2.5D RAM with suitable diagram.

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Memory chip organization

The internal structure of Memory either RAM or ROM is made up of memory cells that contains a memory bit, a group of 8 bits makes a byte.

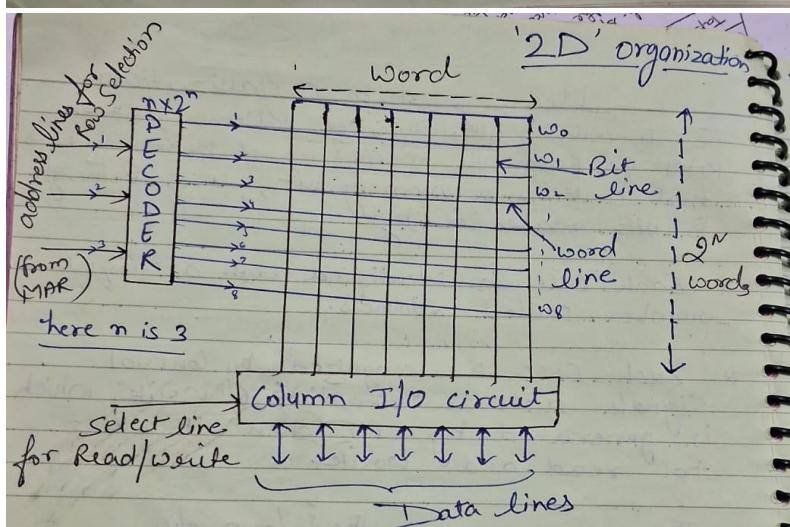
- * Each cell is identified with a unique number called address.
- * Each cell is recognized by control signals such as "read" & "write", which is generated by CPU when it wants to read and write.
- * The memory is in the form of a multi-dimensional array of rows and columns, in which each cell stores a bit and a complete row contains a word.

Memory can be represented as: $2^n = N$

n : No. of address lines

N : Total memory in bytes

it means there will be 2^n words.

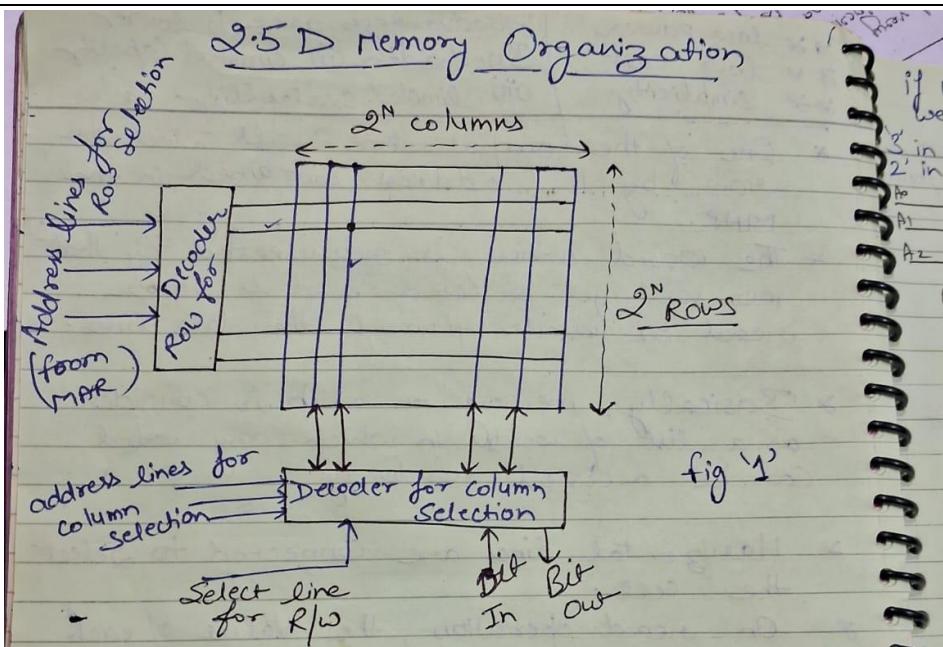


Here in the 2D organization memory is divided in the form of rows & columns that looks like a matrix.

Each row contains a word.

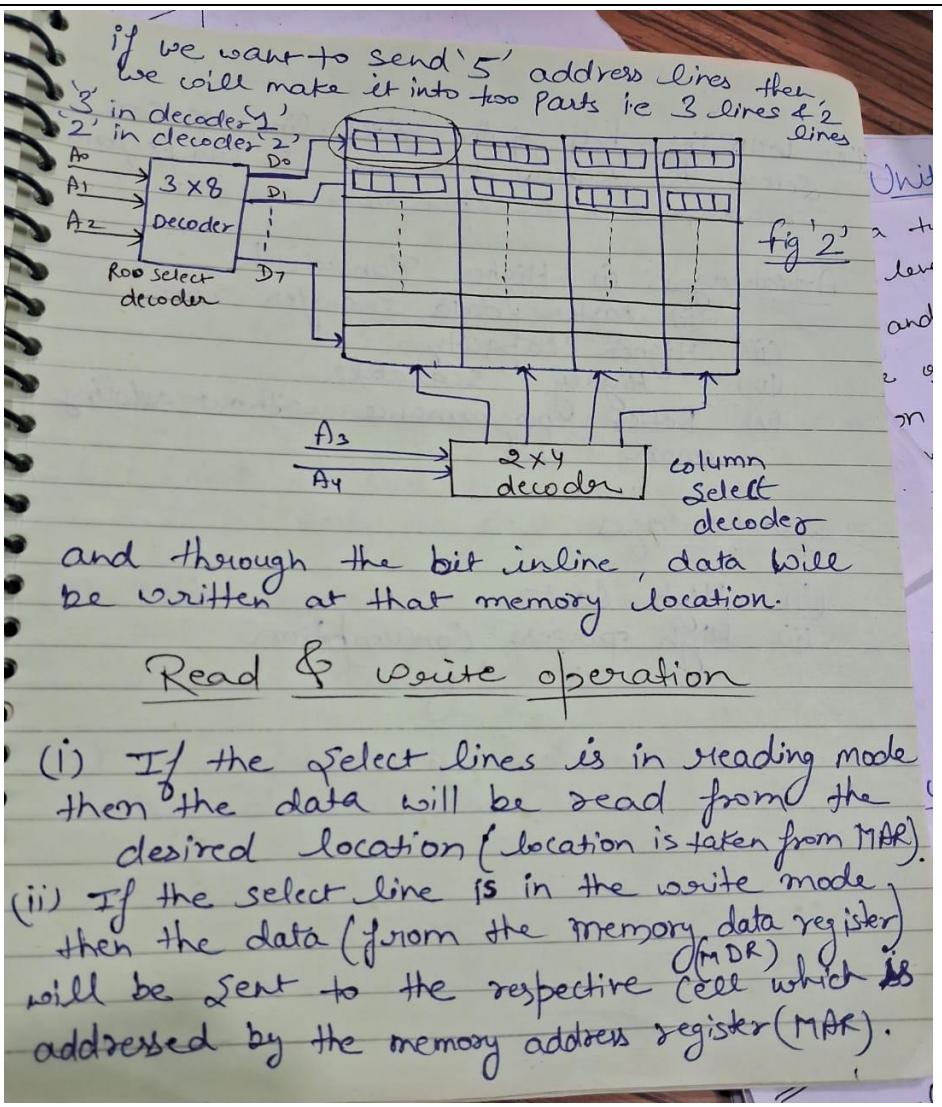
Here, one decoder is used that produces 2^N output lines if N is input lines. (Here N is 3 it means output lines will be 8)

<ul style="list-style-type: none"> <input checked="" type="checkbox"/> low Power <input checked="" type="checkbox"/> low cost <input checked="" type="checkbox"/> Simplicity 	<p style="text-align: right;">Disadvantages are:</p> <ul style="list-style-type: none"> (i) lower Bandwidth (ii) limited capacity (iii) limited scalability
<ul style="list-style-type: none"> * One of the output line will select the row by the address contained in the MAR. * The word which is represented by that row will get selected and is either read or write through the data lines. * Basically, memory on chip is considered as a list of words in which any word can be accessed randomly. * Horizontal lines are connected to select the cell. * On read operation, the value of each bit is passed through data lines. * On write operation, the decoder selects the desired word or locations to place the data into the memory. <p style="text-align: center;">This is how the word is selected of a particular row for performing read/write operations.</p>	



In this 2.5D organization the scenario is same but we have two different decoders. One is a column decoder and another is a row decoder.

- * The address from 'MAR' goes as the decoder's input and then decoder will select the respective cell through the bit-out line, the data from the location will be read.



(iii) With the help of the select line, we can select the desired data and we can perform read and write operations on it.

Advantages: (i) Higher Bandwidth
(ii) faster data transfer rate
(iii) Higher capacity
(iv) Highly scalable
(v) Better performance without adding more chips

Disadvantages

- (i) High Cost
- (ii) High power consumption

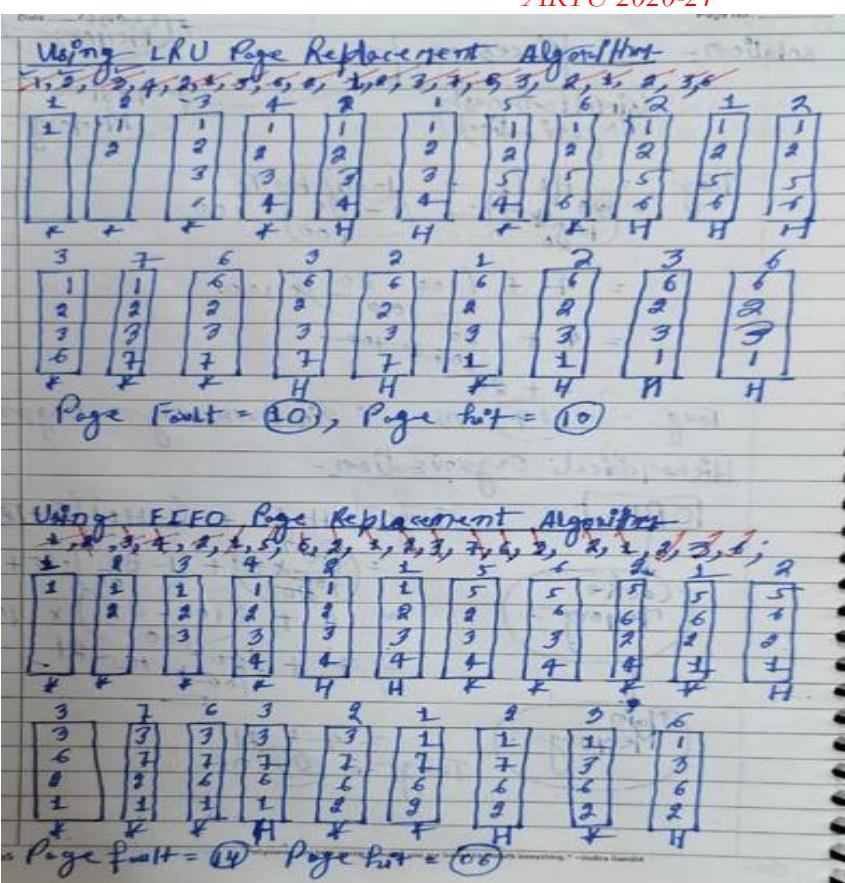
Comparison B/w 2D & 2.5D

- (i) In 2D hardware is fixed but in 2.5D hardware changes.
- (ii) 2D organization requires more gates while 2.5D requires less gates
- (iii) 2D is more complex (hard) to implement
- (iv) hard to find error in 2D whereas it is easy to find errors in 2.5D
- (v) This organization is commonly used in ROM circuits / chips whereas 2.5D uses in making RAM chips
- (vi) One decoder is used in 2D but in 2.5D two decoders are used.

13. Calculate the page fault for a given string with the help of LRU & FIFO page replacement algorithm , Size of frames =4 and string 1,2,3,4,2,1,5,6,2,1,2,3,7,6,3,2,1,2,3,6

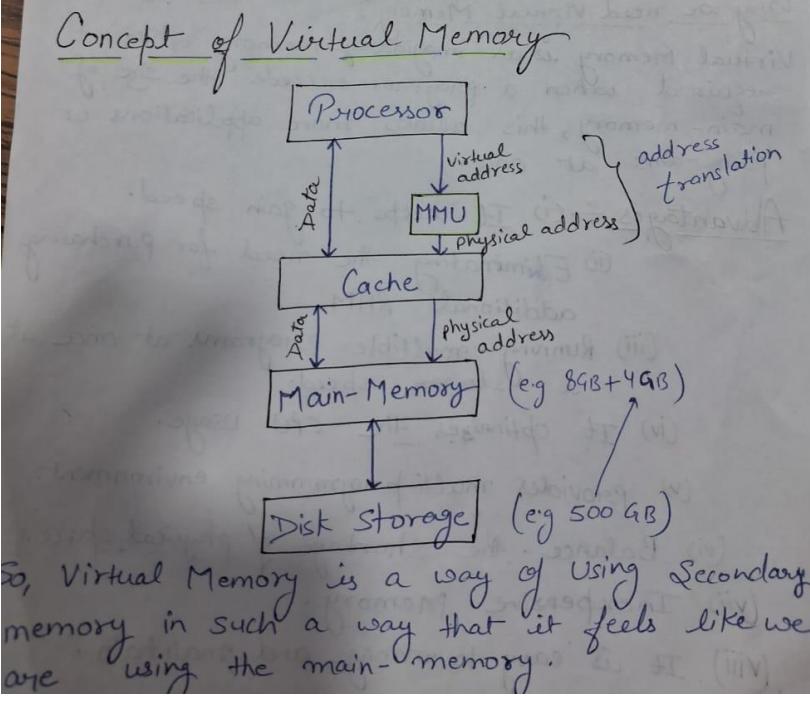
AKTU 2020-21

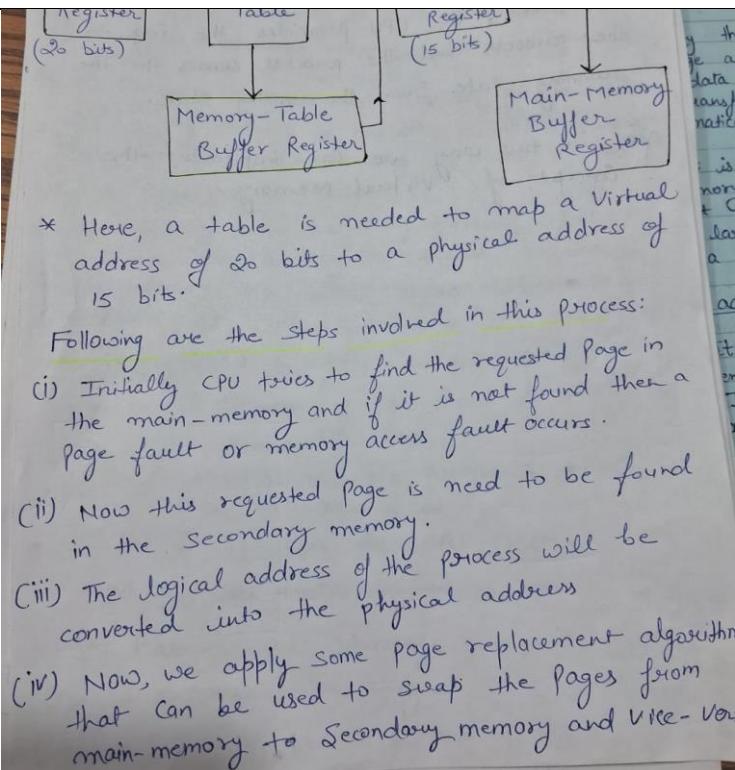
CO₄



14. (v) It doesn't offer the same performance as RAM.

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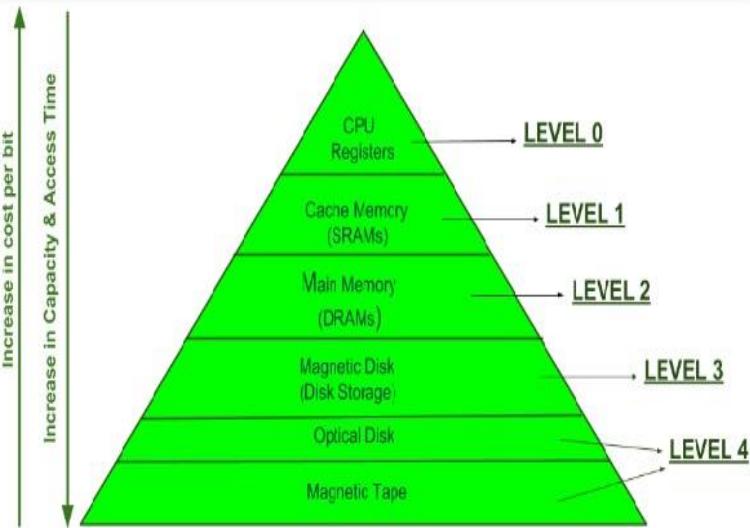
15.

Discuss the memory hierarchy in computer system in the context of speed, size and cost. *AKTU 2020-21*

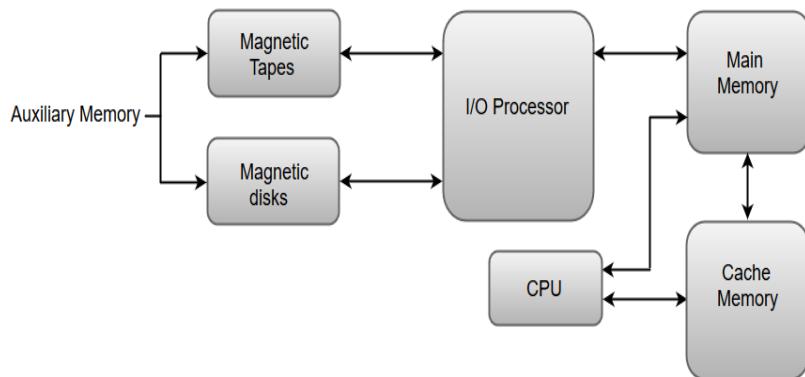
Memory Hierarchy : The Computer memory hierarchy looks like a pyramid structure which is used to describe the differences among memory types. It separates the computer storage based on hierarchy.

Memory hierarchy is arranging different kinds of storage present on a computing device based on speed of access. At the very top, the highest performing storage is CPU registers which are the fastest to read and write to. Next is cache memory followed by conventional DRAM memory, followed by disk storage with different levels of performance including SSD, optical and magnetic disk drives.

CO₄K₁



Memory Hierarchy in a Computer System:



Single memory unit can not accommodate all the programs and data. The memory unit that directly communicates with the CPU is called main memory e.g. RAM & ROM.

Devices that provide backup storage are called auxiliary memory e.g. magnetic disks & tapes.

A special and very high speed memory called a cache is used to provide program and data available to CPU at rapid rate

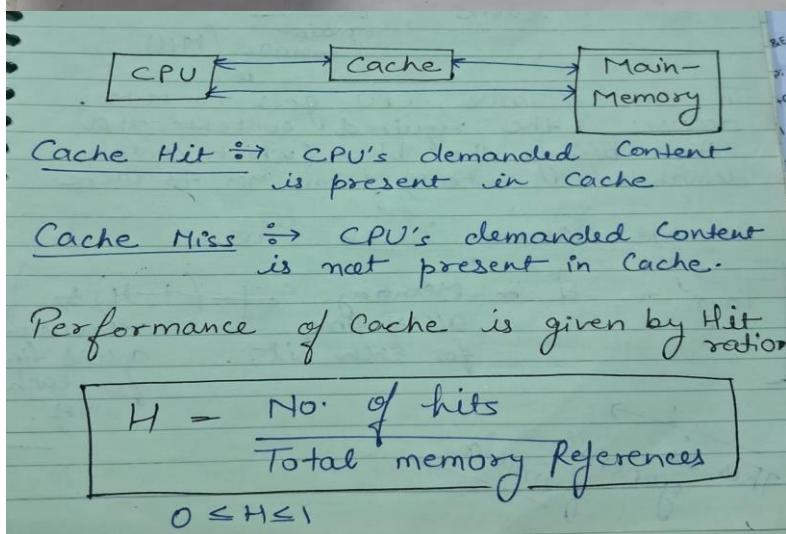
Memory hierarchy consists of all storage devices from smaller and faster cache memory to high capacity and slow auxiliary memory.

16. Discuss the following:
 a) RAM Vs ROM
 b) HIT Ratio and MISS Ratio
 c) FIFO Vs LRU

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- | | |
|--|--|
| i) Random Access memory | i) Read only Memory |
| ii) Read/write can be performed. | ii) Only read performed. |
| (iii) volatile | (iii) Non-Volatile |
| (iv) Faster | (iv) Slower |
| (v) Expensive | (v) less expensive |
| (vi) Storage data requires to be refreshed in RAM. | (vi) Storage data does not need to be refreshed in ROM |
| (vii) Large in size | (vii) smaller in size |
| (viii) SRAM, DRAM | (viii) EPROM, PROM, EEPROM, MROM. |



FIFO	LRU
i) It Replaces the least recently used page.	(i) It Replace the oldest page.
ii) May ^{not always} provide optimal performance.	(ii) Better Performance
iii) Simple to implement	(iii) More Complex
iv) Requires additional Data-structure for tracking page usage order.	(iv) No additional data structure required.

17. Discuss the different mapping techniques used in cache memories and their relative merits and demerits.

CO₄

- When the CPU needs to access memory, the cache is examined. If the word is found in the cache, it is read from the fast memory, i.e. Cache Memory. If the word addressed by the CPU is not found in the cache, the Main memory is accessed to read the word.
- When the CPU refers to memory and finds the word in cache, it is said to produce a hit.
- When the CPU refers to memory and not finds the word in cache, it is said to produce a miss.
- The average memory access time of a computer system can be improved by use of a cache if the hit ratio is high so that most of the CPU access failures comes only when we forget our ideals and objectives and principles." Jawaharlal Nehru

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the cache memory instead of main memory so that the average access time is closer to the access time of cache memory.

Characteristics of Cache Memory -

- (1) Fast access time.
- (2) Very little storage space.
- (3) Not much time must be wasted when searching for words in the cache.
- (4) Transformation of data from main memory to cache memory is referred to as a mapping from process.

Organization of memory, three types of mapping processes;

- (1) Direct Mapping.
- (2) Associative mapping.
- (3) Set-Associative mapping.

(1) Direct Mapping -

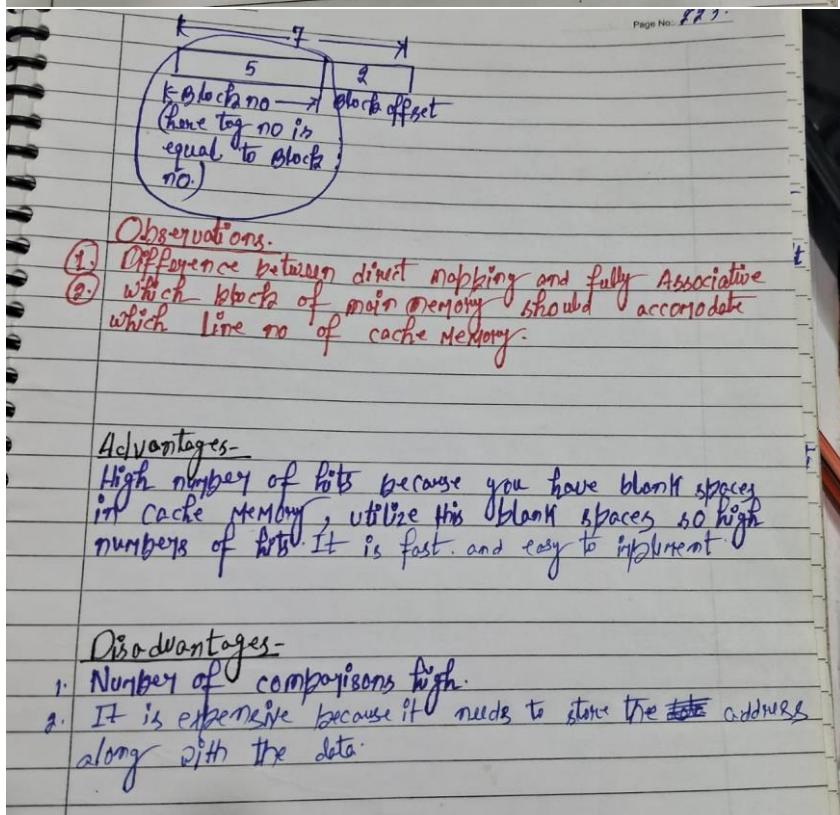
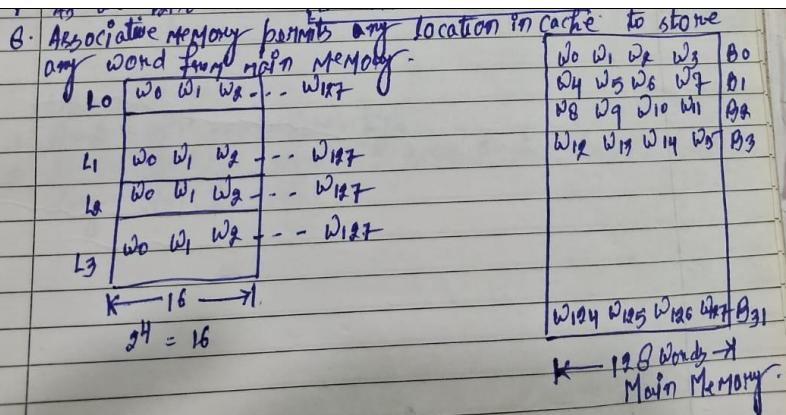
K — 16 Words —>				16S Words			
L ₀	B ₀ B ₄ B ₈ B ₁₂	W ₀ W ₁ W ₂ W ₃	B ₀	W ₄ W ₅ W ₆ W ₇	B ₁	W ₈ W ₉ W ₁₀ W ₁₁	B ₂
L ₁	B ₁ B ₅ B ₉ B ₁₃	W ₁₂ W ₁₃ W ₁₄ W ₁₅	B ₃	W ₁₆ W ₁₇ W ₁₈ W ₁₉	B ₄	RAM	
L ₂	B ₂ B ₆ B ₁₀ B ₁₄						
L ₃	B ₃ B ₇ B ₁₁ B ₁₅						

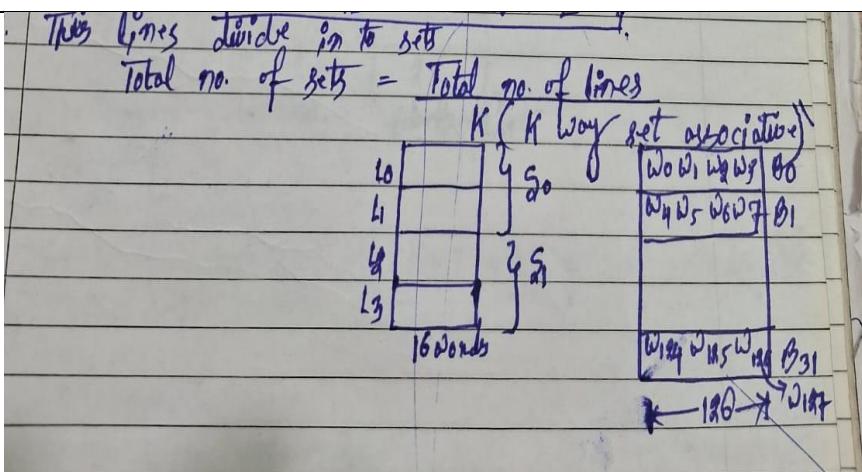
$\lceil K \text{ Mod } n \rceil$
 where
 $K = \text{no. of blocks}$
 $n = \text{no. of lines}$.
 Main Memory generate physical address.
 $\lceil \text{No of blocks offset} / \text{Block size} \rceil$
 $K - PA \rightarrow$
 $\lceil \text{PA} = 32 \quad 1 \text{ } 0 \text{ } 2 \text{ } 4 \quad 1 \rceil$
 $K \quad 7 \quad \rightarrow *$
 Block size | Block offset - How many no. of words in
 every block.

Date K — PA = 7 — Page No.: 181
 $\lceil 3 \ 1 \ 2 \quad | \ 8 \rceil$
 tag no. line no. block offset
 No of blocks divide into tag no and line no
 in case of direct mapping.

$K \text{ Mod } n$
 $0 \text{ Mod } 4 = 0$ (Block 0 always occupy in Line 0)
 $1 \text{ Mod } 4 = 1$ (Block 1 always occupy in Line 1)
 $2 \text{ Mod } 4 = 2$ (Block 2 always occupy in Line 2)
 $3 \text{ Mod } 4 = 3$ (Block 3 always occupy in Line 3)
 $4 \text{ Mod } 4 = 0$ (Block 4 always occupy in Line 0)

Tag field - In multiple blocks which blocks at present till tag field.





- Date _____ / _____ / _____ Page No.: 229
8. To find total no. of sets = $\frac{\text{total no. of lines}}{K}$ = $\frac{16}{4} = (04)$
9. Now which blocks should accommodate which line
 K Mod 7
 0 Mod 2 = 0 (set 0 but in which line, so accept)
 1 Mod 2 = 1 in any line (fully associative)
 2 Mod 2 = 0
 3 Mod 2 = 1
 ; ; ;
10. After selection sets now blocks will accommodate which line no; this selection with the help of fully associative mapping.
- ← 7 →
 [5 | 2]
 Block no Block offset
- ← 7 →
 [4 | 1 | 2]
 Tag Set no Block offset
- Advantages -
- (1) Better performance.
 - (2) It is the combination of direct mapping and set associative.
 - (3) Highest hit ratio.
 - (4) Disadvantage -
- It is more expensive.

Date _____ / _____ / _____

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Q- A computer has a 956 M by 16, 4-way set associative write back data cache with block size of 32 bytes. The processor send 32-bit address to the cache controller. Each cache tag directory entry contains in addition to address tag 2 valid bit, 1 Modified bit, and 1 replacement bit.

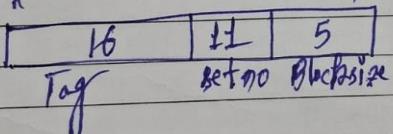
The number of bits in the tag field of an address is ; (1) 11 (2) 14 (3) 16 (4) 27.

No of blocks = $\frac{100 \times 64 \times 8}{32 \times 8} = 8K = 2^3 \times 2^{10} \Rightarrow 2^{13}$

\rightarrow no. of blocks = 2^{13} .

No. of sets = total no of line
 $= \frac{2^{13}}{2^2} \Rightarrow 2^{11}$

no of sets = 2^{11}

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 $[16 + 11 + 5 = 32]$

18. A computer uses RAM chips of $1024 * 1$ capacity.
- (a.) How many chips are needed & how should their address line be connected to provide a memory capacity of $1024 * 8$?
- (b.) How many chips are needed to provide a memory capacity of 16 KB ?
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Solution-

(a) Available RAM chips capacity = 1024×1
 Capacity of required chips = 1024×8

$$\text{Number of chips required} = \frac{\text{Capacity of required RAM}}{\text{Available chips}}$$

$$= \frac{1024 \times 8}{1024 \times 1}$$

Number of chips = 8

→ Now required address line of memory = 1024×8

$\xrightarrow{\text{Address line}} 2^{\text{No. of bits}}$

So required address line = 10

(b) Available chip capacity = 1024×1
 Required Memory capacity = 16 KB

$$\text{Number of chips required} = \frac{\text{Required Memory size}}{\text{Available chip size}}$$

$$= \frac{16 \times 1024 \times 1024}{1024 \times 1}$$

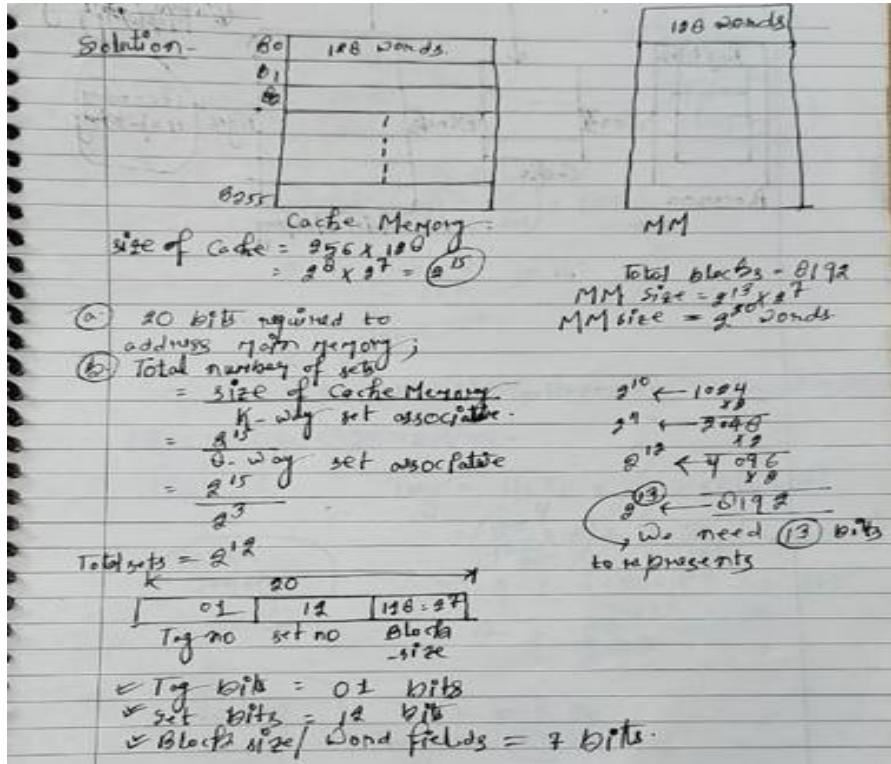
Number of chips = 198

19. An eight way set associative cache consists of a total of 256 blocks. The main memory contain 8192 blocks ,each consisting of 128 words.
 (a.) How many bits are there in the main memory address?
 (b)How many bits are there in TAG, SET and WORD fields ?

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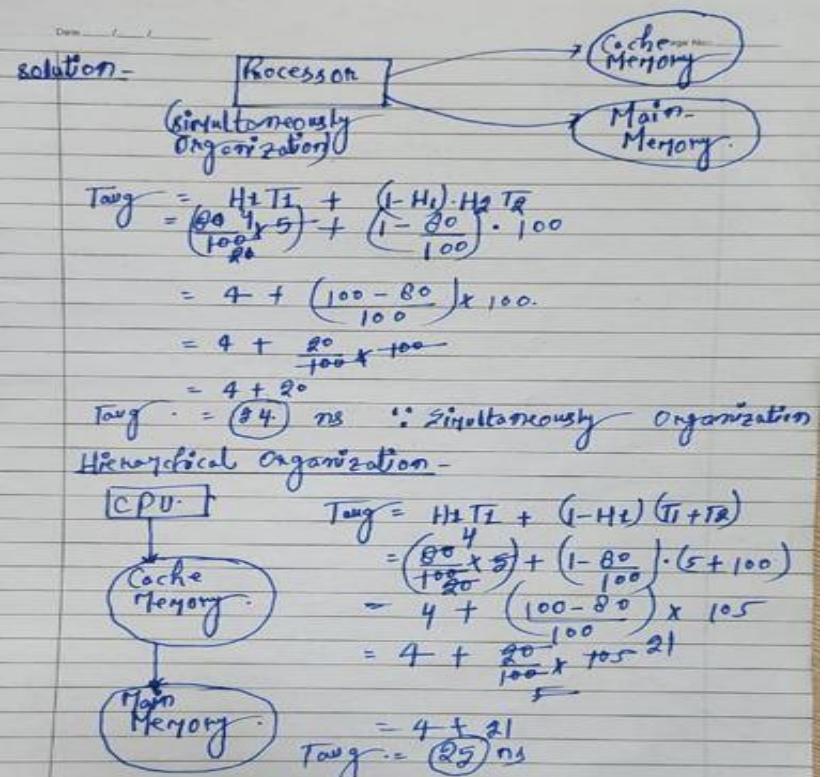
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20. What is the average memory access time for a machine with a cache hit rate of 80 % and cache access time of 5 ns and main memory access time of 100 ns when
(a.) Simultaneously access memory organizations is used
(b.) Hierachical memory organizations is used.

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Ques 3: A certain magnetic disk has the following specification:

- (a) No. of recording = 10
- (b) No. of tracks/surface = 256
- (c) No. of sectors/track = 32
- (d) No. of bytes/sector = 128

Given Disk rotation speed = 2400 rpm

Calculate the following:-

- (i) Disk capacity
- (ii) Transfer rate
- (iii) Latency time

Sol: (i) Disk capacity = No. of surfaces \times No. of tracks in each surface \times No. of sectors in a track \times No. of bytes in a sector

$$= 10 \times 256 \times 32 \times 128$$

$$= 10 \times 2^8 \times 2^5 \times 2^7$$

$$= 10 \times 2^{20}$$

$$= 10 \text{ MB.}$$

(ii) Capacity of one track = No. of sectors in a track \times No. of bytes in a sector.

$$= 32 \times 128 = 2^5 \times 2^7 = 2^{12} \text{ bytes.}$$

Disk rotation speed = 2400 rpm

\therefore 2400 rpm rotation in 1 min i.e. 60 sec

$$\Rightarrow 1 \text{ rotation in } \frac{60}{2400} \text{ i.e. } \frac{1}{40} \text{ sec.}$$

In $\frac{1}{40}$ sec, data transfer = $2^{12} \times 40$ bytes.

$$\therefore \text{In 1 sec, data transfer} = 40 \times 2^{12} \text{ bytes.}$$

$$= 160 \text{ KB bytes.}$$

\therefore Transfer rate = 160 KB/sec.

(iii) Latency time = $\frac{1}{2}$ (Time required in one rotation)

$$= \frac{1}{2} \times \frac{1}{40} = \frac{1}{80} \text{ seconds.}$$

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Ques: Consider a disk pack with 16 surfaces, 128 tracks per surface and 256 sectors per track, 512 bytes of data are stored in a bit serial manner in a sector. What is capacity of the disk pack and no. of bits required to specify a particular sector in the disk.

$$\text{Sol: Disk Capacity} = 16 \times 128 \times 256 \times 512 \\ = 2^4 \times 2^7 \times 2^8 \times 2^9 = 2^{28}$$

$$= 256 \text{ MB.}$$

No. of bits required to specify a particular

$$\text{sector in the disk} = 256 \times 16 \times 128 \\ = 2^8 \times 2^7 \times 2^9 = 2^{24} \text{ bits}$$

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M	T	W	T	F	S	S
1	2	3				
4	5	6	7	8	9	10
11	12	13	14	15	16	17
18	19	20	21	22	23	24
25	26	27	28	29	30	31

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Example:

Find the average time to read or write a 512B sector for a disk rotating at 15,000 RPM with average seek time of 4 ms, a 100MB/sec transfer rate, and a 0.2 ms controller overhead

Solution:

$$\text{Access Time} = \text{avg seek time} + \text{avg rot delay} + \text{transfer time} + \text{controller overhead}$$

$$\text{Avg disk read/write} = 4.0 \text{ ms} + 0.5 / (15,000 \text{ RPM} / (60 * 1000)) + 0.5 \text{ MB} / (100 \text{ MB} / 1 * 1000 \text{ ms}) + 0.2 \text{ ms}$$

$$= 4.0 + 2.0 + 5 + 0.2 \\ = 11.2 \text{ ms}$$

If the measured average seek time is 25% of the advertised average seek time, then

$$\text{Avg disk read/write} = 1.0 + 2.0 + 5 + 0.2 = 8.2 \text{ ms}$$

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- Access Time = avg seek time + avg rot delay + transfer time + controller overhead

Example:

- Transfer size is 8K bytes
- Advertised average seek is 12 ms
- Disk spins at 7200 RPM
- Transfer rate is 4 MB/sec

Solution:

$$\begin{aligned}\text{Access Time} &= \text{avg seek time} + \text{avg rot delay} + \text{transfer time} + \text{controller overhead} \\ &= 12 \text{ ms} + 0.5/(7200 \text{ RPM}/60*1000 \text{ ms}) + 8 \text{ KB}/4 \text{ MB/s} + .2 \text{ ms} \\ &= 12 + 4.15 + 2 + .2 \\ &= 18.35 \text{ ms}\end{aligned}$$

- measured average seek time is 1/4 to 1/3 of the advertised average seek time, then

$$\begin{aligned}\text{Avg disk read/write} &= 4.0 + 4.15 + 2 + .2 \\ &= 10.35 \text{ ms}\end{aligned}$$