CS220: Computer Organization
Quiz#1 Solution

Name:
Roll No.:

1. A purely combinational logic module takes two inputs A and B, each of which is three-bit wide. The module computes four outputs. The first output is $a = A + B$. The second output is $m = A \times B$. The third output is the quotient q when A is divided by B. The fourth output is the remainder r when A is divided by B. Assume that when B is zero, both q and r are equal to A. If this module is implemented using a read-only memory (ROM), calculate the number of rows and the width of the ROM. **(1+4 points)**

Solution: There are 64 possible input combinations (eight for A and eight for B). So, the number of rows is 64. To compute the output width, note that a is four-bit wide (maximum attainable value is 14), m is six-bit wide (maximum attainable value is 49), q is three-bit wide (maximum attainable value is 7), and r is three-bit wide (maximum attainable value is six). To be able to store a, m, q, r, the ROM width needs to be 16 bits.

2. An SRAM module with 4M rows and eight-bit width is implemented using four ranks of 1K$\times$1024-bit SRAM chips. To get eight-bit output, the chips in one of the ranks are selected. Calculate the number of address bits used to generate the row address, column address, and chip select. **(1+1+1 points)**

Solution: Number of chips in a rank = (4M$\times$8)/(4$\times$1K$\times$1024) = 8. So, each chip in a rank contributes one bit column output. The number of row address bits is $\log_2(1K)$ or 10. The number of column address bits is $\log_2(1024)$ or 10. The number of chip select bits is same as the number of rank select bits (since all chips in a rank must be selected), which is $\log_2(4)$ or 2.

3. Consider a combinational logic function f that takes input x and produces output y. A positive edge-triggered flip-flop provides the input x and another positive edge-triggered flip-flop stores the output y. The hold time and the setup time of the flip-flops are 150 picoseconds and 200 picoseconds, respectively. The propagation delay through each flip-flop is 100 picoseconds. Assume the clock skew to be zero. A 1 GHz clock is applied to this design. Calculate the maximum and minimum allowable times (in picoseconds) to compute f so that the design works correctly. **(1+1 points)**

Solution: Propagation delay + max latency of f + setup time must be at most the clock cycle time which is 1000 picoseconds. So, max latency of f is 700 picoseconds. Propagation delay + min latency of f is at least the hold time. So, min latency of f is 50 picoseconds.