

राष्ट्रीय इलेक्ट्रॉनिकी एवं सूचना प्रौद्योगिकी संस्थान (रा.इ.सू.प्रौ.सं)

NATIONAL INSTITUTE OF ELECTRONICS AND INFORMATION TECHNOLOGY (NIELIT)

इलेक्ट्रॉनिकी और सूचना प्रौद्योगिकी मंत्रालय, भारत सरकार

Ministry of Electronics & Information Technology (MeitY), Govt. of India



Certificate No.: NIELIT/NOI/OL/B67/25273

प्रमाणपत्र
CERTIFICATE

नाम Name : ABHISHEK GUPTA
माता का नाम Mother's Name : SUMAN GUPTA
पिता का नाम Father's Name : ANIL KUMAR SHAW
रजिस्ट्रेशन संख्या Registration No. : NIELIT/NOI/OL/B67/25273

This is to certify that the above mentioned candidate has successfully completed program
Industrial Training Program on VLSI Design flow (RTL to GDS-II)
of 06 Weeks / 90 hour(s) duration from 15.07.2025 to 25.08.2025
conducted by National Institute of Electronics and Information Technology (NIELIT),
CoE Noida in Online mode with S grade.

Curriculum of the Course

Overview of VLSI Design Flow , Hardware Modeling, Introduction to Verilog using Icarus Verilog, RTL Synthesis
with YOSYS tool, Static Timing Analysis using Open STA, Basic Concepts for Physical Design, Floor planning,
Clock Tree Synthesis, Routing , Layout Design using Magic Tool.

श्रेणियों का आख्यान GRADE LEGENDS	80% and above एस S	70% to <80% ए A	60% to <70% बी B	50% to <60% सी C
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Program Coordinator
Issued Date: 26.08.2025

Director

Issued by
National Institute of Electronics & Information Technology, CoE Noida
PS-1D, Behind Brahmampurtra Shopping Complex, Sector 29, Noida, UP - 201303

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