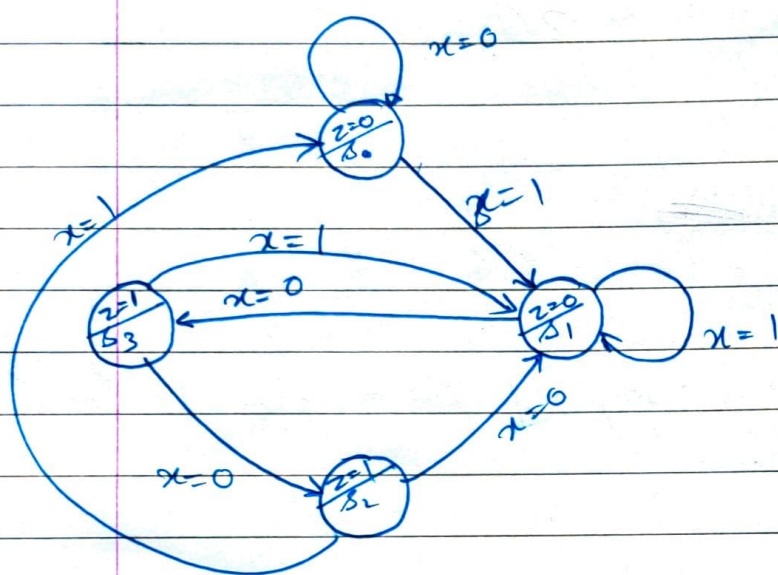
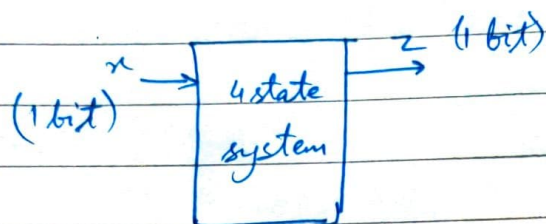


## ★ Finite State Machine (Pg 302)

- FSM: \*A machine/system that goes through a finite/fixed no. of states.
  - \* It has a fixed no. of i/p o/p combinations
- Typical uses → control, monitor, calculate
- FSM is a way of designing circuits.
- Sequential circuits :
  - system
    - Counters
    - Traffic Lights
    - digital lock

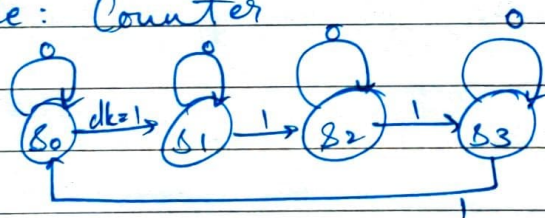
\* Example:



\* Next state  $\propto f(\text{input}, \text{current state})$

	A	B	state variables
S <sub>0</sub>	0	0	
S <sub>1</sub>	0	1	
S <sub>2</sub>	1	0	
S <sub>3</sub>	1	1	

\* Example: Counter



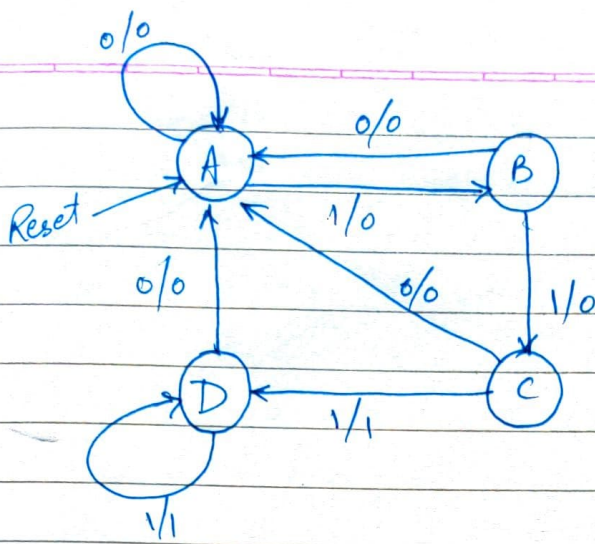
\* Next step  $\propto f(\text{input}, \text{current state})$

\* FSM is just a way at looking at the design.

\* FSM State Diagram  
\* Eg: 3 state FSM: S<sub>a</sub>, S<sub>b</sub>, S<sub>c</sub>

\* Eg: Design a FSM to detect 3 or more 1's in a serial bit stream. The bits are applied serially in synchronism with a clock. The  $z_p$  will become '1' whenever it detects 3 or more consecutive 1's in the stream.

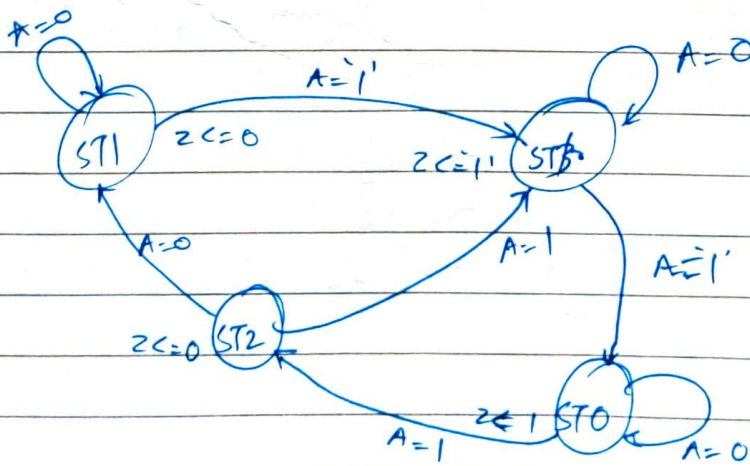




Reset	PS	i/p	NS	o/p
1	-	-	A	0
0	A	0	A	0
0	A	1	B	0
0	B	0	A	0
0	B	1	C	0
0	C	0	A	0
0	C	1	D	1
0	D	0	A	0
0	D	1	D	1

★ Moore FSM (Pg 308)

\* o/p  $\propto$  { (present state only)



library  
use

```
entity MOORE_FSM is  
  port (A, clock: in bit;  
        z: out std_logic);  
end MOORE_FSM;
```

architecture FSM\_Example of MOORE\_FSM is  
 type state\_type is (ST0, ST1, ST2, ST3);  
 signal Moore\_state: state\_type;  
begin

process (clock)

begin

if clock = '0' then -- falling edge

case Moore\_state is

when ST0 =>

z <= '1';

if A = '1' then

Moore\_state <= ST2;

end if;

when ST1 =>

z <= '0';

if A = '1' then

Moore\_state <= ST3;

end if;

when ST2 =>

z <= '0';

if A = '0' then

Moore\_state <= ST1;

else

Moore\_state <= ST3;

end if;



```

when ST3 =>
    z <= '1';
    if A = '1' then
        Moore state <= ST0;
    end if;
end case;
end process;
end FSM_Example;

```

★ Mealy FSM (Pg 310)

\* o/p < f(i/p, present state)

	0	1	← Input A
ST0	ST0 / 0	ST3 / 1	
ST1	ST1 / 1	ST0 / 0	
ST2	ST2 / 0	ST1 / 1	
ST3	ST2 / 0	ST1 / 0	

↑  
present state

next state / o/p

Q Draw the state transition diagram for above.

\* HDL Code :

```

library
use

```

entity Mealy-FSM is

port(a, clock: in bit;

z: out std-logic);

end Mealy-FSM;

architecture FSM-en of Mealy-FSM is  
type Mealy\_Type is (ST0, ST1, ST2, ST3);  
signal P\_state, N\_state: Mealy\_Type;  
begin

SEQ\_Part: process (clock)

begin

if clock = '0' then -- falling edge

P\_state <= N\_state;

end if;

end process SEQ\_Part;

COMB\_Part: Process (P\_state, A)

begin

case P\_state is

when ST0 =>

if A = '1' then

Z <= '1';

N\_state <= ST3;

else

Z <= '0';

end if;

when ST1 =>

if A = '1' then

Z <= '0';

N\_state <= ST0;

else

Z <= '1';

end if;

when ST2 =>

if A = '0' then

Z <= '0';

else

Z <= '1'; N\_state <= ST1;

end if;



when ST3 =>  
 if A = '0' then  
 $z \leftarrow '0'$ ;  
 $N\_state \leq ST2$ ;  
 else  
 $N\_state \leq ST1$ ;  
 end if;  
 end case;  
 end process COMB Part;  
 end FSM\_ex;

### ★ Coding Styles for ~~VHDL~~ FSM

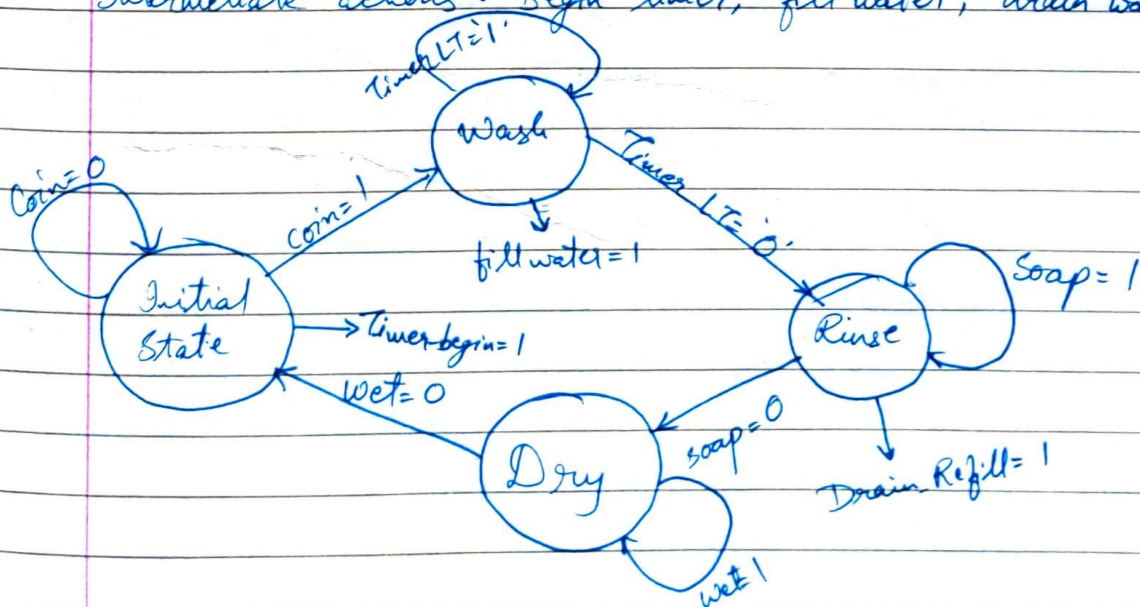
- 1) Single process → Normal VHDL code
- 2) Double process → Separate processes for sequential & combinational logic.
- 3) Triple process → 1 Sequential & 2 combinational processes.

### ★ Example: Washing Machine

States: Wash, Rinse, Dry

I/p: Coin

Intermediate actions: Begin timer, fill water, drain water,



## Washer - Dryer

I/p: coin if

Soap present

Timer of 30min

Wetness Indicator

O/p: Begin timer

fill water

Drain then refill

Drain completely

Q] Write VHDL code for the above system.

★ Example: Turnstile

CS	I/P	NS	O/P
Locked	Coin	Unlocked	Unlocks the turnstile
locked	Push	Locked	Nothing, You are locked
Unlocked	Coin	Unlocked	Nothing, You have wasted a coin
Unlocked	Push	Locked	When you have pushed through, locks the turnstile.