Verilog

Lecture 1: Introduction to Hardware Modeling using Verilog

Reference: NPTEL lecture by Prof. Indranil Sengupta from IIT Kharagpur.

* Verilog is a language with which one can specify the behaviour / functionality / structure of a given hardware circuit.

* VLSI Design Flow
  - Specification
  - Synthesis
  - Simulation
  - Layout
  - Testability analysis
  - ⋮

* Computer Aided Design (CAD) Tools
  - based on HDL
  - HDL provides formats for representing the o/ps of various design steps
  - A CAD tool will generate a more detailed information about the circuit
    - behavioural level to register transfer level
    - register transfer level to gate level
    - gate level to transistor level
    - transistor level to the layout level

* HDL ⟶ 1) VHDL
  2) Verilog
  3) System C
  4) System Verilog
  ⋮

* Simplistic View of Design Flow

Design Idea
↓
Behavioral Design
↓
Data Path Design
↓
Logic Design
↓
Physical Design
↓
Manufacturing
↓
Chip / Board

☆ History of Verilog

- Verilog originated in 1983 at Gateway Design Automation
- 1995: Original IEEE verilog standard was approved
- 2001: IEEE 1364-2001 → latest Verilog standard.