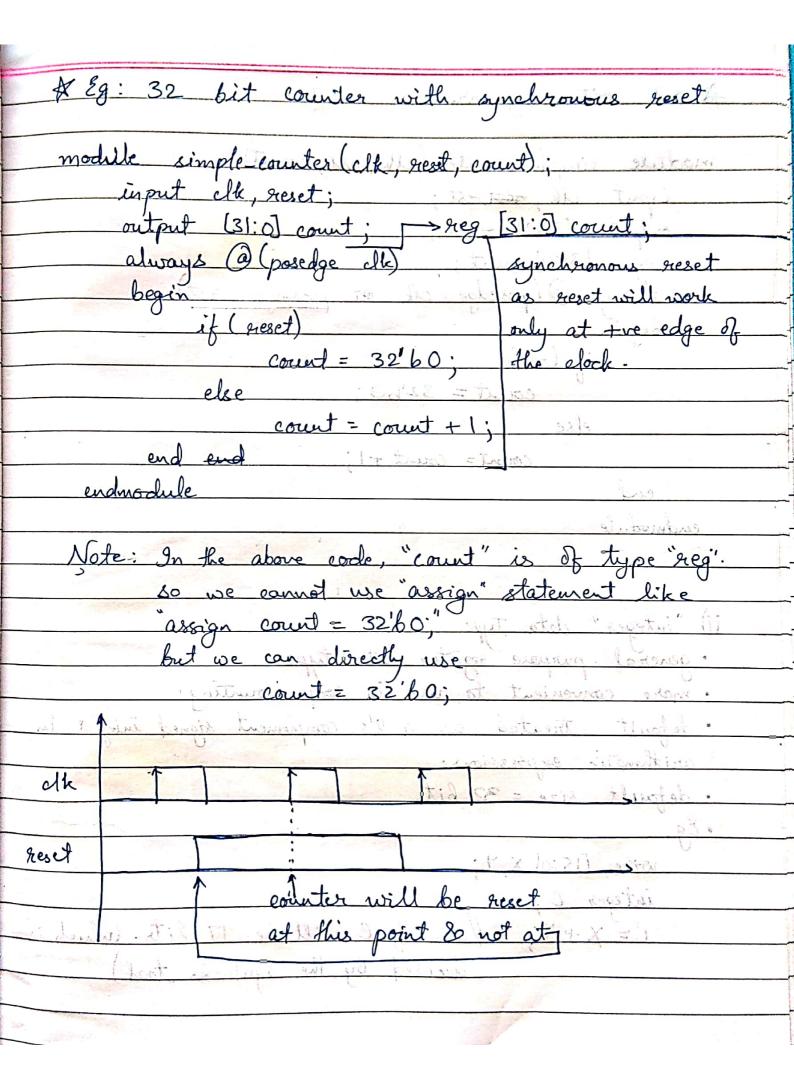
Lecture-3
* Recap: . module
· assign statement
NET type variables
RECISTER type variables
the Carlotte of the Carlotte o
id as a first to the second se
** Register Data Type
· Register is a variable that can hold a value
· Register cannot be used with "assign" statement as
LMS of assign statement should be of type "NET".
· Register statement not necessarily maps to a
hardware register during synthesis.
* Types of Register data types in Verilog:
i) reg
ii) integer
iii) real
iv) time (not used in synthesis, only used for simulation)
i) reg data type
· default value of a reg type is 'X'.
gedaration explicatly upgaints the
Eg: reg x,y; I single bit register variables reg [15:0] bus; // A 16 bit bus reg is treated as an unerqued ma
reg [15:0) bus; / A 16 bit bus
· reg is treated as an unsigned no. in arithmatic
expressions
reg must be used when we model actual sequential model elements like counters, shift registers, etc.
sequential model elements like counters edit
registere, etc.



```
A 32 bit asynchronous counter
module simple counter (elk, rst, count);
    input clk, mederst;
output 131:01 court;
reg [51:0] court;
     always @ (posedge alk or posedge est)
  Begin
       if (rue)
              count = count +1;
 ii) "integer" data type
 · general purpose souter data type
 · more convenient to use in loop counting.
 · default treated as a 2's complement signed integer in
  writhmatic expressions.
 · default size = 32 hits
      wire [15:0] X,7;
      integer C;
       C= X+7; //size of C will be 17 bits- (which is decided by the synthesis tool)
```

iii) "geal" data type	2 oksev Ap
· used to store floating point	
· when a "Heal" value is as	saned to an integer,
the real no. is nounded of	n to the nearest integer.
Omeal leppi;	10:17 agrant
initial / "initial	Mix aired in textbench
[9] star begin Watch a dely	stal For ild cor
e = 2.718;	
pi = 314.159e-2;	- Hisas pertion &
end sotier o	
A thee code:	8 F To: 181:01 7 R.
Another eade:	
integer x;	
begin 1	
n= pi; // n' g	ets souls 3 months
	15-120 Jat - 1-02
and i lat	acl ST = Cont
:) "+ 10 det time	1100191-130
iv) "time" data type	+ 3 L : 1
· In verilog, simulation is care clock called simulation time.	aced when misser a regical
"time" data type ean be us	ed to slove simulation
· Eg: time curr time;	<u> </u>
initial	
crovered cover time = \$ time	ne;
end	

* Vectors		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1			
NETS or "reg" type variables can be declared as vectors of variable bit widths.					
: Eg:	11 in ala 1	hit mlues			
wire 1,4,2; // single bit values wire [7:0] sun; // MSB is sum [7], LSB is sum[0]					
reg [1:10] data; // MSB is data[1], LSB is data[10]					
sea [1:10] data.	/ //MSB	is data[1] LSB is data[10]			
719 719 4814,		717.4			
	· 4-0101.	Di = 216.			
* Using section of	a vector				
· £q:					
reg [31:0] IR;		i am i Agilla No			
reg [5:0] opcode;		integes - v			
reg [4:0) regl, reg					
reg [10:0] offset;	•	Niest			
opcode = IR[31:2		v ot ≈ 10.			
regl = IR[es: 21];					
reg2 = IR [20:16]];				
reg 3 = [15:11];		in office the date they			
Aset = IR[10:0]	1	to In would winds to			
V	المرابع المناب	elsely which are			
31 Janes agate of hale	in the	o the data tree on			
grode rog 1 reg 2	reg3	offset			
IR	(5)	with your court was			
	mi.				
	I.i.				

# Multid	imension	ral Arrays & Memories	Marie Salara e como esta en activa de la como esta en activa de la como		
· Eg:	Made of F	1 1 50 COLUMN OF OR			
	15	register bank [15]	A CO		
	14	armon a set are estante tomaria	A CONTRACTOR OF THE PROPERTY O		
is stall	1	where the second of the second	4		
	1	•	3		
	(carmeter the op 10=0.			
Jan Jak	15'8	personales up = 26'00 ; som =			
1	0/0 8	CONTRACTED RED - CO 1000 HELLOWIE			
	0	register bank [0]			
			-		
not keg to	[31:0]	register-bank [15:0]; // 16 32-bit	register		
	dat	is it is is apply steady			
· Eg: suit	teger	matrin [7:0] [15:0];	SW		
1	0	1			
32 bis	by	8 rows 16 columns	: 3.		
defau	U		O		
· Ea: 400 mem hit [0:2047]: 1/2 Kh memory					
· Eg: reg membit [0:2047]; /2 Kh memory reg [7:0] membyte [0:1023]; // 1 KB memory					
0	1	ingus choos choole			
-	Alleria .	tamo [M:0] togtoe			
Decitying Constant Values					
· can be specified in sized or russized form					
· Eg: 4'b0101 //4 bit binary no. 0101					
1160					
1'b0 // logic 0 (16it)					
121h B3C // 12 bit hen no.					
12/h 8x F // 12 bit her no. (1000 xxxx [1]]					
2	5	1) signed integer			
		the feature of the second of t	470 J. F. 14		

- Parameters	A Midlight your follows
- Equivalent to "#define" constant with a given na	of Clanguage i.e. a
constant with a given na	ne
· we cannot specify size of	t a parameter
· cize gets decided from	the constant value itself
· G:	Bis No. 1 I I I I I I I I I I I I I I I I I I
parameter M1 = 25,	0=5
parameter up = 2 b'o	0, down = 26'61, steady = 26'10;
parameter RED = 36'10	0, 4ELLOW= 36'010,
GREEN = 3	6'001;
0 50	
In above examples; it is	easier to understand the
code et MJ LO, up, gou	cornesponding values.
used rather than the	Cornesponding values.
En. N. A.t. committee de la	Bree By Bree
· Eg: N bit counter	strawd
module counter (clear, clock	, court);
parameter N=7;	
input clear clock;	
output [0:N] count;	
	testino) privinga X
always @ (negedge dock)	con to first of in the
	18 A W 10101 1/1 A BE
count <= 0;	// <= vs = will be
else	1/ covered later
count <= count	41;11
end	Agril 1 Sept 1 Sept 1
endmodule	
MOTE: Any occasionale main	
1016, 1110 Against marion	ed unide always block
must be of type	reg.