

★ Inertial Delay Model (Pg. 110)

- * It models the delay found in switching ckt
- * An ip must be stable for a fixed duration b4 a value is allowed to propagate to the o/p
- * I/p must be stable for a specified "pulse rejection limit" duration for it to propagate

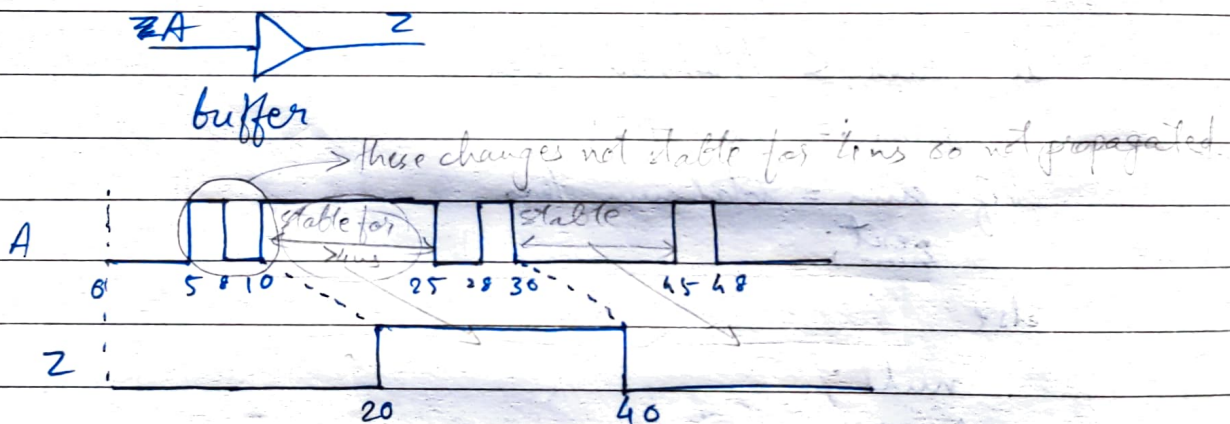
* Syntax:

signal o/p <= reject pulse_rejection_limit inertial expression after inertial_delay_value

- * If No pulse rejection limit is specified, the default pulse rejection limit is the inertial delay value

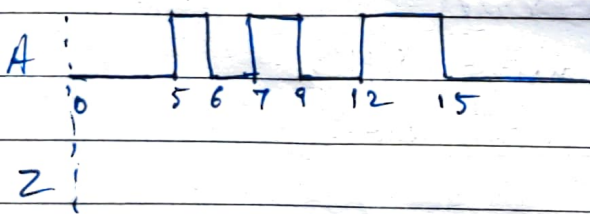
* Eg:

$z <= \text{reject } 4\text{ns inertial } A \text{ after } 10\text{ns};$



~~★~~

★ Examples:



$z <= \text{reject } 2\text{ns inertial after } 5\text{ns}$

- * By default, it is inertial delay.

Eg:- $z <= A \text{ after } 10\text{ns}; = z <= \text{inertial after } 10\text{ns};$

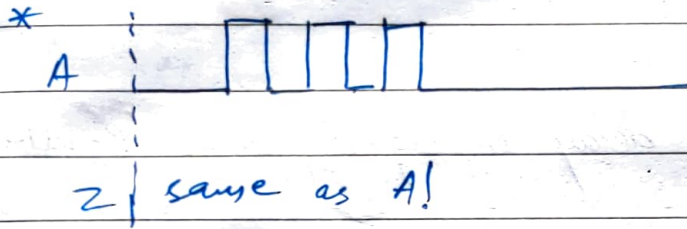
- * Advantage of Inertial Delay: Signal spikes can be removed.

* Transport Delay Model (Pg. 111)

* Pure propagation delay

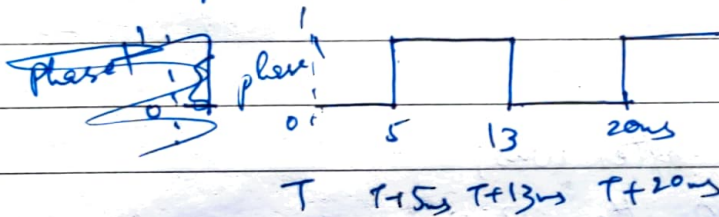
* Syntax:

$Z \leftarrow \text{transport } A \text{ after } 10 \text{ ns}$



* Creating Signal Waveform (Pg. 112)

* $\text{phase1} \leftarrow 0, '1' \text{ after } 5\text{ns}, '0' \text{ after } 13\text{ns}, '1' \text{ after } 20\text{ns};$



* delay value must always appear in increasing order only.

Lecture - 8

* Signal Drivers (Pg. 113)

Q What if there is more than one assignment to the same signal within a process?

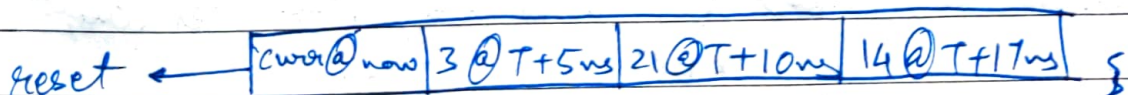
→ * Drivers:

• A driver is created for every signal that is assigned a value

• Driver holds the current value & all future values as a seq. of transactions

* Eg: process

$\text{reset} \leftarrow 3 \text{ after } 5\text{ns}, 21 \text{ after } 10\text{ns}, 14 \text{ after } 17\text{ns};$
end process;



* Draw signal drivers for the following:
 $a \leq '0'$, '1' after 5ns, '0' after 10ns, '1' after 20ns;

$b \leq 5$ after 10ns, 6 after 15ns, 7 after 20ns;

* Effect of Transport delay on signal driver (Pg. 114)

* Example:

signal Rx_Data: natural;

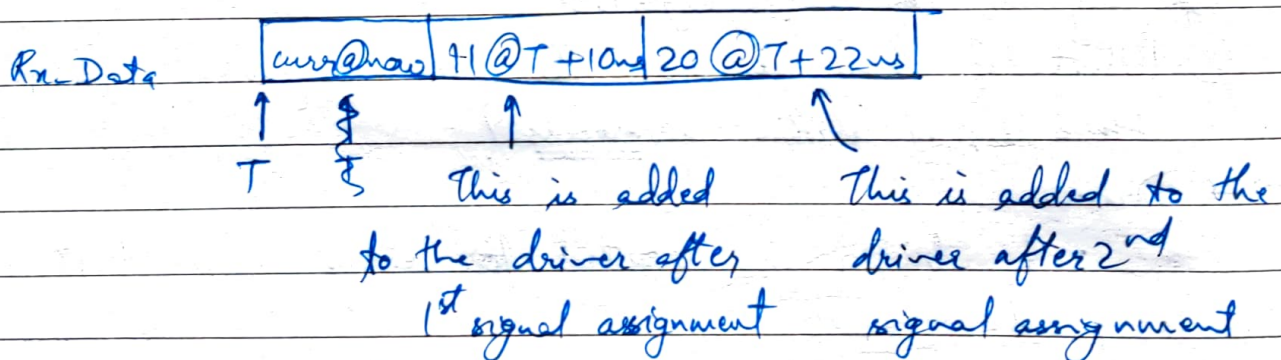
process
begin

Rx_Data \leq transport 11 after 10ns;

Rx_Data \leq transport 20 after 22ns;

Rx_Data \leq transport 35 after 18ns;

end process;



At 3rd signal assignment, 18ns < 22ns so 2nd signal assignment gets deleted.

Rx_Data ←

curr@now	11 @ T+10ns	35 @ T+18ns
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 → Answer

~~Do this~~
 * Data_Bus \leq transport X"01" after 5ns, X"FA" after 10ns,
 X"E8" after 15ns;
 Data_Bus \leq transport X"B5" after 12ns;

★ Effect of Inertial Delay on Signal Drivers (Pg. 116)

× Rules:

- i) All Xactions on or after new Xaction are deleted.
- ii) Append new Xactions at the end of the signal driver.
- iii) Which old transactions to delete? \Rightarrow

All old transactions that occur b/w time of 1st new Xaction (F) & $(F - \text{pulse reject limit})$ & whose value is different the value at F.

- iv) For a single signal assignment statement, if the 1st waveform element is added to the driver then all subsequent waveform elements are also added.

× Example:

process
begin

TxData <= 11 after 10ns;

TxData <= reject 15ns inertial 22 after 20ns;

TxData <= 33 after 15ns

end process;

Steps:

TxData ← [curr@now | 11@T+10ns]

↑
T

TxData ← [curr@now | 11@T+10ns]

Delete this as it lies b/w
5 to 20 i.e. $([F - \text{pulse reject limit}] - F)$

TxData ← [curr@now | 22@T+20ns]

TxData ← [curr@now | 22@T+20ns]

Delete this @ 20ns > 15ns

TxData ← [curr@now | 33@T+15ns]

Try this

× Add Bus <= 1 after 5ns, 21 after 9ns, 6 after 10ns, 12 after 19ns;
Add Bus <= reject 4ns inertial 6 after 12ns, 20 after 19ns;