④ Down Counter

Lecture - 10

☆ Dataflow Modeling (Chapter 5, Pg. 123)

* Concurrent signal assignment
* all statements are executed simultaneously.

Q] In behavioral style of modeling, sentences were executed based on SENSITIVITY LIST. So what is the equivalent in dataflow style of modeling?

→ Concurrent signal assignment statements are executed whenever an event occurs on a signal used in their expression.

☆ Ex: OR Gate

```
library ieee;
use ieee.std_logic_1164.all;
entity OR_G is
    port(a, b: in bit;
         y: out bit);
end OR_G;
architecture df of ORG is
begin
    y <= a or b;
end df;
```

→ This assignment gets executed whenever there is an event on either 'a' or b or both!
So 'a' & 'b' form the sensitivity list for this statement.

✡ Concurrent VS Sequential Signal Assignment

① process (b)
begin
a <= b; ..... a get value of b at T+Δ
z <= a; ..... z get value of a (at T) at T+Δ
end process

② archi
begin
a <= b; ... a gets value of b after event on b
z <= a; ... z get value of a after event on a!
end archi

* So statements in ② gives sequential execution & seq. assignment
BUT statements in ① give seq. execution but the assignment is not sequential.

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ar
signal b, c : bit;
begin
Z <= not c; } Concurrent statements.
c <= not B; } Will give same o/p even
B <= not A; } if you change the sequence!
end

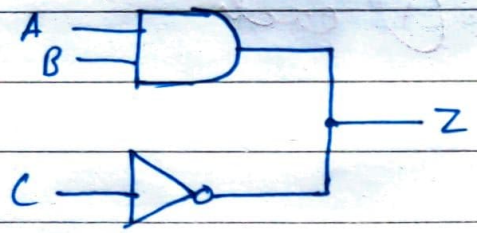
✡ Recap : Concurrent vs Sequential

✡ Assignment

✡ Multiple Drivers (Pg. 30)

Q] What happens when there are more than 1 signal assignments 2 d same signal

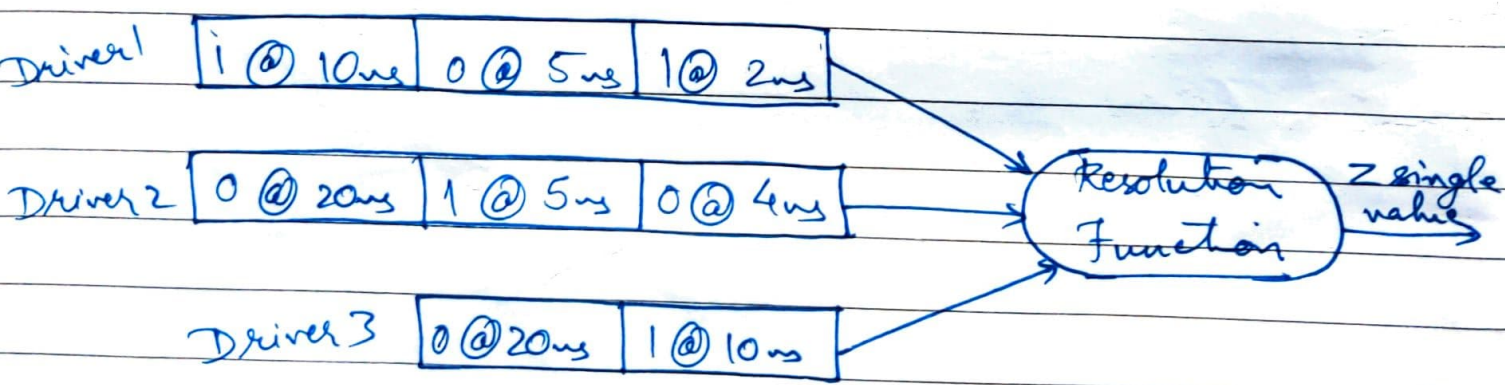
→ *Eg:




```
architecture DF of Multiple_Drivers is
begin
    Z <= A and B after 10ns;
    Z <= not C after 5ns;
end DF;
```

* User defined Resolution Function

```
* architecture DF1 of Dummy is
begin
    Z <= '1' after 2ns, '0' after 5ns, '1' after 10ns;
    Z <= '0' after 4ns, '1' after 5ns, '0' after 20ns;
    Z <= '1' after 10ns, '0' after 20ns;
end DF1;
```



Assignment : ① Digital Clock
② Calculator with provision to +, −, ×, /
③ Square root
④ Fibonacci Series
⑤ Factorial
⑥ A no. prime or not ?

✱ Resolution Function

* It can be a user defined function
* It can perform any function like wired-and, wired-OR, count the no. of events, etc.

* Example:

```
function WIREDOR (inputs : bit_vector) return bit is
begin
    for j in inputs'range
    loop
        if (inputs(j) = '1' then
            return '1';
        end if;
    end loop;
    return '0';
end WIRED_OR;
```