

Lab 6 - 2

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Lab Title: Full Adder

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Objective: To write VHDL and Vlog program for full Adder and test it using DE10C-1 FPGA Board.

Implementation:

Full adder is a combinational logic circuit which has 3 input and 2 output.

VHDL procedure:

- Write a code for 4 full adder.
- We will use signal for both input and output.

```
Signal A: std_logic_vector(3 downto 0);  
Signal B: std_logic_vector(7 downto 4);  
Signal carry: std_logic_vector(6 downto 4);  
Signal cout: std_logic;  
Signal cin: std_logic;
```

```
where A <= sw(3 downto 0);  
B <= sw(7 downto 4);  
CIN <= C;
```

```
Sum(0) <= (A(0) XOR B(4)) XOR CIN;  
Carry(4) <= (A(0) AND B(4)) OR (CIN AND (A(0) XOR B(4)));  
and line wise for all 3 full adder.
```



- at the end we will get 4 sum bit and 1 carry bit.
- Sum and carry will be shown on seven segment as well as on LED.
- Then do pin assignment and compile your program.
- After compiling download your program on board and Test it for different case.

### Vlog procedure:

This time Again we are going to use reg for output and wire for input.

```

Wire [3:0] A = SW[3:0];
Wire [7:4] B = SW[7:4];
reg [3:0] sum;
reg [6:4] carry;
reg cout;

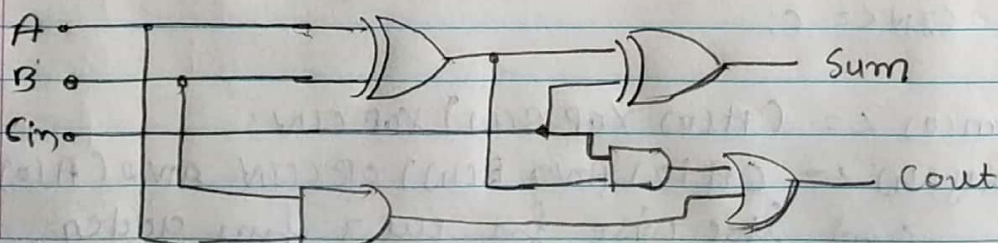
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after writing your logic compile your code and go for pin assignment.

in this case also sum and carry will be shown on seven segment and leds both.

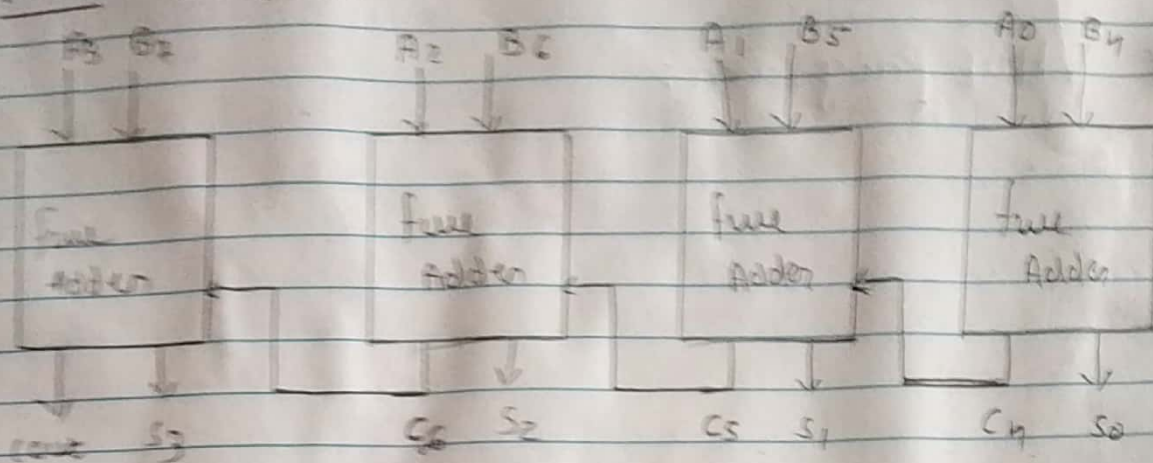
- Load your code on board and test it for different cases.

### Full Adder:





## Circuit Diagram:



## Truth Table

A	B	Cin	Sum	Cout	A	B	Cin	Sum	Cout
0	0	0	0	0	1	0	1	0	1
0	0	1	1	0	1	1	0	0	1
0	1	0	1	0	1	1	1	1	1
0	1	1	0	1					
1	0	0	1	0					

## Pin Assignment:

in	CIN	Input	PIN_AD10	out	SLED2[2]	Output	PIN_AD30
in	FLIP	Input	PIN_AE12	out	SLED2[1]	Output	PIN_AC29
out	LED[4]	Output	PIN_W17	out	SLED2[0]	Output	PIN_AC30
out	LED[3]	Output	PIN_V18	out	SLED3[6]	Output	PIN_AD26
out	LED[2]	Output	PIN_V17	out	SLED3[5]	Output	PIN_AC27
out	LED[1]	Output	PIN_W16	out	SLED3[4]	Output	PIN_AD25
out	LED[0]	Output	PIN_V16	out	SLED3[3]	Output	PIN_AC25
out	SLED0[6]	Output	PIN_AE26	out	SLED3[2]	Output	PIN_AB28
out	SLED0[5]	Output	PIN_AE27	out	SLED3[1]	Output	PIN_AB25
out	SLED0[4]	Output	PIN_AE28	out	SLED3[0]	Output	PIN_AB22
out	SLED0[3]	Output	PIN_AG27	out	SLED4[6]	Output	PIN_AA24
out	SLED0[2]	Output	PIN_AF28	out	SLED4[5]	Output	PIN_Y23
out	SLED0[1]	Output	PIN_AG28	out	SLED4[4]	Output	PIN_Y24
out	SLED0[0]	Output	PIN_AH28	out	SLED4[3]	Output	PIN_W22
out	SLED1[6]	Output	PIN_AJ29	out	SLED4[2]	Output	PIN_W24
out	SLED1[5]	Output	PIN_AH29	out	SLED4[1]	Output	PIN_V23
out	SLED1[4]	Output	PIN_AH30	out	SLED4[0]	Output	PIN_W25
out	SLED1[3]	Output	PIN_AG30	in	SW[7]	Input	PIN_AC9
out	SLED1[2]	Output	PIN_AF29	in	SW[6]	Input	PIN_AE11
out	SLED1[1]	Output	PIN_AF30	in	SW[5]	Input	PIN_AD12
out	SLED1[0]	Output	PIN_AD27	in	SW[4]	Input	PIN_AD11
out	SLED2[6]	Output	PIN_AB23	in	SW[3]	Input	PIN_AF10
out	SLED2[5]	Output	PIN_AE29	in	SW[2]	Input	PIN_AF9
out	SLED2[4]	Output	PIN_AD29	in	SW[1]	Input	PIN_AC12
out	SLED2[3]	Output	PIN_AC28	in	SW[0]	Input	PIN_AB12



# Programs

## \* VHDL program:

```
1  library ieee;
2  use ieee.std_logic_1164.all;
3
4
5
6  entity abhesaniyalab62 is
7  port(
8      SW : in std_logic_vector(7 downto 0);
9      FLIP : in std_logic;
10     C : in std_logic;
11     LED : out std_logic_vector(4 downto 0);
12     SLED0 : out std_logic_vector(6 downto 0);
13     SLED1 : out std_logic_vector(6 downto 0);
14     SLED2 : out std_logic_vector(6 downto 0);
15     SLED3 : out std_logic_vector(6 downto 0);
16     SLED4 : out std_logic_vector(6 downto 0);
17 );
18 end abhesaniyalab62;
19
20 architecture fulladder of abhesaniyalab62 is
21
22     signal A : std_logic_vector(3 downto 0);
23     signal B : std_logic_vector(7 downto 4);
24     signal SUM : std_logic_vector(3 downto 0);
25     signal CARRY : std_logic_vector(6 downto 4);
26     signal COUT : std_logic;
27     signal CIN : std_logic;
28
29
30 begin
31
32     A <= SW(3 downto 0);
33     B <= SW(7 downto 4);
34     CIN <= C;
35
36     SUM(0) <= (A(0) XOR B(4)) XOR CIN;
37     CARRY(4) <= (A(0) AND B(4)) OR (CIN AND (A(0) XOR B(4)));
38
39     SUM(1) <= (A(1) XOR B(5)) XOR CARRY(4);
40     CARRY(5) <= (A(1) AND B(5)) OR (CARRY(4) AND (A(1) XOR B(5)));
41
42     SUM(2) <= (A(2) XOR B(6)) XOR CARRY(5);
43     CARRY(6) <= (A(2) AND B(6)) OR (CARRY(5) AND (A(2) XOR B(6)));
44
45     SUM(3) <= (A(3) XOR B(7)) XOR CARRY(6);
46     COUT <= (A(3) AND B(7)) OR (CARRY(6) AND (A(3) XOR B(7)));
47
48     LED(0) <= SUM(0);
49     LED(1) <= SUM(1);
50     LED(2) <= SUM(2);
51     LED(3) <= SUM(3);
52     LED(4) <= COUT;
53
54
55
56 process (SUM, CARRY, FLIP)
57 begin
58     if (FLIP = '0') then
59         SLED4 <= "0100100";
60
61         if (SUM(0) = '0') then
62             SLED0 <= "0000001";
63         else if (SUM(0) = '1') then
64             SLED0 <= "1001111";
65         end if;
66
67         if (SUM(1) = '0') then
68             SLED1 <= "0000001";
69         else if (SUM(1) = '1') then
70             SLED1 <= "1001111";
71         end if;
72
73         if (SUM(2) = '0') then
74             SLED2 <= "0000001";
75         else if (SUM(2) = '1') then
76             SLED2 <= "1001111";
77         end if;
78
79         if (SUM(3) = '0') then
80             SLED3 <= "0000001";
81         else if (SUM(3) = '1') then
82             SLED3 <= "1001111";
83         end if;
84     end if;
85 end process;
```



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if (SUM(3) == '0') then
else if (SUM(3) == '1') then
end if;
else if (FLIP == '1') then
SLED4 <= "0110001";
SLED1 <= "1111111";
SLED2 <= "1111111";
SLED3 <= "1111111";
if (COUT == '0') then
else if (COUT == '1') then
end if;
end if;
end process;

```

46

# Vlog Program

## VLOG Program

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module abhesanfiyalab662 (SW,FLIP,CIN,LED,SLED0,SLED1,SLED2,SLED3, SLED4);
input [7:0] SW;
input FLIP;
input CIN;
output [4:0] LED;
output [6:0] SLED0;
output [6:0] SLED1;
output [6:0] SLED2;
output [6:0] SLED3;
output [6:0] SLED4;

reg [4:0] LED;
reg [6:0] SLED0;
reg [6:0] SLED1;
reg [6:0] SLED2;
reg [6:0] SLED3;
reg [6:0] SLED4;

wire [3:0] A = SW[3:0];
wire [7:4] B = SW[7:4];
reg [3:0] SUM;
reg [6:4] CARRY;
reg COUT;

always @(A or CIN or B or FLIP)
begin
SUM[0] = (A[0] ^ B[4]) ^ CIN;
CARRY[4] = (A[0] & B[4]) | ((A[0] ^ B[4]) & CIN);
SUM[1] = (A[1] ^ B[5]) ^ CARRY[4];
CARRY[5] = (A[1] & B[5]) | ((A[1] ^ B[5]) & CARRY[4]);
SUM[2] = (A[2] ^ B[6]) ^ CARRY[5];
CARRY[6] = (A[2] & B[6]) | ((A[2] ^ B[6]) & CARRY[5]);
SUM[3] = (A[3] ^ B[7]) ^ CARRY[6];
COUT = (A[3] & B[7]) | ((A[3] ^ B[7]) & CARRY[6]);

LED[3:0] = SUM;
LED[4] = COUT;

if (FLIP == 0)
begin
SLED4 = 7'b0100100;
if (SUM[0] == 0)
SLED0 = 7'b0000001;
else if (SUM[0] == 1)
SLED0 = 7'b1001111;

if (SUM[1] == 0)
SLED1 = 7'b0000001;
else if (SUM[1] == 1)
SLED1 = 7'b1001111;

if (SUM[2] == 0)
SLED2 = 7'b0000001;
else if (SUM[2] == 1)
SLED2 = 7'b1001111;

if (SUM[3] == 0)
SLED3 = 7'b0000001;
else if (SUM[3] == 1)
SLED3 = 7'b1001111;
end
else if (FLIP == 1)
begin
SLED4 = 7'b0110001;
SLED1 = 7'b1111111;
SLED2 = 7'b1111111;
SLED3 = 7'b1111111;

if (COUT == 0)
SLED0 = 7'b0000001;
else if (COUT == 1)
SLED0 = 7'b1001111;
end
end
endmodule

```

## Discussion:

LSB A MSB  
SW0 SW3

$$\begin{array}{r} \phantom{0}1\phantom{0}1\phantom{0}1 \\ A \phantom{0}1\phantom{0}0\phantom{0}1\phantom{0}0 \\ B \phantom{0}1\phantom{0}1\phantom{0}1\phantom{0}0 \\ \hline 1\phantom{0}1\phantom{0}0\phantom{0}0\phantom{0}1 \\ \hline \end{array}$$

