LAB 2

LAB Title : AND Gate

Date & Time : 22 January 2020 8:00AM to 10:00AM

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Objective : To write a program for 3 input AND Gate for both VHDL and Vlog and to see output on DE soc board.

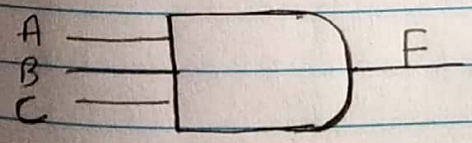
Pin Assignment :

Table 2.1 Pin assignment to input-output Variable for VHDL & Vlog

Input or output Variable	Signal name	FPGA Pin No.
X	SW[7]	PIN_AC9
Y	SW[8]	PIN_AD10
Z	SW[9]	PIN_AE12
F	LEDR[0]	PIN_V16

3 input AND Gate:

- Symbol



- Boolean Expression

$F = X \cdot Y \cdot Z$

Truth Table :

Table 2.2 Truth table for 3 input And gate

Input			Output
X	Y	Z	F
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

Program :

- VHDL

```
library ieee;
use ieee.std_logic_1164.all;

entity abhesaniyalab2 is
port (x, y, z: in std_logic;
F: out std_logic);
end abhesaniyalab2;

architecture Andgate of abhesaniyalab2 is
begin
F <= x and y and z;
end Andgate;
```

- Vlog

```
module abhesaniyalab22 (x,y,z,f);
input x, y, z;
output f;
assign F = x & y & z;
endmodule
```