LAB - 4

date : 5th February, 2020

LAB Title : Octal - Decoder

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Objective :- To write program for octal decoder in VHDL and Vlog and implement your design in Quartus II.

Implementation :

- octal decoder is combinational logic circuit which has 3 input and 8 output.

Procedure :-

* VHDL Procedure : write the code for the octal decoder

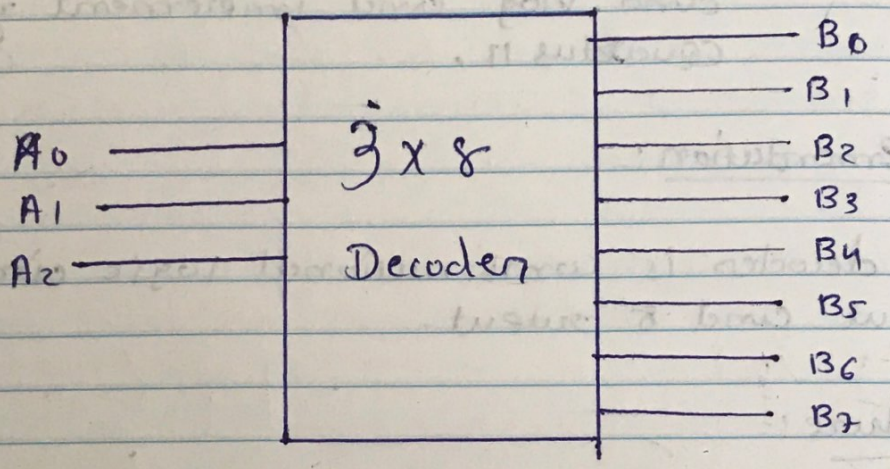
- for library section use library IEEE;
  use ieee.std_logic_1164.all;
- for the entity section use vector for input and output variable to use vector following instruction
  x : in std_logic_vector(2 to 0)
  y : out std_logic_vector(7 to 0)
- In Architecture section we are going to use when statment.
- After compiling assign pin for both input and output.
- then download program into FPGA board and do the demo.

* Vlog Procedure : Enter the Vlog code for octal decod

- define input & output as follow : Input [2:0] x;
  output [7:0] y;
- and do same as VHDL

- for the architecture section use assign statement
- end module.
- do same as VHDL Procedure.

Circuit Diagram for octal Decoder:



* Truth Table for octal decoder

Input			output							
A_0	A_1	A_2	B_0	B_1	B_2	B_3	B_4	B_5	B_6	B_7
0	0	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	1	0	0	0	0	0	0	1	0	0
0	1	1	0	0	0	0	1	0	0	0
1	0	0	0	0	0	1	0	0	0	0
1	0	1	0	0	1	0	0	0	0	0
1	1	0	0	1	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0

Pin Assignment :

Input Variable	Signal Name	FBGA PIN NO.
A_0	SW[0]	PIN - AB12
A_1	SW[1]	PIN - AC12
A_2	SW[2]	PIN - AF9
EN	SW[9]	PIN - AE12
Output Variable	**Signal Name**	**FBGA PIN NO.**
B_0	LEDR[0]	PIN - V_{16}
B_1	LEDR[1]	PIN - W_{16}
B_2	LEDR[2]	PIN - V_{17}
B_3	LEDR[3]	PIN - V_{18}
B_4	LEDR[4]	PIN - W17
B_5	LEDR[5]	PIN - W19
B_6	LEDR[6]	PIN - Y19
B_7	LEDR[7]	PIN - W20

VHDL program

VHDL Program and It's Output

Quartus Prime Standard Edition - G:/Semester 1/Digital Design/Labs/Lab4/abhesaniyalab4 - abh

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abhesaniyalab4

abhesaniyalab4.vhd

```
1   library ieee;
2   use ieee.std_logic_1164.all;
3
4   entity abhesaniyalab4 is
5   port(EN:in std_logic;
6    A:in std_logic_vector(2 downto 0);
7    B:out std_logic_vector(7 downto 0)
8   );
9   end abhesaniyalab4;
10
11  architecture octaldecoder of abhesaniyalab4 is
12  begin
13   process(A,EN)
14    begin
15    if(EN='1')
16       then
17       case A is
18       when "000"=>B<="00000001";
19       when "001"=>B<="00000010";
20       when "010"=>B<="00000100";
21       when "011"=>B<="00001000";
22       when "100"=>B<="00010000";
23       when "101"=>B<="00100000";
24       when "110"=>B<="01000000";
25       when "111"=>B<="10000000";
26       end case;
27
28   else
29     B <= "00000000";
30
31   end if;
32  end process;
33  end octaldecoder;
```

Quartus Prime Standard Edition - G:/Semester 1/Digital Design/Labs/Lab4/abhesaniyalab4 - abhesaniyalab4

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abhesaniyalab4

abhesaniyalab4.vhd

Simulation Waveform Editor - G:/Semester 1/Digital Design/Labs/Lab4/abhesaniyalab4 - abhesaniyalab4 - [abhesaniyalab4_20200204

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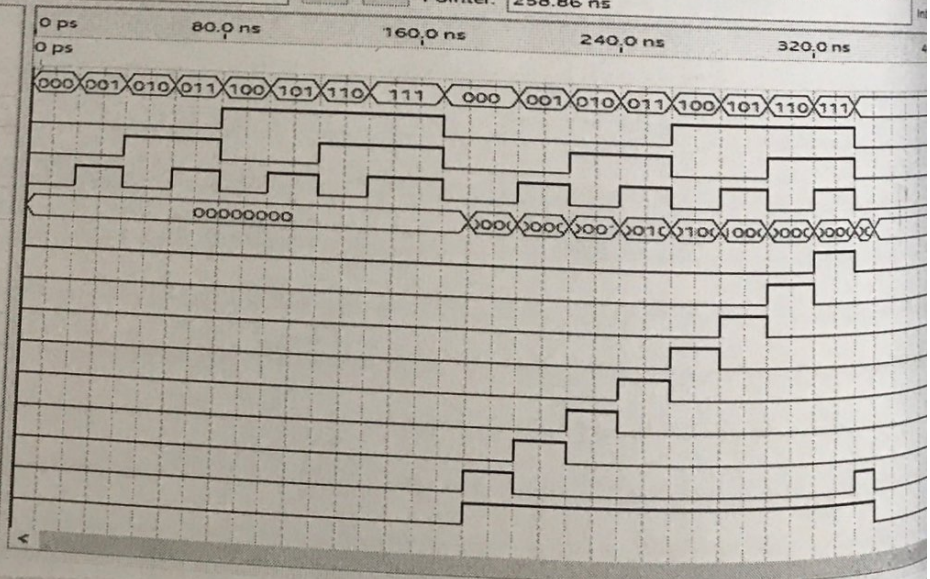
Master Time Bar: 0 ps

Pointer: 258.86 ns

Name	Value at 0 ps
A	B 000
A[2]	B 0
A[1]	B 0
A[0]	B 0
B	B 00000000
B[7]	B 0
B[6]	B 0
B[5]	B 0
B[4]	B 0
B[3]	B 0
B[2]	B 0
B[1]	B 0
B[0]	B 0
EN	B 0



Vlog Program

Vlog Program and It's Output

esign/Labs/Lab44/abhesaniyalab44 - abhesaniyalab44

Tools Window Help

Compilation Report - abhesaniyalab44

abhesaniyalab44.v

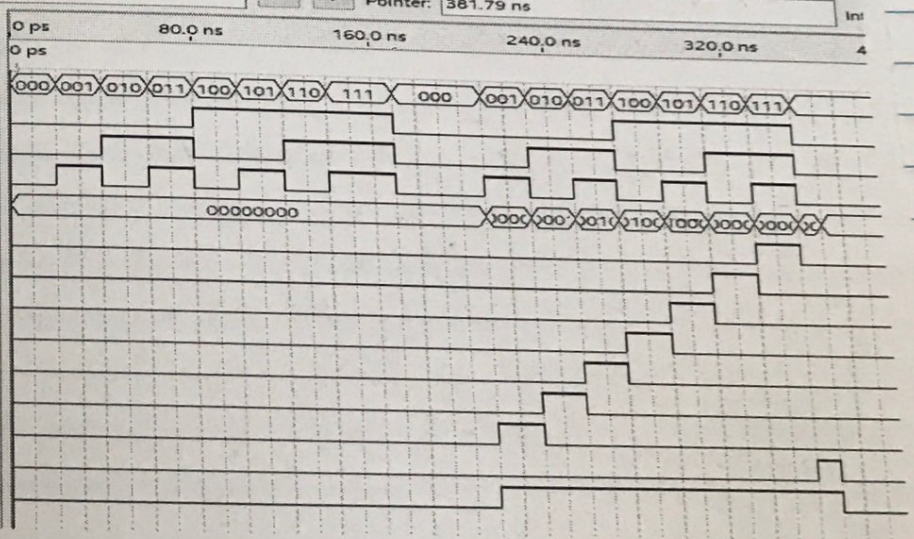
```
1  module abhesaniyalab44 (A,B,EN);
2
3    input [2:0]A;
4    input EN;
5    output[7:0]B;
6    reg [7:0] B;
7    //assign
8    always @(A or EN)
9    begin
10         if(EN == 1)
11         begin
12             B = (A == 3'B000) ? 8'B00000001:
13                 (A == 3'B001) ? 8'B00000010:
14                 (A == 3'B010) ? 8'B00000100:
15                 (A == 3'B011) ? 8'B00001000:
16                 (A == 3'B100) ? 8'B00010000:
17                 (A == 3'B101) ? 8'B00100000:
18                 (A == 3'B110) ? 8'B01000000:
19                 (A == 3'B111) ? 8'B10000000:
20                 8'B00000000;
21         end
22         else  B = 8'B00000000;
23
24   end
25   endmodule
```

Simulation Waveform Editor - G:/Semester 1/Digital Design/Labs/Lab44/abhesaniyalab44 - abhesaniyalab44 - [abhesaniyalab44_202002

File Edit View Simulation Help

Master Time Bar: 0 ps Pointer: 381.79 ns

Name	Value at 0 ps
A	B 000
A[2]	B 0
A[1]	B 0
A[0]	B 0
B	B 00000000
B[7]	B 0
B[6]	B 0
B[5]	B 0
B[4]	B 0
B[3]	B 0
B[2]	B 0
B[1]	B 0
B[0]	B 0
EN	B 0



Discussion:

I haven't came across any errors while I was doing programming for octal decoder.

Enable	I/P SW2 MSB	SW0 LSB	O/P LED7 MSB	LED0 LSB
S4				
0 C0	L2	010	00000100	
1 L4				
2 L2				
3 L3	L4	100	00001000	
4 L4				
5 L5				
C L6	L6	110	00100000	
7 L7				

11.25