

LAB - 1

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Lab Title : OR gate

Date & Time : 15 Jun, 2020 8:00 AM To 10:00 AM

Recorded and Submitted by Bheshniyer Abhishek

Objective : To built program for or gate in VHDL and Vlog And to see out put on DE-Soc board

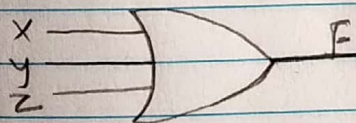
Pin Assignment :

Table 1.1 Pin assignment for both VHDL & Vlog

Input or Output Variable	Signal Name	FPGA Pin No.
X	SW[7]	PIN-Ac9
Y	SW[8]	PIN-A210
Z	SW[9]	PIN-AE12
F	LEDR[0]	PIN-V16

3 input OR Gate :

- Symbol



- Boolean expression

$$F = X + Y + Z$$

Truth Table :

Table 1.2 truth table for 3 input or gate

Input			Output
X	Y	Z	F
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

Program :

- VHDL

```
library ieee;  
use ieee.std_logic_1164.all;
```

```
entity abhesaniyulab1 is  
  port (X, Y, Z : in std_logic;  
        F : out std_logic);  
end abhesaniyulab1;
```

```
architecture orgate of abhesaniyulab1 is  
begin  
  F <= X or Y or Z;  
end orgate;
```


- Vlog

```
module abhesamiyellab12 (x, y, z, f);  
input x, y, z;  
output f;  
assign f = x | y | z;  
endmodule
```