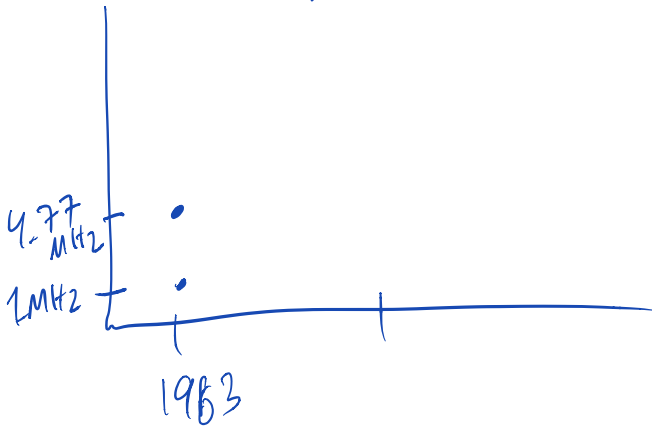
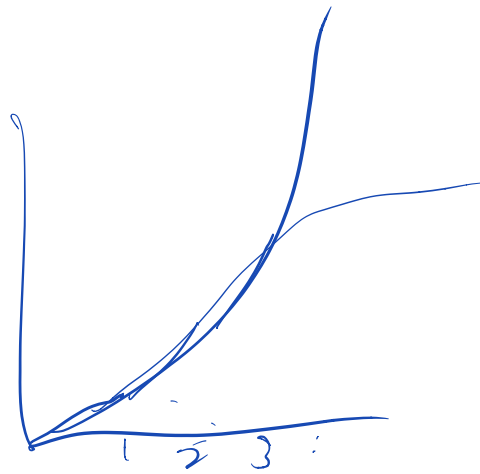
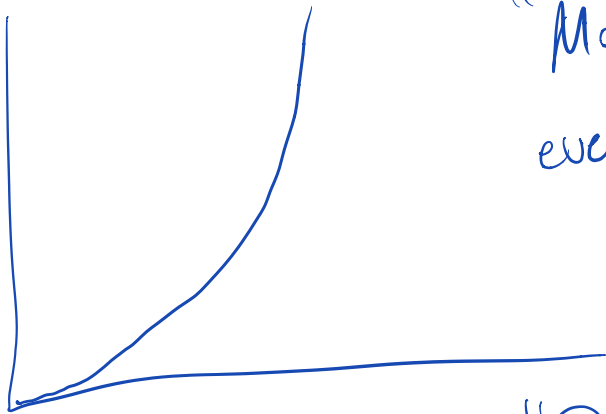


20 MHz



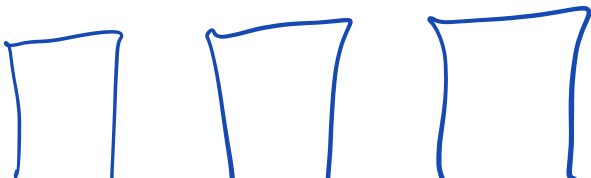
"Moore's Law"

every 18 m.s.
of transistors
on chip doubles

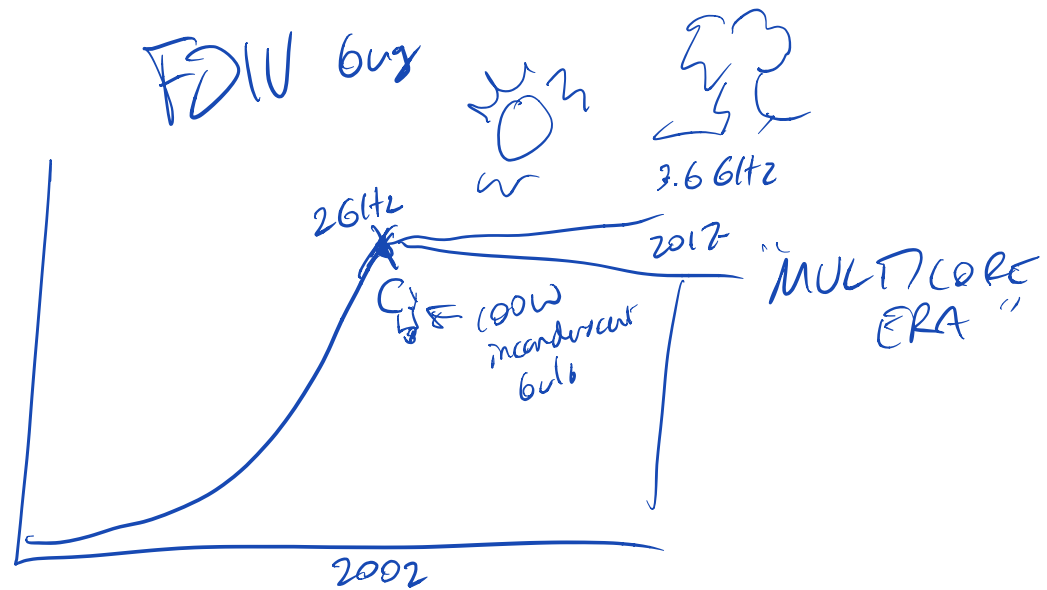


"Dennard scaling"

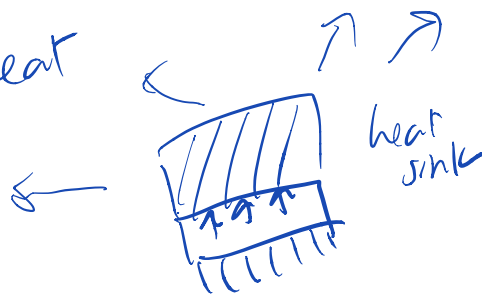
clock speed
scales linearly
w/ # of transistors



Synchronous



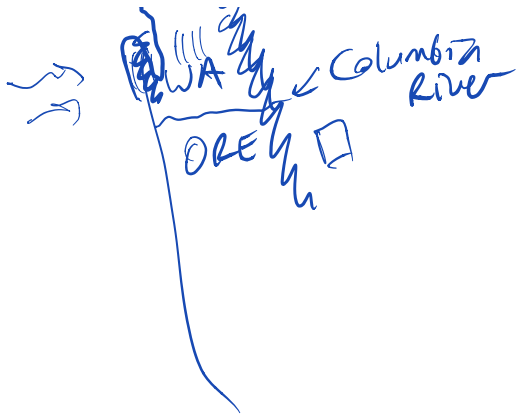
— power consumption
— heat



COOLING

FB, Amazon, Google
data center

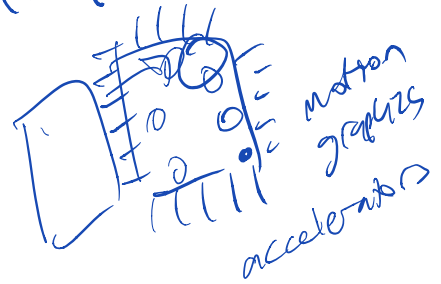
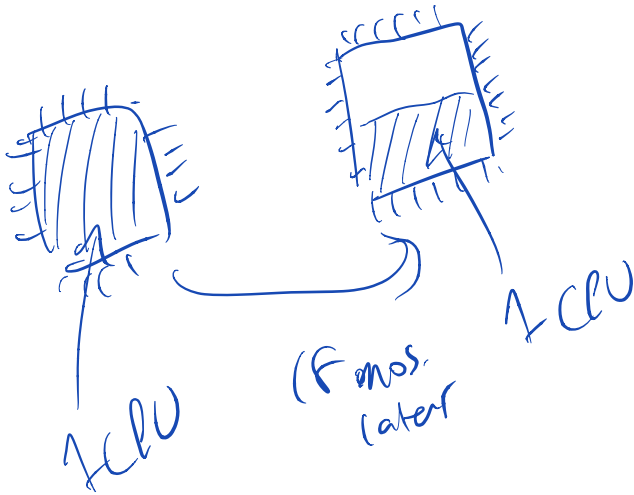
↳ Cascades



Voltage scaling

DUPS

dynamic voltage & freq. scaling

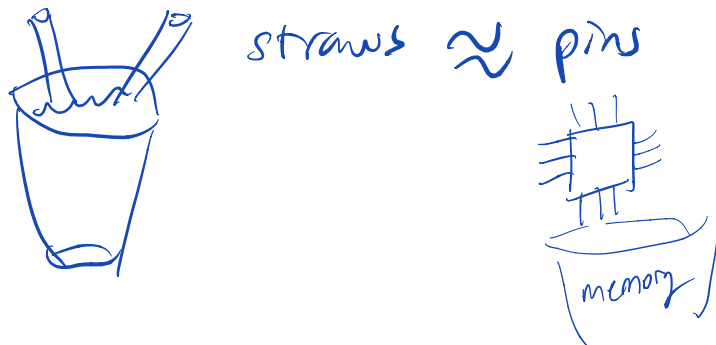
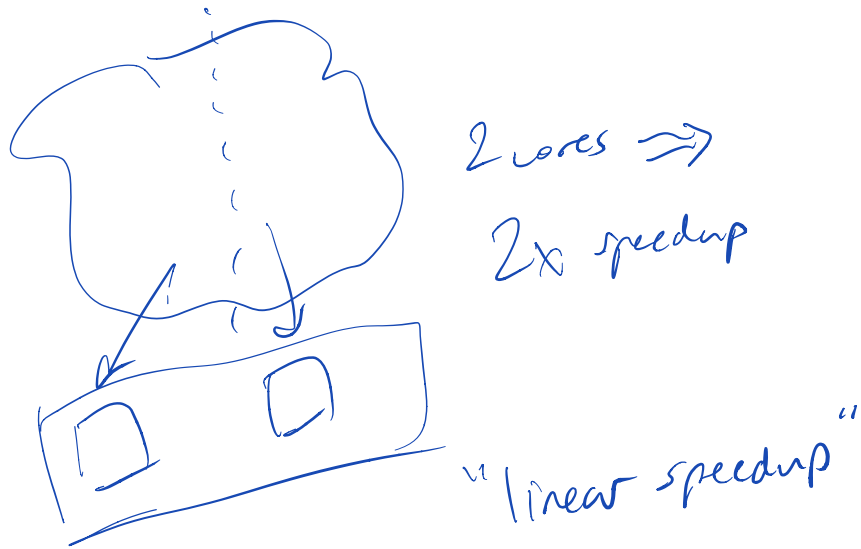
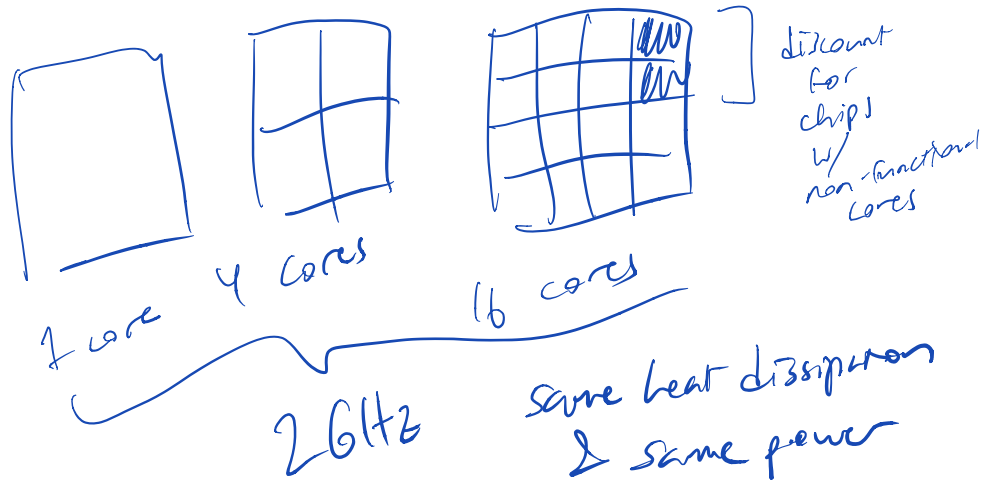


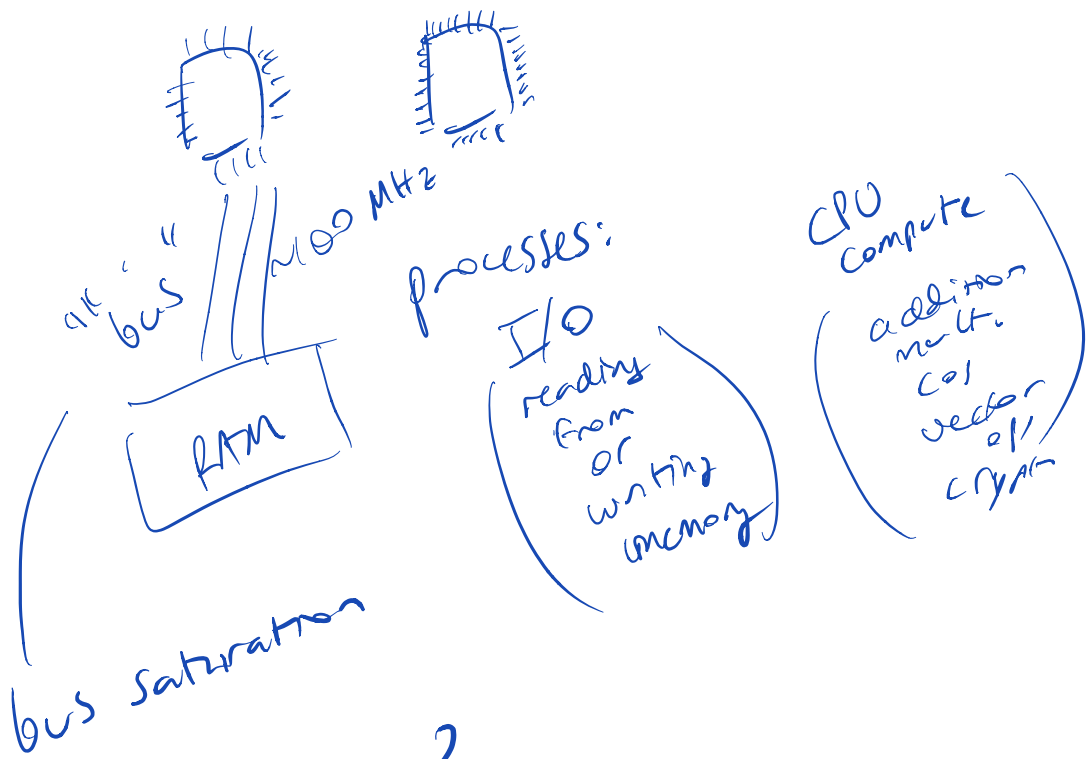
"MULTICORE ERA"

yield

$\frac{\text{good}}{\text{total}}$

$\approx 85\%$

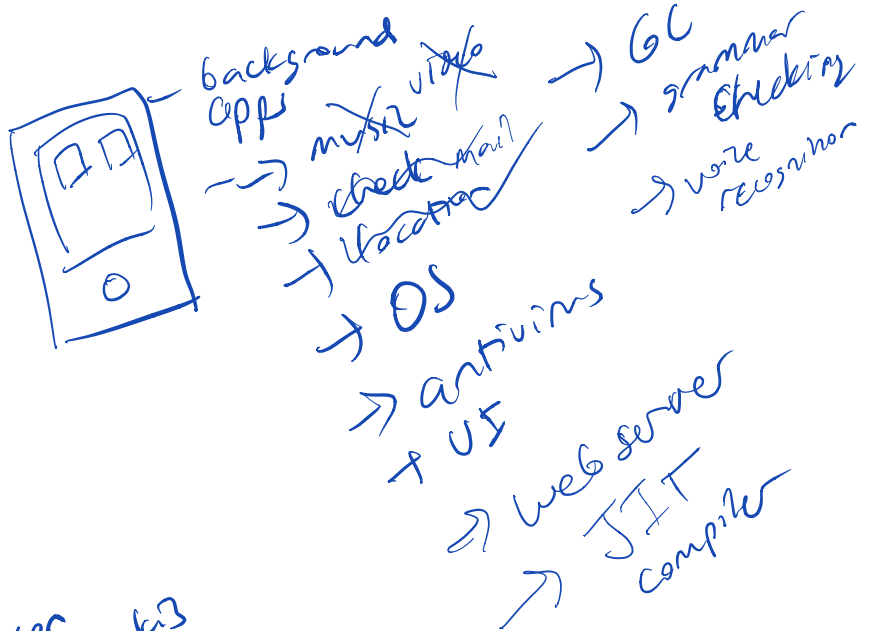




bus saturation

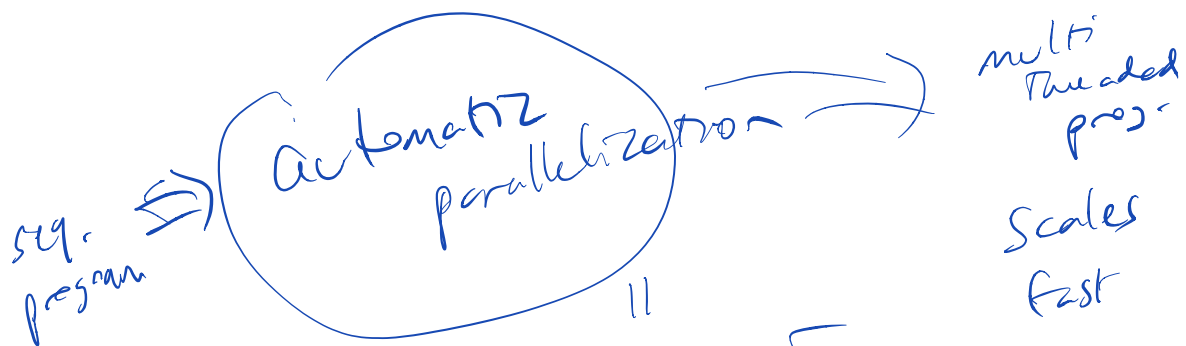
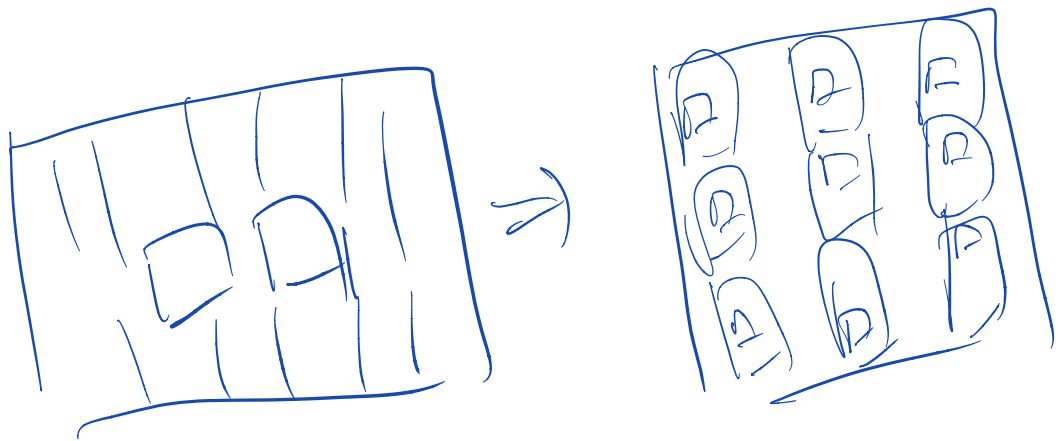
harnessing cores?

- multithreading
- multiprocessing



I RAM
intelligent
RAM
Patterson
Kozyrakis

Dave
Christof



Systems - 6 - data-science.cs.umass.edu