Josephson-Junction
Superconducting Qubit Fabrication

1. Introduction

Intractable questions of human civilization look towards the computing technology to provide answers to their complex, multidimensional problem. Often the mathematical formulation of a subject in question, requires powerful computing system to analyse and process data. Limitation of classical system and advent of quantum physics encourages to develop platform for quantum based computer. Centre to the quantum computer, is super-conducting technology to develop qubit - an analogous of MOSFET from classical computer and building block of quantum processing unit.

In pursuit to harness quantum phenomena, English physicist Brian D Josephson predicted the current between two superconductors based on Bardeen–Cooper–Schrieffer theory. This predication paved the way to develop Josephson junction – a device where two superconductor are separated by a thin barrier/insulating material. Superconductor at absolute zero temperature gives zero resistance to current through it and also maintain
current flow even without power source, and give no current when power is connected due to oscillation. This device exhibit quantum phenomena at macroscopic/atomic scale and basis of many existing quantum processor.

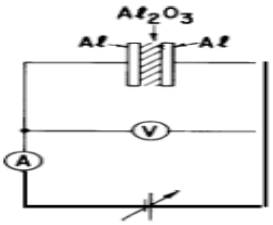


Figure 1
Josephson Junction (JJ) [8]

2. Process Overview

The conceptual design of Josephson junction shows a simple device to fabricate where two superconducting material separated by a thin insulating barrier. Fabrication complexity appears as device design changes since device need to connect to external capacitive and further inductive control source through superconductor layer as figure 2 shows.

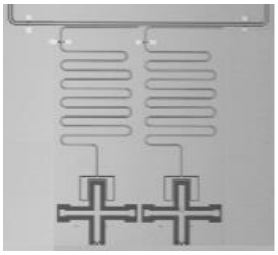
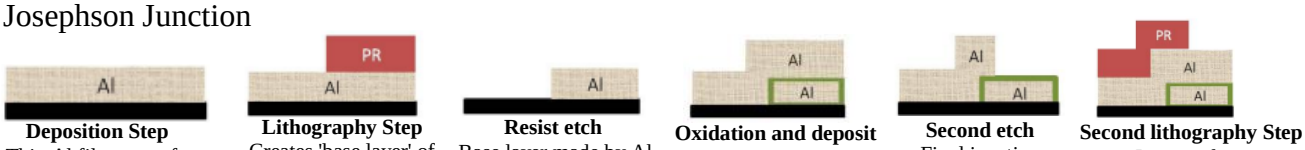


Figure 2
JJ and lead with External source [4]

Device sandwiched tri-layer is fabricated with two Aluminium or Niobium based superconductor with Aluminium Oxide insulating layer between them. This report highlights Aluminium/ Aluminium Oxide/Aluminium based Josephson junction.
This report highlights Aluminium/ Aluminium Oxide/Aluminium based Josephson junction. Fabrication starts with deposition of Al on Si substrate followed by positive photoresist deposition. Lithography followed by etch gives the required lead pattern and junction at the crossing of two lead, on base resist layer. Formation of base Al layer is followed by oxide junction - AlOx formation. Further deposition of second Al layer followed by positive photoresist deposition, lithography to etch to pattern second layer pattern gives the final Josephson Junction



Deposition Step
Thin Al film on wafer

Lithography Step
Creates 'base layer' of photo-resist.

Resist etch
Base layer made by Al

Oxidation and deposit
Second Al layer

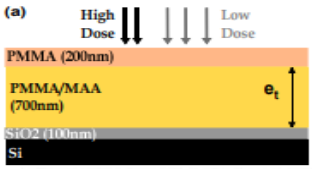
Second etch
Final junction

Second lithography Step
Junction layer

Figure 3 Josephson Junction Basic Fabrication Step [5]

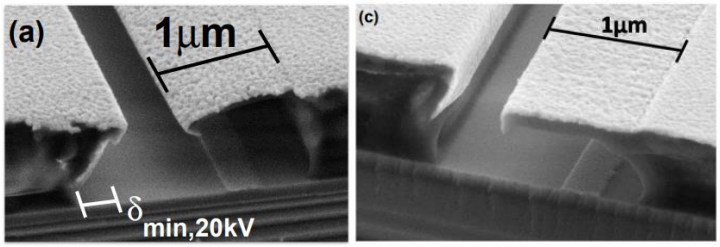
3. Device fabrication steps and challenges

Lead connection to two superconducting layers as shown in figure 2 necessitates design charges and fabrication methodology. Lead connected layer without having connection between two superconducting junction and lead layer is needed. There are multiple fabrication technique but this report is inspired from Controlled Undercut Technique - CUT. CUT requires the formation of controlled strongly asymmetric undercut shown in Figure 4. Two photoresist layer one of poly-methyl methacrylate (PMMA) and another is of PMMA/MAA having thickness of 700nm and 200nm (top layer) is deposited on wafer. Selectivity of PMMA is three times lower than PMMA/MAA gives desired asymmetric undercut. Two successive exposure of E-beam writer at 100KV with high (for required opening in top resist layer) and low doses (for depth in second resist layer) produce asymmetric undercut in photoresist. Exposure is followed by 30s of development using MIBK and IPA in 1:3 ratio and rinsing with pure IPA. Final asymmetric undercut with one side depth of 1um and other side 50nm (undesired) is obtained. Angle evaporation on substrate through opening in photoresist determine metal deposition on substrate or on resist wall.



Two layer resist on Substrate[2]

Asymmetric depth
Metal deposition on substrate and resist by two angled evaporation [2]



Scanning Electron Microscope Image of CUT Process show asymmetric undercut and metal deposition on substrate [2]

Figure 4

4. Description of fabrication process and Impact on device fabrication

Josephson junction device is fabricated on 0.5 mm thick high resistive silicon substrate. Centre of groove/lead cross form the space for micrometre to nanometre size junction with 0.04 μm^2 to 10 μm^2. Complete fabrication process is carried in one vacuum cycle to avoid unnecessary oxidation of Al layer.

Resist pattern after lithography and development (Top View)

Resist pattern and lead width 'l' and junction width 'L'after lithography and development (Lateral View) [1]

Figure 5

Recipe starts with cleaning of substrate and deposition of E-beam MicroChemPMMA 950A5 PMMA resist (Polymethyl methacrylate) having thickness 400nm at 6800 rpm. Wafer with resist is baked at 180^0 Celsius for 2 minutes. E-beam lithography at 20KV to 30 KVe beam

voltage with 420 μC/cm^2 to 480 μC/cm^2 dosage followed by development 1:3 MIBK/IMPA developed for 40 second to obtain the required pattern for lead and junction as shown in figure 6. Strong argon plasma etching cleans the residual PMMA after development.

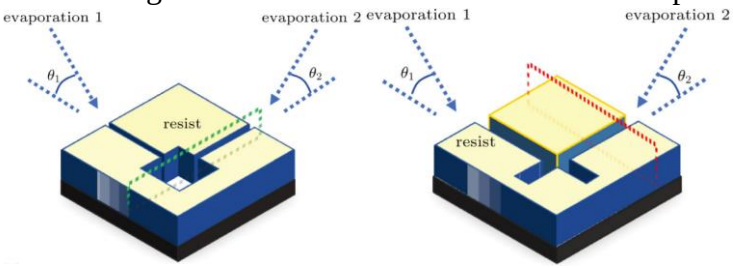
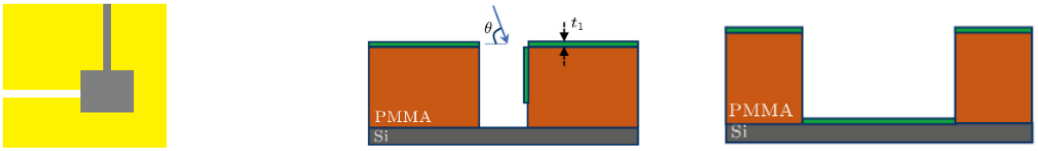


Figure 6 Resist patter with both evaporation process [1]

First superconducting Al layer deposition by evaporating Al at angle of substrate plane through pattern opening in resist. Evaporation angle control junction size and keep load single layered shown in Figure 7. For first layer evaporation at angle θ_1 only deposit first layer with its lead and shadow effect with evaporation angle do not allow any metal deposition in other lead area shown in figure 7, provides the data of first layer deposition on 15nm thickness.



Al First Layer deposition (Top View)

Al First Layer deposition (Lateral View)
No deposition on groove perpendicular to evaporation angle (Left), Deposition area on Junction area (Right) and on the groove along evaporation direction[1]

Figure 7

First Al layer deposited, gives platform for in-situ oxidation to form Silicon Oxide junction in junction area of 500nm thick (50nm for quantum computing) as shown in figure 8 through oxidation (PECVD) process for 10min at 30 mbar oxygen at 250^0 Celsius.

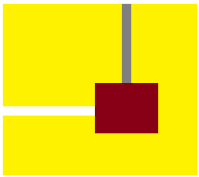
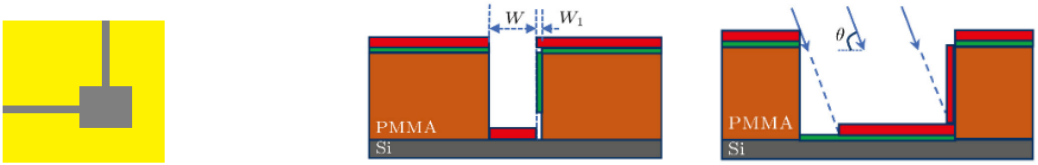


Figure 8 Silicon Oxide Junction formation on first deposited Al layer (not on lead)

Oxide Junction formation followed by second superconducting layer deposition by evaporation process. Sample is rotated by 90 degree, and resist shadow with angle evaporation at an angle θ_2 deposit second Al layer on Oxide junction with thickness 30nm as Zhang et al and the connecting lead and with no deposition in first lead area.

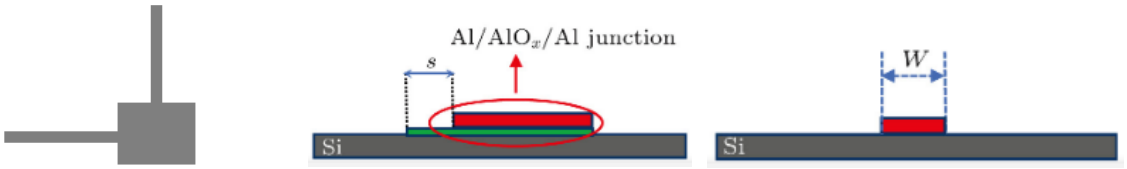


Al Second Layer deposition (Top View)

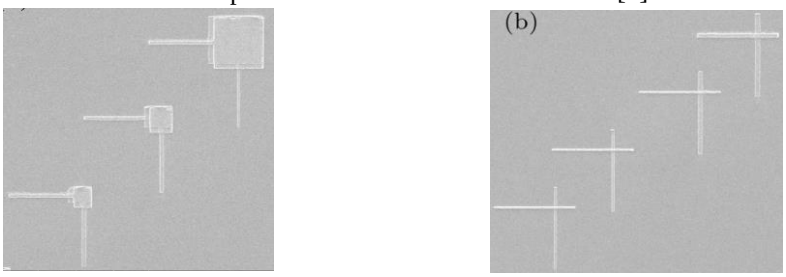
Al Second Layer deposition (Lateral View),
Deposition on groove along the direction of evaporation (Left),
Deposition area on Junction area (Right) [1]

Figure 9

Second layer deposition followed by final PMMA resist lifting off to get final Junction with lead connecting two superconducting layer on silicon substrate shown in figure 10.



Final Josephson Junction on silicon substrate. [1]



SEM image of micrometre and nanometre size junction [1]

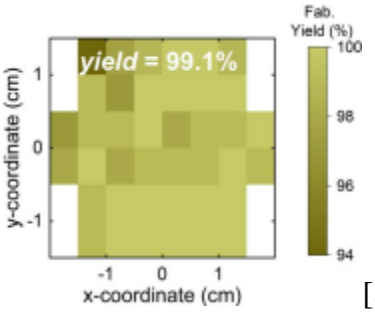
Figure 10

Osman et al [3] provides the data for junction on 76 mm wafer. It shows fabrication of 45 chips with 0.5 x 0.5 cm2 size having 100 junction with 10 different sizes on each chip with Junction size of 0.01 to 0.16 μm^2 size.

Josephson junction fabrication is constrained by evaporation angle and resist thickness

t / tan θ > l ---------- equation (1)

t = layer thickness resist and l = lead wire width



[3]

Figure 11

When equation 1 is satisfied, no deposition in grooves perpendicular to evaporation direction, help to create a two separated junction and both leads are not shorted.

Josephson junction size is constrained by resist interaction area, resist thickness and evaporation angle (photo resist Shadow effect) Evaporation angle confirm if film should not overlapped during evaporation and junction size.

This angled evaporation and resist thickness to deposit metal, reduce actual junction size by S = t/ tan θ

Final junction size obtained, is L – t/tan theta

Where L = intersection length

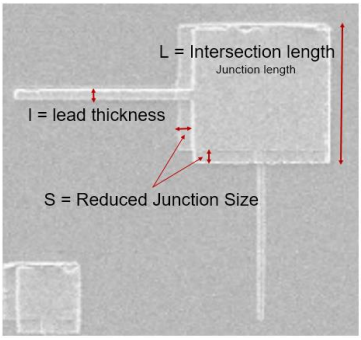


Figure 12

5. Conclusions

Inspired from Controlled Undercut Technique, shadowed evaporation encourages simple and scalable fabrication process to produce highly coherence qubit device. Single vacuum cycle process enable realization of varying size Josephson Junction which can be varied by changing the resist pattern size during lithography. CUT technique needs only two perpendicular groove in resist followed by deposition of two superconducting Al layer by evaporation with intermediate oxidation to form junction in between two layer deposition.

References

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