

Chapter 11

D/A CONVERSION AND A/D CONVERSION

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CHAPTER OBJECTIVES

- Be able to do calculations related to variable resistor and binary ladder networks.
- Recall some of the sections of a typical D/A converter and calculate D/A resolution.
- Understand A/D conversion using the simultaneous, counter, continuous, and dual-slope methods.
- Discuss the accuracy and resolution of A/D converters.

Digital-to-analog (D/A) and analog-to-digital (A/D) conversion form two very important aspects of digital data processing. Digital-to-analog conversion involves translation of digital information into equivalent analog information. As an example, the output of a digital system might be changed to analog form for the purpose of driving a pen recorder. Similarly, an analog signal might be required for the servomotors which drive the cursor arms of a plotter. In this respect, a D/A converter is sometimes considered a decoding device.

The process of changing an analog signal to an equivalent digital signal is accomplished by the use of an A/D converter. For example, an A/D converter is used to change the analog output signals from transducers (measuring temperature, pressure, vibration, etc.) into equivalent digital signals. These signals would then be in a form suitable for entry into a digital system. An A/D converter is often referred to as an *encoding* device since it is used to encode signals for entry into a digital system.

Digital-to-analog conversion is a straightforward process and is considerably easier than A/D conversion. In fact, a D/A converter is usually an integral part of any A/D converter. For this reason, we consider the D/A conversion process first.

ary equivalent weight

11-1 VARIABLE-RESISTOR NETWORKS

The basic problem in converting a digital signal into an equivalent analog signal is to change the n digital voltage levels into one equivalent analog voltage. This can be most easily accomplished by designing a resistive network that will change each digital level into an equivalent binary weighted voltage (or current).

BINARY EQUIVALENT WEIGHT

As an example of what is meant by *binary equivalent weight*, consider the truth table for the 3-bit binary signal shown in Fig. 11-1. Suppose that we want to change the eight possible digital signals in this figure into equivalent analog voltages. The smallest number represented is 000; let us make this equal to 0 V. The largest number is 111; let us make this equal to +7 V. This then establishes the range of the analog signal to be developed. (There is nothing special about the voltage levels chosen; they were simply selected for convenience.)

Now, notice that between 000 and 111 there are seven discrete levels to be defined. Therefore, it will be convenient to divide the analog signal into seven levels. The smallest incremental change in the digital signal is represented by the least-significant bit (LSB), 2^0 . Thus we would like to have this bit cause a change in the analog output that is equal to one-seventh of the full-scale analog output voltage. The resistive divider will then be designed such that a 1 in the 2^0 position will cause $+7 \times \frac{1}{7} = +1$ V at the output.

Since $2^1 = 2$ and $2^0 = 1$, it can be clearly seen that the 2^1 bit represents a number that is twice the size of the 2^0 bit. Therefore, a 1 in the 2^1 bit position must cause a change in the analog output voltage that is twice the size of the LSB. The resistive divider must then be constructed such that a 1 in the 2^1 bit position will cause a change of $+7 \times \frac{2}{7} = +2$ V in the analog output voltage.

2^2	2^1	2^0
0	0	0
0	0	1
0	1	0
0	1	1
0	0	0
1	0	1
1	1	0
1	1	1

Fig. 11-1

Bit	Weight
2^0	$1/7$
2^1	$2/7$
2^2	$4/7$
Sum	7/7

(a)

Bit	Weight
2^0	$1/15$
2^1	$2/15$
2^2	$4/15$
2^3	$8/15$
Sum	15/15

(b)

Fig. 11-2 Binary equivalent weights.

Similarly, $2^2 = 4 = 2 \times 2^1 = 4 \times 2^0$, and thus the 2^2 bit must cause a change in the output voltage equal to four times that of the LSB. The 2^2 bit must then cause an output voltage change of $+7 \times \frac{4}{7} = +4$ V.

The process can be continued, and it will be seen that each successive bit must have a value twice that of the preceding bit. Thus the LSB is given a binary equivalent weight of $\frac{1}{7}$ or 1 part in 7. The next LSB is given a weight of $\frac{2}{7}$, which is twice the LSB, or 2 parts in 7. The MSB (in the case of this 3-bit system) is given a weight of $\frac{4}{7}$, which is 4 times the LSB or 4 parts in 7. Notice that the sum of the weights must equal 1. Thus $\frac{1}{7} + \frac{2}{7} + \frac{4}{7} = \frac{7}{7} = 1$. In general, the binary equivalent weight assigned to the LSB is $1/(2^n - 1)$, where n is the number of bits. The remaining weights are found by multiplying by 2, 4, 8, and so on. Remember,

$$\text{LSB weight} = \frac{1}{(2^n - 1)}$$

Example 11-1

Find the binary equivalent weight of each bit in a 4-bit system.

Solution

The LSB has a weight of $1/(2^4 - 1) = 1/(16 - 1) = \frac{1}{15}$, or 1 part in 15. The second LSB has a weight of $2 \times \frac{1}{15} = \frac{2}{15}$. The third LSB has a weight of $4 \times \frac{1}{15} = \frac{4}{15}$, and the MSB has a weight of $8 \times \frac{1}{15} = \frac{8}{15}$. As a check, the sum of the weights must equal 1. Thus $\frac{1}{15} + \frac{2}{15} + \frac{4}{15} + \frac{8}{15} = \frac{15}{15} = 1$. The binary equivalent weights for 3-bit and 4-bit system are summarized in Fig. 11-2.

RESISTIVE DIVIDER

What is now desired is a resistive divider that has three digital inputs and one analog output as shown in Fig. 11-3a on the next page. Assume that the digital input levels are 0 = 0 V and 1 = +7 V. Now, for an input of 001, the output will be +1 V. Similarly, an input of 010 will provide an output of +2 V, and an input of 100 will provide an output of +4 V. The digital input 011 is seen to be a combination of the signals 001 and 010. If the +1 V from the 2^0 bit is added to the +2 V from the 2^1 bit, the desired +3 V output for the 011 input is achieved. The other desired voltage levels are shown in Fig. 11-3b; they, too, are additive combinations of voltages.

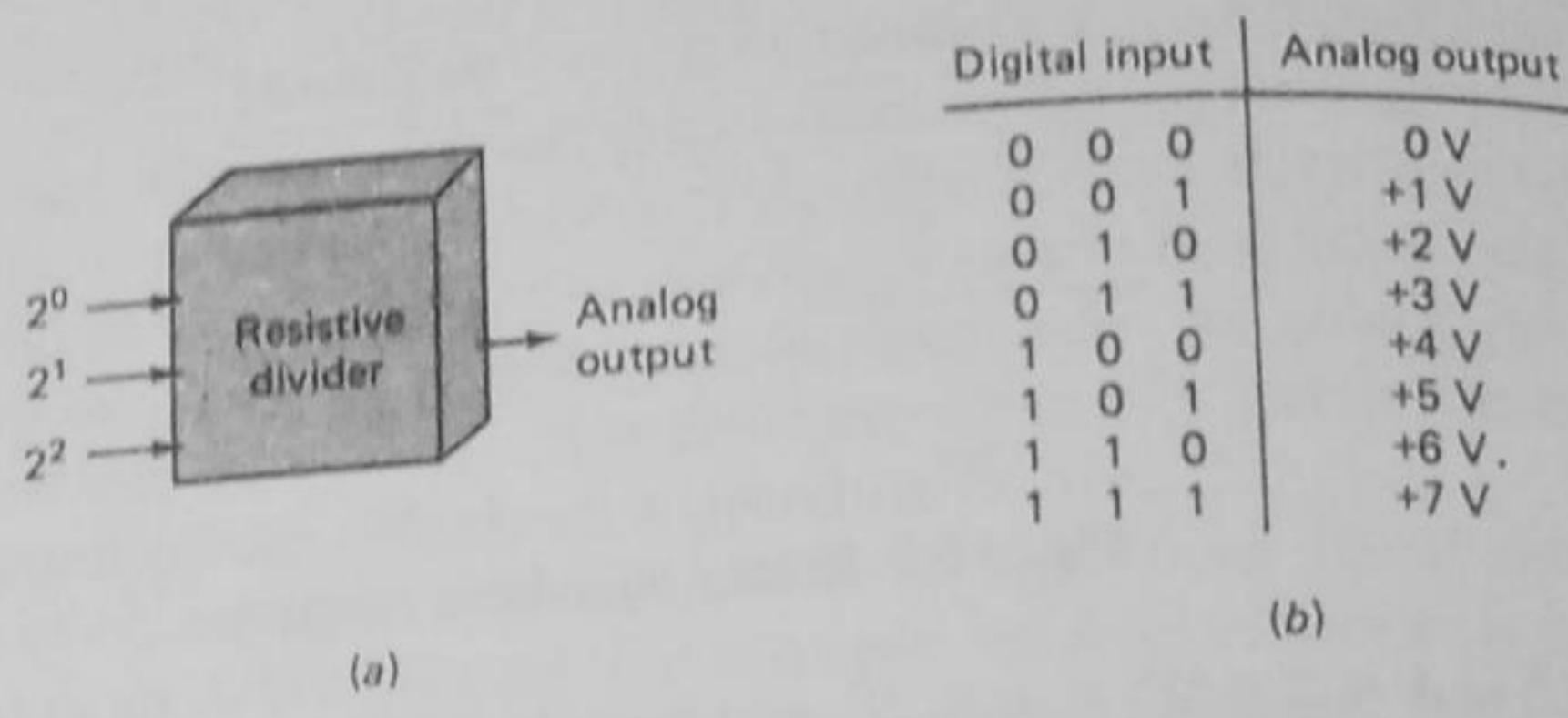


Fig. 11-3

Thus the resistive divider must do two things in order to change the digital input into an equivalent analog output voltage:

1. The 2^0 bit must be changed to +1 V, and 2^1 bit must be changed to +2 V, and 2^2 bit must be changed to +4 V.
2. These three voltages representing the digital bits must be summed together to form the analog output voltage.

A resistive divider that performs these functions is shown in Fig. 11-4. Resistors R_0 , R_1 , and R_2 form the divider network. Resistance R_L represents the load to which the divider is connected and is considered to be large enough that it does not load the divider network.

Assume that the digital input signal 001 is applied to this network. Recalling that 0 = 0 V and 1 = +7 V, you can draw the equivalent circuit shown in Fig. 11-5. Resistance R_L is considered large and is neglected. The analog output voltage V_A can be more easily found by use of Millman's theorem, which states that the voltage appearing at a node in a resistive network is equal to the summation of the currents entering the node (found by assuming that the node voltage is zero) divided by the summation of the conductances connected to the node. In equation form, Millman's theorem is

$$V = \frac{V_1/R_1 + V_2/R_2 + V_3/R_3 + \dots}{1/R_1 + 1/R_2 + 1/R_3 + \dots}$$

Applying Millman's theorem to Fig. 11-5, we obtain

$$\begin{aligned} V_A &= \frac{V_0/R_0 + V_1/(R_0/2) + V_2/(R_0/4)}{1/R_0 + 1/(R_0/2) + 1/(R_0/4)} \\ &= \frac{7/R_0}{1/R_0 + 2/R_0 + 4/R_0} = \frac{7}{7} = +1 \text{ V} \end{aligned}$$

Drawing the equivalent circuits for the other 7-input combinations and applying Millman's theorem will lead to the table of voltages shown in Fig. 11-3 (see Prob.

Example 11-2

For a 4-input resistive divider ($0 = 0 \text{ V}$, $1 = +10 \text{ V}$), find (a) the full-scale voltage; (b) the output voltage change due to the LSB; (c) the analog output voltage for digital input of 1011.

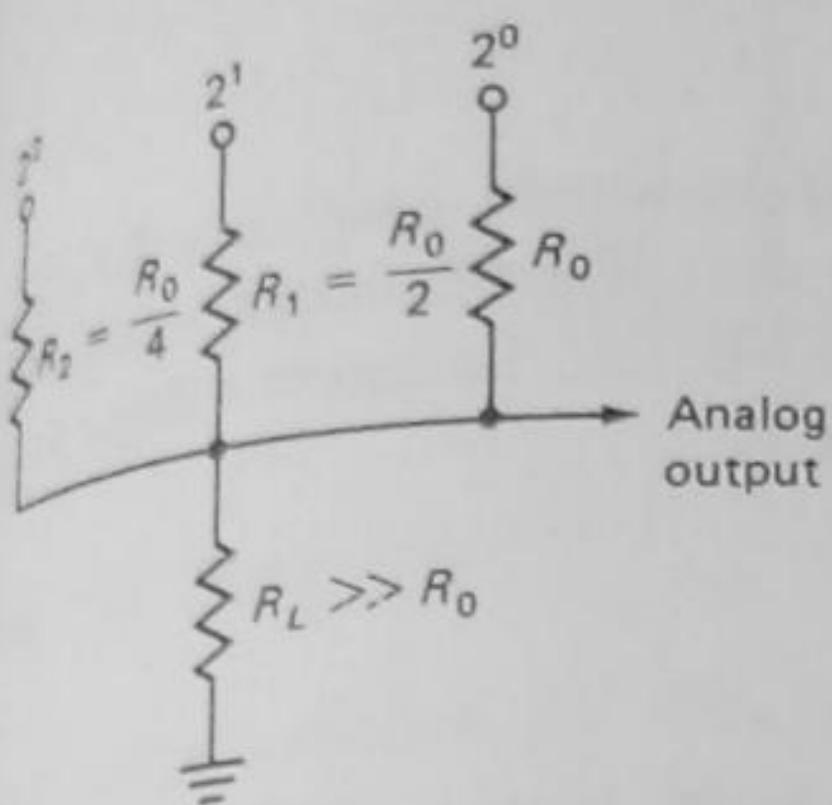


Fig. 11-4 Resistive ladder.

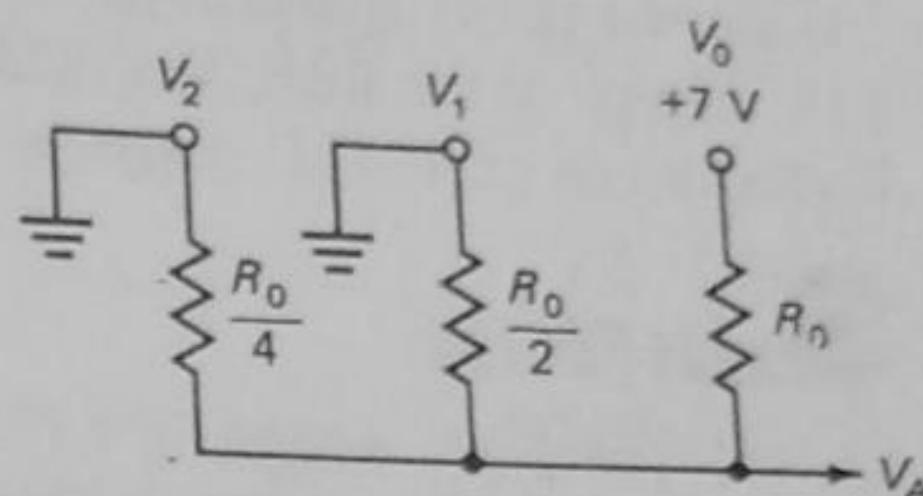


Fig. 11-5

Solution

(a) The maximum output voltage occurs when all the inputs are at +10 V. If all four inputs are at +10 V, the output must also be at +10 V (ignoring the effects of R_L).

(b) For a 4-bit digital number, there are 16 possible states. There are 15 steps between these 16 states, and the LSB must be equal to $\frac{1}{15}$ of the full-scale output voltage. Therefore, the change in output voltage due to the LSB is $+10 \times \frac{1}{15} = +\frac{2}{3}$ V.

(c) According to Millman's theorem, the output voltage for a digital input of 1011 is

$$V_A = \frac{\frac{10}{R_0} + \frac{10}{(R_0/2)} + 0/(R_0/4) + 10/(R_0/8)}{\frac{1}{R_0} + \frac{1}{(R_0/2)} + \frac{1}{(R_0/4)} + \frac{1}{(R_0/8)}} \\ = \frac{110}{15} = \frac{22}{3} = +7\frac{1}{3} \text{ V}$$

To summarize, a resistive divider can be built to change a digital voltage into an equivalent analog voltage. The following criteria can be applied to this divider:

1. There must be one input resistor for each digital bit.
2. Beginning with the LSB, each following resistor value is one-half the size of the previous resistor.
3. The full-scale output voltage is equal to the positive voltage of the digital input signal. (The divider would work equally well with input voltages of 0 and -V.)
4. The LSB has a weight of $1/(2^n - 1)$, where n is the number of input bits.
5. The change in output voltage due to a change in the LSB is equal to $V/(2^n - 1)$, where V is the digital input voltage level.
6. The output voltage V_A can be found for any digital input signal by using the following modified form of Millman's theorem:

$$V_A = \frac{V_0 2^0 + V_1 2^1 + V_2 2^2 + V_3 2^3 + \cdots + V_{n-1} 2^{n-1}}{2^n - 1} \quad (11-1)$$

where $V_0, V_1, V_2, V_3, \dots, V_{n-1}$ are the digital input voltage levels (0 or V) and n is the number of input bits.

ladder

binary ladder

Example 11-3

For a 5-bit resistive divider, determine the following: (a) the weight assigned to the LSB; (b) the weight assigned to the second and third LSB; (c) the change in output voltage due to a change in the LSB, the second LSB, and the third LSB; (d) the output voltage for a digital input of 10101. Assume $0 = 0 \text{ V}$ and $1 = +10 \text{ V}$.

Solution

(a) The LSB weight is $1/(2^5 - 1) = 1/31$.

(b) The second LSB weight is $2/31$, and the third LSB weight is $4/31$.

(c) The LSB causes a change in the output voltage of $10/31 \text{ V}$. The second LSB causes an output voltage change of $20/31 \text{ V}$, and the third LSB causes an output voltage change of $40/31 \text{ V}$.

(d) The output voltage for a digital input of 10101 is

$$V_A = \frac{10 \times 2^0 + 0 \times 2^1 + 10 \times 2^2 + 0 \times 2^3 + 10 \times 2^4}{2^5 - 1}$$

$$= \frac{10(1 + 4 + 16)}{32 - 1} = \frac{210}{31} = +6.77 \text{ V}$$

This resistive divider has two serious drawbacks. The first is the fact that each resistor in the network has a different value. Since these dividers are usually constructed by using precision resistors, the added expense becomes unattractive. Moreover, the resistor used for the MSB is required to handle a much greater current than that used for the LSB resistor. For example, in a 10-bit system, the current through the MSB resistor is approximately 500 times as large as the current through the LSB resistor (see Prob. 11-5). For these reasons, a second type of resistive network, called a *ladder*, has been developed.

SELF-TEST

1. What is the LSB weight of a 6-bit resistive ladder?
2. What is the value of V_A in Example 11-2 if the MSB is 0?

11-2 BINARY LADDERS

The *binary ladder* is a resistive network whose output voltage is a properly weighted sum of the digital inputs. Such a ladder, designed for 4 bits, is shown in Fig. 11-6. It is constructed of resistors that have only two values and thus overcomes one of the objections to the resistive divider previously discussed. The left end of the ladder is terminated in a resistance of $2R$, and we shall assume for the moment that the right end of the ladder (the output) is open-circuited.

Let us now examine the resistive properties of the network, assuming that all the digital inputs are at ground. Beginning at node A, the total resistance looking into the

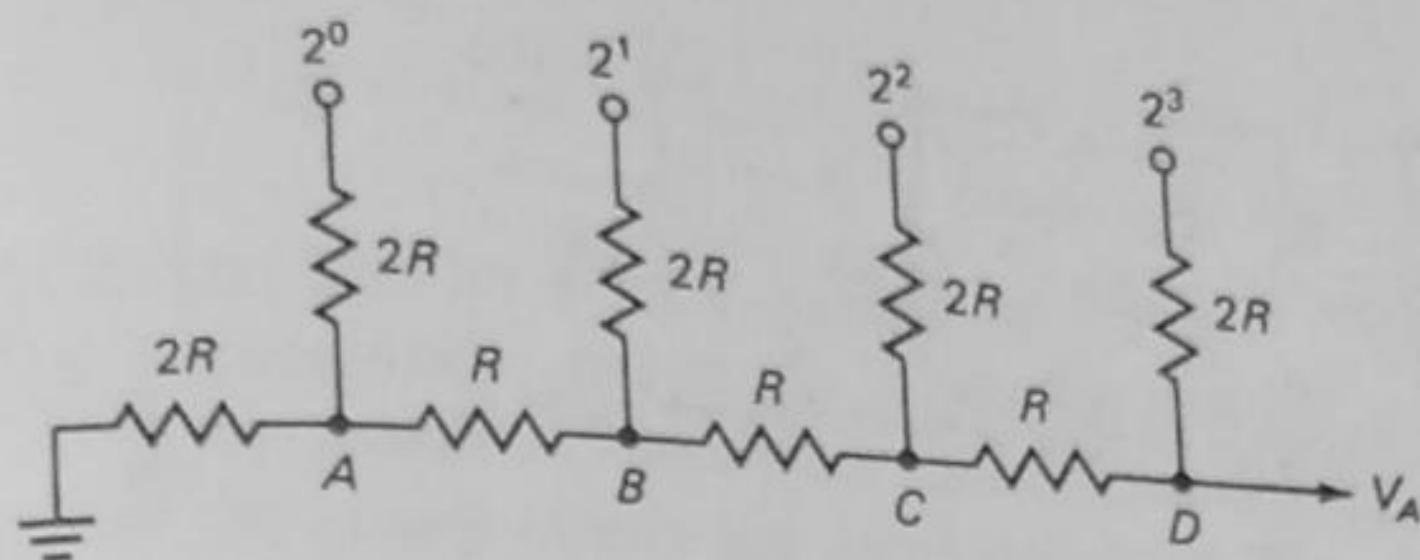


Fig. 11-6 Binary ladder.

terminating resistor is $2R$. The total resistance looking out toward the 2^0 input is also $2R$. These two resistors can be combined to form an equivalent resistor of value R as shown in Fig. 11-7a.

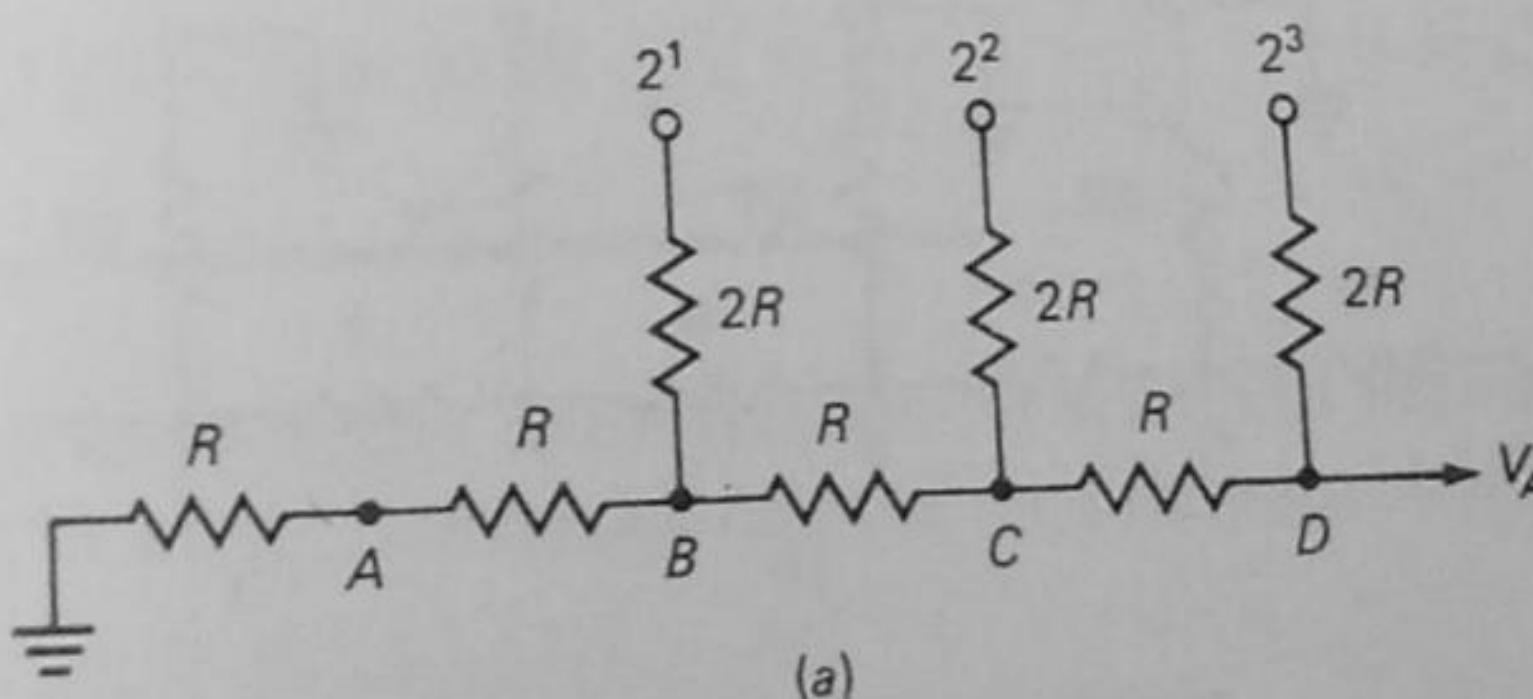
Now, moving to node B , we see that the total resistance looking into the branch toward node A is $2R$, as is the total resistance looking out toward the 2^1 input. These resistors can be combined to simplify the network as shown in Fig. 11-7b.

From Fig. 11-7b, it can be seen that the total resistance looking from node C down the branch toward node B or out the branch toward the 2^2 input is still $2R$. The circuit in Fig. 11-7b can then be reduced to the equivalent as shown in Fig. 11-7c.

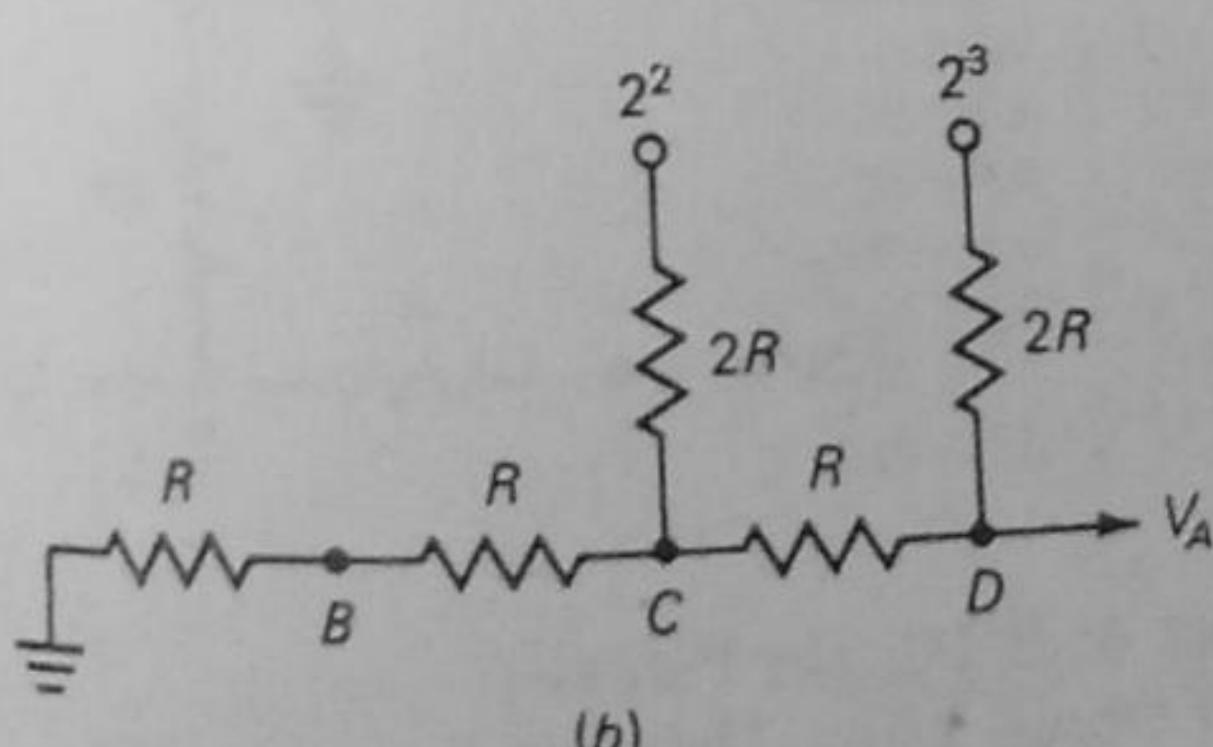
From this equivalent circuit, it is clear that the resistance looking back toward node C is $2R$, as is the resistance looking out toward the 2^3 input.

From the preceding discussion, we can conclude that the total resistance looking from any node back toward the terminating resistor or out toward the digital input is $2R$. Notice that this is true regardless of whether the digital inputs are at ground or $+V$. The justification for this statement is the fact that the internal impedance of an ideal voltage source is $0\ \Omega$, and we are assuming that the digital inputs are ideal voltage sources.

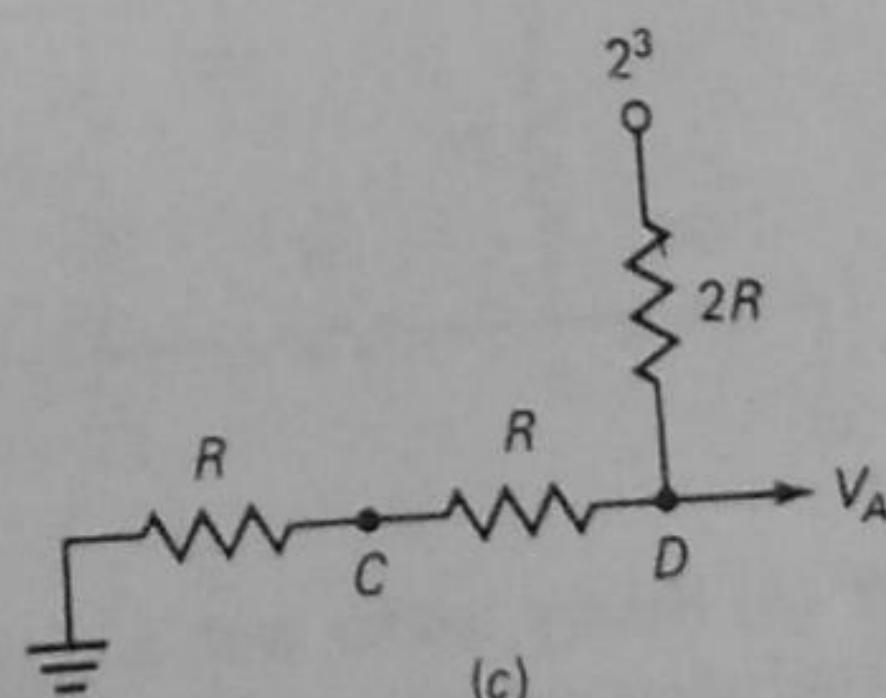
We can use the resistance characteristics of the ladder to determine the output voltages for the various digital inputs. First, assume that the digital input signal is 1000. With



(a)



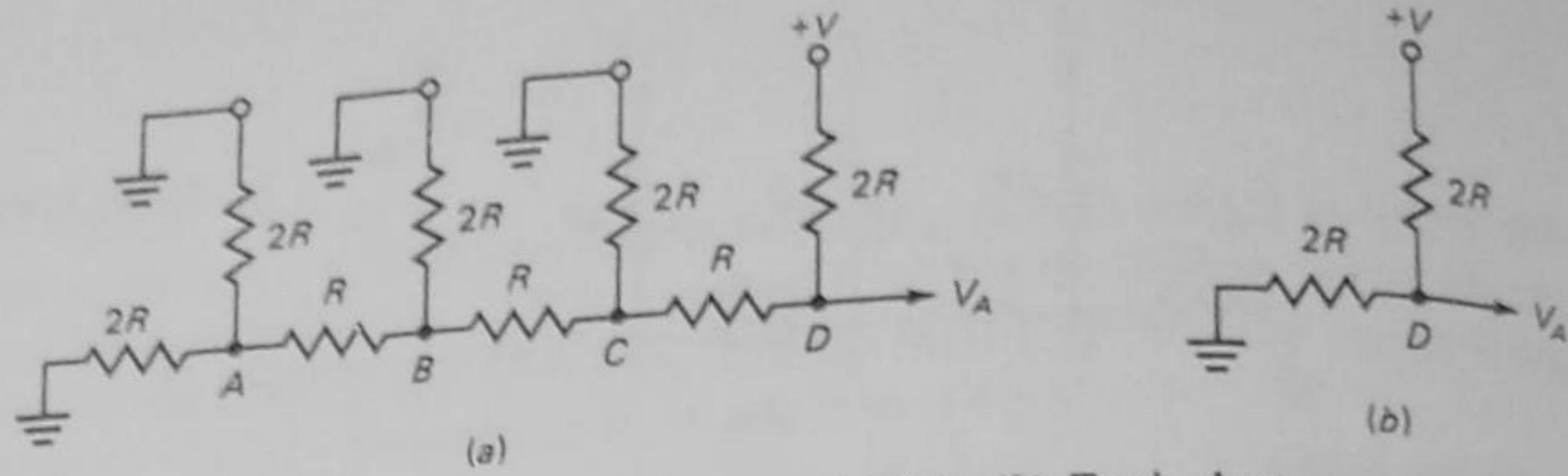
(b)



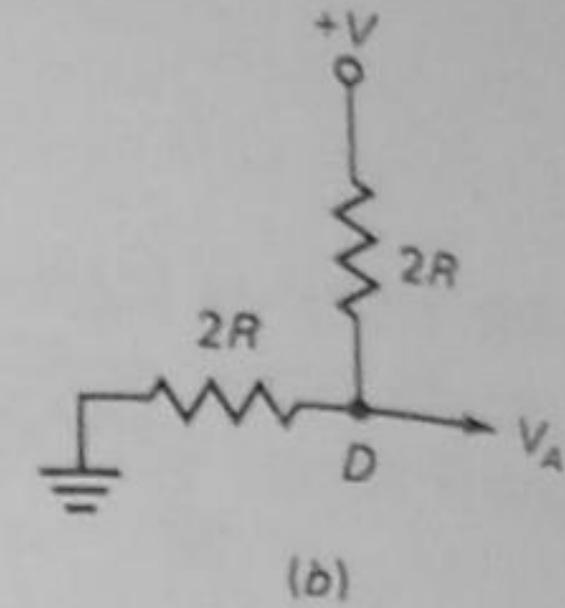
(c)

Fig. 11-7

D/A CONVERSION AND A/D CONVERSION



(a)



(b)

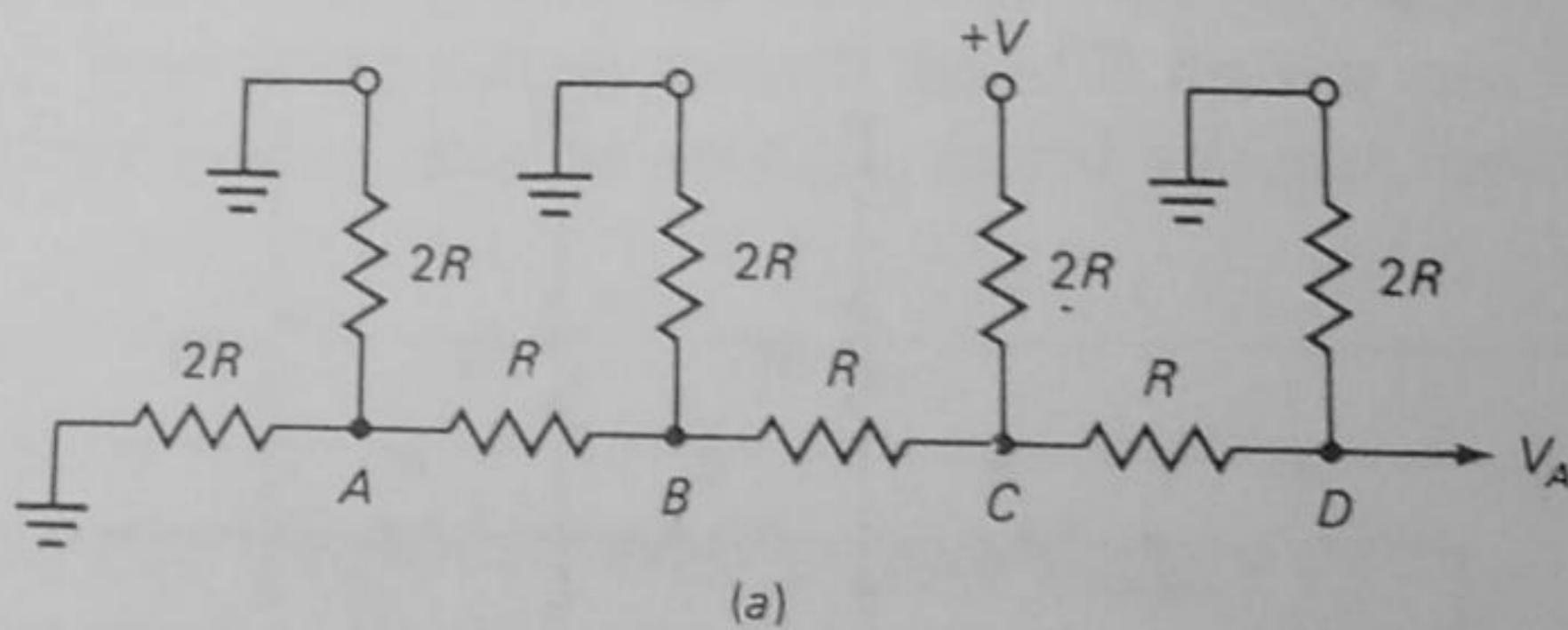
Fig. 11-8 (a) Binary ladder with a digital input of 1000. (b) Equivalent circuit for a digital input of 1000.

this input signal, the binary ladder can be drawn as shown in Fig. 11-8a. Since there are no voltage sources to the left of node D , the entire network to the left of this node can be replaced by a resistance of $2R$ to form the equivalent circuit shown in Fig. 11-8b. From this equivalent circuit, it can be easily seen that the output voltage is

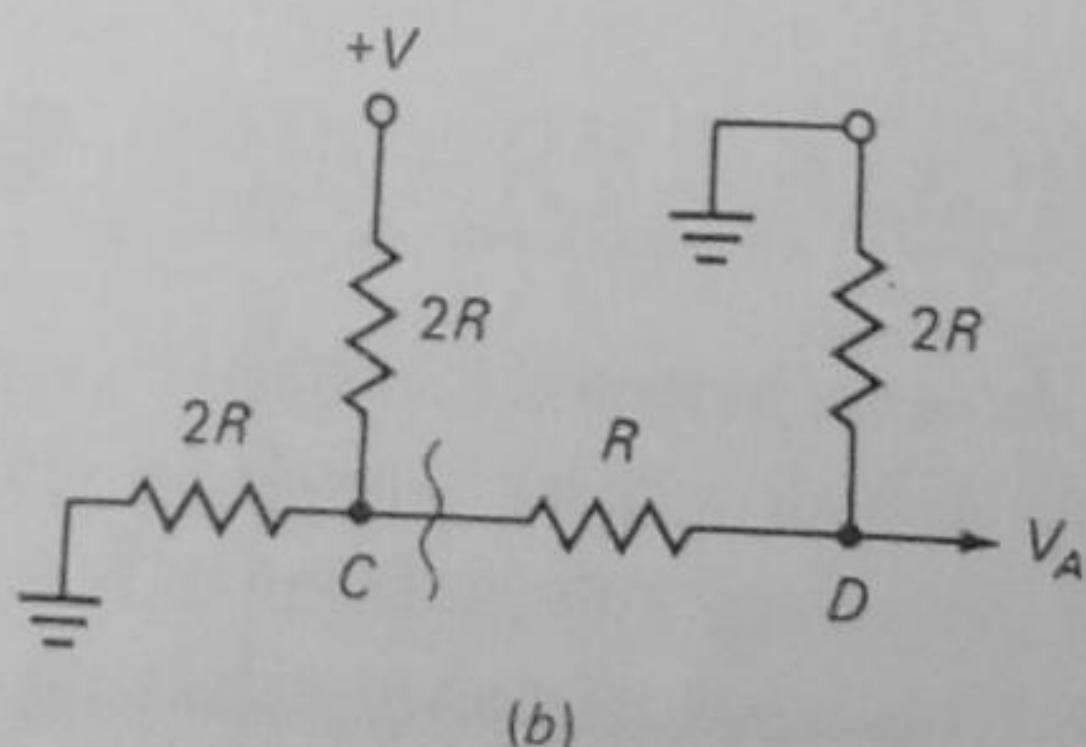
$$V_A = V \times \frac{2R}{2R + 2R} = \frac{+V}{2}$$

Thus a 1 in the MSB position will provide an output voltage of $+V/2$.

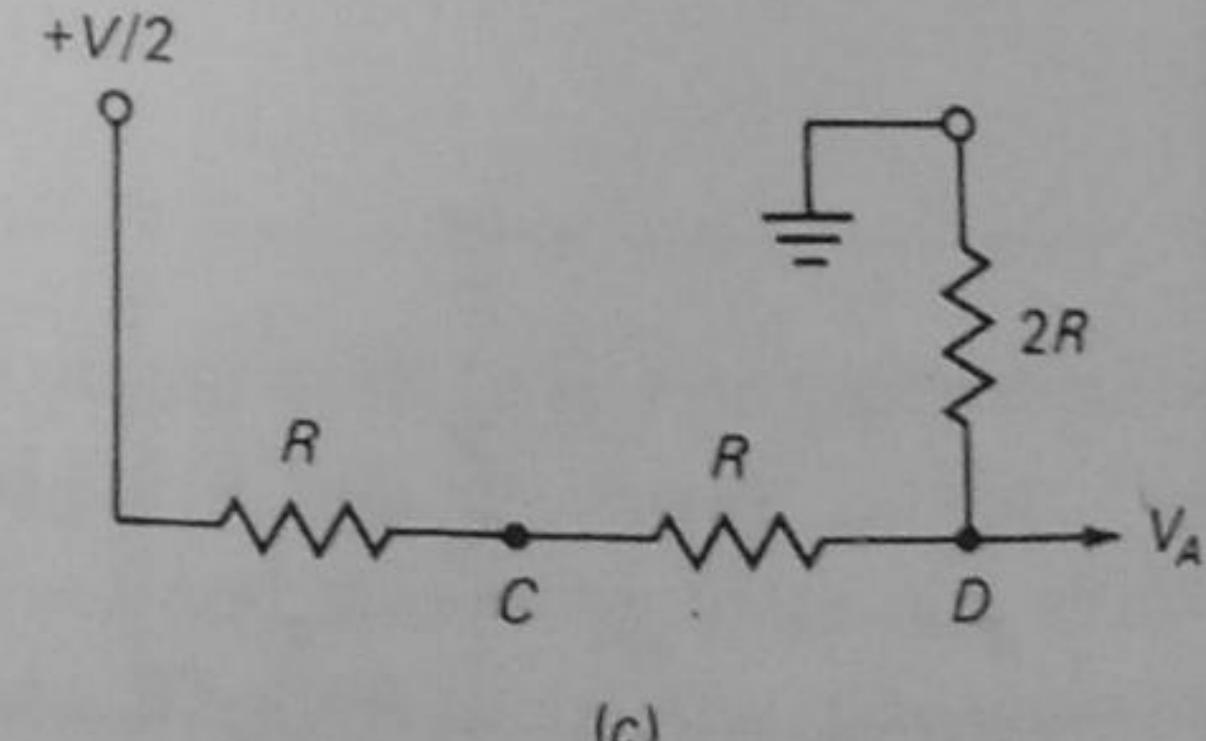
To determine the output voltage due to the second MSB, assume a digital input signal of 0100. This can be represented by the circuit shown in Fig. 11-9a. Since there are no voltage sources to the left of node C , the entire network to the left of this node can be replaced by a resistance of $2R$, as shown in Fig. 11-9b. Let us now replace the network to the left of node C with its Thévenin equivalent by cutting the circuit on the jagged line shown in Fig. 11-9b. The Thévenin equivalent is clearly a resistance R in series with a voltage source $+V/2$. The final equivalent circuit with the Thévenin equivalent included is shown in Fig. 11-9c. From this circuit, the output voltage is clearly



(a)



(b)



(c)

Fig. 11-9 (a) Binary ladder with a digital input of 0100. (b) Partially reduced equivalent circuit. (c) Final equivalent circuit using Thévenin's theorem.

$$V_A = \frac{+V}{2} \times \frac{2R}{R + R + 2R} = \frac{+V}{4}$$

Thus the second MSB provides an output voltage of $+V/4$. This process can be continued, and it can be shown that the third MSB provides an output voltage of $+V/8$, the fourth MSB provides an output voltage of $+V/16$, and so on. The output voltages for the binary ladder are summarized in Fig. 11-10; notice that each digital input is transformed into a properly weighted binary output voltage.

Example 11-4

What are the output voltages caused by each bit in a 5-bit ladder if the input levels are $0 = 0 \text{ V}$ and $1 = +10 \text{ V}$?

Solution

The output voltages can be easily calculated by using Fig. 11-10. They are

$$\text{First MSB } V_A = \frac{V}{2} = \frac{+10}{2} = +5 \text{ V}$$

$$\text{Second MSB } V_A = \frac{V}{4} = \frac{+10}{4} = +2.5 \text{ V}$$

$$\text{Third MSB } V_A = \frac{V}{8} = \frac{+10}{8} = +1.25 \text{ V}$$

$$\text{Fourth MSB } V_A = \frac{V}{16} = \frac{+10}{16} = +0.625 \text{ V}$$

$$\text{LSB = fifth MSB } V_A = \frac{V}{32} = \frac{+10}{32} = +0.3125 \text{ V}$$

Since this ladder is composed of linear resistors, it is a linear network and the principle of superposition can be used. This means that the total output voltage due to a combination

Bit position	Binary weight	Output voltage
MSB	$1/2$	$V/2$
2d MSB	$1/4$	$V/4$
3d MSB	$1/8$	$V/8$
4th MSB	$1/16$	$V/16$
5th MSB	$1/32$	$V/32$
6th MSB	$1/64$	$V/64$
7th MSB	$1/128$	$V/128$
:	:	:
:	:	:
N th MSB	$1/2^N$	$V/2^N$

Fig. 11-10 Binary ladder output voltages.

of input digital levels can be found by simply taking the sum of the output levels caused by each digital input individually.

In equation form, the output voltage is given by

$$V_A = \frac{V}{2} + \frac{V}{4} + \frac{V}{8} + \frac{V}{16} + \cdots + \frac{V}{2^n} \quad (11-2)$$

where n is the total number of bits at the input.

This equation can be simplified somewhat by factoring and collecting terms. The output voltage can then be given in the form

$$V_A = \frac{V_0 2^0 + V_1 2^1 + V_2 2^2 + V_3 2^3 + \cdots + V_{n-1} 2^{n-1}}{2^n} \quad (11-3)$$

where $V_0, V_1, V_2, V_3, \dots, V_{n-1}$ are the digital input voltage levels. Equation (11-3) can be used to find the output voltage from the ladder for any digital input signal.

Example 11-5

Find the output voltage from a 5-bit ladder that has a digital input of 11010. Assume that 0 = 0 V and 1 = +10 V.

Solution

By Eq. (11-3):

$$\begin{aligned} V_A &= \frac{0 \times 2^0 + 10 \times 2^1 + 0 \times 2^2 + 10 \times 2^3 + 10 \times 2^4}{2^5} \\ &= \frac{10(2 + 8 + 16)}{32} = \frac{10 \times 26}{32} = +8.125 \text{ V} \end{aligned}$$

This solution can be checked by adding the individual bit contributions calculated in Example 11-4.

Notice that Eq. (11-3) is very similar to Eq. (11-1), which was developed for the resistive divider. They are, in fact, identical with the exception of the denominators. This is a subtle but very important difference. Recall that the full-scale voltage for the resistive divider is equal to the voltage level of the digital input 1. On the other hand, examination of Eq. (11-2) reveals that the full-scale voltage for the ladder is given by

$$V_A = V \left(\frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \frac{1}{16} + \cdots + \frac{1}{2^n} \right)$$

The terms inside the brackets form a geometric series whose sum approaches 1, given a sufficient number of terms. However, it never quite reaches 1. Therefore, the full-scale output voltage of the ladder approaches V in the limit, but never quite reaches it.

Example 11-6

What is the full-scale output voltage of the 5-bit ladder in Example 11-4?

Solution

The full-scale voltage is simply the sum of the individual bit voltages. Thus

$$V = 5 + 2.5 + 1.25 + 0.625 + 0.3125 = +9.6875 \text{ V}$$

To keep the ladder in perfect balance and to maintain symmetry, the output of the ladder should be terminated in a resistance of $2R$. This will result in a lowering of the output voltage, but if the $2R$ load is maintained constant, the output voltages will still be a properly weighted sum of the binary input bits. If the load is varied, the output voltage will not be a properly weighted sum, and care must be exercised to ensure that the load resistance is constant.

Terminating the output of the ladder with a load of $2R$ also ensures that the input resistance to the ladder seen by each of the digital voltage sources is constant. With the ladder balanced in this manner, the resistance looking into any branch from any node has a value of $2R$. Thus the input resistance seen by any input digital source is $3R$. This is a definite advantage over the resistive divider, since the digital voltage sources can now all be designed for the same load.

Example 11-7

Suppose that the value of R for the 5-bit ladder described in Example 11-4 is 1000Ω . Determine the current that each input digital voltage source must be capable of supplying. Also determine the full-scale output voltage, assuming that the ladder is terminated with a load resistance of 2000Ω .

Solution

The input resistance into the ladder seen by each of the digital sources is $3R = 3000 \Omega$. Thus, for a voltage level of $+10 \text{ V}$, each source must be capable of supplying $I = 10/(3 \times 10^3) = 3\frac{1}{3} \text{ mA}$ (without the $2R$ load resistor, the resistance looking into the MSB terminal is actually $4R$). The no-load output voltage of the ladder has already been determined in Example 11-6. This open-circuit output voltage along with the open-circuit output resistance can be used to form a Thévenin equivalent circuit for the output of the ladder. The resistance looking back into the ladder is clearly $R = 1000 \Omega$. Thus the Thévenin equivalent is as shown in Fig. 11-11 on the next page. From this figure, the output voltage is

$$V_A = +9.6875 \times \frac{2R}{2R + R} = +6.4583 \text{ V}$$

The operational amplifier (OA) shown in Fig. 11-12a on the next page is connected as a unity-gain noninverting amplifier. It has a very high input impedance, and the output voltage is equal to the input voltage. It is thus a good buffer amplifier for connection to the output of a resistive ladder. It will not load down the ladder and thus will not disturb the ladder output voltage V_A ; V_A will then appear at the output of the OA.

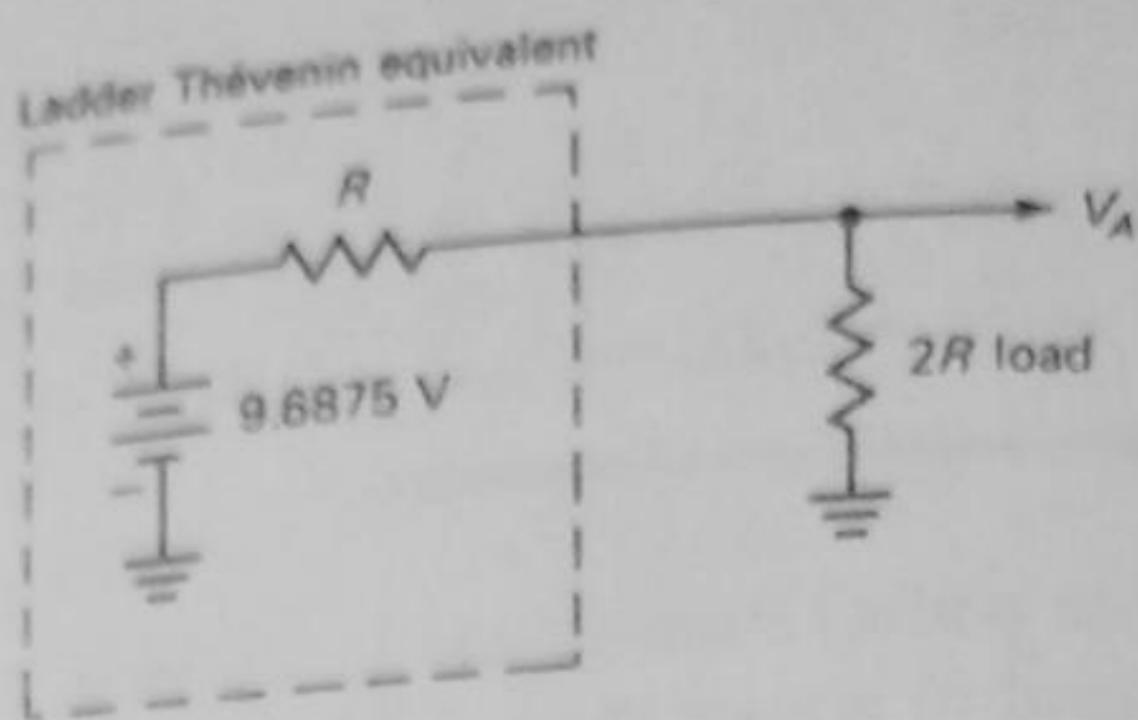
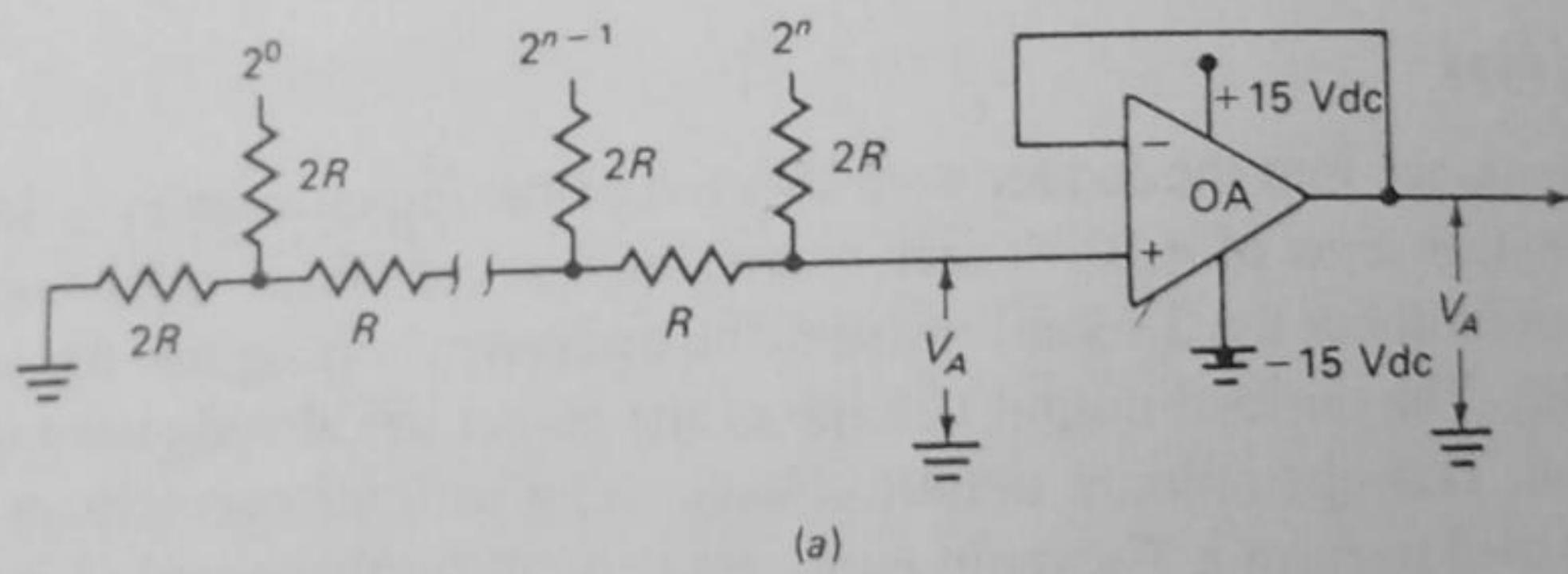


Fig. 11-11 Example 11-7.

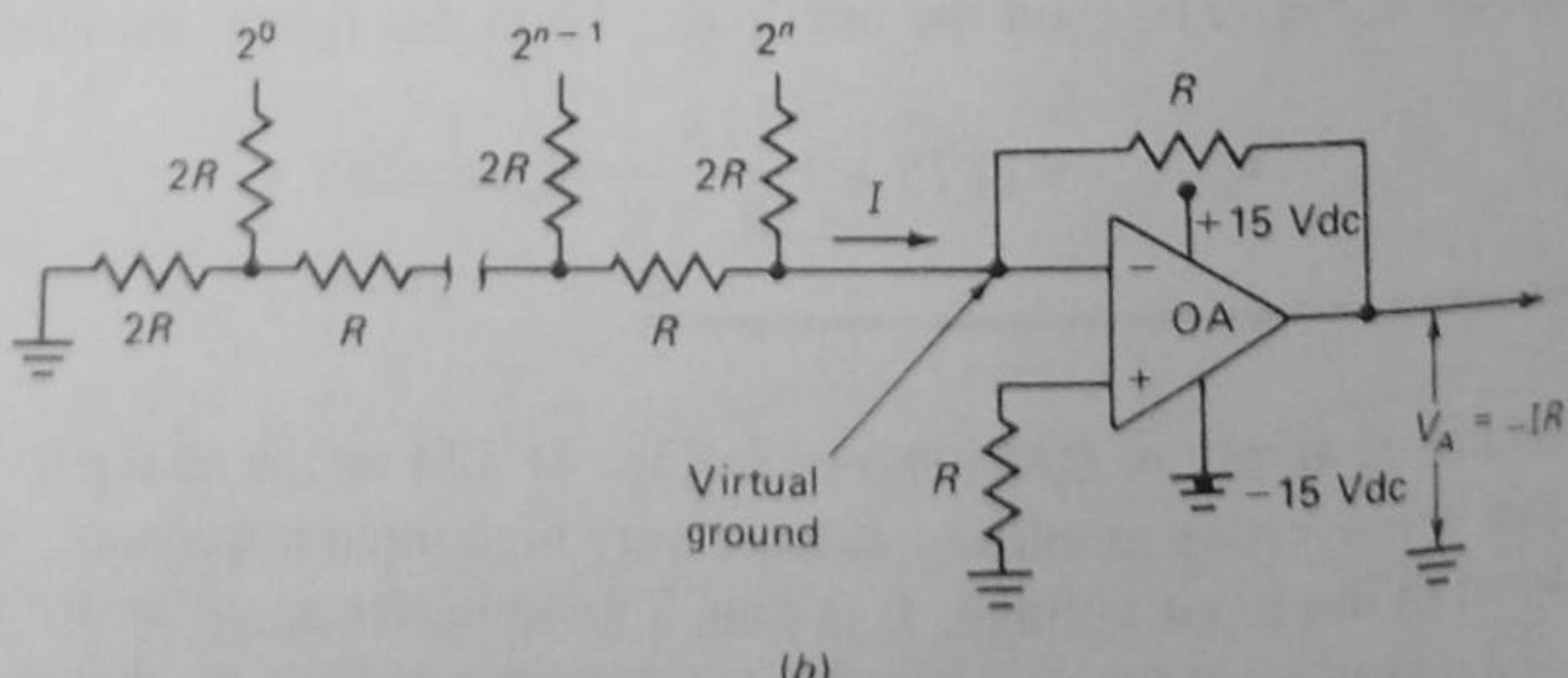
Connecting an OA with a feedback resistor R as shown in Fig. 11-12b results in an amplifier that acts as an inverting current-to-voltage amplifier. That is, the output voltage V_A is equal to the negative of the input current I multiplied by R . The input impedance of this amplifier is essentially 0Ω ; thus, when it is connected to an R - $2R$ ladder, the connecting point is virtually at ground potential. In this configuration, the R - $2R$ ladder will produce a current output I that is a binary weighted sum of the input digital levels. For instance, the MSB produces a current of $V/2R$. The second MSB produces a current of $V/4R$, and so on. But the OA multiplies these currents by $-R$, and thus V_A is

$$V_A = (-R)\left(\frac{V}{2R} + \frac{V}{4R} + \dots\right) = -\frac{V}{2} - \frac{V}{4} - \dots$$

This is exactly the same expression given in Eqs. (11-2) and (11-3) except for the sign. Thus the D/A converter in Fig. 11-12a and b will provide the same output voltage.



(a)



(b)

Fig. 11-12

except for sign. In Fig. 11-12a, the $R-2R$ ladder and OA are said to operate in a voltage mode, while the connection in Fig. 11-12b is said to operate in a current mode.

SELF-TEST

3. If the ladder in Example 11-4 is increased to 6 bits, what is the output voltage due to the sixth bit alone?
4. If the ladder in Example 11-4 is increased to 6 bits, what is its full-scale output voltage?

11.3 D/A CONVERTERS

Either the resistive divider or the ladder can be used as the basis for a digital-to-analog (D/A) converter. It is in the resistive network that the actual translation from a digital signal to an analog voltage takes place. There is, however, the need for additional circuitry to complete the design of the D/A converter.

As an integral part of the D/A converter there must be a register that can be used to store the digital information. This register could be any one of the many types discussed in previous chapters. The simplest register is formed by use of *RS* flip-flops, with one flip-flop per bit. There must also be level amplifiers between the register and the resistive network to ensure that the digital signals presented to the network are all of the same level and are constant. Finally, there must be some form of gating on the input of the register such that the flip-flops can be set with the proper information from the digital system. A complete D/A converter in block-diagram form is shown in Fig. 11-13a on the next page.

Let us expand on the block diagram shown in this Fig. 11-13a by drawing the complete schematic for a 4-bit D/A converter as shown in Fig. 11-13b. You will recognize that the resistor network used is of the ladder type.

The level amplifiers each have two inputs: one input is the +10 V from the precision voltage source, and the other is from a flip-flop. The amplifiers work in such a way that when the input from a flip-flop is high, the output of the amplifier is at +10 V. When the input from the flip-flop is low, the output is 0 V.

The four flip-flops form the register necessary for storing the digital information. The flip-flop on the right represents the MSB, and the flip-flop on the left represents the LSB. Each flip-flop is a simple *RS* latch and requires a positive level at the *R* or *S* input to reset or set it. The gating scheme for entering information into the register is straightforward and should be easy to understand. With this particular gating scheme, the flip-flops need not be reset (or set) each time new information is entered. When the READ IN line goes high, only one of the two gate outputs connected to each flip-flop is high, and the flip-flop is set or reset accordingly. Thus data are entered into the register each time the READ IN (strobe) pulse occurs. *D* flip-flops could be used in place of the *RS* flip-flops.

MULTIPLE SIGNALS

Quite often it is necessary to decode more than one signal—for example, the *X* and *Y* coordinates for a plotting board. In this event, there are two ways in which to decode the signals.

D/A CONVERSION AND A/D CONVERSION

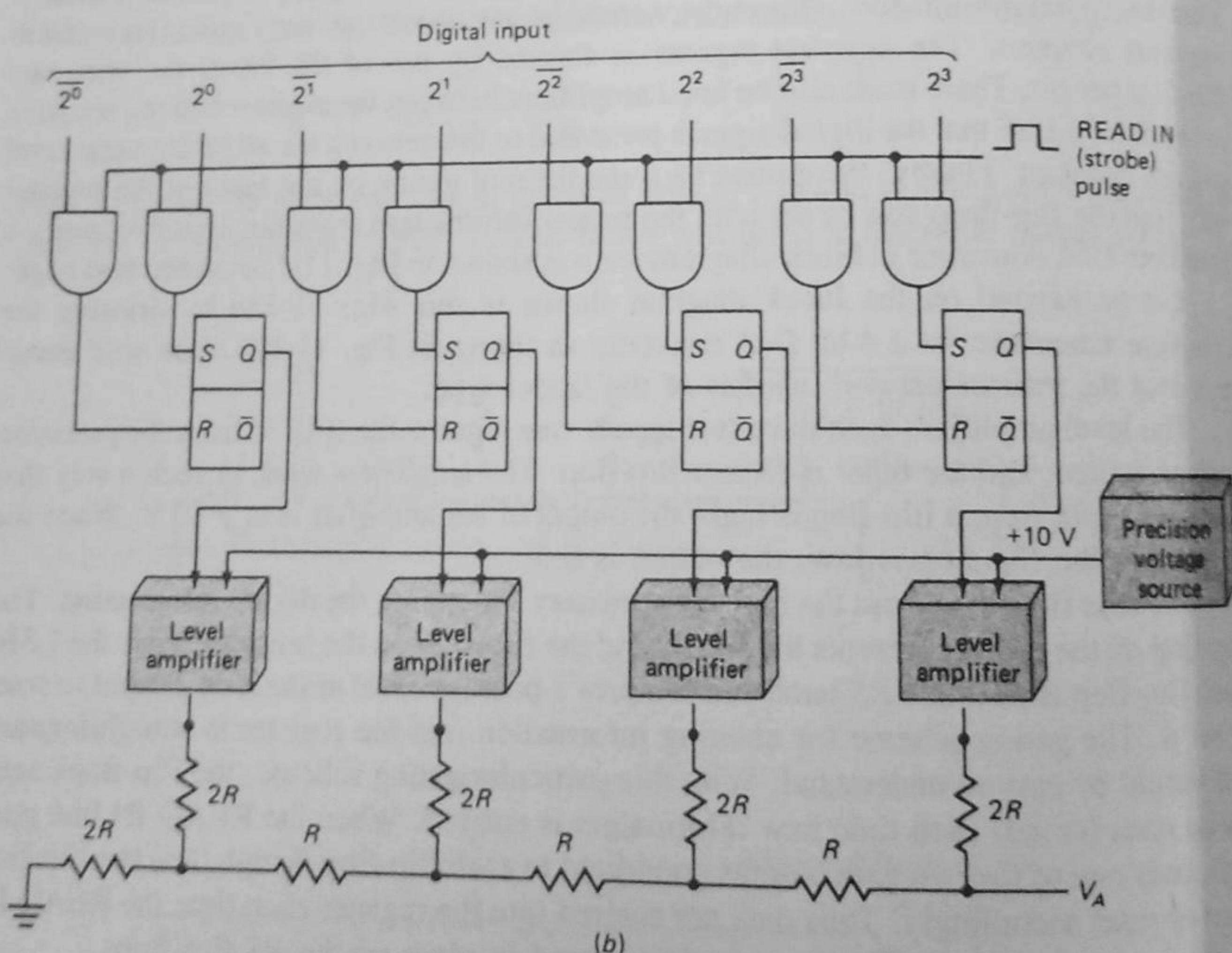
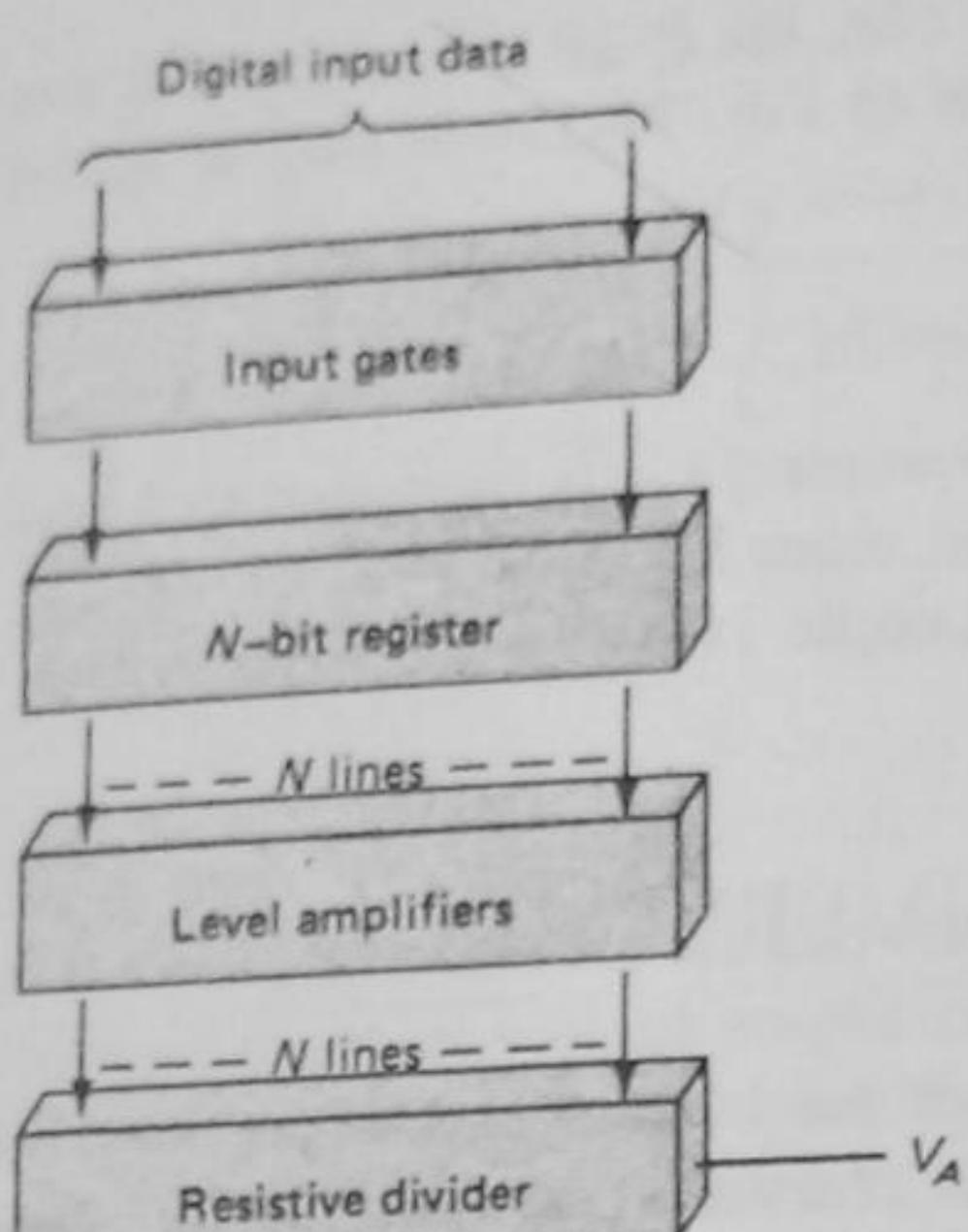
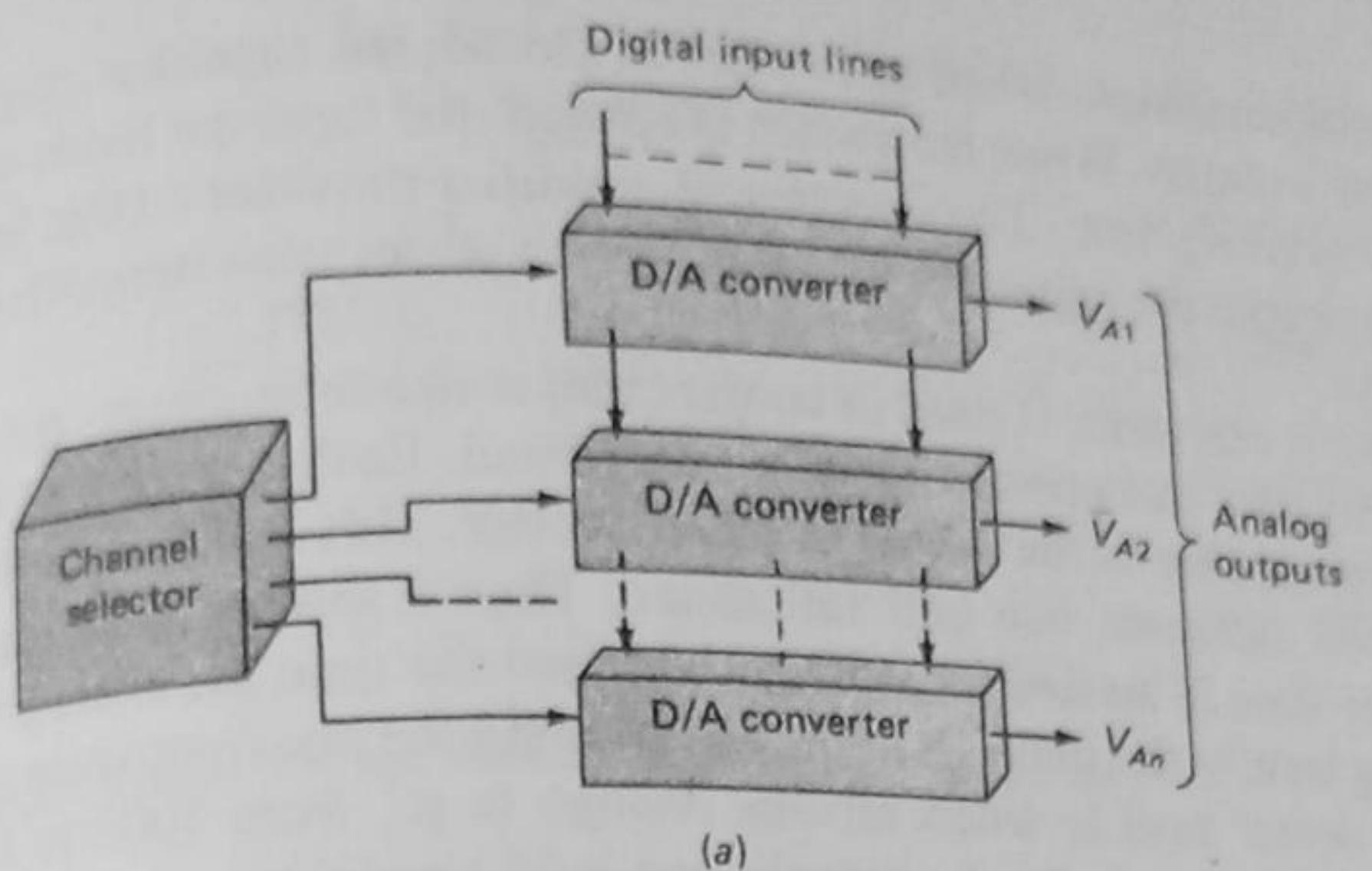
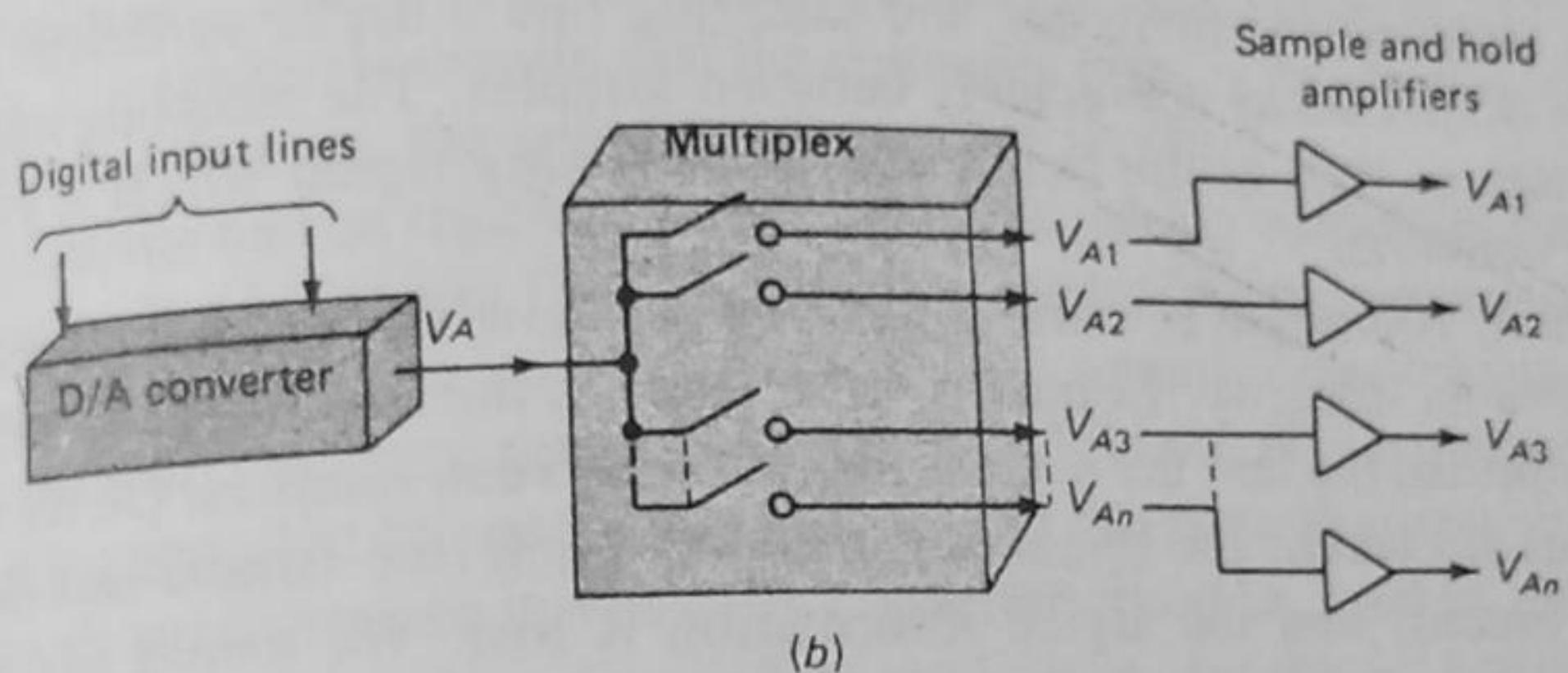


Fig. 11-13 4-bit D/A converter.



(a)



(b)

Fig. 11-14 Decoding a number of signals. (a) Channel selection method.
 (b) Multiplex method.

The first and most obvious method is simply to use one D/A converter for each signal. This method, shown in Fig. 11-14a, has the advantage that each signal to be decoded is held in its register and the analog output voltage is then held fixed. The digital input lines are connected in parallel to each converter. The proper converter is then selected for decoding by the select lines.

The second method involves the use of only one D/A converter and switching its output. This is called *multiplexing*, and such a system is shown in Fig. 11-14b. The disadvantage here is that the analog output signal must be held between sampling periods, and the outputs must therefore be equipped with sample-and-hold amplifiers.

An OA connected as in Fig. 11-15a is a unity-gain noninverting voltage amplifier—that is, $V_o = V_i$. Two such OAs are used with a capacitor in Fig. 11-15b to form a

multiplexing

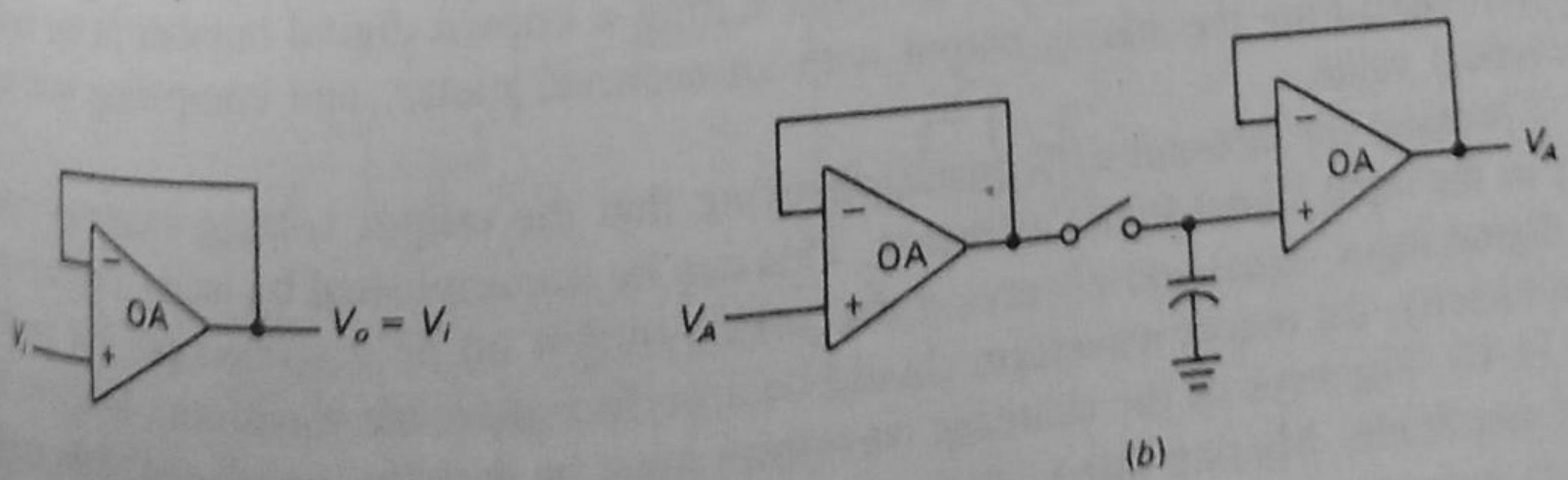


Fig. 11-15 (a) Unity gain amplifier. (b) Sample-and-hold circuit.

steady-state accuracy test sample-and-hold amplifier. When the switch is closed, the capacitor charges to the D/A converter output voltage. When the switch is opened, the capacitor holds the voltage level until the next sampling time. The operational amplifier provides a large input impedance so as not to discharge the capacitor appreciably and at the same time offers gain to drive external circuits.

When the D/A converter is used in conjunction with a multiplexer, the maximum rate at which the converter can operate must be considered. Each time data is shifted into the register, transients appear at the output of the converter. This is due mainly to the fact that each flip-flop has different rise and fall times. Thus a settling time must be allowed between the time data is shifted into the register and the time the analog voltage is read out. This settling time is the main factor in determining the maximum rate of multiplexing the output. The worst case is when all bits change (e.g., from 1000 to 0111).

Naturally, the capacitors on the sample-and-hold amplifiers are not capable of holding a voltage indefinitely; therefore, the sampling rate must be sufficient to ensure that these voltages do not decay appreciably between samples. The sampling rate is a function of the capacitors as well as the frequency of the analog signal which is expected at the output of the converter.

At this point, you might be curious to know just how fast a signal must be sampled in order to preserve its integrity. Common sense leads to the conclusion that the more often the signal is sampled, the less the sample degrades between samples. On the other hand, if too few samples are taken, the signal degrades too much (the sample-and-hold capacitors discharge too much), and the signal information is lost. We would like to reduce the sampling rate to the minimum necessary to extract all the necessary information from the signal. The solution to this problem involves more than we have time for here, but the results are easy enough to apply.

First, if the signal in question is sinusoidal, it is necessary to sample at only *twice* the signal frequency. For instance, if the signal is a 5-kHz sine wave, it must be sampled at a rate greater than or equal to 10 kHz. In other words, a sample must be taken every $\frac{1}{10000} \text{ s} = 100 \mu\text{s}$. What if the waveform is not sinusoidal? Any waveform that is periodic can be represented by a summation of sine and cosine terms, with each succeeding term having a higher frequency. In this case, it will be necessary to sample at a rate equal to twice the highest frequency of interest.

D/A CONVERTER TESTING

Two simple but important tests that can be performed to check the proper operation of the D/A converter are the *steady-state accuracy test* and the *monotonicity test*.

The steady-state accuracy test involves setting a known digital number in the input register, measuring the analog output with an accurate meter, and comparing with the theoretical value.

Checking for monotonicity means checking that the output voltage increases regularly as the input digital signal increases. This can be accomplished by using a counter as the digital input signal and observing the analog output on an oscilloscope. For proper monotonicity, the output waveform should be a perfect staircase waveform, as shown in Fig. 11-16. The steps on the staircase waveform must be equally spaced and of the exact same amplitude. Missing steps, steps of different amplitude, or steps in a downward fashion indicate malfunctions.

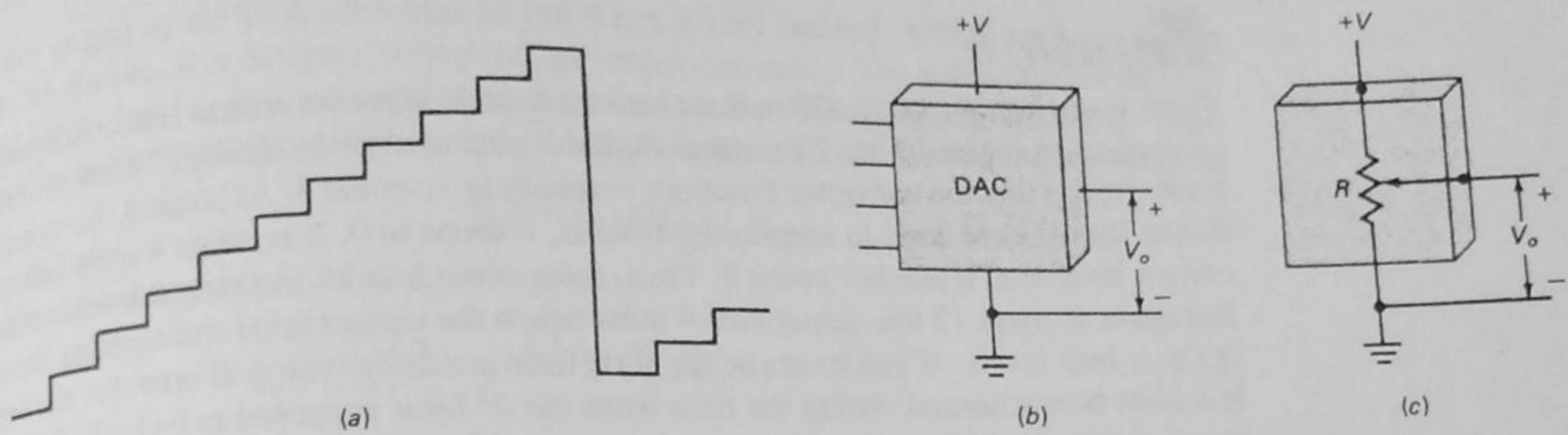


Fig. 11-16 Correct output voltage waveform for monotonicity test.

The monotonicity test does not check the system for accuracy, but if the system passes the test, it is relatively certain that the converter error is less than 1 LSB. Converter accuracy and resolution are the subjects of the next section.

A D/A converter can be regarded as a logic block having numerous digital inputs and a single analog output as seen in Fig. 11-16b. It is interesting to compare this logic block with the potentiometer shown in Fig. 11-16c. The analog output voltage of the D/A converter is controlled by the digital input signals, while the analog output voltage of the potentiometer is controlled by mechanical rotation of the potentiometer shaft. Considered in this fashion, it is easy to see how a D/A converter could be used to generate a voltage waveform (sawtooth, triangular, sinusoidal, etc.). It is, in effect, a digitally controlled voltage generator!

Example 11-8

Suppose that in the course of a monotonicity check on the 4-bit converter in Fig. 11-13, the waveform shown in Fig. 11-17 is observed. What is the probable malfunction in the converter?

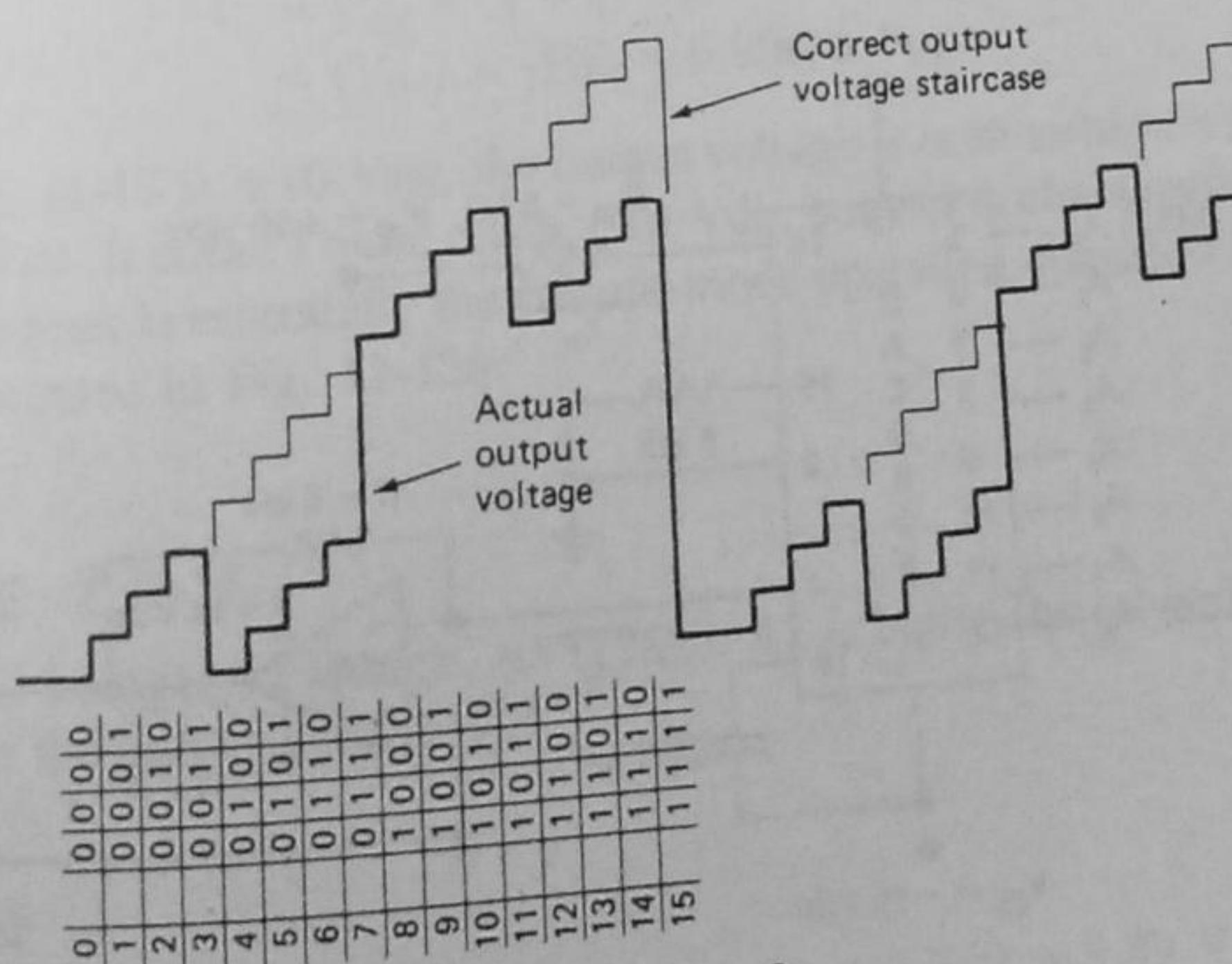


Fig. 11-17 Irregular output voltage for Example 11-8.

Solution

There is obviously some malfunction since the actual output waveform is not continuously increasing as it should be. The actual digital inputs are shown directly below the waveform. Notice that the converter functions correctly up to count 3. At count 4, however, the output should be 4 units in amplitude. Instead, it drops to 0. It remains 4 units below the correct level until it reaches count 8. Then, from count 8 to 11, the output level is correct. But again at count 12 the output falls 4 units below the correct level and remains there for the next four levels. If you examine the waveform carefully, you will note that the output is 4 units below normal during the time when the 2^2 bit is supposed to be high. This then suggests that the 2^2 bit is being dropped (i.e., the 2^2 input to the ladder is not being held high). This means that the 2^2 -level amplifier is malfunctioning or the 2^2 AND gate is not operating properly. In any case, the monotonicity check has clearly shown that the second MSB is not being used and that the converter is not operating properly.

AVAILABLE D/A CONVERTERS

D/A converters, as well as sample-and-hold amplifiers, are readily obtainable commercial products. Each unit is constructed in a single package; general-purpose economy units are available with 6-, 8-, 10-, and 12-bit resolution, and high-resolution units with up to 16-bit resolution are available.

An inexpensive and very popular D/A converter is the DAC0808, an 8-bit D/A converter available from National Semiconductor. Motorola manufactures an 8-bit D/A converter, the MC1508/1408. In Fig. 11-18, a DAC0808 is connected to provide a full-scale output voltage of $V_o = +10$ Vdc when all 8 digital inputs are 1s (high). If the 8 digital inputs are all 0s (low), the output voltage will be $V_o = 0$ Vdc. Let's look at this circuit in detail.

First of all, two dc power-supply voltages are required for the DAC0808: $V_{CC} = +5$ Vdc and $V_{EE} = -15$ Vdc. The $0.1\text{-}\mu\text{F}$ capacitor is to prevent unwanted circuit oscillations, and to isolate any variations in V_{EE} . Pin 2 is ground (GND), and pin 15 is also referenced to ground through a resistor.

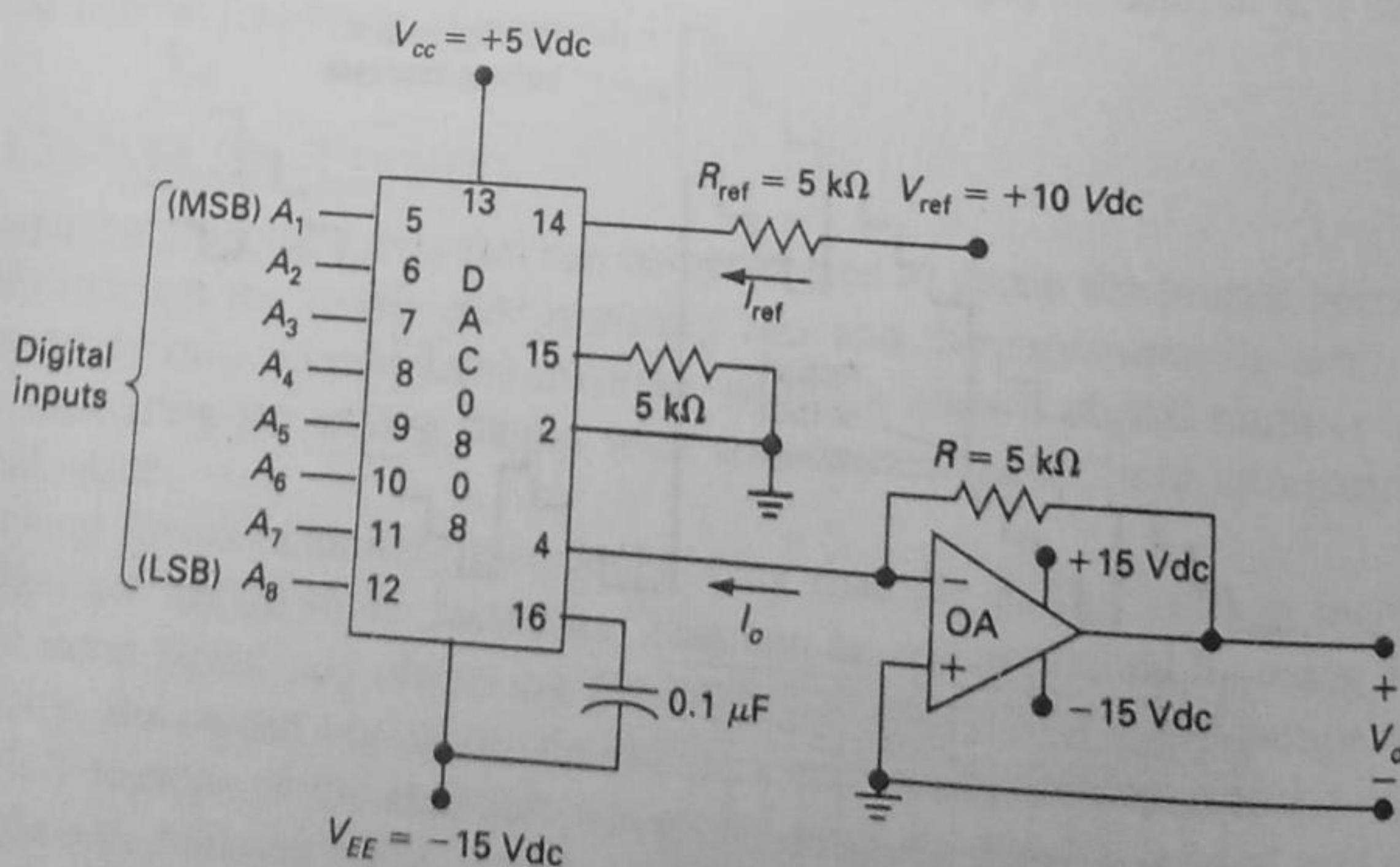


Fig. 11-18

The output of the D/A converter on pin 4 has a very limited voltage range (+0.5 to -0.6 V). Rather, it is designed to provide an output current I_o . The minimum current (all digital inputs low) is 0.0 mA, and the maximum current (all digital inputs high) is I_{ref} . This reference current is established with the resistor at pin 14 and the reference voltage as

$$I_{ref} = V_{ref}/R_{ref} \quad (11-4)$$

The D/A converter output current I_o is given as

$$I_o = I_{ref} \left(\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \dots + \frac{A8}{256} \right) \quad (11-5)$$

where $A1, A2, A3, \dots, A8$ are the digital input levels (1 or 0).

The OA is connected as a current-to-voltage converter, and the output voltage is given as

$$V_o = I_o \times R \quad (11-6)$$

Substituting Eqs. (11-4) and (11-5) into Eq. (11-6),

$$V_o = V_{ref}/R_{ref} \times \left(\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \dots + \frac{A8}{256} \right) \times R \quad (11-7)$$

If we set the OA feedback resistor R equal to R_{ref} , then

$$V_o = V_{ref} \times \left(\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \dots + \frac{A8}{256} \right) \quad (11-8)$$

Let's try out Eq. (11-8). Suppose all digital inputs are 0s (all low). Then

$$\begin{aligned} V_o &= V_{ref} \times \left(\frac{0}{2} + \frac{0}{4} + \frac{0}{8} + \dots + \frac{0}{256} \right) \\ &= V_{ref} \times 0 = 0.0 \text{ Vdc} \end{aligned}$$

Now, suppose all digital inputs are 1s (all high). Then

$$\begin{aligned} V_o &= V_{ref} \times \left(\frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \dots + \frac{1}{256} \right) \\ &= (V_{ref}) \times \left(\frac{255}{256} \right) = 0.996 \times V_{ref} \end{aligned}$$

Since V_{ref} in Fig. 11-18 is +10 Vdc, the output voltage is seen to have a range between 0.0 and +9.96 Vdc. It doesn't quite reach +10 Vdc, but this is characteristic of this type of circuit. This circuit is essentially the current-mode operation discussed in the previous section and illustrated in Fig. 11-12b.

Example 11-9

In Fig. 11-18, $A1$ is high, $A2$ is high, $A5$ is high, $A7$ is high. The other digital inputs are all low. What is the output voltage V_o ?

Solution

$$V_o = 10 \times \left(\frac{1}{2} + \frac{1}{4} + \frac{1}{32} + \frac{1}{128} \right) = 10 \times 0.789 = 7.89 \text{ V}$$

SELF-TEST

5. What is a monotonicity test?
6. What would be the full-scale output voltage in Fig. 11-18 if V_{ref} were changed to +5 Vdc?

11-4 D/A ACCURACY AND RESOLUTION

Two very important aspects of the D/A converter are the resolution and the accuracy of the conversion. There is a definite distinction between the two, and you should clearly understand the differences.

The accuracy of the D/A converter is primarily a function of the accuracy of the precision resistors used in the ladder and the precision of the reference voltage supply used. Accuracy is a measure of how close the actual output voltage is to the theoretical output value.

For example, suppose that the theoretical output voltage for a particular input should be +10 V. An accuracy of 10 percent means that the actual output voltage must be somewhere between +9 and +11 V. Similarly, if the actual output voltage were somewhere between +9.9 and +10.1 V, this would imply an accuracy of 1 percent.

Resolution, on the other hand, defines the smallest increment in voltage that can be discerned. Resolution is primarily a function of the number of bits in the digital input signal; that is, the smallest increment in output voltage is determined by the LSB.

In a 4-bit system using a ladder, for example, the LSB has a weight of $\frac{1}{16}$. This means that the smallest increment in output voltage is $\frac{1}{16}$ of the input voltage. To make the arithmetic easy, let us assume that this 4-bit system has input voltage levels of +16 V. Since the LSB has a weight of $\frac{1}{16}$, a change in the LSB results in a change of 1 V in the output. Thus the output voltage changes in steps (or increments) of 1 V. The output voltage of this converter is then the staircase shown in Fig. 11-16 and ranges from 0 to +15 V in 1-V increments. This converter can be used to represent analog voltages from 0 to +15 V, but it cannot resolve voltages into increments smaller than 1 V. If we desired to produce +4.2 V using this converter, therefore, the actual output voltage would be +4.0 V. Similarly, if we desired a voltage of +7.8 V, the actual output voltage would be +8.0 V. It is clear that this converter is not capable of distinguishing voltages finer than 1 V, which is the resolution of the converter.

If we wanted to represent voltages to a finer resolution, we would have to use a converter with more input bits. As an example, the LSB of a 10-bit converter has a weight of $\frac{1}{1024}$. Thus the smallest incremental change in the output of this converter is approximately $\frac{1}{1024}$ of the full-scale voltage. If this converter has a +10-V full-scale output, the resolution is approximately $+10 \times \frac{1}{1024} = 10 \text{ mV}$. This converter is then capable of representing voltages to within 10 mV.

Example 11-10

What is the resolution of a 9-bit D/A converter which uses a ladder network? What is this resolution expressed as a percent? If the full-scale output voltage of this converter is +5 V, what is the resolution in volts?

Solution

The LSB in a 9-bit system has a weight of $\frac{1}{512}$. Thus this converter has a resolution of 1 part in 512. The resolution expressed as a percentage is $\frac{1}{512} \times 100$ percent ≈ 0.2 percent. The voltage resolution is obtained by multiplying the weight of the LSB by the full-scale output voltage. Thus the resolution in volts is $\frac{1}{512} \times 5 \approx 10$ mV.

analog-to-digital
(A/D) conversion

Example 11-11

How many bits are required at the input of a converter if it is necessary to resolve voltages to 5 mV and the ladder has +10 V full scale?

Solution

The LSB of an 11-bit system has a resolution of $\frac{1}{2048}$. This would provide a resolution at the output of $\frac{1}{2048} \times +10 \approx +5$ mV.

It is important to realize that resolution and accuracy in a system should be compatible. For example, in the 4-bit system previously discussed, the resolution was found to be 1 V. Clearly it would be unjustifiable to construct such a system to an accuracy of 0.1 percent. This would mean that the system would be accurate to 16 mV but would be capable of distinguishing only to the nearest 1 V.

Similarly, it would be wasteful to construct the 11-bit system described in Example 11-11 to an accuracy of only 1 percent. This would mean that the output voltage would be accurate only to 100 mV, whereas it is capable of distinguishing to the nearest 5 mV.

SELF-TEST

7. What is the resolution of the DAC0808 in Fig. 11-18?

11-5 A/D CONVERTER—SIMULTANEOUS CONVERSION

The process of converting an analog voltage into an equivalent digital signal is known as *analog-to-digital (A/D) conversion*. This operation is somewhat more complicated than the converse operation of D/A conversion. A number of different methods have been developed, the simplest of which is probably the simultaneous method.

The simultaneous method of A/D conversion is based on the use of a number of comparator circuits. One such system using three comparator circuits is shown in Fig. 11-19 on the next page. The analog signal to be digitized serves as one of the inputs to each comparator. The second input is a standard reference voltage. The reference voltages used are $+V/4$, $+V/2$, and $+3V/4$. The system is then capable of accepting an analog input voltage between 0 and $+V$.

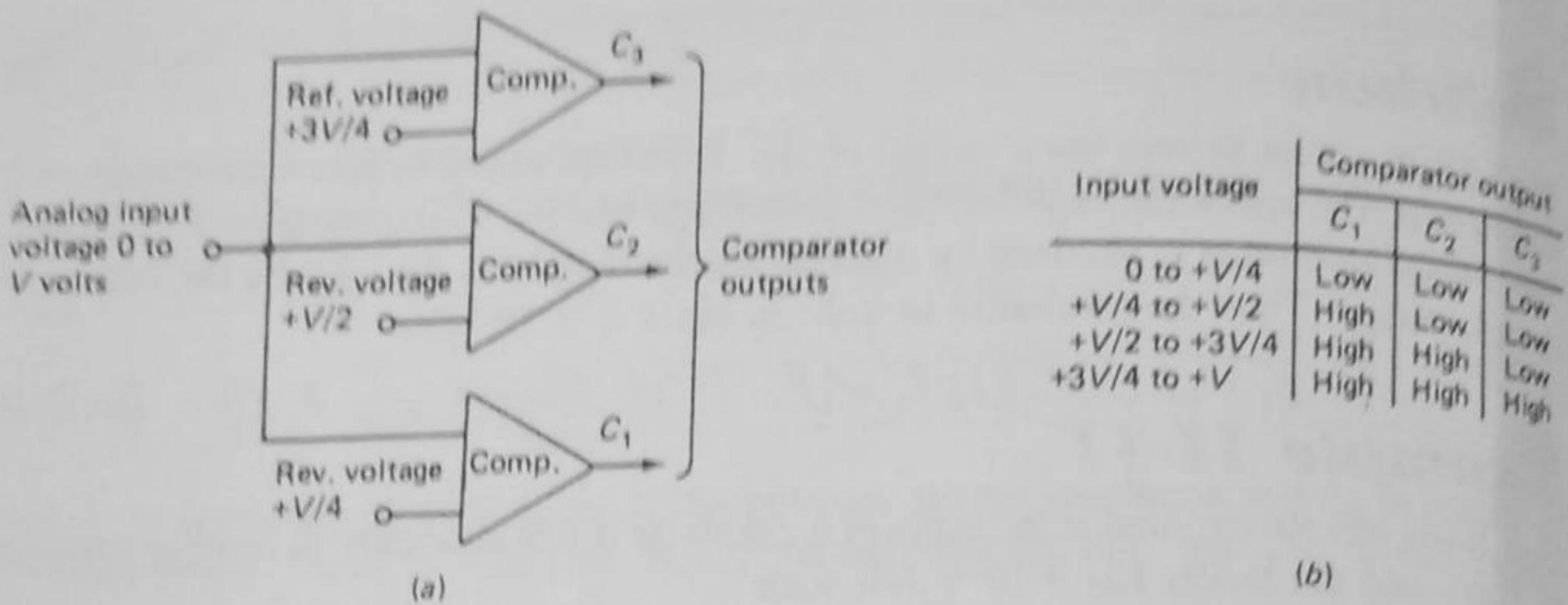


Fig. 11-19 Simultaneous A/D conversion. (a) Logic diagram. (b) Comparator outputs for input voltage ranges.

If the analog input signal exceeds the reference voltage to any comparator, that comparator turns on. (Let's assume that this means that the output of the comparator goes high.) Now, if all the comparators are off, the analog input signal must be between 0 and $+V/4$. If C_1 is high (comparator C_1 is on) and C_2 and C_3 are low, the input must be between $+V/4$ and $+V/2$ V. If C_1 and C_2 are high while C_3 is low, the input must be between $+V/2$ and $+3V/4$. Finally, if all comparator outputs are high, the input signal must be between $+3V/4$ and $+V$. The comparator output levels for the various ranges of input voltages are summarized in Fig. 11-19b.

Examination of Fig. 11-19 reveals that there are four voltage ranges that can be detected by this converter. Four ranges can be effectively discerned by two binary digits (bits). The three comparator outputs can then be fed into a coding network to provide 2 bits which are equivalent to the input analog voltage. The bits of the coding network can then be entered into a flip-flop register for storage. The complete block diagram for such an A/D converter is shown in Fig. 11-20.

In order to gain a clear understanding of the operation of the simultaneous A/D converter, let us investigate the 3-bit converter shown in Fig. 11-21a. Notice that in order to convert the input signal to a digital signal having 3 bits, it is necessary to have seven comparators (this allows a division of the input into eight ranges). For the 2-bit converter,

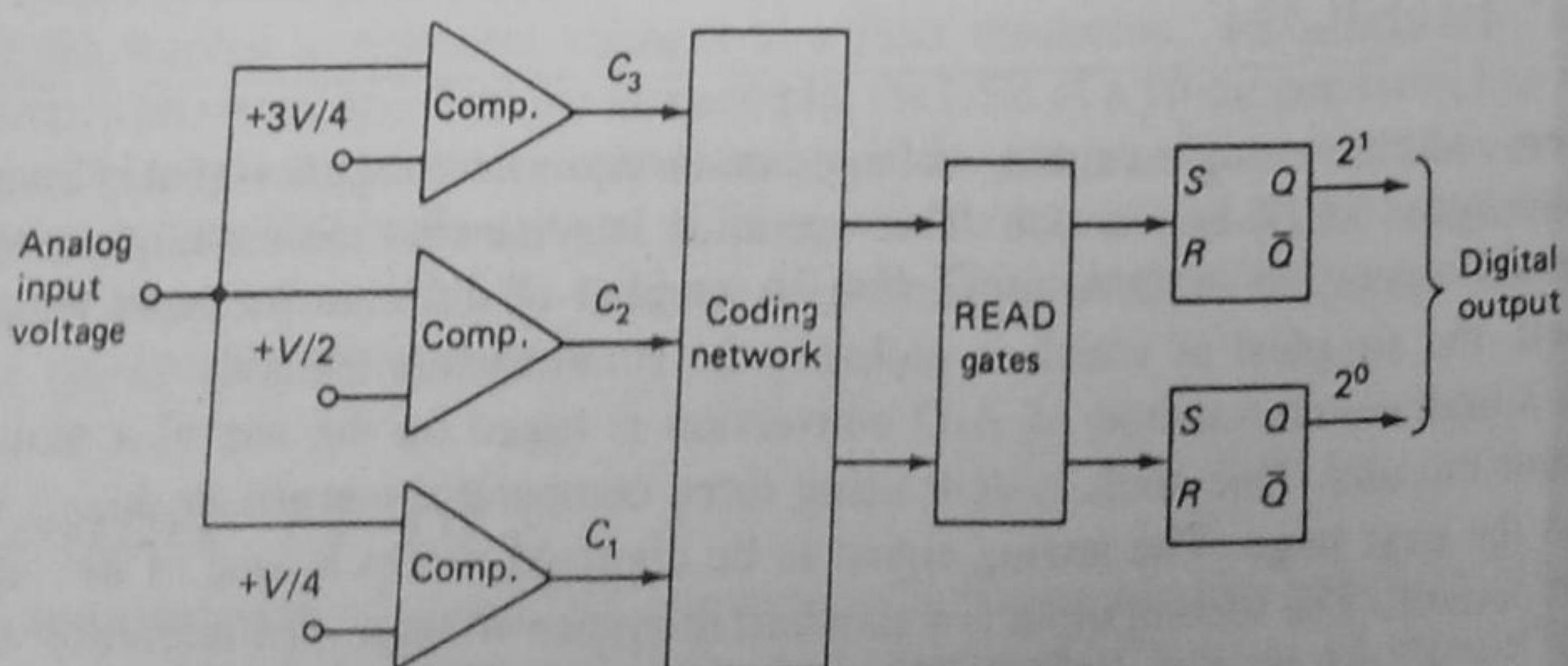
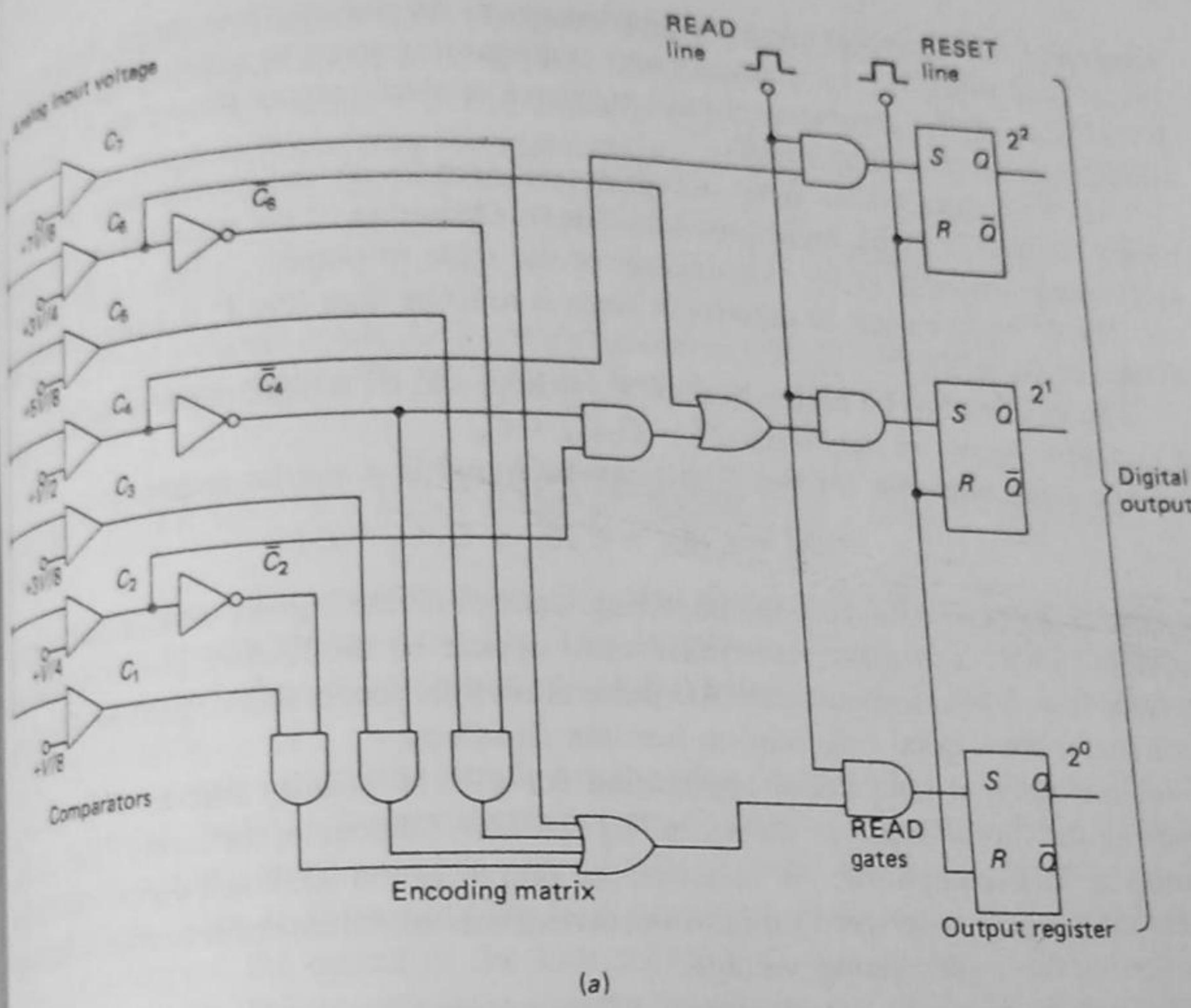
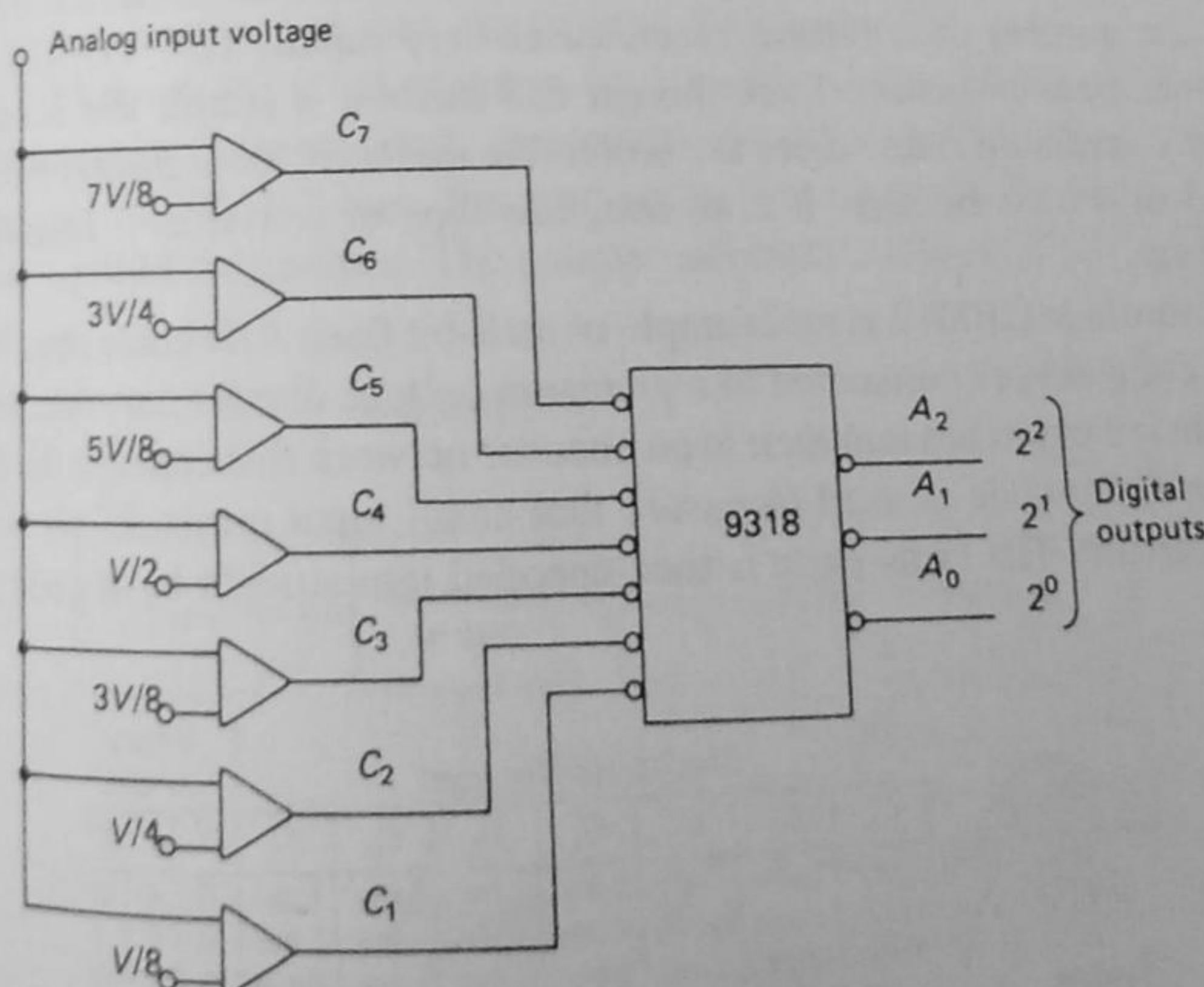


Fig. 11-20 2-bit simultaneous A/D converter.



(a)



(b)

4.11.21 3-bit simultaneous A/D converter. (a) Logic diagram.
Using a 9318 priority encoder.

flash converter

remember that three comparators were necessary for defining four ranges. In general, it can be said that $2^n - 1$ comparators are required to convert to a digital signal that has n bits. Some of the comparators have inverters at their outputs since both C and \bar{C} are needed for the encoding matrix.

The encoding matrix must accept seven input levels and encode them into a 3-bit binary number (having eight possible states). Operation of the encoding matrix can be most easily understood by examination of the table of outputs in Fig. 11-22.

The 2^2 bit is easiest to determine since it must be high (the 2^2 flip-flop must be set) whenever C_4 is high.

The 2^1 line must be high whenever C_2 is high and \bar{C}_4 is high, or whenever C_6 is high. In equation form, we can write $2^1 = C_2 C_4 + C_6$.

The logic equation for the 2^0 bit can be found in a similar manner; it is

$$2^0 = C_1 \bar{C}_2 + C_3 \bar{C}_4 + C_5 \bar{C}_6 + C_7$$

The transfer of data from the encoding matrix into the register must be carried out in two steps. First, a positive reset pulse must appear on the RESET line to reset all the flip-flops low. Then, a positive READ pulse allows the proper READ gates to go high and thus transfer the digital information into the flip-flops.

Interestingly, a convenient application for a 9318 priority encoder is to use it to replace all the digital logic as shown in Fig. 11-21b. Of course, the inputs C_1, C_2, \dots, C_7 must be TTL-compatible. In essence, the output of the 9318 is a digital number that reflects the highest-order zero input; this corresponds to the lowest reference voltage that still exceeds the input analog voltage.

The construction of a simultaneous A/D converter is quite straightforward and relatively easy to understand. However, as the number of bits in the desired digital number increases, the number of comparators increases very rapidly ($2^n - 1$), and the problem soon becomes unmanageable. Even though this method is simple and is capable of extremely fast conversion rates, there are preferable methods for digitizing numbers having more than 3 or 4 bits. Because it is so fast, this type of converter is frequently called a *flash converter*.

The Motorola MC10319 is an example of an 8-bit flash A/D converter. The input has 256 parallel comparators connected to a precision voltage divider network. The comparator outputs are fed to latches and then to an encoder network that captures the digital signal in Gray code. Gray code is used to ensure that small input errors do not result in large digital signal errors. The Gray code is then decoded into straight binary and presented to

Input voltage	Comparator for level							Binary output		
	C_1	C_2	C_3	C_4	C_5	C_6	C_7	2^2	2^1	2^0
0 to $V/8$	Low	Low	Low	Low	Low	Low	Low	0	0	0
$V/8$ to $V/4$	High	Low	Low	Low	Low	Low	Low	0	0	1
$V/4$ to $3V/8$	High	High	Low	Low	Low	Low	Low	0	1	0
$3V/8$ to $V/2$	High	High	High	Low	Low	Low	Low	0	1	1
$V/2$ to $5V/8$	High	High	High	High	Low	Low	Low	0	1	1
$5V/8$ to $3V/4$	High	High	High	High	High	Low	Low	1	0	0
$3V/4$ to $7V/8$	High	High	High	High	High	High	Low	1	0	1
$7V/8$ to V	High	High	High	High	High	High	High	1	1	0
								1	1	1

Fig. 11-22 Logic table for the converter in Fig. 11-21(a).

the outputs, which are tri-state TTL = compatible. The flash A/D converter is capable of operation with a 25-MHz clock! It comes in a 24-pin DIP and requires two dc supply voltages—typically +5 Vdc and -5 Vdc. Possible applications include radar signal processing, video displays, high-speed instrumentation, and television broadcasting.

SELF-TEST

8. Why is a simultaneous A/D converter called a flash converter?
9. What is one application for a flash converter?

11-6 A/D CONVERTER-COUNTER METHOD

A higher-resolution A/D converter using only one comparator could be constructed if a variable reference voltage were available. This reference voltage could then be applied to the comparator, and when it became equal to the input analog voltage, the conversion would be complete.

To construct such a converter, let us begin with a simple binary counter. The digital output signals will be taken from this counter, and thus we want it to be an n -bit counter, where n is the desired number of bits. Now let us connect the output of this counter to a standard binary ladder to form a simple D/A converter. If a clock is now applied to the input of the counter, the output of the binary ladder is the familiar staircase waveform shown in Fig. 11-16. This waveform is exactly the reference voltage signal we would like to have for the comparator! With a minimum of gating and control circuitry, this simple D/A converter can be changed into the desired A/D converter.

Figure 11-23 shows the block diagram for a counter-type A/D converter. The operation of the counter is as follows. First, the counter is reset to all 0s. Then, when a convert signal appears on the START line, the gate opens and clock pulses are allowed to pass through to the input of the counter. The counter advances through its normal binary count

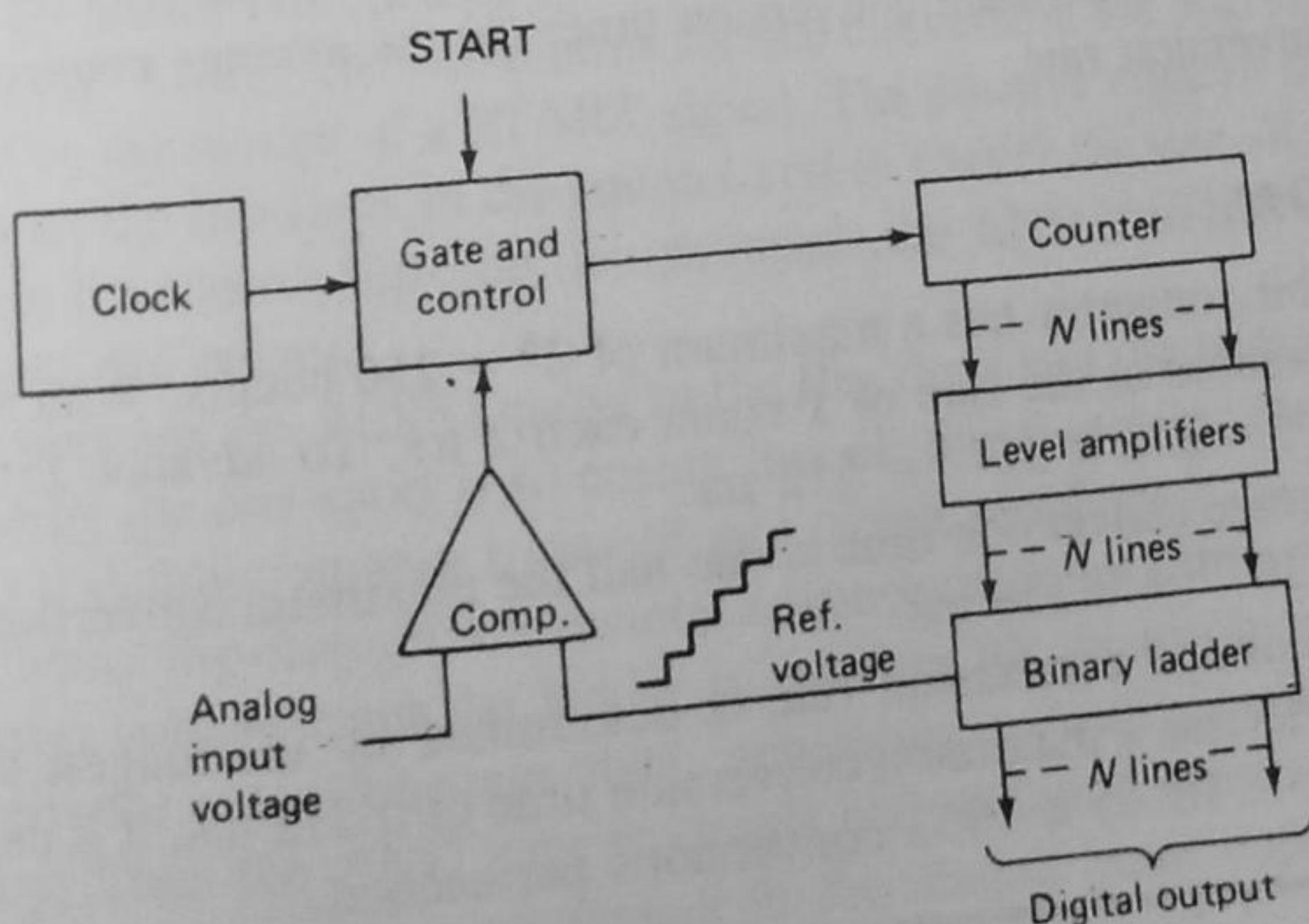


Fig. 11-23 Counter type A/D converter.

sequence, and the staircase waveform is generated at the output of the ladder. This waveform is applied to one side of the comparator, and the analog input voltage is applied to the other side. When the reference voltage equals (or exceeds) the input analog voltage, the gate is closed, the counter stops, and the conversion is complete. The number stored in the counter is now the digital equivalent of the analog input voltage.

Notice that this converter is composed of a D/A converter (the counter, level amplifiers, and the binary ladder), one comparator, a clock, and the gate and control circuitry. This can really be considered as a closed-loop control system. An error signal is generated at the output of the comparator by taking the difference between the analog input signal and the feedback signal (staircase reference voltage). The error is detected by the control circuit, and the clock is allowed to advance the counter. The counter advances in such a way as to reduce the error signal by increasing the feedback voltage. When the error is reduced to zero, the feedback voltage is equal to the analog input signal; the control circuitry stops the clock from advancing the counter, and the system comes to rest.

The counter-type A/D converter provides a very good method for digitizing to a high resolution. This method is much simpler than the simultaneous method for high resolution, but the conversion time required is longer. Since the counter always begins at zero and counts through its normal binary sequence, as many as 2^n counts may be necessary before conversion is complete. The average conversion time is, of course, $2^n/2$ or 2^{n-1} counts.

The counter advances one count for each cycle of the clock, and the clock therefore determines the conversion rate. Suppose, for example, that we have a 10-bit converter. It requires 1024 clock cycles for a full-scale count. If we are using a 1-MHz clock, the counter advances 1 count every microsecond. Thus, to count full scale requires $1024 \times 10^{-6} = 1.024$ ms. The converter reaches one-half full scale in half this time, or in 0.512 ms. The time required to reach one-half full scale can be considered the *average* conversion time for a large number of conversions.

Example 11-12

Suppose that the converter shown in Fig. 11-23 is an 8-bit converter driven by a 500-kHz clock. Find (a) the maximum conversion time; (b) the average conversion time; (c) the maximum conversion rate.

Solution

(a) An 8-bit converter has a maximum of $2^8 = 256$ counts. With a 500-kHz clock, the counter advances at the rate of 1 count each $2 \mu\text{s}$. To advance 256 counts requires $256 \times 2 \times 10^{-6} = 512 \times 10^{-6} = 512 \mu\text{s}$.

(b) The average conversion time is one-half the maximum conversion time. Thus it is $1/2 \times 0.512 \times 10^{-3} = 0.256$ ms.

(c) The maximum conversion rate is determined by the longest conversion time. Since the converter has a maximum conversion time of 0.512 ms, it is capable of making at least $1/(0.512 \times 10^{-3}) \cong 1953$ conversions per second.

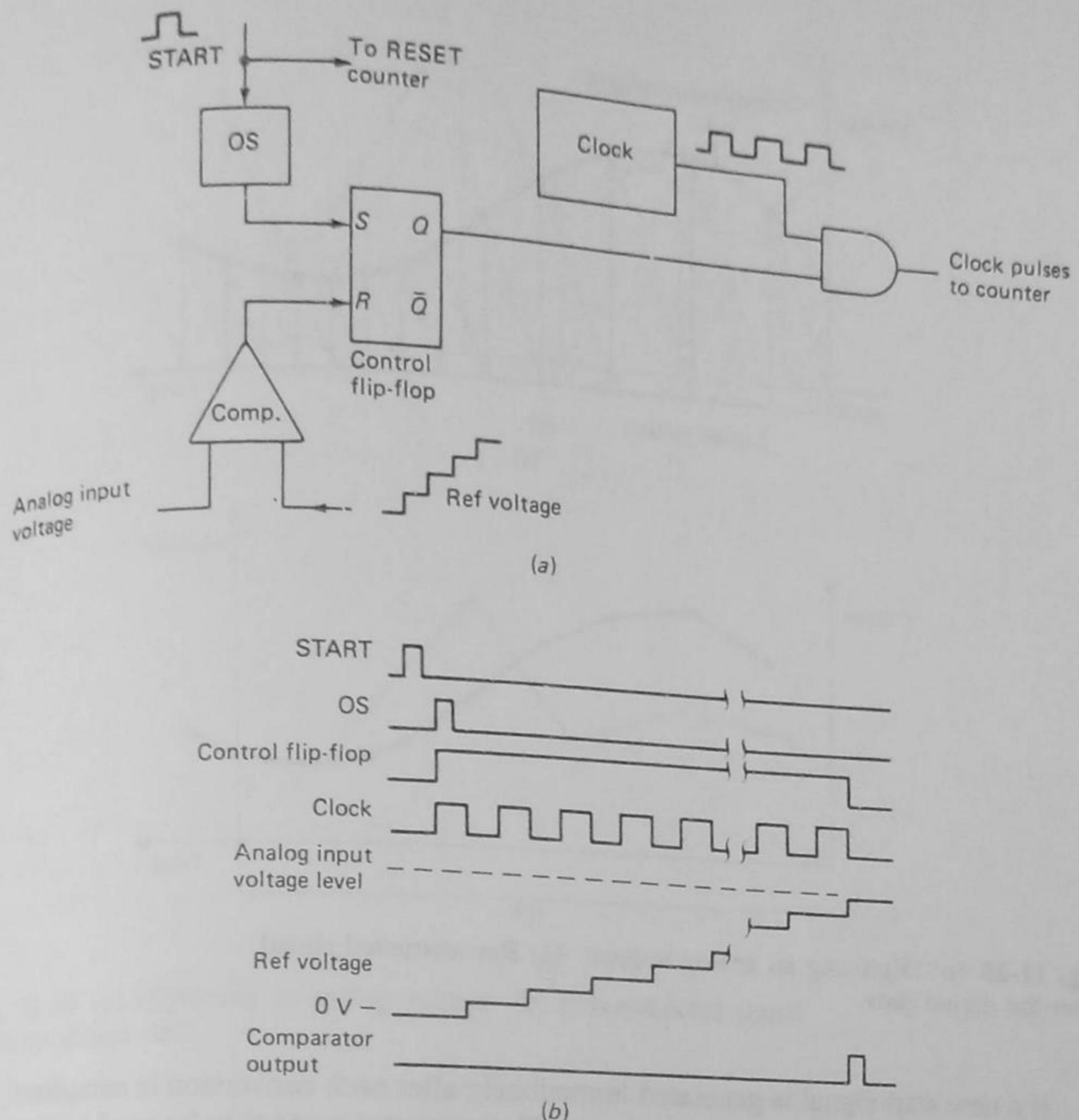


Fig. 11-24 Control of the A/D converter in Fig. 11-23.

Figure 11-24 shows one method of implementing the control circuitry for the converter shown in Fig. 11-23. The waveforms for one conversion are also shown. A conversion is initiated by the receipt of a START signal. The positive edge of the START pulse is used to reset all the flip-flops in the counter and to trigger the one-shot. The output of the one-shot sets the control flip-flop, which makes the AND gate true and allows clock pulses to advance the counter.

The delay between the RESET pulse to the flip-flops and the beginning of the clock pulses (ensured by the one-shot) is to ensure that all flip-flops are reset before counting begins. This is a definite attempt to avoid any racing problems.

With the control flip-flop set, the counter advances through its normal count sequence until the staircase voltage from the ladder is equal to the analog input voltage. At this time, the comparator output changes state, generating a positive pulse which resets the control flip-flop. Thus the AND gate is closed and counting ceases. The counter now holds a digital number which is equivalent to the analog input voltage. The converter remains in this state until another conversion signal is received.

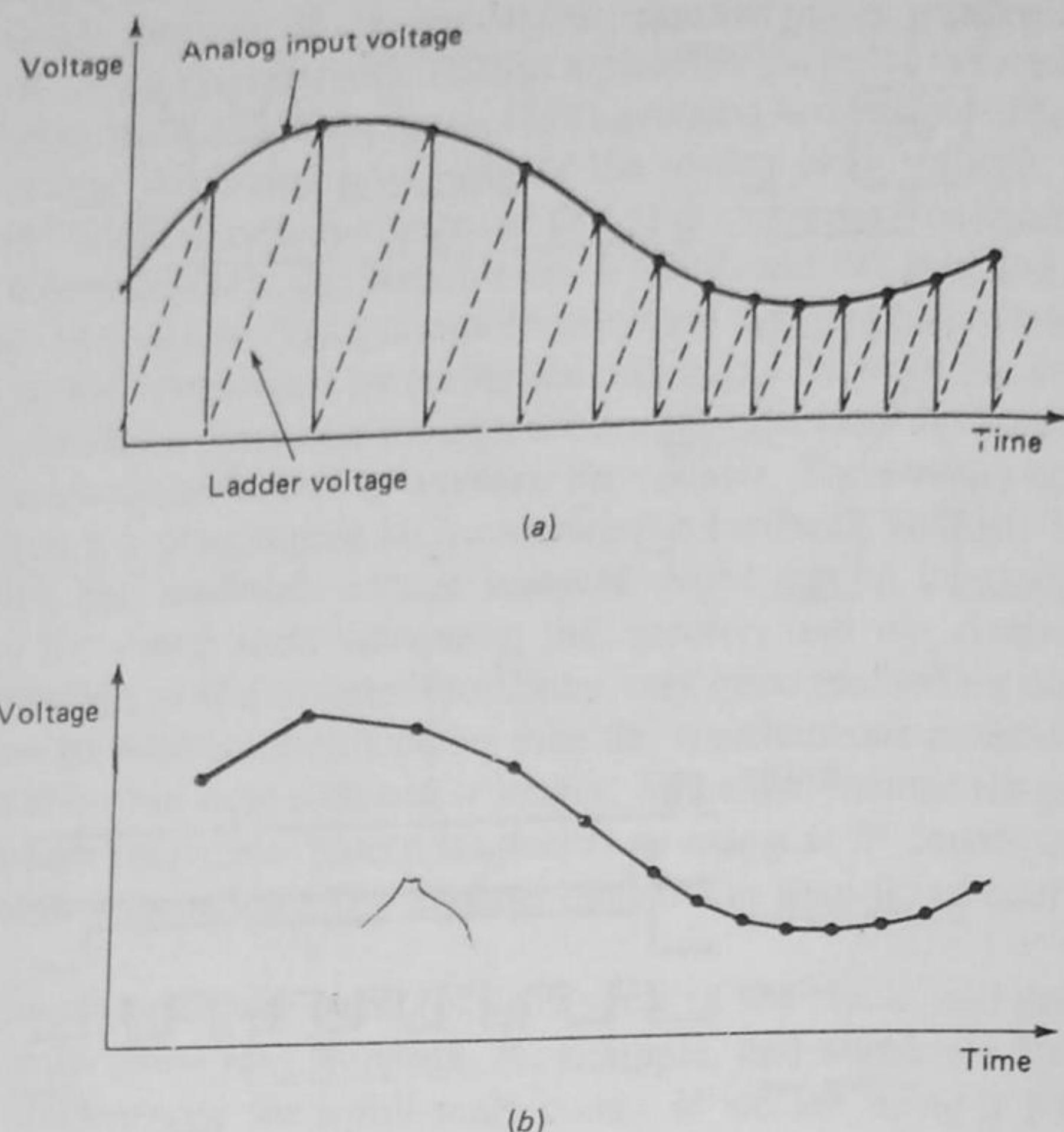


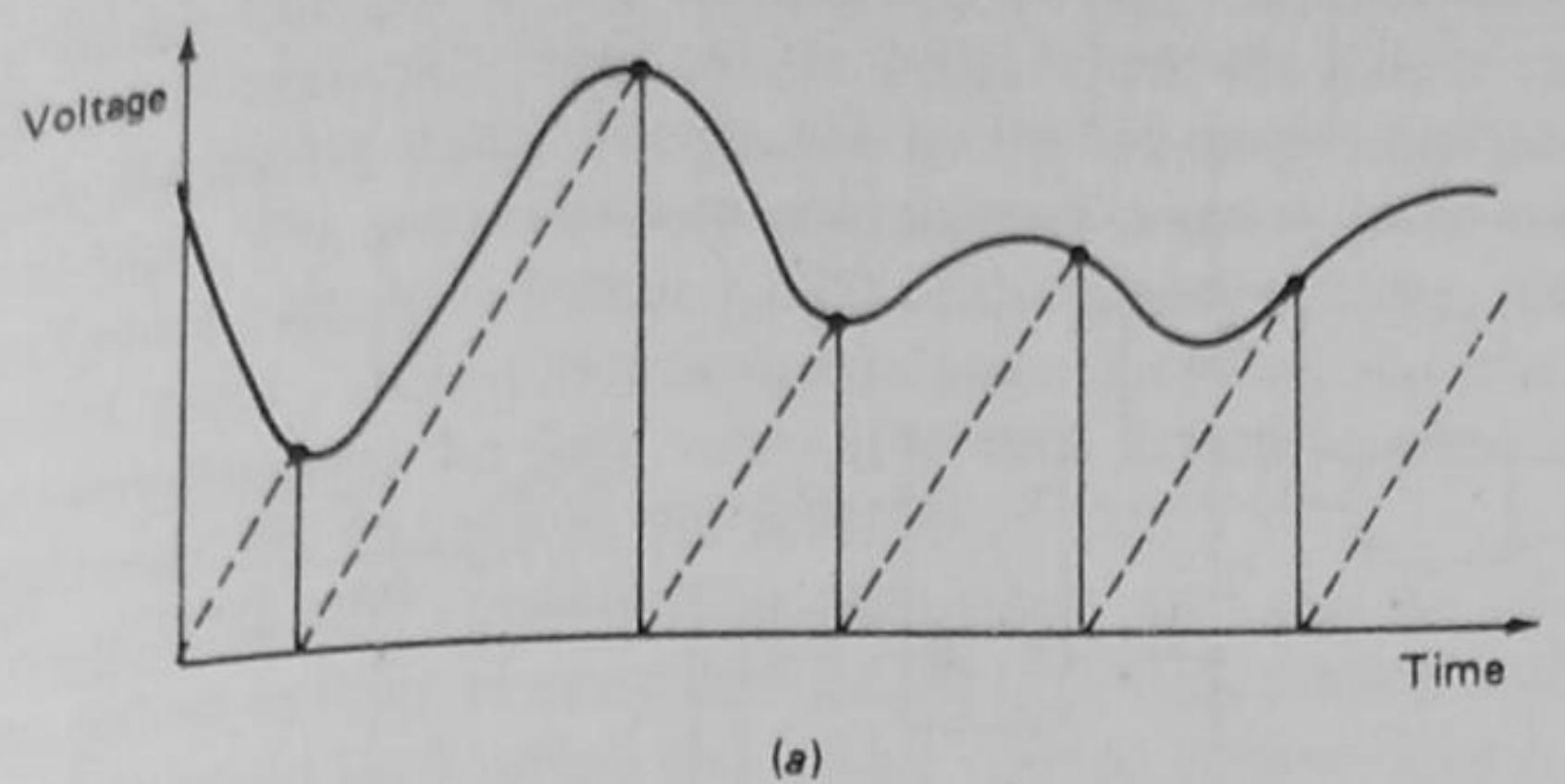
Fig. 11-25 (a) Digitizing an analog voltage. (b) Reconstructed signal from the digital data.

If a new start signal is generated immediately after each conversion is completed, the converter will operate at its maximum rate. The converter could then be used to digitize a signal as shown in Fig. 11-25a. Notice that the conversion times in digitizing this signal are not constant but depend on the amplitude of the input signal. The analog input signal can be reconstructed from the digital information by drawing straight lines from each digitized point to the next. Such a reconstruction is shown in Fig. 11-25b; it is, indeed, a reasonable representation of the original input signal. In this case, it is important to note that the conversion times are smaller than the transient time of the input waveform.

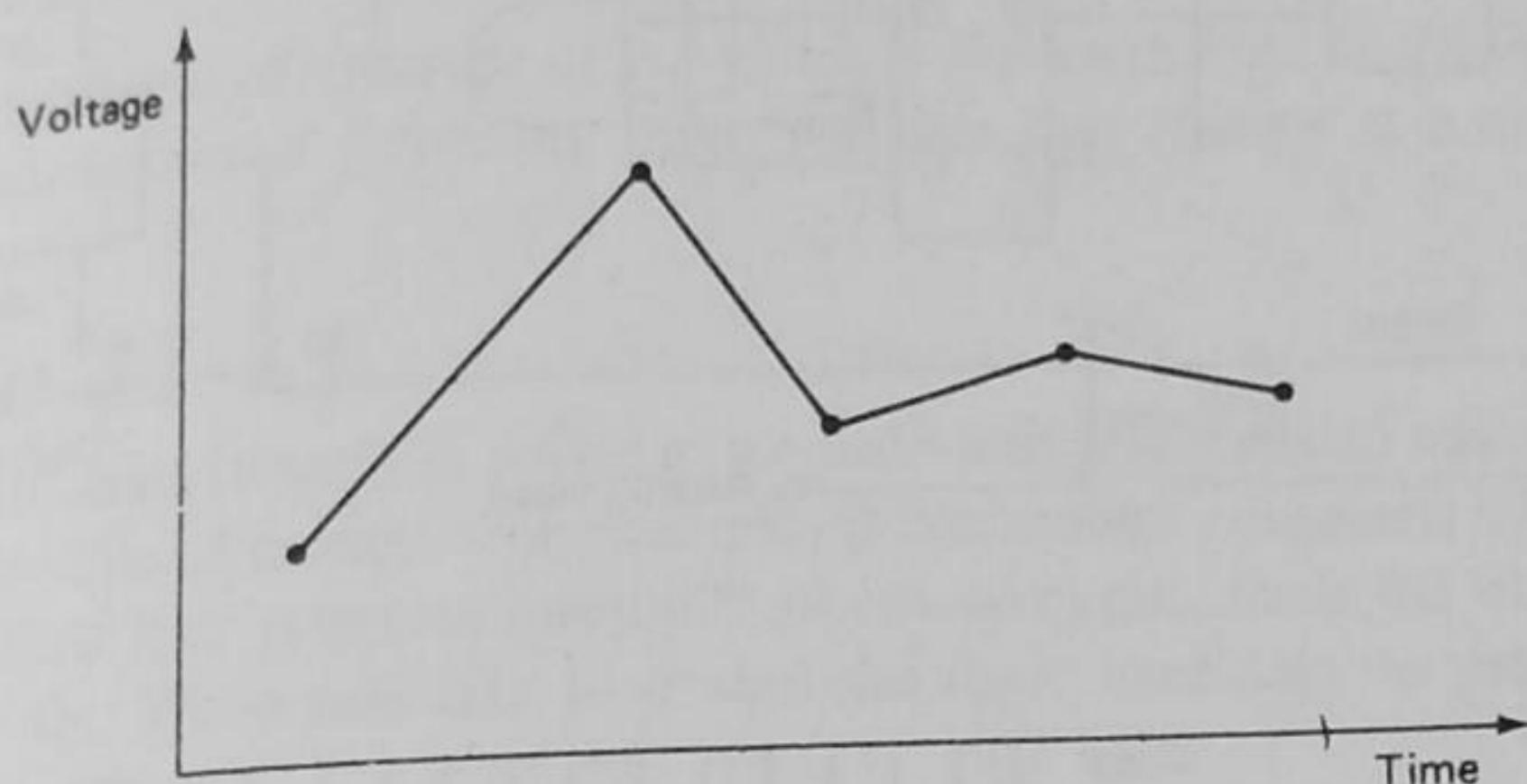
On the other hand, if the transient time of the input waveform approaches the conversion time, the reconstructed output signal is not quite so accurate. Such a situation is shown in Fig. 11-26a and b. In this case, the input waveform changes at a rate faster than the converter is capable of recognizing. Thus the need for reducing conversion time is apparent.

SELF-TEST

10. The A/D converter in Fig. 11-23 has 8 bits and is driven by a 2-MHz clock.
What is the maximum conversion time?
11. What is the average conversion time for the converter in question 10?



(a)



(b)

Fig. 11-26 (a) Digitizing an analog voltage. (b) Reconstructed signal from the digital data.

11-7 CONTINUOUS A/D CONVERSION

An obvious method for speeding up the conversion of the signal as shown in Fig. 11-26 is to eliminate the need for resetting the counter each time a conversion is made. If this were done, the counter would not begin at zero each time, but instead would begin at the value of the last converted point. This means that the counter would have to be capable of counting either up or down. This is no problem; we are already familiar with the operation of up-down counters.

There is, however, the need for additional logic circuitry, since we must decide whether to count up or down by examining the output of the comparator. An A/D converter which uses an up-down counter is shown in Fig. 11-27 on the next page. This method is known as *continuous conversion*, and thus the converter is called a *continuous-type A/D converter*.

The D/A portion of this converter is the same as those previously discussed, with the exception of the counter. It is an up-down counter and has the up and down count control lines in addition to the advance line at its input.

The output of the ladder is fed into a comparator which has two outputs instead of one as before. When the analog voltage is more positive than the ladder output, the *up* output

continuous conversion

continuous-type A/D converter

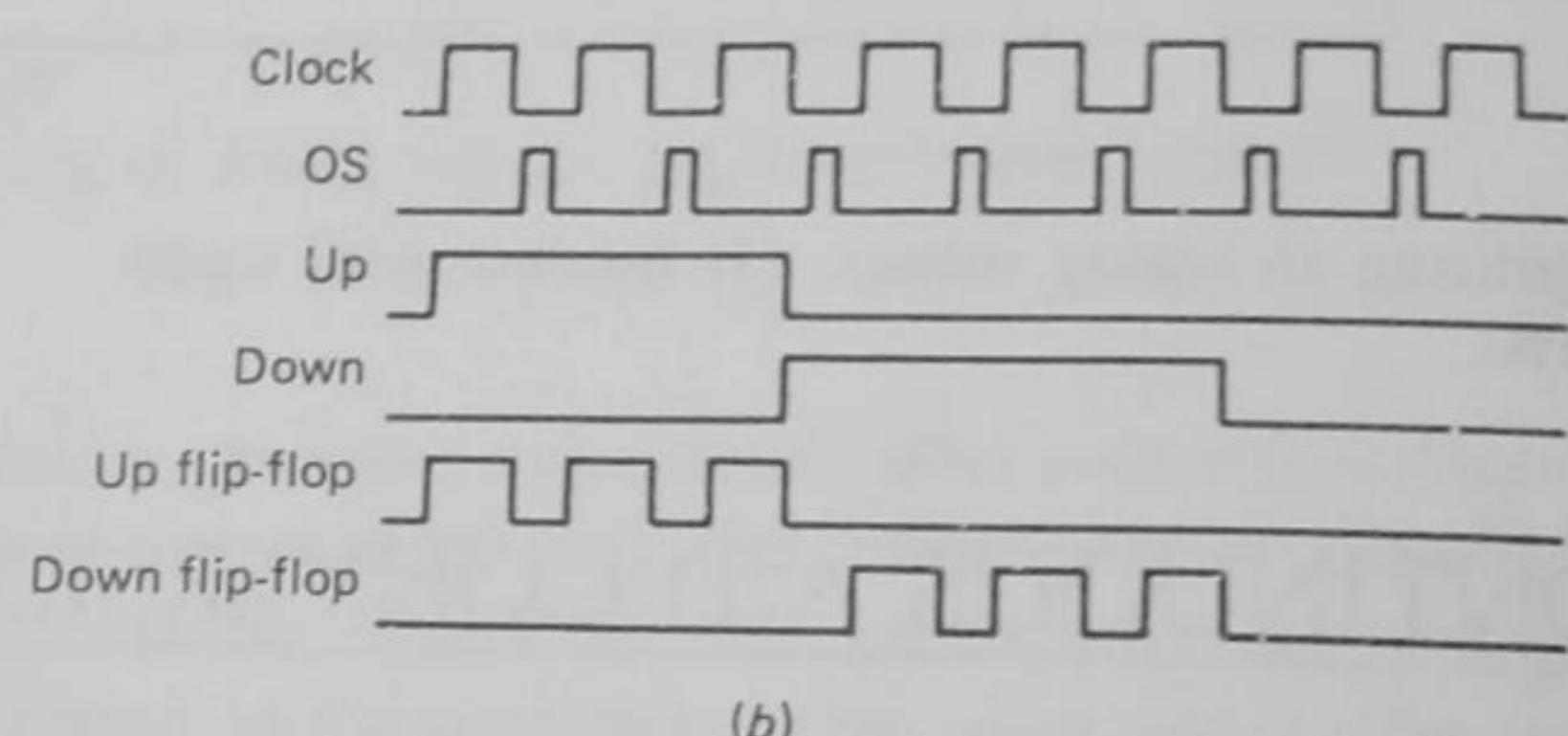
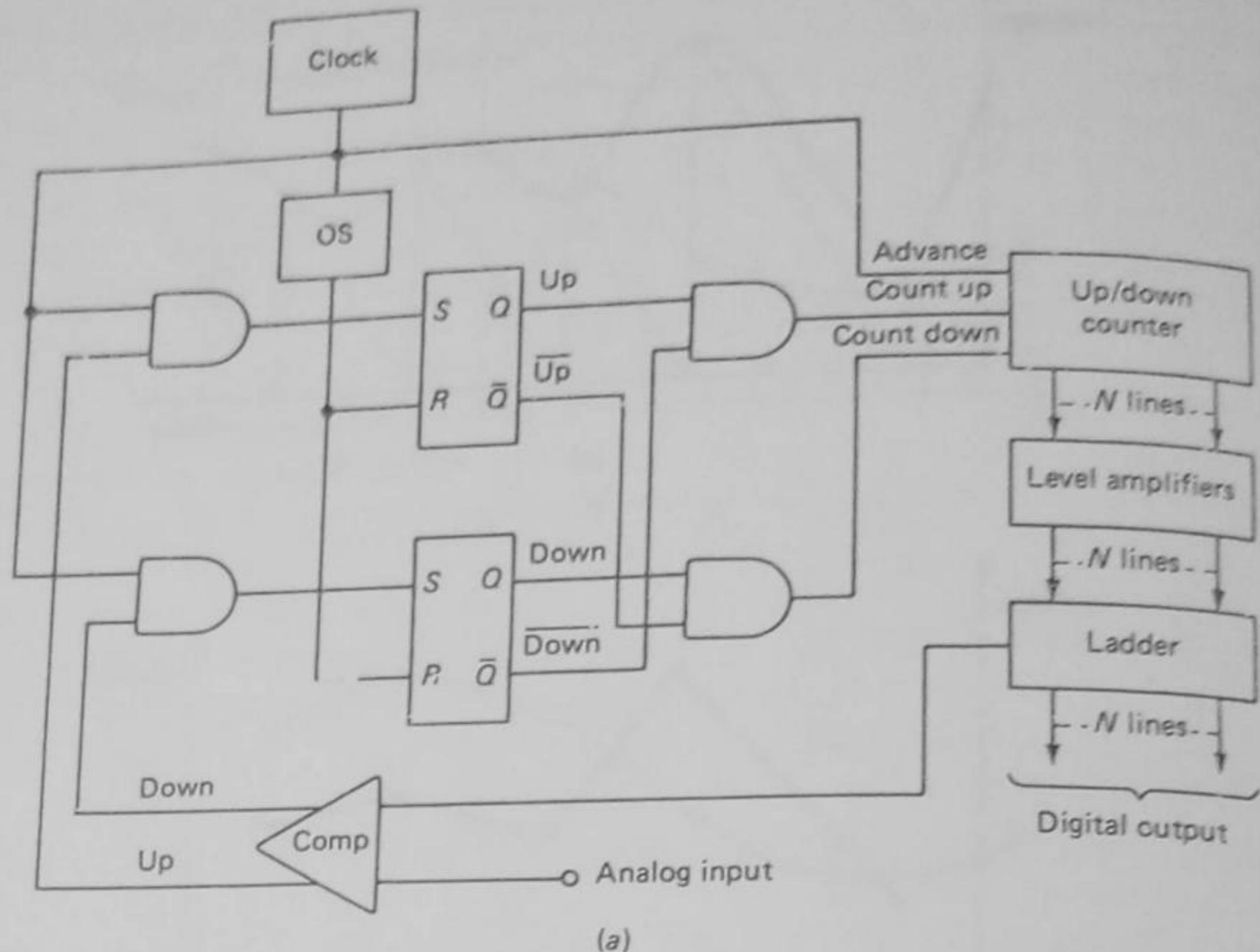


Fig. 11-27 Continuous A/D converter.

of the comparator is high. When the analog voltage is more negative than the ladder output, the *down* output is high.

If the *up* output of the comparator is high, the AND gate at the input of the *up* flip-flop is open, and the first time the clock goes positive, the *up* flip-flop is set. If we assume for the moment that the *down* flip-flop is reset, the AND gate which controls the *count-up* line of the counter will be true and the counter will advance one count. The counter can advance only one count since the output of the one-shot resets both the *up* and the *down* flip-flops just after the clock goes low. This can then be considered as one *count-up* conversion cycle.

Notice that the AND gate which controls the *count-up* line has inputs of *up* and *down*. Similarly, the *count-down* line AND gate has inputs of *down* and *up*. This could be considered an exclusive-OR arrangement and ensures that the *count-down* and *count-up* lines cannot both be high at the same time.

As long as the *up* line out of the comparator is high, the converter continues to operate one conversion cycle at a time. At the point where the ladder voltage becomes more positive than the analog input voltage, the *up* line of the comparator goes low and the *down* line goes high. The converter then goes through a count-down conversion cycle. At this point, the ladder voltage is within 1 LSB of the analog voltage, and the converter oscillates about this point. This is not desirable since we want the converter to cease operation and not jump around the final value. The trick here is to adjust the comparator such that its outputs do not change at the same time.

We can accomplish this by adjusting the comparator such that the *up* output will not go high unless the ladder voltage is more than $\frac{1}{2}$ LSB below the analog voltage. Similarly, the *down* output will not go high unless the ladder voltage is more than $\frac{1}{2}$ LSB above the analog voltage. This is called *centering on the LSB* and provides a digital output which is within $\frac{1}{2}$ LSB.

A waveform typical of this type of converter is shown in Fig. 11-28. You can see that this converter is capable of following input voltages that change at a much faster rate.

*centering on the
LSB*

Example 11-13

Quite often, additional circuitry is added to a continuous converter to ensure that it cannot count off scale in either direction. For example, if the counter contained all 1s, it would be undesirable to allow it to progress through a count-up cycle, since the next count would advance it to all 0s. We would like to design the logic necessary to prevent this.

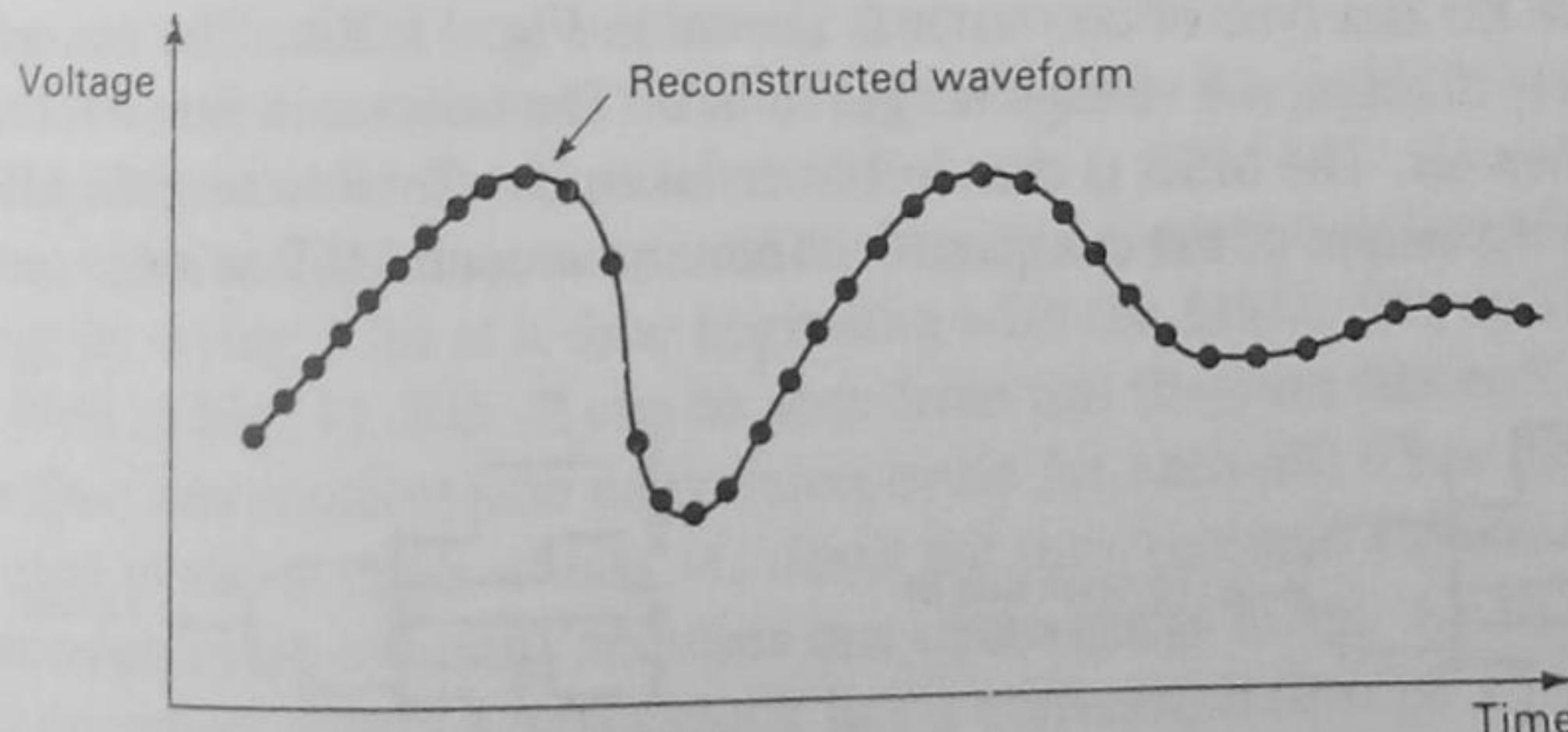
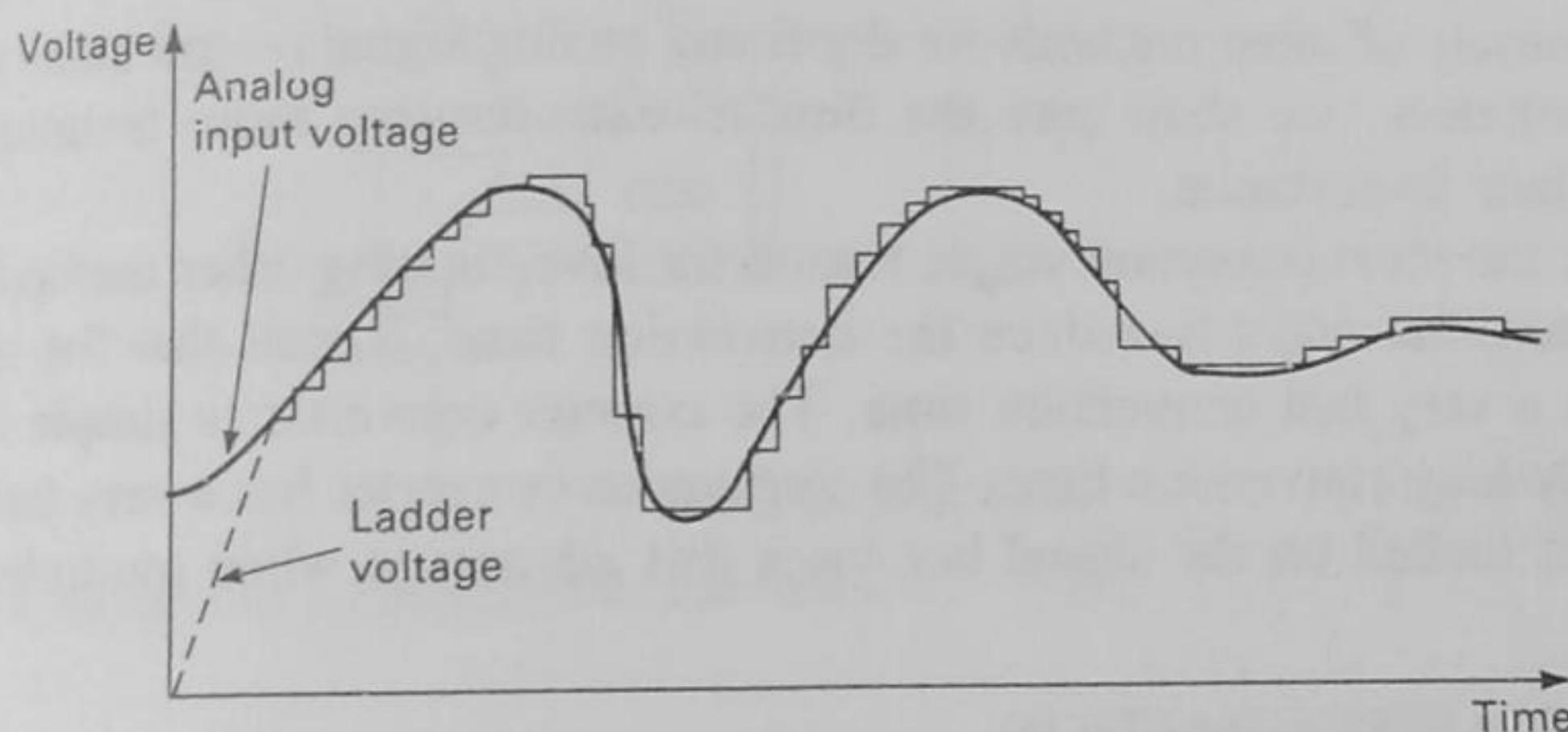


Fig. 11-28 Continuous A/D conversion.

Solution

The two limit points which must be detected are all 1s and all 0s in the counter. Suppose that we construct an AND gate having the 1 sides of all the counter flip-flops as its inputs. The output of this gate will be true whenever the counter contains all 1s. If the gate is then connected to the reset side of the *up* flip-flop, the counter will be unable to count beyond all 1s.

Similarly, we might construct an AND gate in which the inputs are the 0 sides of all the counter flip-flops. The output of this gate can be connected to the reset side of the *down* flip-flop, and the counter will then be unable to count beyond all 0s. The gates are shown in Fig. 11-29.

SELF-TEST

12. How does the continuous-type A/D converter differ from the simple counter-type A/D converter?
13. What advantage does the continuous-type A/D converter offer over the counter-type A/D converter?

11-8 A/D TECHNIQUES

There are a variety of other methods for digitizing analog signals—too many to discuss in detail. Nevertheless, we shall take the time to examine two more techniques and the reasons for their importance.

Probably the most important single reason for investigating other methods of conversion is to determine ways to reduce the conversion time. Recall that the simultaneous converter has a very fast conversion time. The counter converter is simple logically but has a relatively long conversion time. The continuous converter has a very fast conversion time once it is locked on the signal but loses this advantage when multiplexing inputs.

SUCCESSIVE APPROXIMATION

If multiplexing is required, the *successive-approximation converter* is most useful. The block diagram for this type of converter is shown in Fig. 11-30a. The converter operates by successively dividing the voltage ranges in half. The counter is first reset to all 0s, and the MSB is then set. The MSB is then left in or taken out (by resetting the MSB flip-flop) depending on the output of the comparator. Then the second MSB is set in, and a compar-

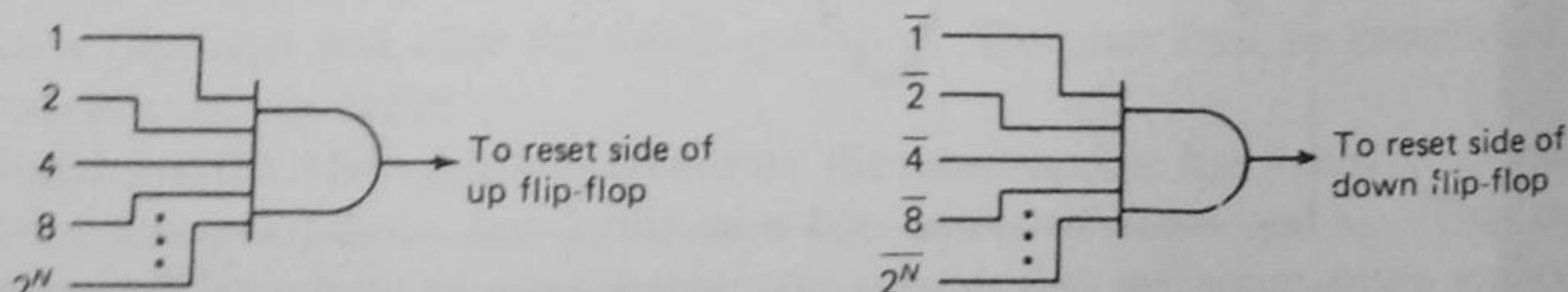
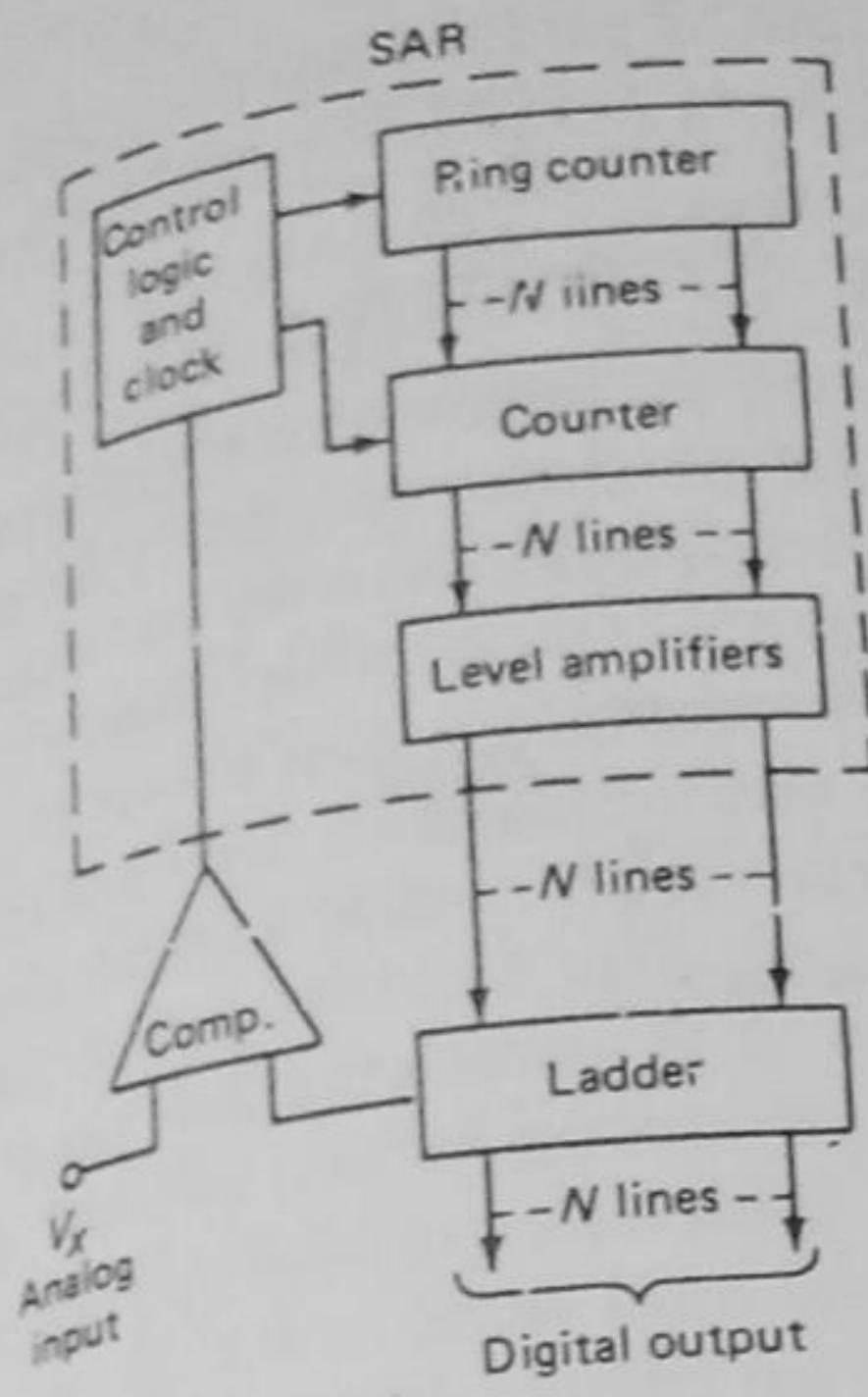
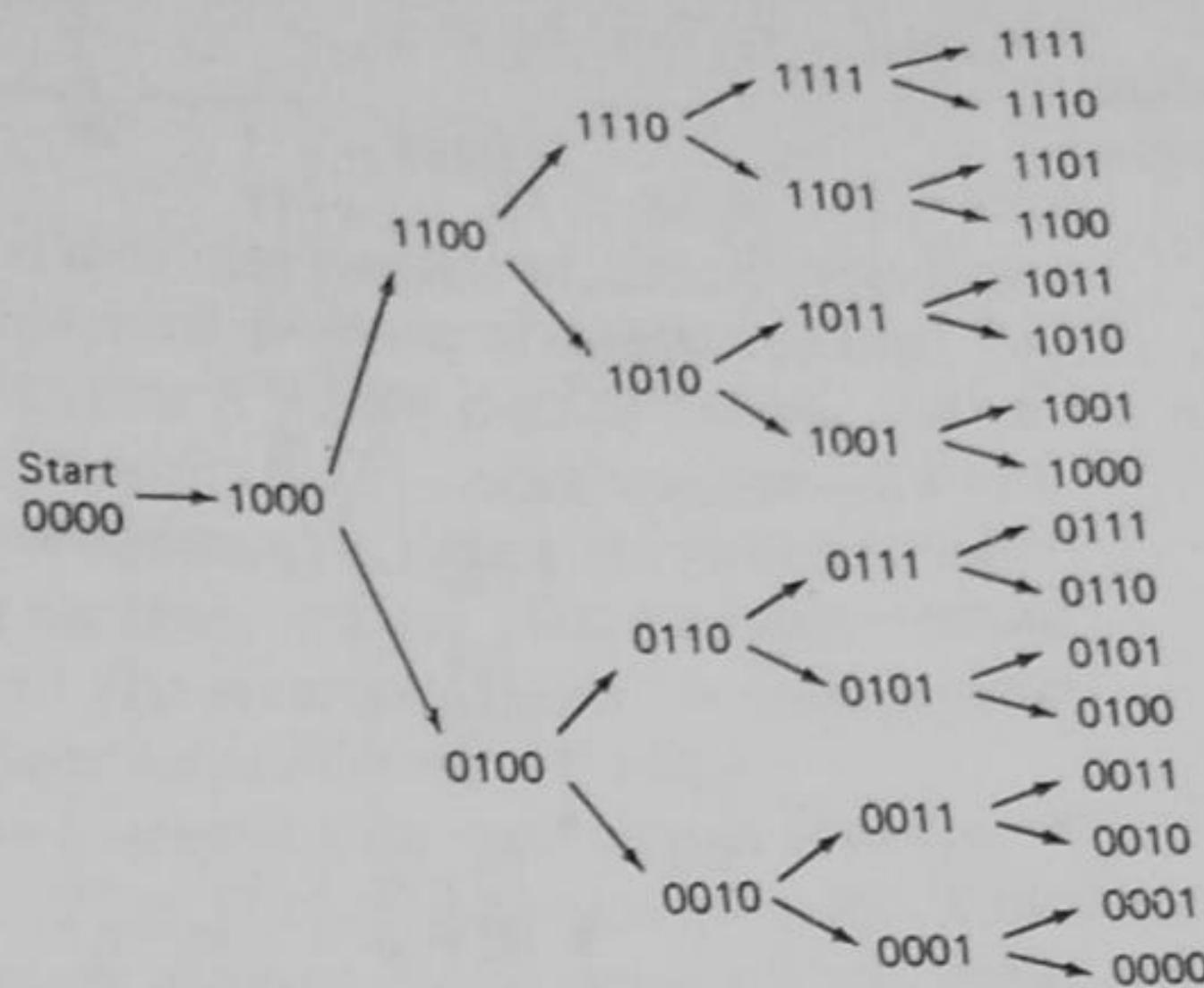


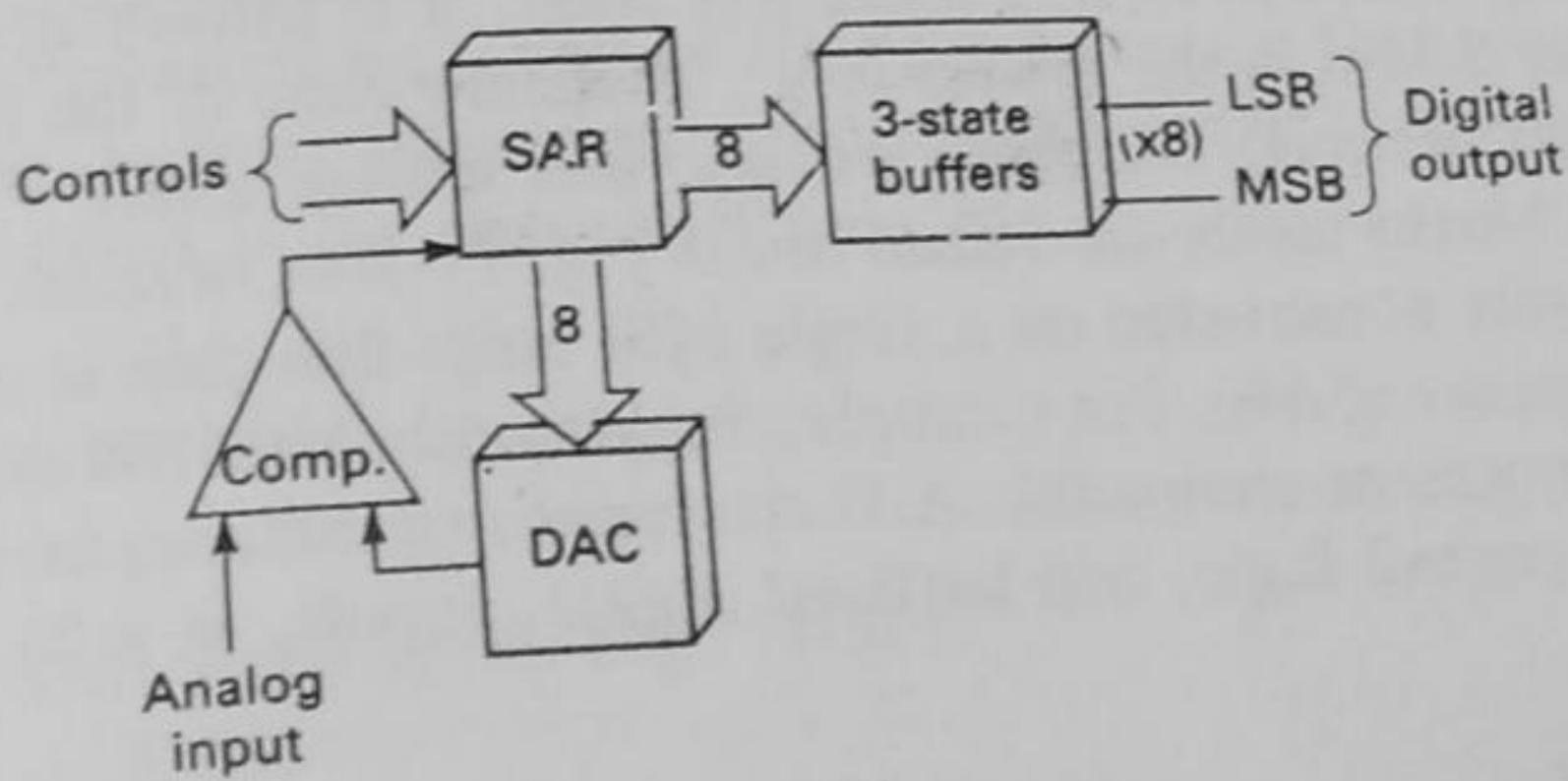
Fig. 11-29 Count-limiting gates for the converter in Fig. 11-27.



(a)



(b)



(c)

Motorola MC6108 ADC

Fig. 11-30 Successive approximation converter.

ison is made to determine whether to reset the second MSB flip-flop. The process is repeated down to the LSB, and at this time the desired number is in the counter. Since the conversion involves operating on one flip-flop at a time, beginning with the MSB, a ring counter may be used for flip-flop selection.

The successive-approximation method thus is the process of approximating the analog voltage by trying 1 bit at a time beginning with the MSB. The operation is shown in diagram form in Fig. 11-30b. It can be seen from this diagram that each conversion takes the same time and requires one conversion cycle for each bit. Thus the total conversion time is equal to the number of bits, n , times the time required for one conversion cycle. One conversion cycle normally requires one cycle of the clock. As an example, a 10-bit converter operating with a 1-MHz clock has a conversion time of $10 \times 10^{-6} = 10^{-5}$ = $10 \mu\text{s}$.

D/A CONVERSION AND A/D CONVERSION

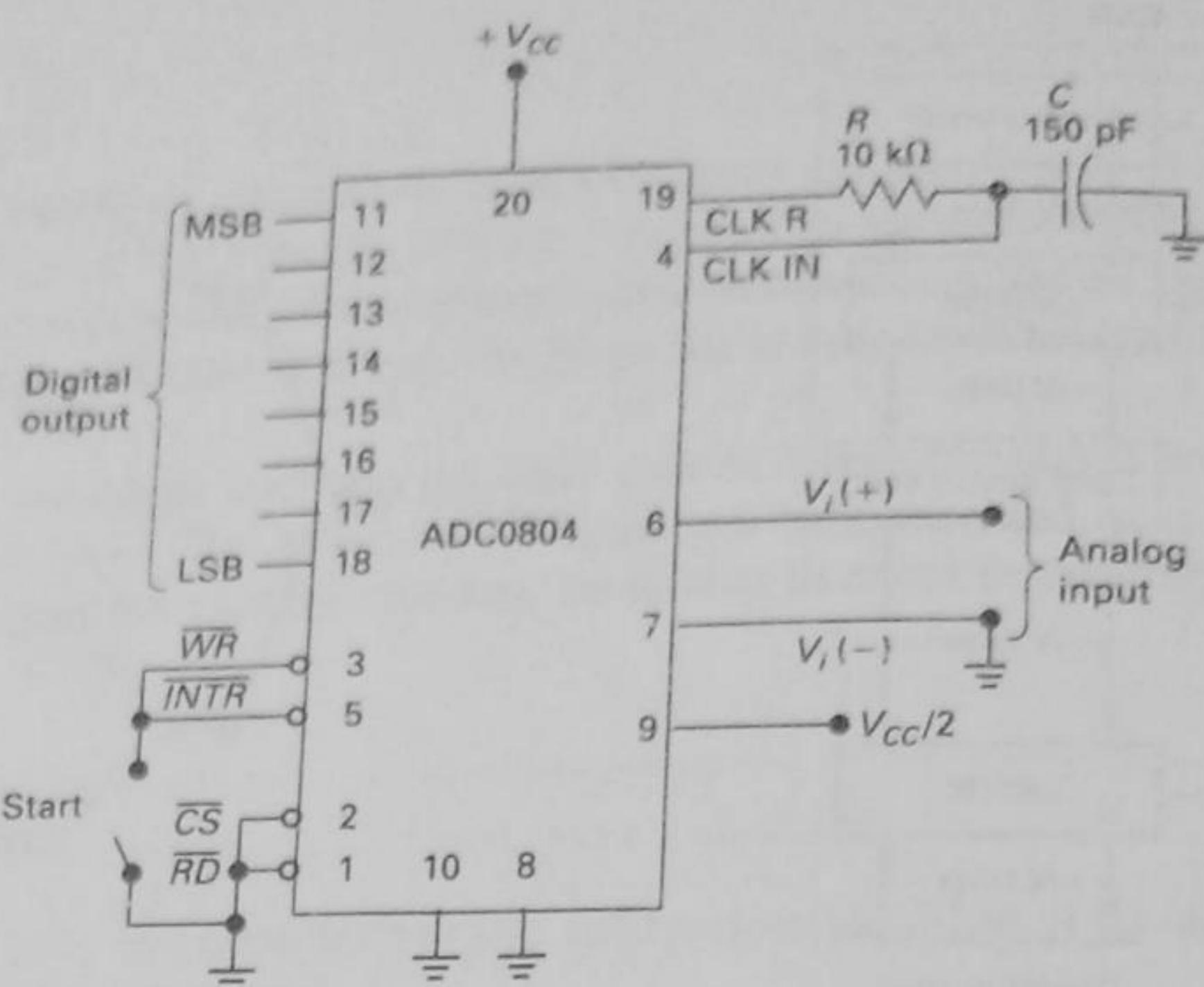


Fig. 11-31

sive-approximation register

ree-running mode

When dealing with conversion times this short, it is usually necessary to take into account the other delays in the system (e.g., switching time of the multiplexer, settling time of the ladder network, comparator delay, and settling time).

All the logic blocks inside the dashed line in Fig. 11-30a, or some equivalent arrangement, are frequently constructed on a single MSI chip; this chip is called a *successive-approximation register* (SAR). For example, the Motorola MC6108 shown in Fig. 11-30c is an 8-bit microprocessor-compatible A/D converter that includes an SAR, D/A conversion capabilities, control logic, and buffered digital outputs, in a 28-pin DIP.

THE ADC0804

The ADC0804 is an inexpensive and very popular A/D converter which is available from a number of different manufacturers, including National Semiconductor. The ADC0804 is an 8-bit CMOS microprocessor-compatible successive-approximation A/D converter that is supplied in a 20-pin DIP. It is capable of digitizing an analog input voltage within the range 0 to +5 Vdc, and it only requires a single dc supply voltage—usually +5 Vdc. The digital outputs are both TTL- and CMOS-compatible.

The block diagram of an ADC0804 is shown in Fig. 11-31. In this case, the controls are wired such that the converter operates continuously. This is the so-called *free-running mode*. The 10-kΩ resistor, along with the 150-pF capacitor, establishes the frequency of operation according to $f \approx 1/1.1(RC)$. In this case,

$$f \approx \frac{1}{1.1 \times (10 \text{ k}\Omega \times 150 \text{ pF})}$$

$$= \frac{1}{1.1 \times (10^4 \times 1.5 \times 10^{-12})} = 607 \text{ kHz}$$

A momentary activation of the START switch is necessary to begin operation. A detailed discussion of the ADC0804 is given in Sec. 14-4.

section counter

SECTION COUNTERS

Another method for reducing the total conversion time of a simple counter converter is to divide the counter into sections. Such a configuration is called a *section counter*. To determine how the total conversion time might be reduced by this method, assume that we have a standard 8-bit counter. If this counter is divided into two equal counters of 4 bits each, we have a section converter. The converter operates by setting the section containing the four LSBs to all 1s and then advancing the other sections until the ladder voltage exceeds the input voltage. At this point the four LSBs are all reset, and this section of the counter is then advanced until the ladder voltage equals the input voltage.

Notice that a maximum of $2^4 = 16$ counts is required for each section to count full scale. Thus this method requires only $2 \times 2^4 = 2^5 = 32$ counts to reach full scale. This is a considerable reduction over the $2^8 = 256$ counts required for the straight 8-bit counter. There is, of course, some extra time required to set the counters initially and to switch from counter to counter during the conversion. This logical operation time is very small, however, compared with the total time saved by this method.

This type of converter is quite often used for digital voltmeters, since it is very convenient to divide the counters by counts of 10. Each counter is then used to represent one of the digits of the decimal number appearing at the output of the voltmeter. We discuss this subject in detail in the next chapter.

single-ramp
method

SELF-TEST

14. What does SAR stand for in Fig. 11-30c?
15. What is an ADC0804?

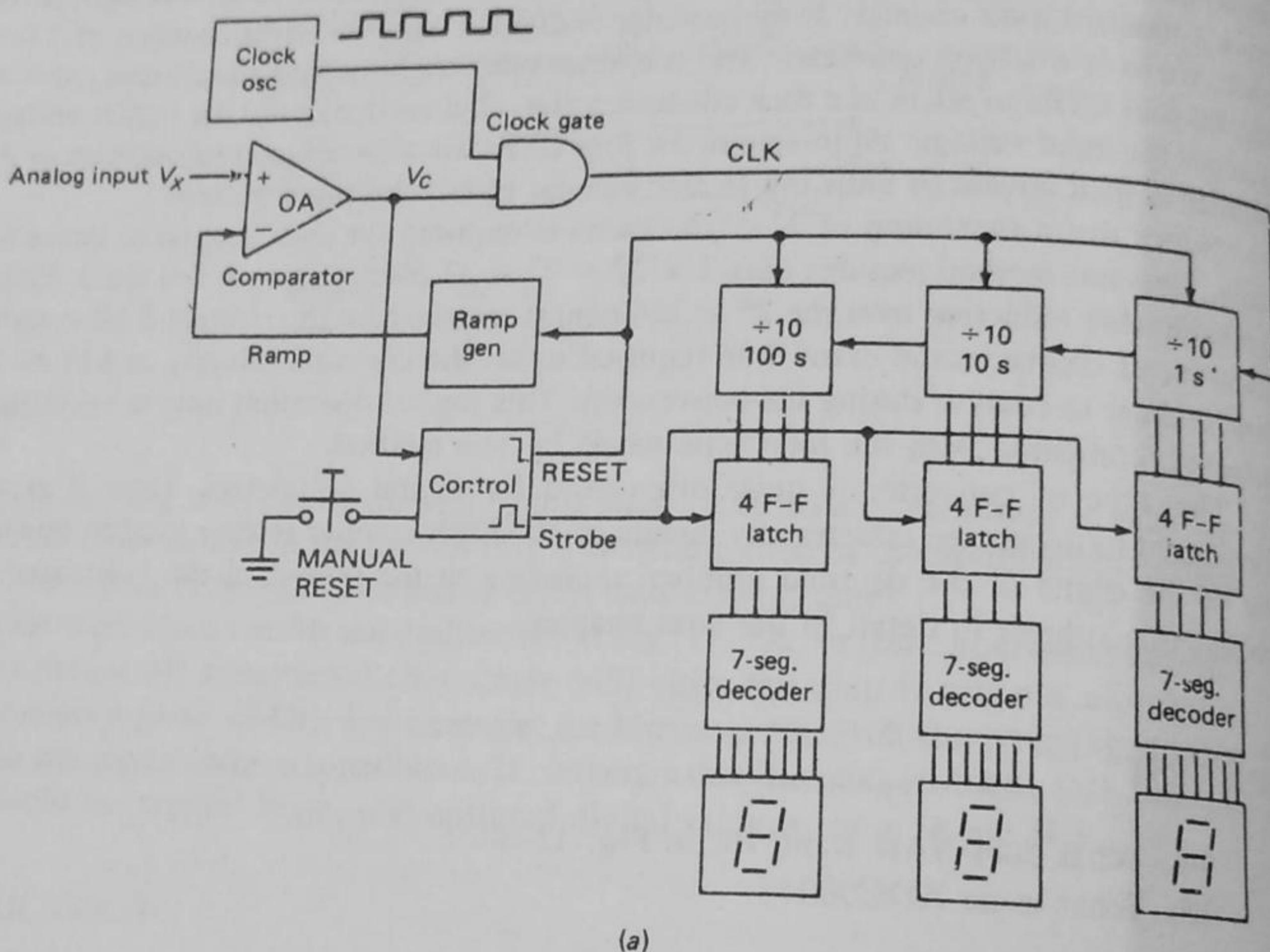
11.9 DUAL-SLOPE A/D CONVERSION

Up to this point, our interest in different methods of A/D conversion has centered on reducing the actual conversion time. If a very short conversion time is not a requirement, there are other methods of A/D conversion that are simpler to implement and much more economical. Basically, these techniques involve comparison of the unknown input voltage with a reference voltage that begins at zero and increases linearly with time. The time required for the reference voltage to increase to the value of the unknown voltage is directly proportional to the magnitude of the unknown voltage, and this time period is measured with a digital counter. This is referred to as a *single-ramp method*, since the reference voltage is sloped like a ramp. A variation on this method involves using an operational amplifier integrating circuit in a dual-ramp configuration. The dual-ramp method is very popular, and widely used in digital voltmeters and digital panel meters. It offers good accuracy, good linearity, and very good noise-rejection characteristics.

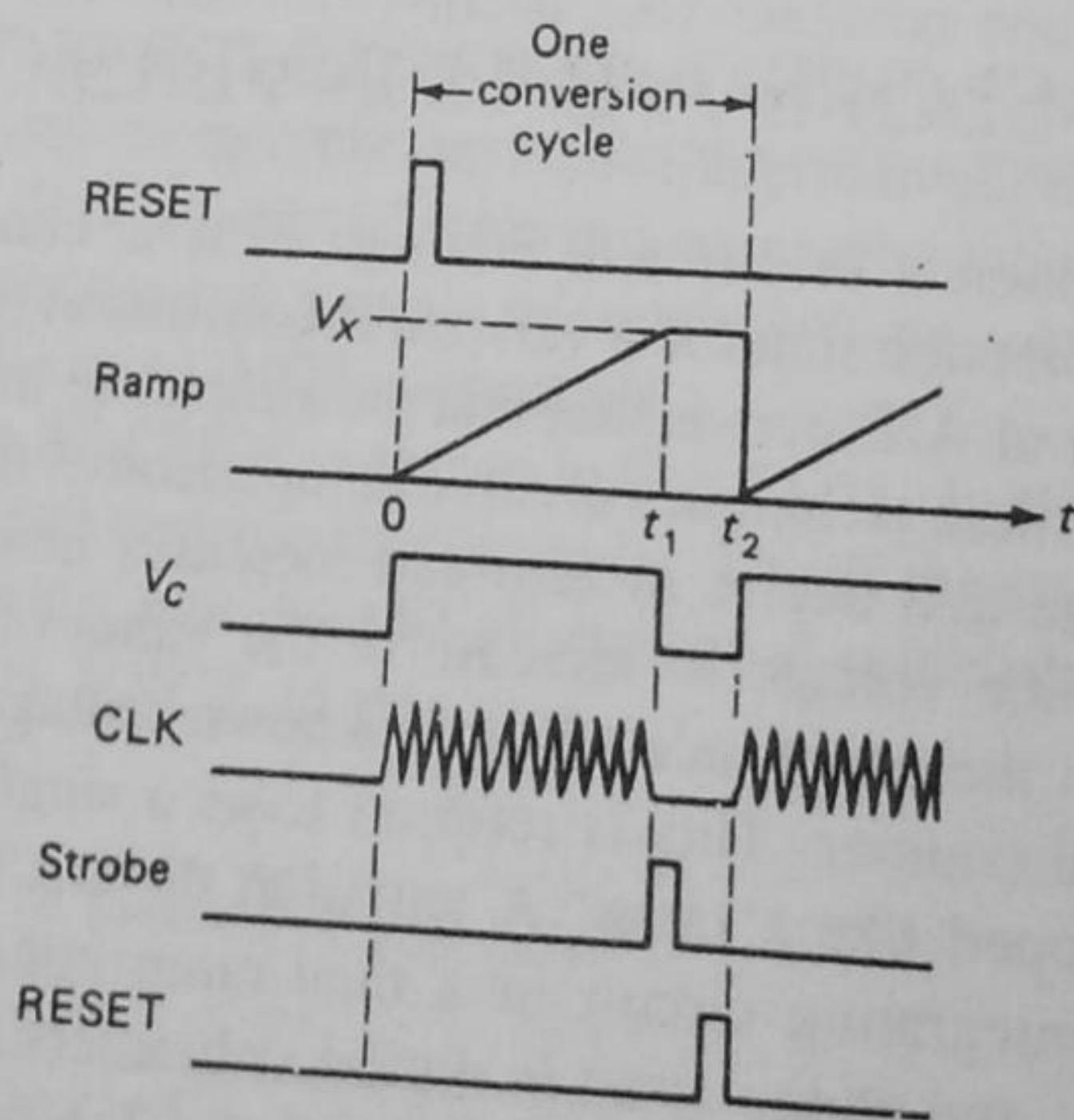
D/A CONVERSION AND A/D CONVERSION

ramp generator**SINGLE-RAMP A/D CONVERTER**

Let's take a look at the single-ramp A/D converter in Fig. 11-32. The heart of this converter is the *ramp generator*. This is a circuit that produces an output voltage ramp as shown in Fig. 11-33a. The output voltage begins at zero and increases linearly up to a maximum voltage V_m . It is important that this voltage be a straight line—that is, it must have a constant slope. For instance, if $V_m = 1.0$ Vdc, and it takes 1.0 ms for the ramp to move from 0.0 up to 1.0 V, the slope is 1 V/ms, or 1000 V/s.



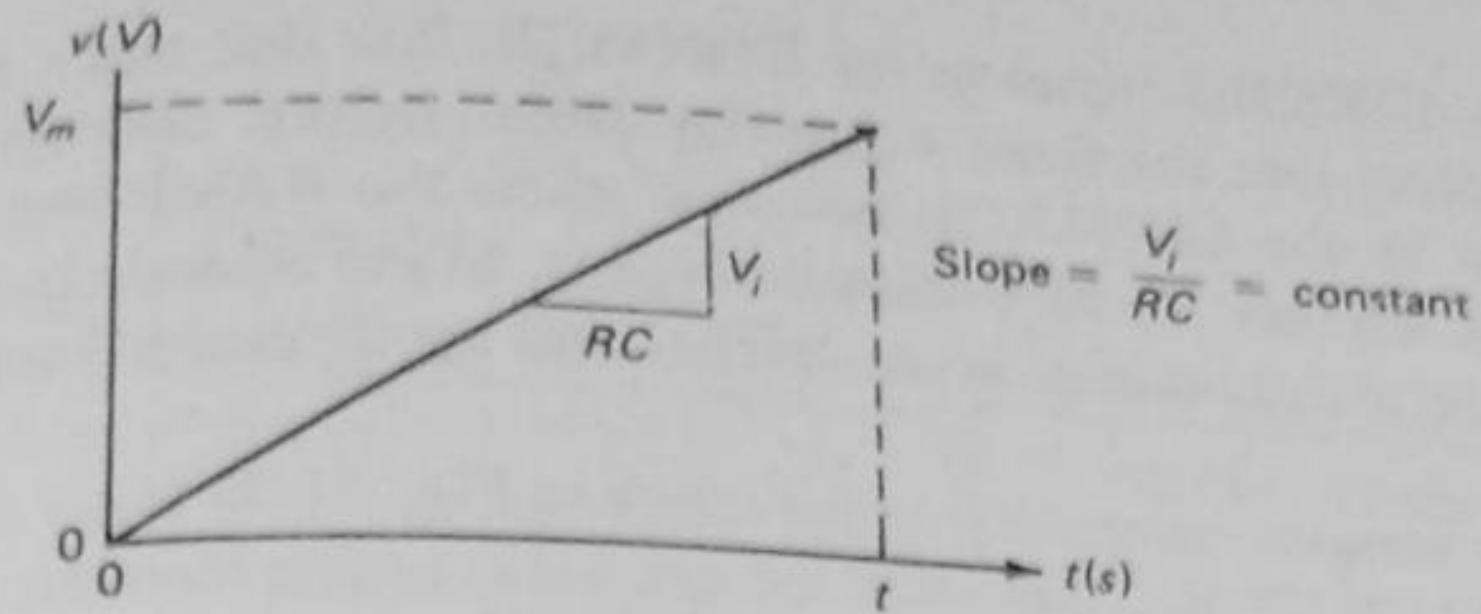
(a)



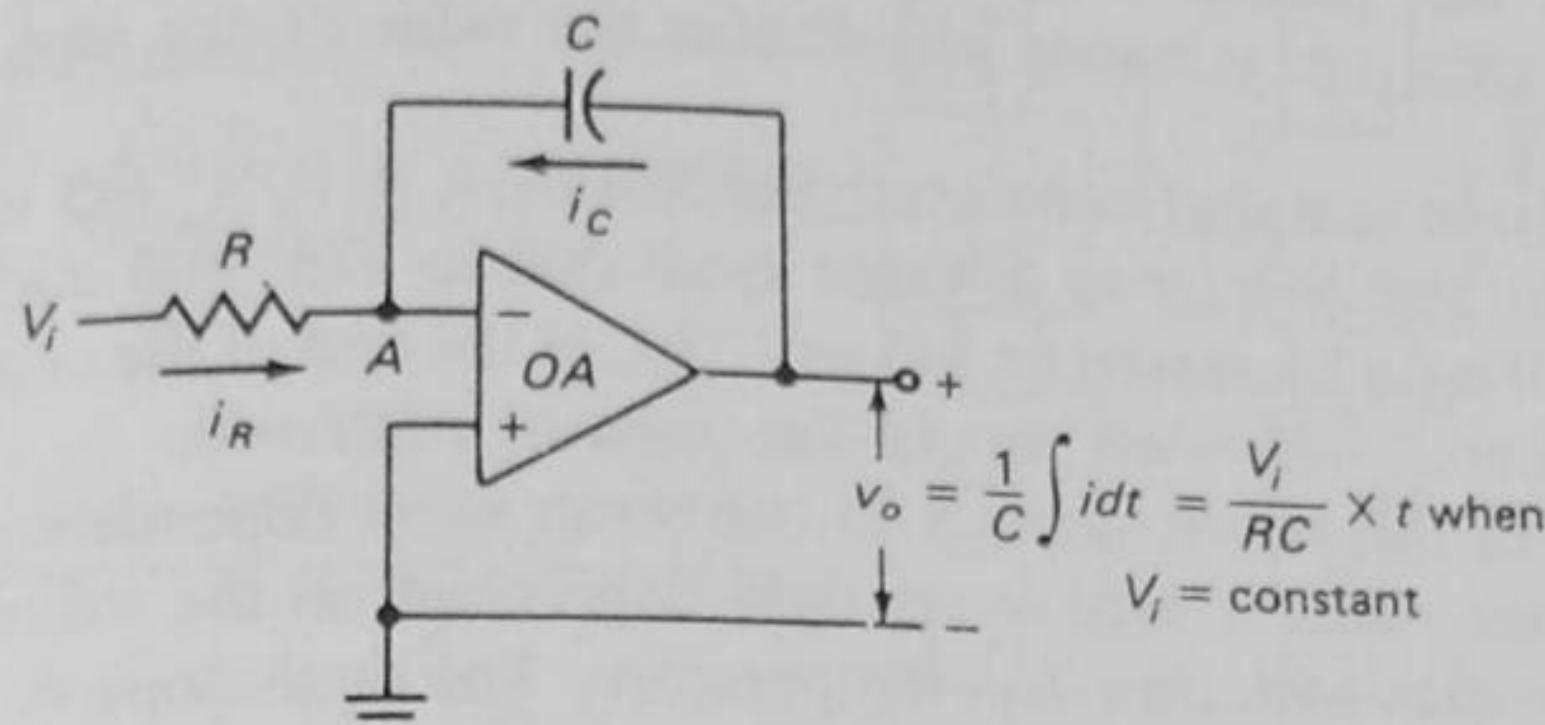
(b)

Fig. 11-32 Single-slope A/D converter.

of this
ramp as
up to a
it must
amp to



(a)



(b)

Fig. 11-33 An integrating circuit.

This ramp generator can be constructed in a number of different ways. One way might be to use a D/A converter driven by a simple binary counter. This would generate the staircase waveform previously discussed and shown in Fig. 11-16a. A second method is to use an operational amplifier (OA) connected as an integrator as shown in Fig. 11-33b. For this circuit, if V_i is a constant, the output voltage is given by the relationship $V_o = (V_i/RC)t$. Since V_i , R , and C are all constants, this is the equation of a straight line that has a slope (V_i/RC) as shown in Fig. 11-33a. Now that we have a way to generate a voltage ramp and we understand its characteristics, let's return to the converter in Fig. 11-32.

We assume that the clock is running continuously and that any input voltage V_x that we wish to digitize is positive. If it is not, there are circuits that we can use to adjust for negative input signals. The three decade counters are connected in cascade, and their outputs can be strobed into three 4-flip-flop latch circuits. The latches are then decoded by seven-segment decoders to drive the LED displays as units, tens, and hundreds of counts. We can begin a conversion cycle by depressing the MANUAL RESET switch.

Refer carefully to the logic diagram and the waveforms in Fig. 11-32. MANUAL RESET generates a RESET pulse that clears all the decade counters to 0s and resets the ramp voltage to zero. Since V_x is positive and RAMP begins at zero, the output of the comparator OA, V_c , must be high. This voltage enables the CLOCK gate allowing the clock, CLK, to be applied to the decade counter. The counter begins counting upward, and the RAMP continues upward until the ramp voltage is equal to the unknown input V_x .

At this point, time t_1 , the output of the comparator V_c goes low, thus disabling the CLOCK gate and the counters cease to advance. Simultaneously, this negative transition

D/A CONVERSION AND A/D CONVERSION

on V_c generates a STROBE signal in the CONTROL box that shifts the contents of the three decade counters into the three 4-flip-flop latch circuits. Shortly thereafter, a reset pulse is generated by the CONTROL box that resets the RAMP and clears the decade counters to 0s, and another conversion cycle begins. In the meantime, the contents of the previous conversion are contained in the latches and are displayed on the seven-segment LEDs.

As a specific example, suppose that the clock in Fig. 11-32 is set at 1.0 MHz and the ramp voltage slope is 1.0 V/ms. Note that the decade counters have the ability to store and display any decimal number from 000 up to 999. From the beginning of a conversion cycle, it will require 999 clock pulses (999 μ s) for the counters to advance full scale. During this same time period, the ramp voltage will have increased from 0.0 V up to 999 mV. So, this circuit as it stands will display the value of any input voltage between 0.0 V and 999 mV.

In effect, we have a digital voltmeter! For instance, if $V_X = 345$ mV, it will require 345 clock pulses for the counter to advance from 000 to 345, and during the same time period the ramp will have increased to 345 mV. So, at the end of the conversion cycle, the display output will read 345—we supply the units of millivolts.

One weakness of the single-slope A/D converter is its dependency on an extremely accurate ramp voltage. This in turn is strongly dependent on the values of R and C and variations of these values with time and temperature. The dual-slope A/D converter overcomes these problems.

DUAL-SLOPE A/D CONVERTER

The logic diagram for a basic dual-slope A/D converter is given in Fig. 11-34. With the exception of the ramp generator and the comparator, the circuit is similar to the single-slope A/D converter in Fig. 11-32. In this case, the integrator forms the desired ramp—in fact, two different ramps—as the input is switched first to the unknown input voltage V_X and then to a known reference voltage V_r . Here's how it works.

We begin with the assumptions that the clock is running, and that the input voltage V_X is positive. A conversion cycle begins with the decade counters cleared to all 0s, the ramp reset to 0.0 V, and the input switched to the unknown input voltage V_X . Since V_X is positive, the integrator output V_c will be a negative ramp. The comparator output V_g is thus positive and the clock is allowed to pass through the CLOCK GATE to the counters. We allow the ramp to proceed for a fixed time period t_1 , determined by the count detector for time t_1 . The actual voltage V_c at the end of the fixed time period t_1 will depend on the unknown input V_X , since we know that $V_c = -(V_X/RC) \times t_1$ for an integrator.

When the counter reaches the fixed count at time t_1 , the CONTROL unit generates a pulse to clear the decade counters to all 0s and switch the integrator input to the negative reference voltage V_r . The integrator will now begin to generate a ramp beginning at $-V_c$ and increasing steadily upward until it reaches 0.0 V. All this time, the counter is counting, and the conversion cycle ends when $V_c = 0.0$ V since the CLOCK GATE is now disabled. The equation for this positive ramp is $V_c = (V_r/RC) \times t_2$. In this case, the slope of this ramp (V_r/RC) is constant, but the time period t_2 is variable.

In fact, since the integrator output voltage begins at 0.0 V, integrates down to $-V_c$, and then integrates back up to 0.0 V, we can equate the two equations given for V_c . That is:

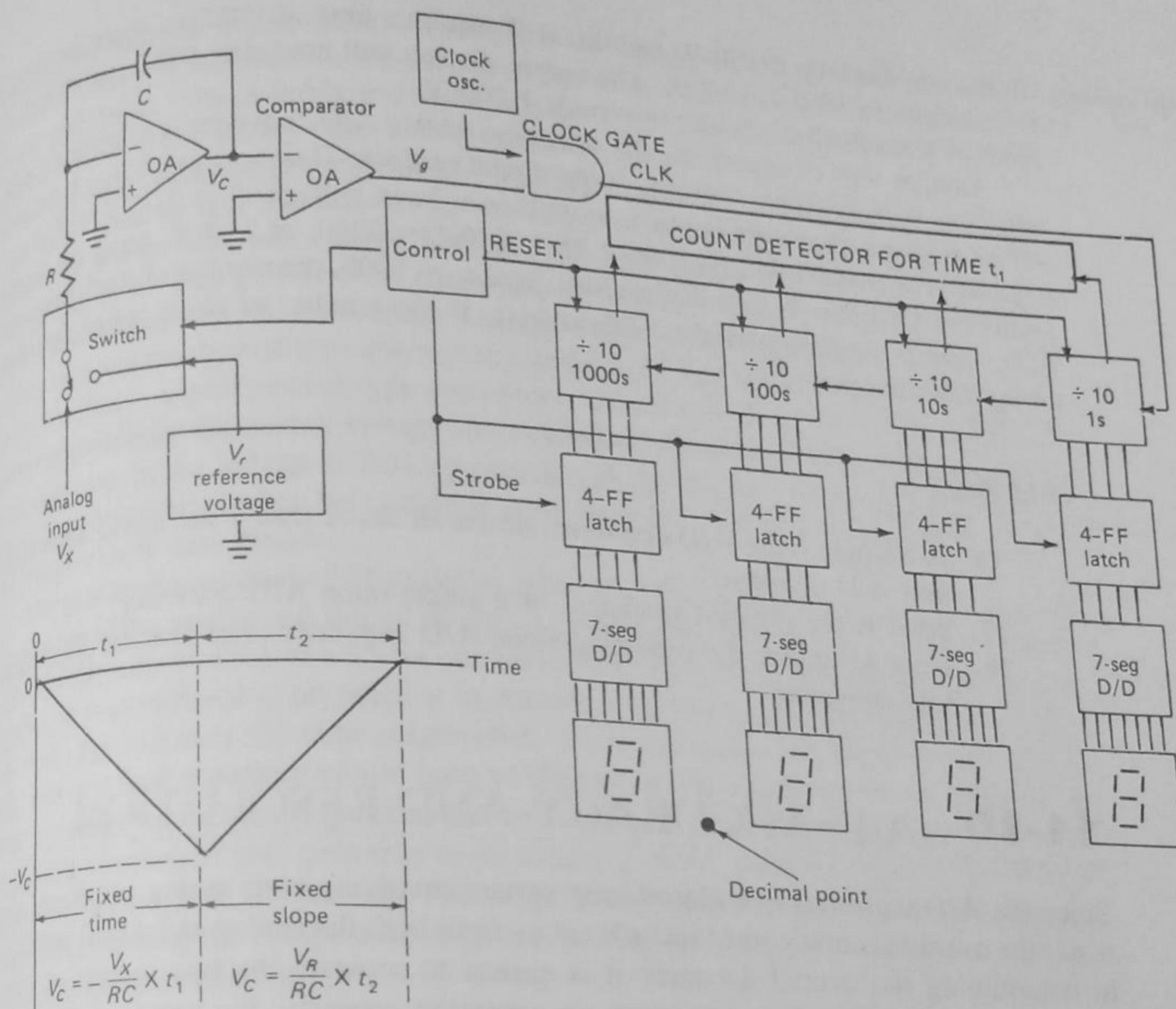


Fig. 11-34 Dual-slope A/D converter.

$$\frac{V_x}{RC} \times t_1 = \frac{V_r}{RC} \times t_2$$

The value RC will cancel from both sides, leaving

$$V_x = V_r \times \frac{t_2}{t_1}$$

Since V_r is a known reference voltage and t_1 is a predetermined time, clearly the unknown input voltage is directly proportional to the variable time period t_2 . However, this time period is exactly the contents of the decade counters at the end of a conversion cycle! The obvious advantage here is that the RC terms cancel from both sides of the equation above—in other words, this technique is free from the absolute values of either R or C and also from variations in either value.

As a concrete example, let's suppose that the clock in Fig. 11-34 is 1.0 MHz, the reference voltage is -1.0 Vdc, the fixed time period t_1 is $1000\ \mu s$, and the RC time constant of the integrator is set at $RC = 1.0$ ms. During the time period t_1 , the integrator voltage V_c will ramp down to -1.0 Vdc if $V_x = 1.0$ V. Then, during time t_2 , V_c will ramp

all the way back up to 0.0 V, and this will require a time of $1000 \mu s$, since the slope of this ramp is fixed at 1.0 V/ms . The output display will now read 1000, and with placement of a decimal as shown, this reads 1.000 V.

Another way of expressing the operation of this A/D converter is to solve the equation $V_X = V_r(t_2/t_1)$ for t_2 , since t_2 is the digital readout. Thus $t_2 = (V_X/V_r)t_1$. If the same values as given above are applied, an unknown input voltage $V_X = 2.75 \text{ V}$ will be digitized and the readout will be $t_2 = (2.75/1.0)1000 = 2750$, or 2.75 V, using the decimal point on the display. Notice that we have used $t_1 = 1000$, the number of clock pulses that occur during the time period t_1 . Likewise, t_2 is the number of clock pulses that occur during the time period t_2 .

SELF-TEST

16. Is a single-ramp A/D converter slower or faster than a successive-approximation A/D converter?
17. What is the greatest weakness of a single-ramp A/D converter?
18. What advantage does the dual-slope A/D converter offer over the single-ramp A/D converter?

11-10 A/D ACCURACY AND RESOLUTION

Since the A/D converter is a closed-loop system involving both analog and digital systems, the overall accuracy must include errors from both the analog and digital positions. In determining the overall accuracy it is easiest to separate the two sources of error.

If we assume that all components are operating properly, the source of the digital error is simply determined by the resolution of the system. In digitizing an analog voltage, we are trying to represent a continuous analog voltage by an equivalent set of digital numbers. When the digital levels are converted back into analog form by the ladder, the output is the familiar staircase waveform. This waveform is a representation of the input voltage but is certainly not a continuous signal. It is, in fact, a discontinuous signal composed of a number of discrete steps. In trying to reproduce the analog input signal, the best we can do is to get on the step which most nearly equals the input voltage in amplitude.

The simple fact that the ladder voltage has steps in it leads to the digital error in the system. The smallest digital step, or quantum, is due to the LSB and can be made smaller only by increasing the number of bits in the counter. This inherent error is often called the *quantization error* and is commonly ± 1 bit. If the comparator is centered, as with the continuous converter, the quantization error can be made $\pm \frac{1}{2}$ LSB.

The main source of analog error in the A/D converter is probably the comparator. Other sources of error are the resistors in the ladder, the reference-voltage supply ripple, and noise. These can, however, usually be made secondary to the sources of error in the comparator.

The sources of error in the comparator are centered around variations in the dc switching point. The dc switching point is the difference between the input voltage levels

that cause the output to change state. Variations in switching are due primarily to offset, gain, and linearity of the amplifier used in the comparator. These parameters usually vary slightly with input voltage levels and quite often with temperature. It is these changes which give rise to the analog error in the system.

An important measure of converter performance is given by the differential linearity. Differential linearity is a measure of the variation in voltage-step size that causes the converter to change from one state to the next. It is usually expressed as a percent of the average step size. This performance characteristic is also a function of the conversion method and is best for the converters having counters that count continuously. The counter-type and continuous-type converters usually have better differential linearity than do the successive-approximation-type converters. This is true since the ladder voltage is always approaching the analog voltage from the same direction in the one case. In the other case, the ladder voltage is first on one side of the analog voltage and then on the other. The comparator is then being used in both directions, and the net analog error from the comparator is thus greater.

The next logical question that might be asked is: what should be the relative order of magnitudes of the analog and digital errors? As mentioned previously, it would be difficult to justify construction of a 15-bit converter that has an overall error of 1 percent. In general, it is considered good practice to construct converters having analog and digital errors of approximately the same magnitudes. There are many arguments for and against this, and any final argument would have to depend on the situation. As an example, an 8-bit converter would have a quantization error of $\frac{1}{256} \approx 0.4$ percent. It would then seem reasonable to construct this converter to an accuracy of 0.5 percent in an effort to achieve an overall accuracy of 1.0 percent. This might mean constructing the ladder to an accuracy of 0.1 percent, the comparator to an accuracy of 0.2 percent, and so on, since these errors are all accumulative.

Example 11-14

What overall accuracy could one reasonably expect from the construction of a 10-bit A/D converter?

Solution

A 10-bit converter has a quantization error of $\frac{1}{1024} \approx 0.1$ percent. If the analog portion can be constructed to an accuracy of 0.1 percent, it would seem reasonable to strive for an overall accuracy of 0.2 percent.

SUMMARY

Digital-to-analog conversion, the process of converting digital input levels into an equivalent analog output voltage, is most easily accomplished by the use of resistance networks. The binary ladder has been found to have definite advantages over the resistance divider. The complete D/A converter consists of a binary ladder (usually) and a flip-flop register to hold the digital input information.

D/A CONVERSION AND A/D CONVERSION

The simultaneous method for A/D conversion is very fast but becomes cumbersome for more than a few bits of resolution. The counter-type A/D converter is somewhat slower but represents a much more reasonable solution for digitizing high-resolution signals. The continuous-converter method, the successive-approximation method, and the section-counter method are all variations of the basic counter-type A/D converter which lead to a much faster conversion time. A dual-slope A/D converter is somewhat slower than the previously discussed methods but offers excellent accuracy in a relatively inexpensive circuit. Dual-slope A/D converters are widely used in digital voltmeters.

The D/A converter and A/D converter logic circuits given in this chapter are all drawn in logic block diagram form and can all be constructed by simply connecting these commercially available logic blocks. For instance, a D/A converter can be constructed by connecting resistors that have values of R and $2R$, or an A/D converter can be constructed by connecting the various inverters, gates, flip-flops, and so on; however, you must realize that these units are now readily available as MSI circuits. The only really practical and economical way to build D/A converters or A/D converters is to make use of these commercially available circuits; this is exactly the subject pursued in the next chapter.

GLOSSARY

A/D conversion The process of converting an analog input voltage to a number of equivalent digital output levels.

binary equivalent weight The value assigned to each bit in a digital number, expressed as a fraction of the total. The values are assigned in binary fashion according to the sequence 1, 2, 4, 8, . . . , 2^n , where n is the total number of bits.

D/A conversion The process of converting a number of digital input signals to one equivalent analog output voltage.

differential linearity A measure of the variation in size of the input voltage to an A/D converter which causes the converter to change from one state to the next.

Millman's theorem A theorem from network analysis which states that the voltage at any node in a resistive network is equal to the sum of the currents entering the node divided by the sum of the conductances connected to the node, all determined by assuming that the voltage at the node is zero.

monotonicity A consistent increase in output in response to a consistent increase in input (voltage or current).

quantization error The error inherent in any digital system due to the size of the LSB.

SAR Sequential approximation register, used in a sequential A/D converter.

PROBLEMS

SECTION 11-1

- 11-1 What is the binary equivalent weight of each bit in a 6-bit resistive divider?
- 11-2 Draw the schematic for a 6-bit resistive divider.
- 11-3 Verify the voltage output levels for the network in Fig. 11-4, using Millman's theorem. Draw the equivalent circuits.

11-4 Assume that the divider in Prob. 11-2 has +10 V full-scale output, and find the following:

- a. The change in output voltage due to a change in the LSB
- b. The output voltage for an input of 110110

11-5 A 10-bit resistive divider is constructed such that the current through the LSB resistor is 100 μ A. Determine the maximum current that will flow through the MSB resistor.

SECTIONS 11-2, 11-3, 11-4

11-6 What is the full-scale output voltage of a 6-bit binary ladder if 0 = 0 V and 1 = +10 V? Of an 8-bit ladder?

11-7 Find the output voltage of a 6-bit binary ladder with the following inputs:

- a. 101001
- c. 110001
- b. 111011

11-8 Check the results of Prob. 11-7 by adding the individual bit contributions.

11-9 What is the resolution of a 12-bit D/A converter which uses a binary ladder? If the full-scale output is +10 V, what is the resolution in volts?

11-10 How many bits are required in a binary ladder to achieve a resolution of 1mV if full scale is +5 V?

SECTION 11-5

11-11 How many comparators are required to build a 5-bit simultaneous A/D converter?

11-12 Redesign the encoding matrix and READ gates in Fig. 11-20, using NAND gates.

11-13 Assuming that the input reference voltage is $V = 10.0$ Vdc, determine the digital output of the A/D converter in Fig. 11-21a for an input voltage of:

- a. 1.25 V
- c. 8.05 V
- b. 3.33 V

SECTION 11-6

11-14 Find the following for a 12-bit counter-type A/D converter using a 1-MHz clock:

- a. Maximum conversion time
- b. Average conversion time
- c. Maximum conversion rate

11-15 What clock frequency must be used with a 10-bit counter-type A/D converter if it must be capable of making at least 7000 conversions per second?

11-16 Design additional control circuitry for Fig. 11-24 such that the A/D converter in Fig. 11-23 will continue to make conversions after an initial START pulse is applied.

SECTIONS 11-7 AND 11-8

11-17 What is the conversion time of a 12-bit successive-approximation-type A/D converter using a 1-MHz clock?

11-18 What is the conversion time of a 12-bit section-counter-type A/D converter using a 1-MHz clock? The counter is divided into three equal sections.

SECTION 11-9

- 11-19 For the integrator in Fig. 11-33, show that the output voltage is given by $V_o = (V_i/RC)t$, assuming that the input voltage V_i is a constant. [Hint: Using Kirchhoff's current law at node A, the resistor current i_R is equal to the capacitor current i_C , but $i_R = V_i/R$ and $i_C = q/t = (V_o C)/t$.]
- 11-20 Design the control logic for the CONTROL box in Fig. 11-32 to generate the proper control signals shown in that figure.
- 11-21 Calculate a value for C in Fig. 11-33 to obtain a fixed slope $V_i/(RC) = 1000 \text{ V/s}$, given $V_i = 1.0 \text{ Vdc}$ and $R = 100 \text{ k}\Omega$.
- 11-22 Can you design an amplifier such that the output is always positive and is equal to the magnitude of the input voltage? In other words, the input can be either $+V_i$ or $-V_i$, but in either case, the output will be $+V_i$.
- 11-23 Design the CONTROL logic for the converter in Fig. 11-34.

SECTION 11-10

- 11-24 What overall accuracy could you reasonably expect from a 12-bit A/D converter?
- 11-25 Discuss the overall acceptable accuracy of a 10-bit A/D converter in terms of quantization error, ladder accuracy, comparator accuracy, converter accuracy, and other factors.

ANSWERS TO SELF-TESTS

1. $1/63$
2. $30/15 = 2 \text{ V}$
3. 0.15625 V
4. 9.84375 V
5. A monotonicity test checks to see that the D/A output voltage increases regularly as the input digital signals increase.
6. $+5 \text{ Vdc}$
7. Resolution = $10/256 = 39.06 \text{ mV}$
8. Its conversion time is very fast.
9. Possibilities include radar signal processing, video displays, high-speed instrumentation, and television broadcasting.
10. $128 \mu\text{s}$
11. $64 \mu\text{s}$
12. The continuous type A/D converter uses an up-down counter.
13. The continuous type A/D converter is faster than the counter-type A/D converter.
14. SAR stands for successive-approximation register.
15. The ADC0804 is an 8-bit CMOS successive-approximation A/D converter.
16. Slower
17. One major weakness of the single-slope A/D converter is that it is extremely sensitive to variations in ramp voltage and hence to errors in ramp voltage.
18. The RC time constant cancels out, making the conversion much less sensitive to variations in ramp voltage accuracy.