Project 55: Fractional Divider

A Comprehensive Study of Advanced Digital Circuits

By: Abhishek Sharma , Ayush Jain , Gati Goyal, Nikunj Agrawal

Documentation Specialist: Dhruv Patel & Nandini Maheshwari

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1 Project Overview

A fractional divider is a circuit or system that divides an input frequency by a non-integer (fractional) value. It's commonly used in digital frequency synthesis, where precise frequency control is necessary, but the desired output frequency isn't an integer multiple of the input clock. This is especially useful in applications such as phase-locked loops (PLLs), where precise frequency control can be essential for synchronization in communication systems, digital signal processing, and clock generation circuits.

2 Fractional Divider

2.1 Key Concept of Fractional Divider

- **Fractional Division Ratio:**

Unlike an integer divider, which divides by whole numbers (e.g., 2, 3, 4), a fractional divider achieves a division by fractional numbers (e.g., 1.5, 2.25). This is done by switching between nearby integer values in a controlled pattern to yield an average that represents the fractional ratio.

- **Sigma-Delta Modulation:**

A popular technique for implementing fractional dividers, sigma-delta modulation changes the divider between two or more integer values at a high rate to achieve the desired fractional average. This method reduces phase noise and jitter, enhancing the stability of the output frequency.

- **Phase Accumulation:**

Phase accumulation involves counting input cycles and periodically altering the divider ratio based on a fractional remainder. This approach ensures that the average output frequency matches the desired fractional division.

- **Jitter and Stability:**

Since fractional division involves varying the divider ratio, it introduces phase noise or jitter in the output signal. Techniques like filtering or using sigma-delta modulation help mitigate these effects, ensuring a stable output.

- **Applications in Frequency Synthesis:**

Fractional dividers are essential in frequency synthesis systems, especially in fractional-N PLLs, where they allow for finely adjustable output frequencies. This is crucial for applications requiring precise timing, such as communication systems, RF circuits, and digital systems with strict clock requirements.

2.2 Working of Fractional Divider

- **Define the Desired Division Ratio:**

The target fractional division ratio is set (e.g., 2.5), indicating that the output frequency will be a fraction of the input frequency.

- **Switch Between Integer Divisions:**

To approximate the fractional ratio, the divider alternates between two nearby integer values. For example, for a division ratio of 2.5, it alternates between 2 and 3.

- **Modulate the Switching Pattern:**

A modulation scheme (often sigma-delta modulation) controls the switching pattern between the integer dividers. This results in an average division that equals the target fractional value over time.

- **Accumulate Phase or Count Cycles:**

A phase accumulator or counter keeps track of input clock cycles and adjusts the division ratio based on the accumulated phase or fractional remainder, maintaining synchronization with the desired frequency.

- **Output the Averaged Frequency:**

The alternation between division ratios produces an output that, on average, achieves the desired fractional frequency. For example, dividing by 2 half the time and by 3 the other half gives an effective division of 2.5.

- **Filter and Smooth the Output:**

Additional filtering or smoothing may be applied to reduce jitter and stabilize the output signal, especially when precise timing is required.

- **Utilize in Frequency Synthesis or PLL Systems:**

The stable, fractional output frequency can then be used in systems like PLLs for precise frequency control, essential in applications like RF communication and digital clocks.

2.3 RTL Code

Listing 1: Fractional Divider

```
1
2  module FractionalDivider #(parameter WIDTH = 8) (
3      input logic [WIDTH-1:0] dividend,
4      input logic [WIDTH-1:0] divisor,
5      output logic [2*WIDTH-1:0] quotient
6  );
7      always_comb begin
8          if (divisor != 0) begin
9              quotient = (dividend << WIDTH) / divisor; // Shift left to
                   handle fractional part
10         end else begin
11             quotient = '0; // undefined if divisor is 0
12         end
13     end
14 endmodule
```

2.4 Testbench

Listing 2: Fractional Divider

```
1
2
3  module FractionalDivider_tb;
4      parameter WIDTH = 8;
5      logic [WIDTH-1:0] dividend, divisor;
6      logic [2*WIDTH-1:0] quotient;
7
8      // Instantiate the Fractional Divider
9      FractionalDivider #(.WIDTH(WIDTH)) uut (
10         .dividend(dividend),
11         .divisor(divisor),
12         .quotient(quotient)
13     );
14
15     initial begin
```

```
        // Test case 1: Simple fractional division
        dividend = 5; divisor = 2;
        #10;
        $display("Dividend=%0d, Divisor=%0d, Quotient=%0d (fractional
            result)", dividend, divisor, quotient);

        // Test case 2: Exact division
        dividend = 16; divisor = 4;
        #10;
        $display("Dividend=%0d, Divisor=%0d, Quotient=%0d (exact
            result)", dividend, divisor, quotient);

        // Test case 3: Division by zero
        dividend = 10; divisor = 0;
        #10;
        $display("Dividend=%0d, Divisor=%0d, Quotient=%0d (undefined
            for zero divisor)", dividend, divisor, quotient);

        $finish;
    end
endmodule
```

3 Results

3.1 Simulation

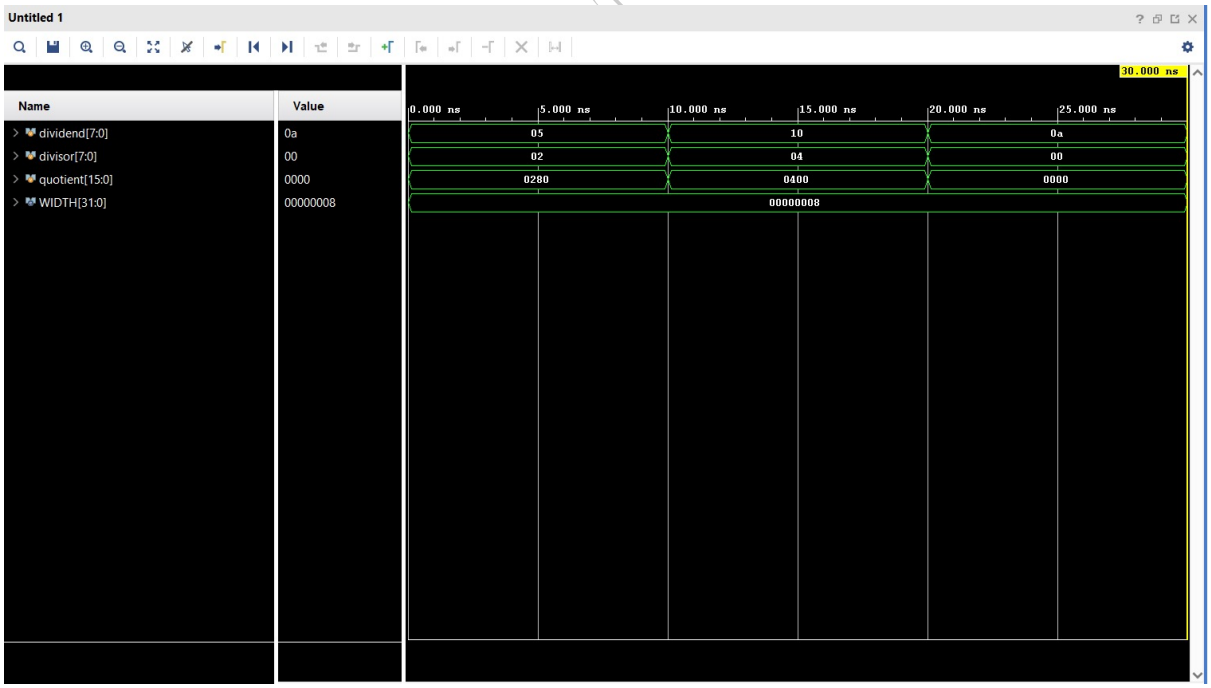

Figure 1: Simulation of Fractional Divider

3.2 Schematic

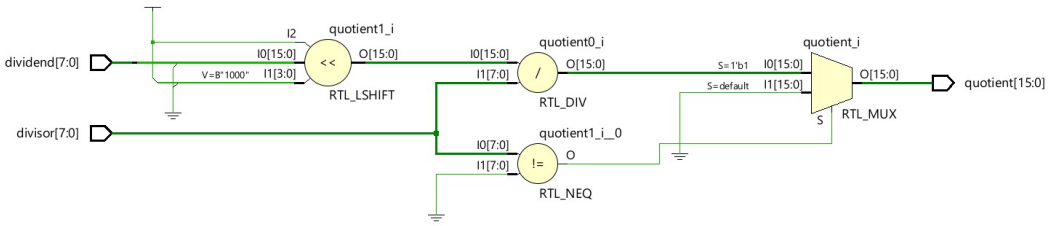

Figure 2: Schematic of Fractional Divider

3.3 Synthesis Design

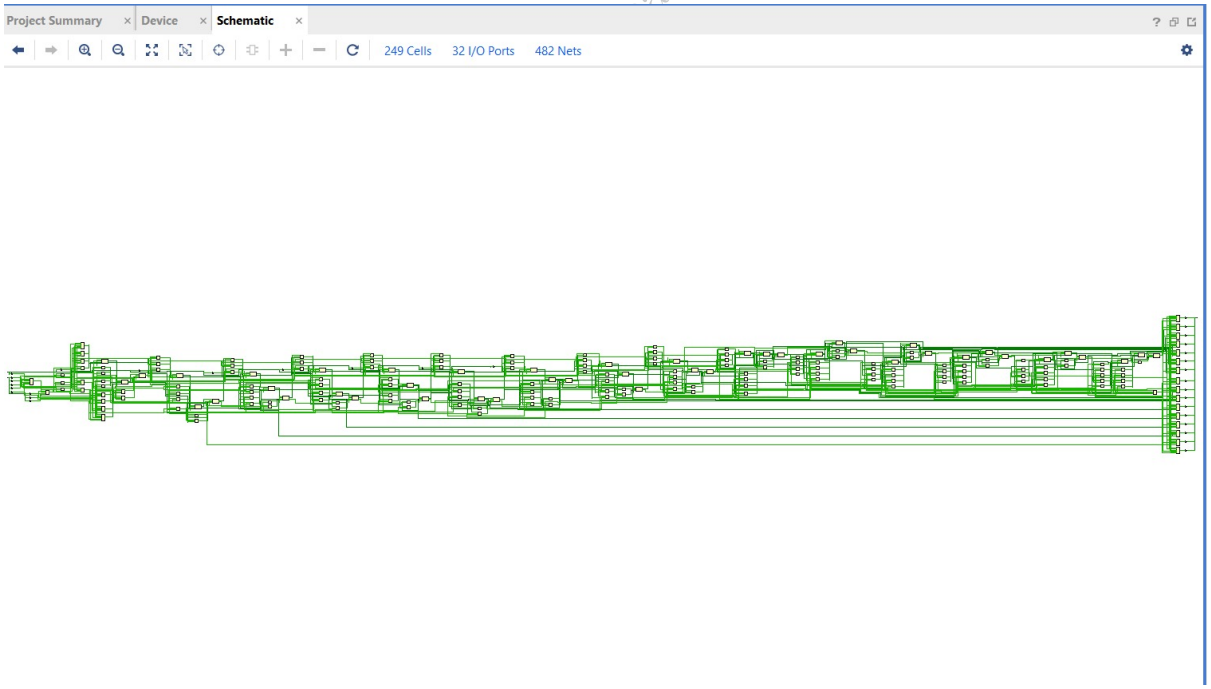

Figure 3: Synthesis Design of Fractional Divider

4 Advantages of Fractional Divider

- **Fine Frequency Resolution:**

Fractional dividers allow for very fine adjustments to the output frequency, enabling precise frequency synthesis that integer dividers cannot achieve. This is crucial for applications requiring high accuracy.

- **Versatility in Frequency Generation:**

Fractional dividers enable the generation of non-integer-related frequencies, making them versatile for a wide range of applications where specific, non-standard frequencies are needed.

- **Improved Frequency Synthesis in PLLs:**

In fractional-N PLLs, fractional dividers allow for smaller step sizes in frequency tuning, improving the flexibility and performance of the system in RF and communication applications.

- **Reduced Power Consumption:**

By enabling finer control, fractional dividers can allow for low-power designs in clock generation circuits, as they can achieve desired frequencies without requiring high-frequency clocks as inputs.

5 Disadvantages of Fractional Divider

- **Phase Noise and Jitter:**

Fractional dividers can introduce phase noise and jitter due to the constant switching between integer division ratios. This can affect the stability of the output signal, especially in sensitive applications.

- **Increased Complexity:**

Implementing fractional division typically requires additional control circuitry (e.g., sigma-delta modulators or phase accumulators) to manage the division pattern, making the design more complex.

- **Filtering Requirements:**

To mitigate the jitter and phase noise introduced, additional filtering or smoothing circuits are often needed. This increases the overall system complexity and may require additional components.

- **Potential for Higher Design Cost:**

Due to the complexity of design and additional components needed for smoothing and filtering, fractional dividers can increase both design and manufacturing costs.

6 Applications of Fractional Divider

- **Fractional-N Phase-Locked Loops (PLLs):**

Fractional dividers are widely used in fractional-N PLLs to achieve precise frequency control with small step sizes. This is critical for frequency synthesis in RF communication systems, such as mobile phones, Wi-Fi, and Bluetooth devices.

- **Clock Generation in Digital Systems:**

Many digital circuits require precise, non-standard clock frequencies. Fractional dividers allow for exact frequency matching, helping to ensure synchronous operation in complex digital systems like microcontrollers and FPGAs.

- **Data Conversion Systems (ADCs and DACs):**

In analog-to-digital and digital-to-analog converters, fractional dividers can provide finely-tuned clock signals that improve data sampling rates and accuracy.

- **Wireless Communication Systems:**

Many wireless protocols require precise carrier frequencies and local oscillators. Fractional dividers provide the flexibility needed to tune these frequencies exactly, which is critical for multi-band or multi-standard devices.

- **High-Speed Serial Interfaces:**

High-speed serial communication protocols, like USB and PCIe, rely on exact clock frequencies for data integrity. Fractional dividers in clocking circuits ensure the required frequency is maintained.

7 Summary

The essence of a fractional divider lies in achieving an accurate fractional division of frequency by averaging over time, which allows it to generate frequencies that are not whole-number multiples of the input.

8 FAQs

1. What is a fractional divider, and how is it different from an integer divider?
A fractional divider divides an input frequency by a non-integer (fractional) number, while an integer divider divides by a whole number. Fractional dividers achieve this by alternating between two or more integer division ratios to produce an average frequency that meets the fractional requirement.

2. How does a fractional divider achieve non-integer division?
Fractional dividers alternate between nearby integer division ratios (e.g., dividing by 2 and 3) in a controlled pattern, so the output frequency averages to a desired fractional value. Techniques like sigma-delta modulation help to control this switching and reduce phase noise.

3. What is sigma-delta modulation in fractional dividers, and why is it used?
Sigma-delta modulation is a technique used to control the division ratio in fractional dividers. By dynamically adjusting the division between two integers in a specific pattern, it creates a fractional average with minimal phase noise. This makes it particularly useful in high-performance applications like PLLs.

4. Why are fractional dividers important in PLLs?
Fractional dividers in fractional-N PLLs allow for fine frequency tuning and smaller steps between frequencies, which is essential for precise frequency synthesis. This is important in applications like RF communication and clock generation, where exact frequencies are necessary.

5. What are the main advantages of using a fractional divider?
The main advantages include fine frequency resolution, versatility in generating non-integer frequencies, improved performance in frequency synthesis, and potential power savings in clocking circuits due to lower frequency inputs.

6. What are some common applications of fractional dividers?
Fractional dividers are used in fractional-N PLLs, clock generation for digital systems, data conversion systems (ADCs and DACs), wireless communication, and high-speed serial interfaces (like USB and PCIe), where precise frequency control is critical.

7. What are the challenges or disadvantages of using fractional dividers?
Some key challenges include phase noise and jitter due to the alternating division ratios, increased design complexity, and the need for additional filtering or smoothing to stabilize the output signal. This

can also raise design and production costs.

8. How does phase noise affect fractional dividers?

Phase noise results from the switching between integer divisions, causing small timing variations or jitter in the output signal. This noise can degrade the performance in applications requiring highly stable frequencies, such as RF communication.

9. How is jitter managed in fractional dividers?

Techniques like sigma-delta modulation reduce phase noise, while additional filtering or smoothing circuits can help mitigate jitter. In PLLs, loop filters also play a key role in stabilizing the output frequency.

10. What's the difference between a fractional divider and a programmable divider?

A programmable divider allows for division by multiple integers, selectable at any given time, while a fractional divider specifically targets fractional ratios by switching between integer values in a controlled pattern to achieve a fractional average.

11. Can fractional dividers be used in digital circuits only?

No, fractional dividers are used in both analog and digital systems, especially in mixed-signal applications like RF transceivers, PLLs, and ADCs/DACs, where precise timing and frequency control are essential.

12. How does phase accumulation work in fractional dividers?

In phase accumulation, an internal counter tracks the input cycles and adjusts the division ratio based on the accumulated phase. This method ensures the output frequency averages to the desired fractional frequency.