Abhishek Sharma

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abhishek-sharma-19april1965 | Abhishek-Sharma182005 | Portfolio

Objective

Final-year Engineering student specializing in VLSI Embedded Systems, with practical expertise in RISC-V pipelined processor design, AXI4-Lite interfaces, and end-to-end RTL-to-GDSII flows. National winner at Smart India Hackathon 2024, current Techtronica Society President, and mentor to 100+ peers in digital design and SoC development. Experienced in FPGA prototyping, edge communication systems, and embedded AI solutions. Passionate about building silicon with purpose—bridging hardware-software co-design and aligned with the India Semiconductor Mission. Excited to contribute to high-impact projects at the intersection of systems, scale, and AI.

Experience

- **ProV Logic** *Hyderabad, India*
  VLSI Design Intern Feb 2025 – June 2025
  – Led design and verification of a 5-stage pipelined RISC-V processor using Verilog on Vivado.
  – Gained hands-on experience in RTL debugging, simulation, and SoC integration flows.
- **Semiconductor Laboratory (MeiTY, Govt. of India)** *Chandigarh, India*
  Advanced VLSI Design Intern June 2024 – July 2024
  – Designed and simulated a Low Noise Amplifier (LNA) for satellite navigation systems.
  – Published research paper; explored CMOS flows and semiconductor process technologies.
- **FlexiGate Technologies** *New Delhi, India*
  Hardware Design Intern Mar 2024 – Sept 2024
  – Designed and tested ESP32 and RS-232-based PCBs for embedded communication systems.
- **CSIR-CEERI** *Pilani, India*
  Engineering Trainee Jan 2024
  – Completed SHILP program with cleanroom exposure to semiconductor fabrication and CMOS tech.
- **Techtronica Society, GLA University** *Sept 2023 – Present*
  President
  – Conducted VLSI and Embedded workshops, hackathons, and guest sessions on RISC-V and AI.
  – Mentored 100+ students on projects, tools, and industry readiness.

Projects

- **Embedded Edge Communication Node**
  Tools: Tiva C, UART, Python May 2025
  – Designed a real-time UART-based embedded system using Tiva C and Raspberry Pi for serial data communication.
  – Implemented live data logging and plotting via Python for edge systems.
- **AI-Driven Optimization of RISC-V Cores (Ongoing)**
  Tools: Basilisk RV64GC, Yosys, OpenROAD, Vivado June – December 2025
  – Developing AutoML and reinforcement learning-based flow to optimize RISC-V cores from ISA to layout.
  – Focusing on power, performance, and area (PPA) gains with FPGA-based validation.
- **5-Stage Pipelined RISC-V Processor**
  Tools: Verilog, Vivado March 2025
  – Implemented a 5-stage pipelined RISC-V processor (IF, ID, EX, MEM, WB) with testbench verification.
  – Validated functionality using custom instruction programs and simulation waveforms.
- **AXI4-Lite Slave Interface – Design & Verification**
  Tools: Verilog, SystemVerilog, Vivado February 2025
  – Developed a synthesizable AXI4-Lite slave interface; verified with assertions and waveform inspection.
- **PragatiX – Wearable for Delivery Agents (SIH 2024 Winner)**
  Tools: Embedded C, Sensors, GitLab December 2024
  – Built a smart wearable device with sensor integration for real-time health monitoring of delivery personnel.
  – Led a 6-member team to a national win at Smart India Hackathon 2024.
- **RTL to GDSII Flow (108+ Projects)**
  Tools: Cadence Genus, Innovus November 2024
  – Executed RTL-to-GDSII implementation for ALUs, FSMs, and datapath modules using industry-standard tools.

Education

- **GLA University** — *Mathura, India*
  B.Tech in ECE (VLSI Specialization) — 2023 – 2026
  – CPI: 8.6/10
- **RBS Polytechnic** — *Agra, India*
  Diploma in Electronics Engineering (Modern Consumer) — 2020 – 2023
  – Score: 78.5%
- **R.B. Public School** — *Agra, India*
  High School (CBSE) — 2019 – 2020
  – Score: 85%

Patents & Publications

[J=Journal, P=Patent]

[J.1] **Sharma, A.**, Kalra, D., Kumar, M., & Bhatia, R. (2024). Design of CMOS Low Noise Amplifier with Inductive Degeneration for Navigation Application. *Journal of Electrical Engineering*, 75(6), 458-466.

[P.1] **Sharma, A.** et al. (2024). AI Based Traffic Management System. Patent No. 45/2024, Published: Nov 2024

[P.2] **Sharma, A.** et al. (2024). GSM Based Vehicle Accident Alert Smart System. Patent No. 48/2024, Published: Nov 2024

[P.3] **Sharma, A.** et al. (2025). PragatiX: AI-Driven Smart Wearables and Skill Empowerment for Delivery Workforce. Patent filed, Status: Under Review

[P.4] **Sharma, A.** et al. (2025). CodeQuest: A Personalized Learning and Challenge Platform for Enhancing Logical and Algorithmic Thinking. Patent filed, Status: Under Review

Technical Skills

- **Programming Languages:** C, Python, Embedded C, Shell Scripting
- **Hardware Interfaces:** UART, SPI, I2C, GPIO, Timers, AXI, Wishbone
- **Networking:** TCP/IP, Ethernet, Wireless Protocols
- **Tools & Frameworks:** Vivado, Yosys, OpenROAD, Cadence (Virtuoso, Genus, Innovus), MATLAB
- **Core Competencies:** RTL Design, SoC Integration, FPGA Prototyping, Embedded Systems, RISC-V Architecture

Achievements & Leadership

- **Winner & Team Lead – Smart India Hackathon 2024** — Dec 2024
  Ministry of Education, Govt. of India — Led national-winning team with IoT-based wearable solution for gig workers.
- **Instructor – Embedded Systems & PCB Design Workshops** — Oct 2024, Feb 2025
  Techtronica Society, GLA University — Conducted sessions on Arduino, Raspberry Pi, and PCB design for 70+ students.
- **Team Lead – 108 RTL Projects** — Aug 2024 – Dec 2024
  GLA University — Led RTL design and verification of 100+ digital blocks; focused on synthesis and modularity.
- **President – Techtronica Society, GLA University** — 2023 – Present
  Initiated technical events, hands-on workshops, and industry speaker sessions on VLSI, AI, and Embedded Systems.

Certifications

- **Cadence Design Systems (2024–2025)** — RTL to GDSII Flow, Semiconductor 101, Student Ambassador, Digital Physical Design, Front-End Digital Design
- **NPTEL (2024)** — C-Based VLSI Design, Computer Architecture, Introduction to IoT

Additional Information

- **Languages:** Hindi (Native), English (Fluent)
- **Interests:** DIY Projects, Nature Hiking, Embedded Systems, VLSI, AI in Semiconductors, Sci-Fi Reading