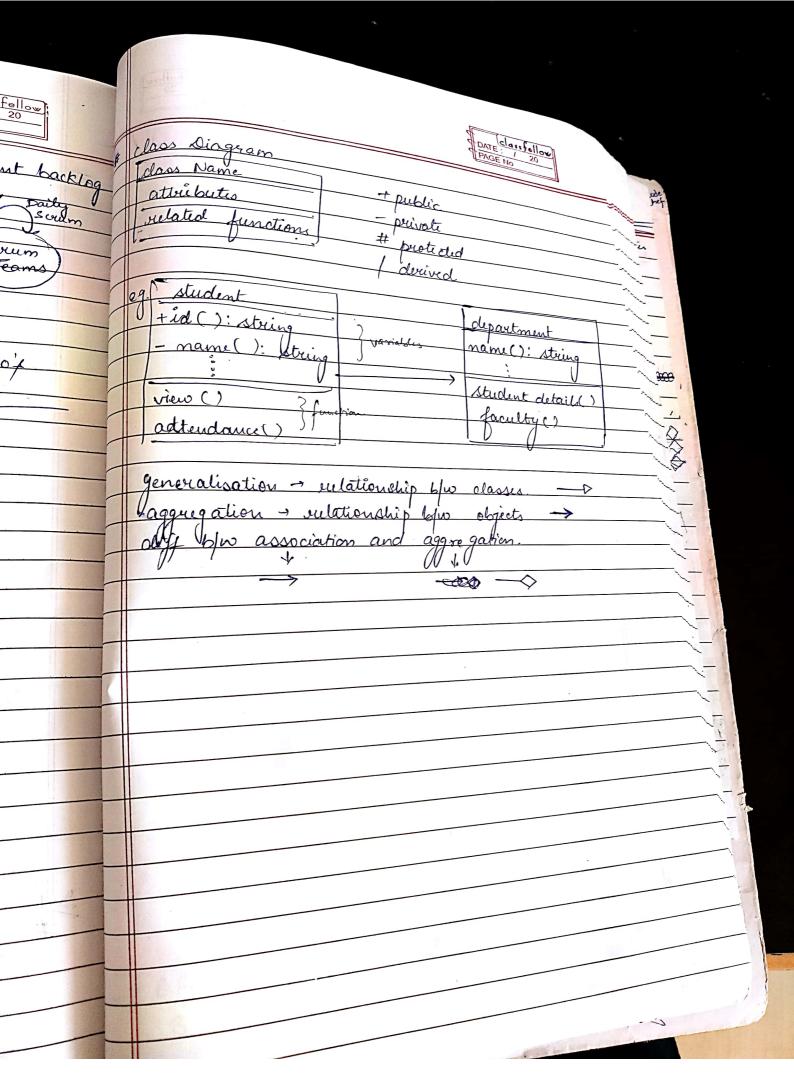
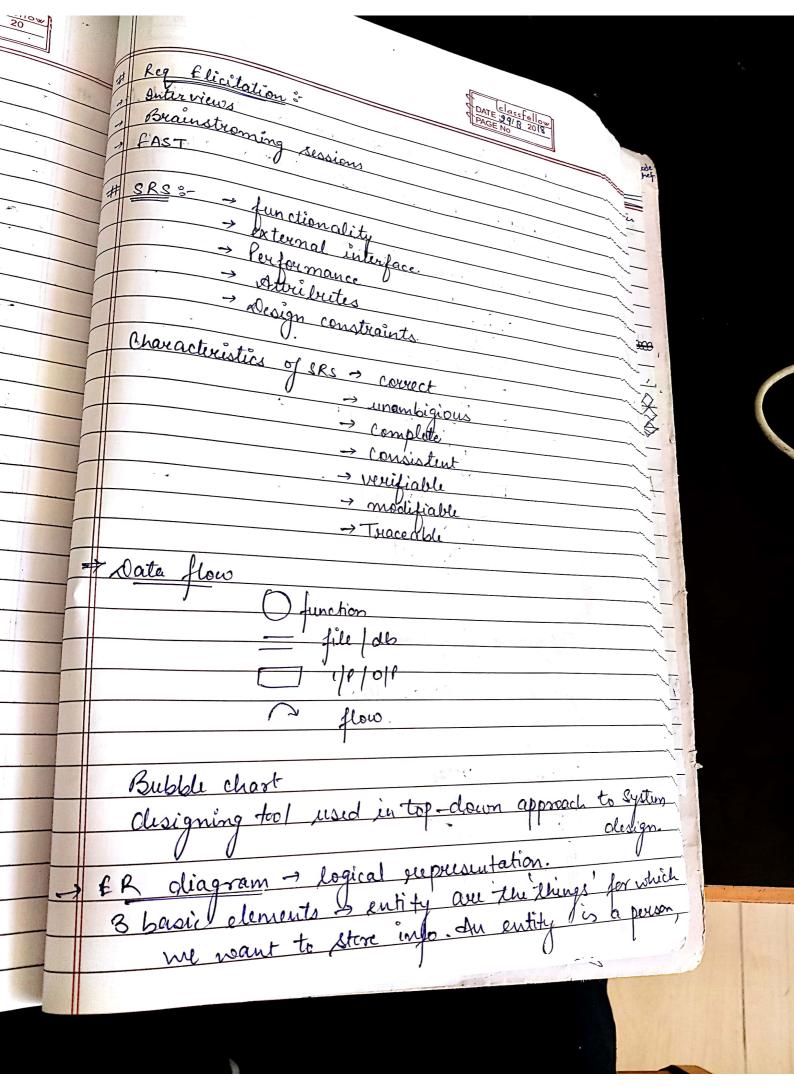
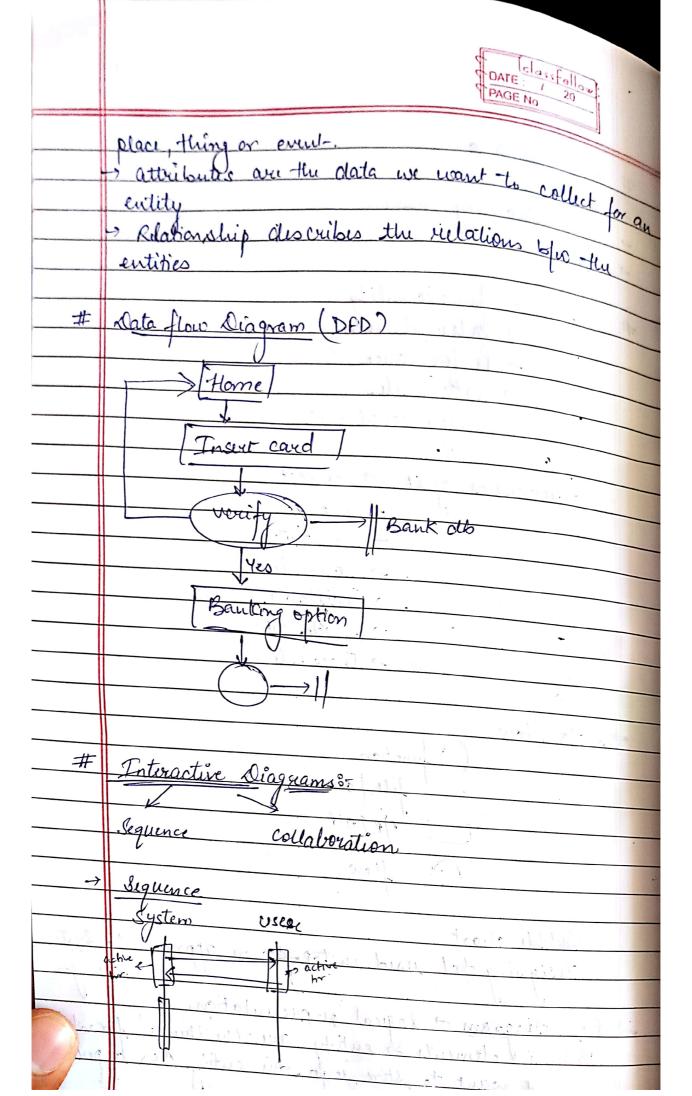


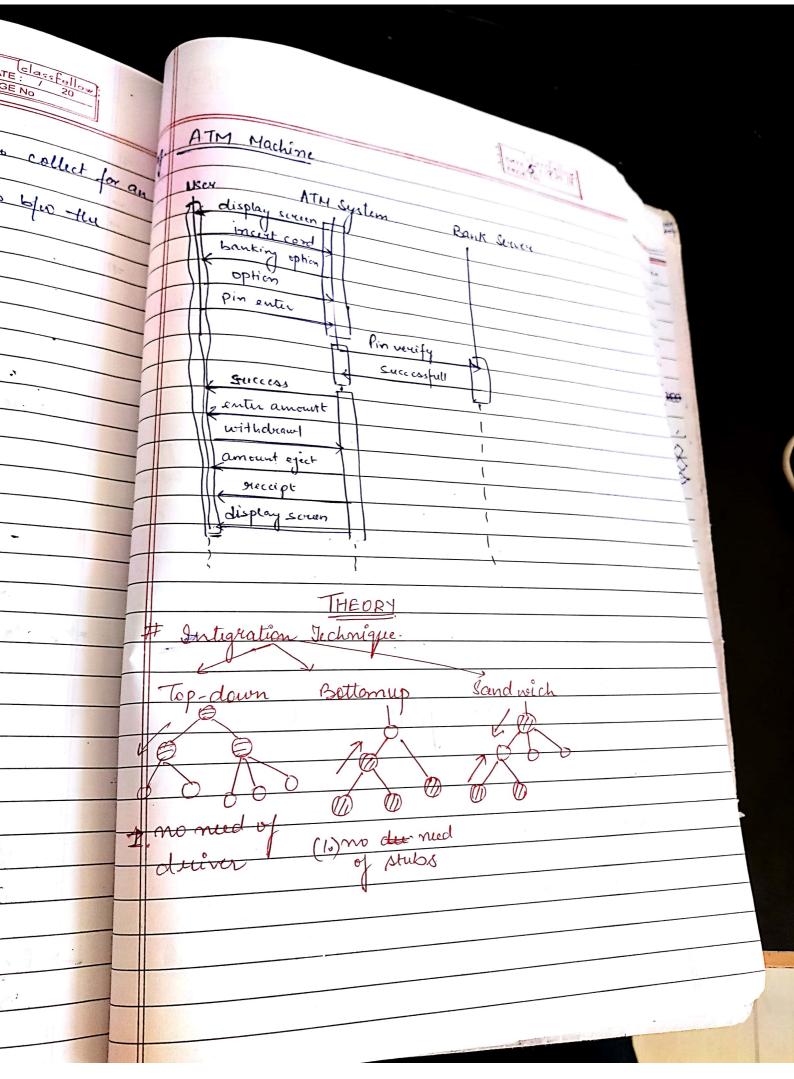
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g dn	DATE / 20 PAGE No	Levelo -	,
		eg.	_
	20 2 new lind every fault and failure in	V	_
	Sain of 2 ster this code.		J.
	15: 20		¥:
	puintf ("sum of nor "led", c);		
	1 multiple		
	nædede will be usasted vio this is failure.	Jevel	
	error - coding. mistake : c=a-b		
			\rightarrow
	fault - fault comes in line (- a-b) due to		
	Tault - jault Comodule do faile.		
1			
	-> Verification and verification and validation		
	-> Validation white developing		
	Verification means har module face ke baad chec	K	
	Karonge module sahi chal saha hai yambi		
	Validation - complete modest you banne ke		\dashv
	band chick karenge ki vo requirement ke		\dashv
	accu sahi bana hai ja nahi		4
	Unit		
	Integration - Verification		
	system /		
	Aceptance - validation		\dashv
	- Continuent		_
	# DFD		
	A STATE OF THE STA		
	Level 0→ context diagram. Level 1 → DfD		\dashv
	herel 1 -> DFD		_
1			
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