Data Acquisition system

➢ High Level Analysis

ADC:

Analog-to-digital converters, abbreviated as "ADCs," work to convert analog (continuous, infinitely variable) signals to digital (discrete-time, discrete-amplitude) signals. Basically an analogue to digital converter takes a snapshot of an analogue voltage at one instant in time and produces a digital output code which represents this analogue voltage. The number of binary digits, or bits used to represent this analogue voltage value depends on the resolution of an A/D converter.

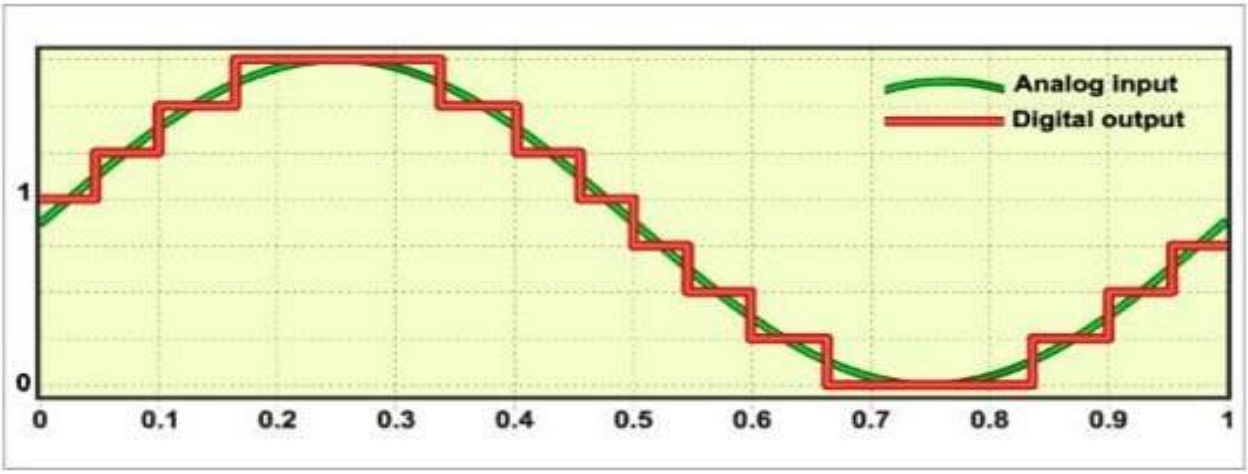

Figure1: ADC

ADC Performance Factors

We can evaluate ADC performance using several factors, the most important of which are:

1. **ADC Signal-to-noise ratio (SNR**): The SNR reflects the average number of non-noise bits in any particular sample (effective number of bits or ENOB).

2. **ADC Bandwidth**: We can determine bandwidth by evaluating the sampling rate – the number of times per second the analog source is sampled to generate discrete values

Common Types of ADC

1. **Flash and Half (Direct Type ADC)**: Flash ADCs, also called "direct ADCs" are very fast—capable of sampling rates in the gigahertz range. They require 2^N-1 comparators, where N is the number of bits (8-bit resolution, therefore, requires 255 comparators).

2. **Semi-flash ADC**: Semi-flash ADCs work around their size limitation by using two separate flash converters, each with a resolution of half the bits of the semi-flash device. One flash converter handles the most significant bits while the other handles the least significant bits (reducing the components to $2*2^{N/2}-1$, resulting in 8-bit resolution with 31 comparators).

3. **Successive Approximation (SAR)**: We can identify these ADCs by their successive approximation registers, which gives them the nickname SAR. These ADCs use a comparator to compare input voltage and the output of an internal digital-to-analog converter, successively judging whether the input is above or below a narrowing range's midpoint. SAR ADCs are considerably slower than flash ADCs, but they offer higher possible resolutions without the component size and cost of flash systems.

4. **Sigma-Delta ADC**: ΣΔ is a relatively recent ADC design. Sigma Deltas are very slow compared to other designs but offer the highest resolution of all ADC types.).

5. **Pipelined ADC**: Pipelined ADCs, also called "sub ranging quantizers," are similar in concept to SARs, but more refined. The pipelined ADC performs a coarse conversion then compares that conversion to the input signal. The ADC performs a finer conversion, allowing for an interim conversion of a range of bits.

EEPROM:

EEPROM stands for Electrically Erasable Programmable Read-Only Memory. EEPROM is a type of non-volatile primary memory and modified version of EPROM (Erasable Programmable Read-Only Memory) which uses electrical signals to erase and program the contents rather than UV signals which was used previously in EPROM. It is used as a chip in computers to store the digital data.

There are two types of EEPROM:

- Serial EEPROM
- Parallel EEPROM

Characteristics

- Less time consuming: EEPROM takes 5-10 milliseconds to erase the content electronically unlike; EPROM takes minutes to erase the same content using UV signals.
- Programmable and erasable content: It can reprogrammed n number of times and that life cycle has to be defined by the manufacture and it can be maximum of 1 million life cycles in modern EEPROMs.
- No detaching of chip: To reprogram or erase the content, there is no need to take the chip out of the computer.

➢Low Level Analysis

ADC controller specifications

1. 12-bit ADC.
2. Sampling rate can be as fast as every 15 ADC clock cycles.
3. Support for internal ADC clock divider logic.
4. Support for configuring the delay between samples also the sampling time.
5. Support for interleaving TS capture and general-purpose ADC modes
6. Programmable FSM sequencer that supports 16 steps:

– Optional start of conversion HW synchronized to Pen touch or external HW event (but not both)
– Single conversion (one-shot)
– Continuous conversions
– Sequence through all input channels based on a mask
– Programmable Open Delay before sampling each channel
– Programmable sampling delay for each channel
– Programmable averaging of input samples - 16/8/4/2/1
– Differential or singled ended mode setting for each channel
– Store data in either of two FIFO groups
– Option to encode channel number with data
– Support for servicing FIFOs via DMA or CPU
– Programmable DMA Request event (for each FIFO)
– Dynamically enable or disable channel inputs during operation
– Stop bit to end conversion

ADC Functional Block Diagram

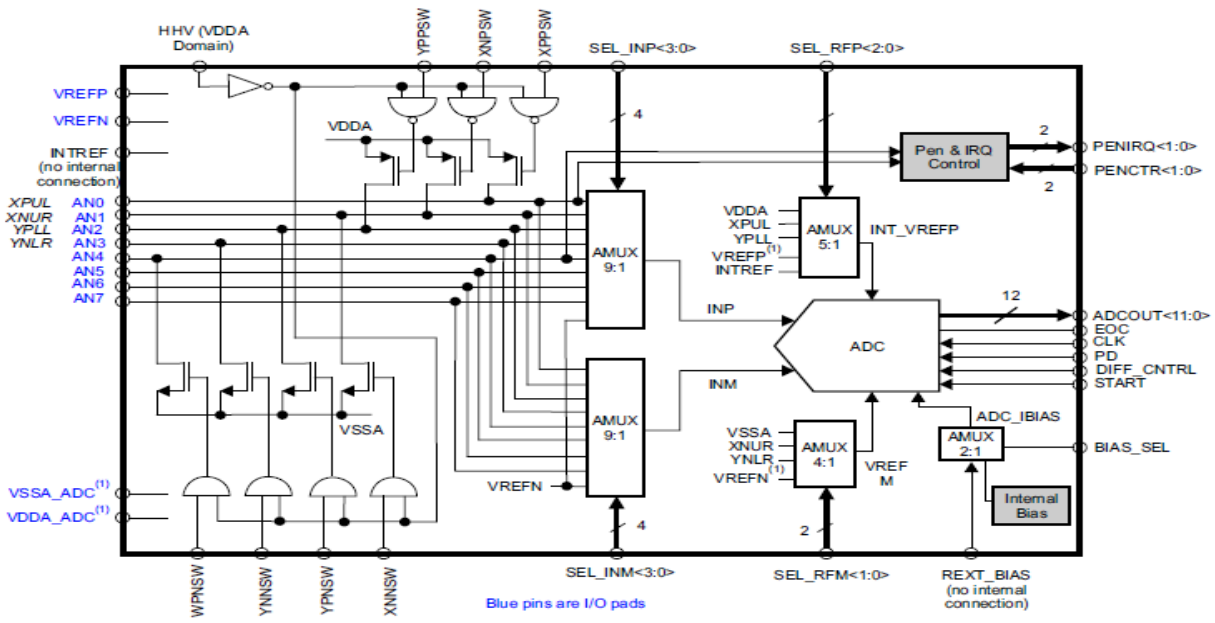

Figure 2: ADC Functional Block Diagram

Schematic diagram of LM35 interface with ADC channel

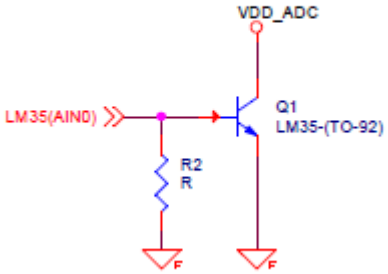

Figure 3: LM35 interface with ADC channel

EEPROM Write I2C communication protocol format

BYTE WRITE: A write operation requires an 8-bit data word address following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a zero and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a zero and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally timed write cycle, tWR, to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete.

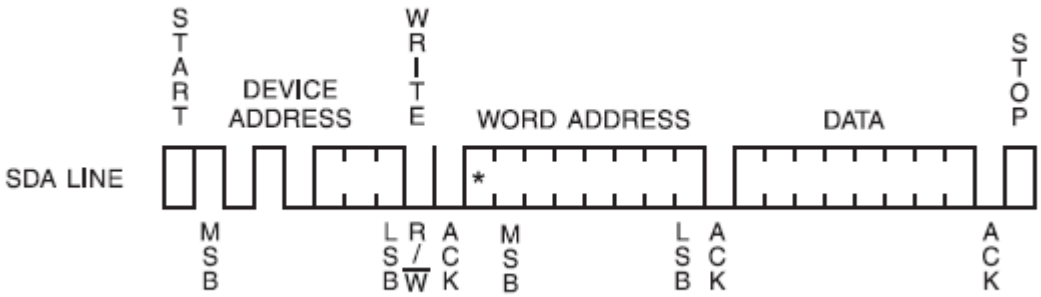

Figure 4: Byte write

PAGE WRITE: The 1K/2K EEPROM is capable of an 8-byte page write. A page write is initiated the same as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to seven (1K/2K) or fifteen (4K, 8K, 16K) more data words. The EEPROM will respond with a zero after each data word received. The microcontroller must terminate the page write sequence with a stop condition.

The data word address lower three (1K/2K) or four (4K, 8K, 16K) bits are internally Incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than

eight (1K/2K) or sixteen (4K, 8K, 16K) data words are transmitted to the EEPROM, the data word address will “roll over” and previous data will be overwritten.

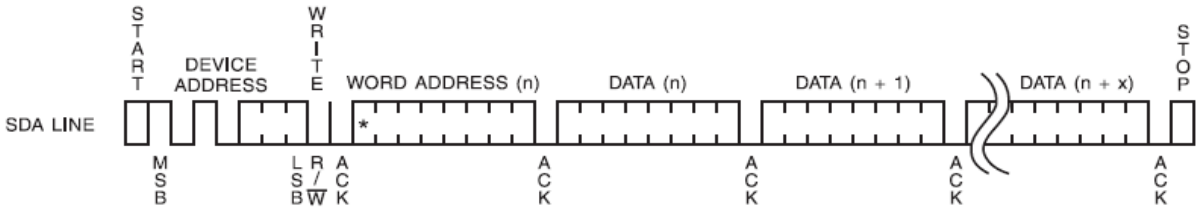

Figure 5: Page write

ADC-AM3358 Functional Block diagram

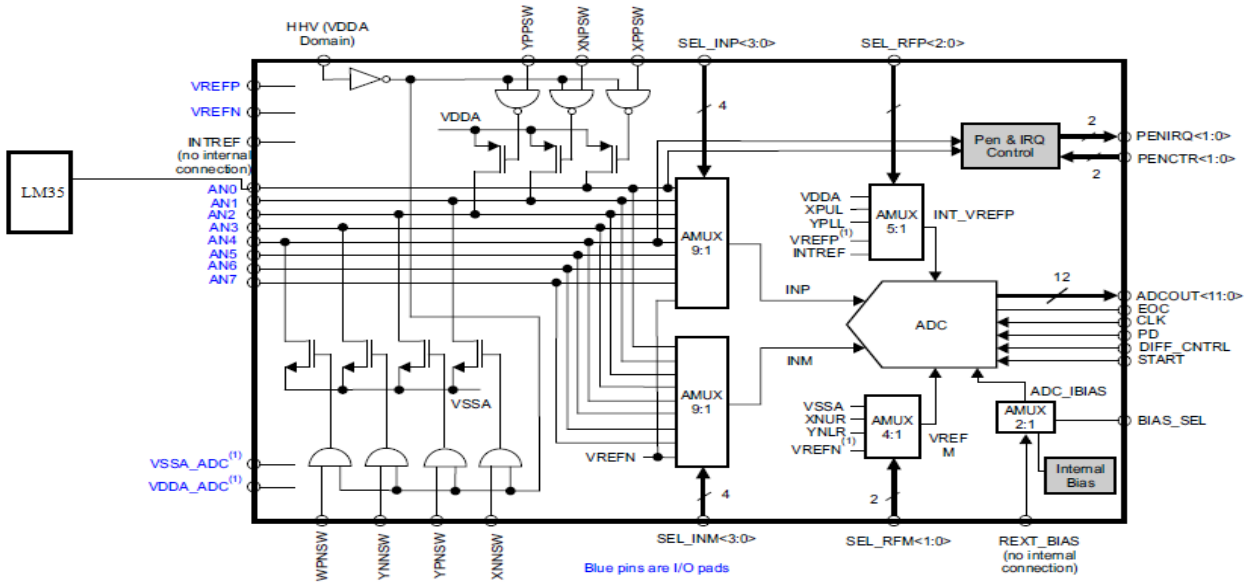

Figure 6: ADC-AM3358 Functional Block diagram

EEPROM-AM3358 Functional Block diagram

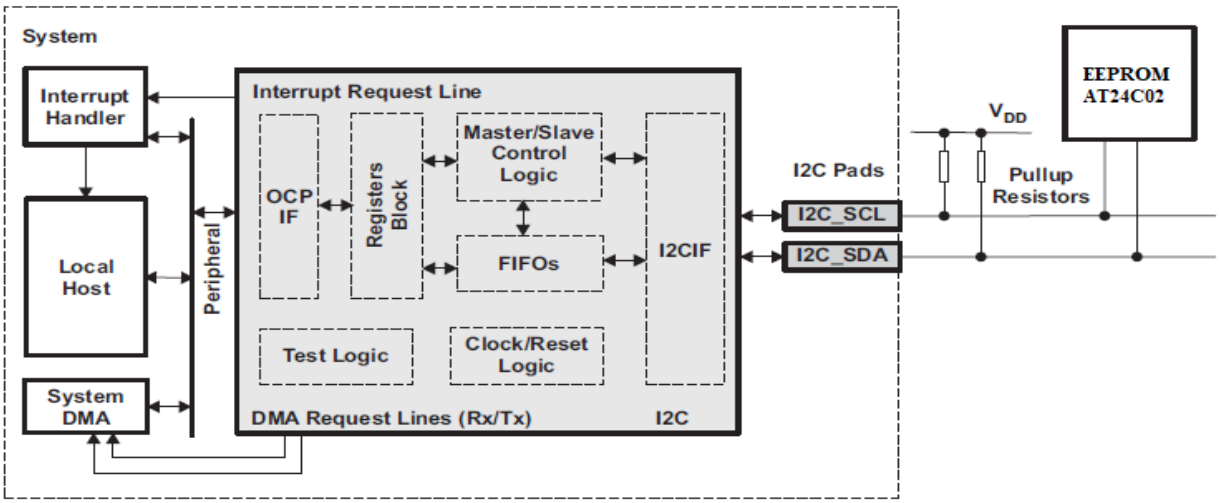

Figure 7: EEPROM-AM3358 Functional Block diagram