HANDWRITTEN PRACTICAL FILE

VLSI DESIGN

LAB

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EXP 1

AIM — To study the MOS characteristics & introduction to Mentor Graphics & tanner EDA Software tools

Software Used: Pyxis

Theory & Introduction :—

VLSI technology → It is the modern technology of producing very large scale integrated circuits

VLSI Design flow → The design process at various levels is usually evoluntionary in nature. The V-chart illustrates a simplified design flow for most logic chip using design activities on 3 different axes. The V-chart consists of 3 domain of representation namely (i) behavioural (ii) structural (iii) geometric layered.

Tanner EDA Software tools

Tanner EDA is a suite of tools for the design of integrated circuits. These tools allow you to schematics, perform SPICE simulation, do physical design and perform design rule check. and layout verses schematics. There are three tools used for this.

S-edit :- a shematic capture tool

T-edit :- The spice simulation engine integrated with S-edit

L-edit :- the physical design tool.

Tanner EDA helps to transform your ideas into design. it has created a software platform that is cost efficient. it is powerful enough to handle complex design.

① S-edit → in S-edit shematics design of circuits enables us to check our design for common errors such as undriven nets, unconnected pins, and net driven by multiple outputs so you can catch errors early before running simulations.

② T-Spice → It let you precise characterise the circuits behaviour using virtual data measurements. For greater efficiency & productivity, T-spice controls over your simulation process with an easy to use graphical interface.

③ L-edit - layout is essentially a drawing process L-edit gives you the flexibility and control you need to master the editing process

Additionally we also have,

④ W-edit → The W-edit waveform analysis tool is a compreenhensive viewer for comparing, displaying and analysing simulated results. W-edit is dynamically linked to T-Spice & S-edit with

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Result :— The Tanner EDA tools and Mentor Graphics Pyxus tool were studied & MOS structure was also studied.

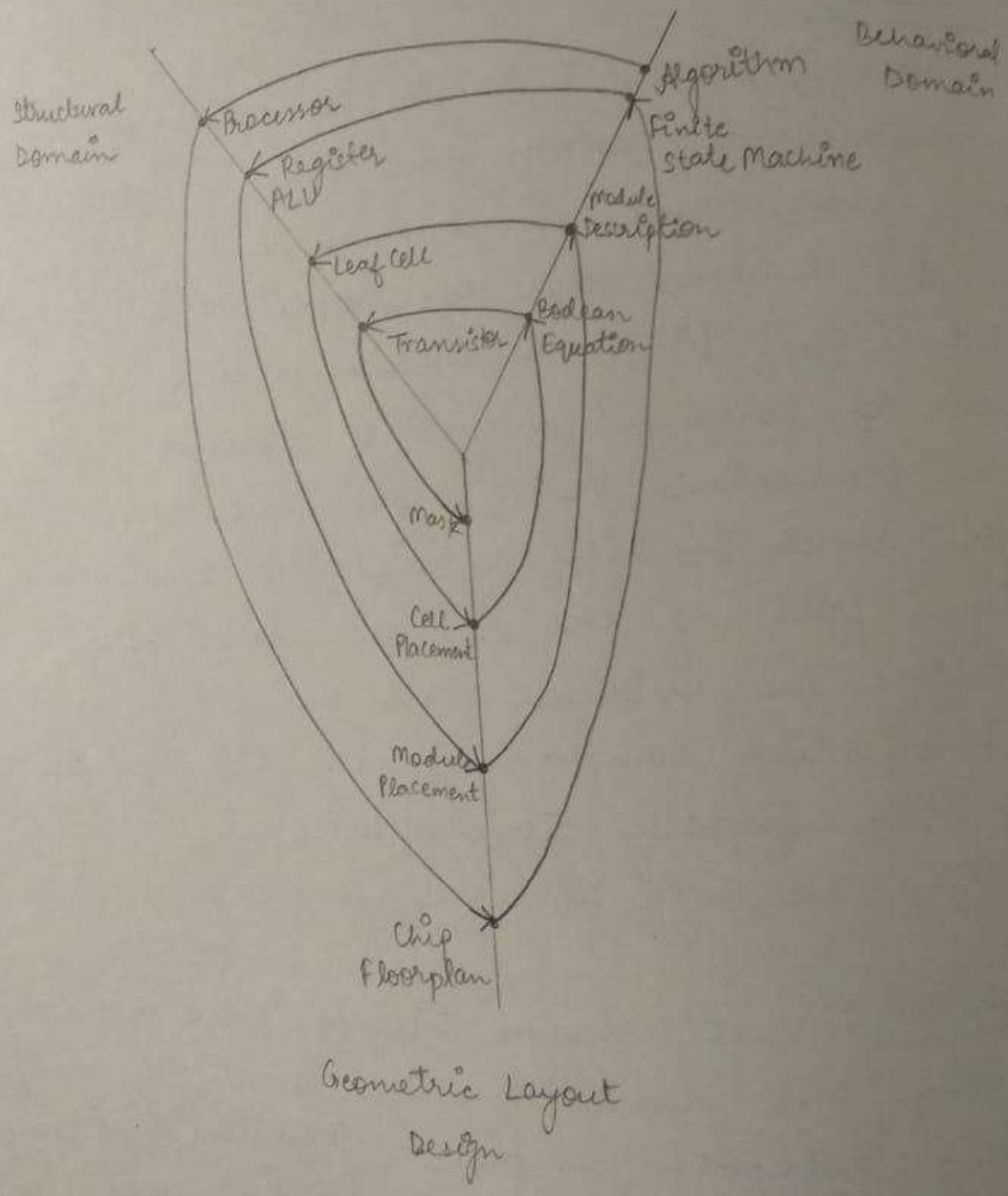
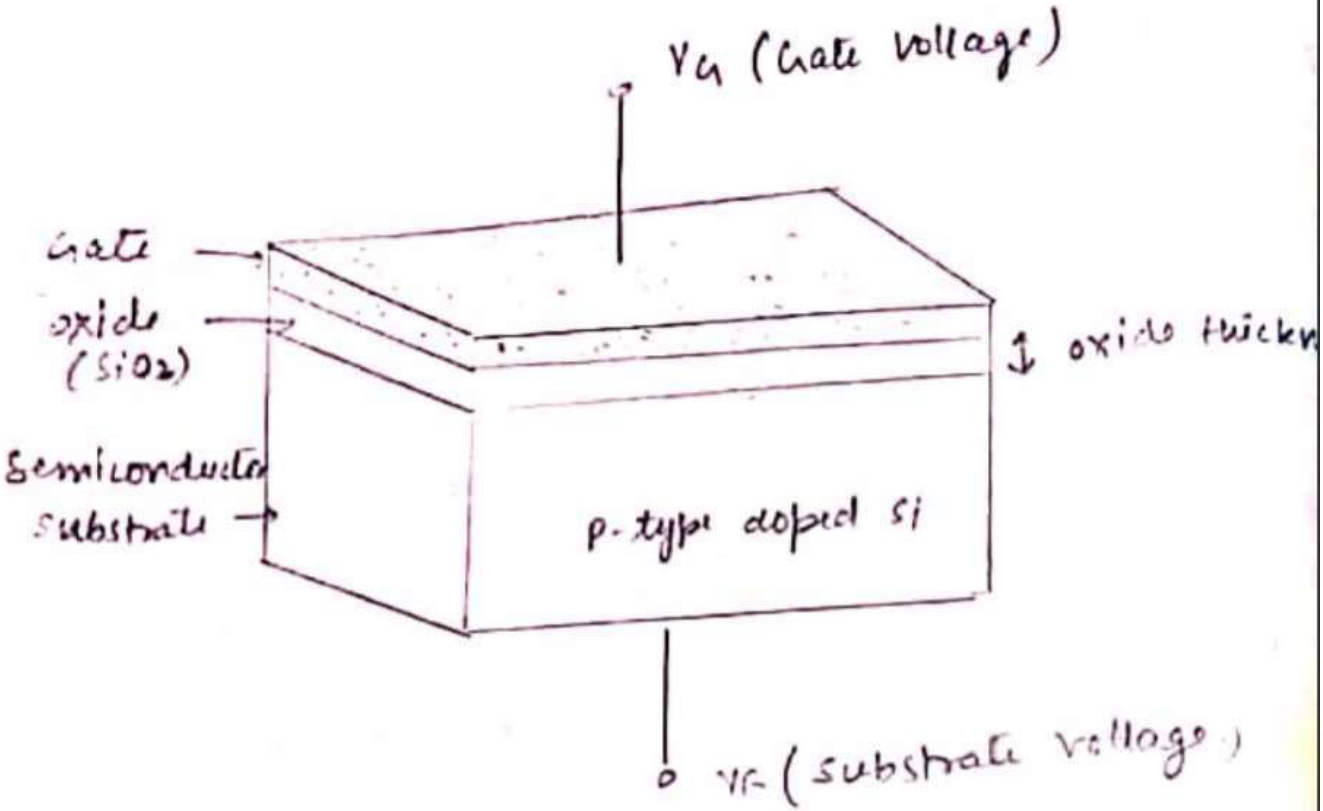


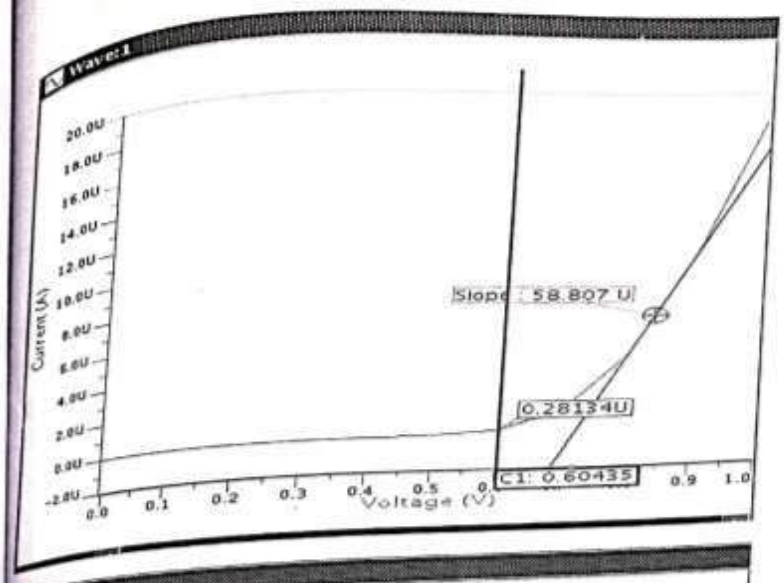
Fig 1. Simplied VLSI Design flow in three domain (Y-chart)

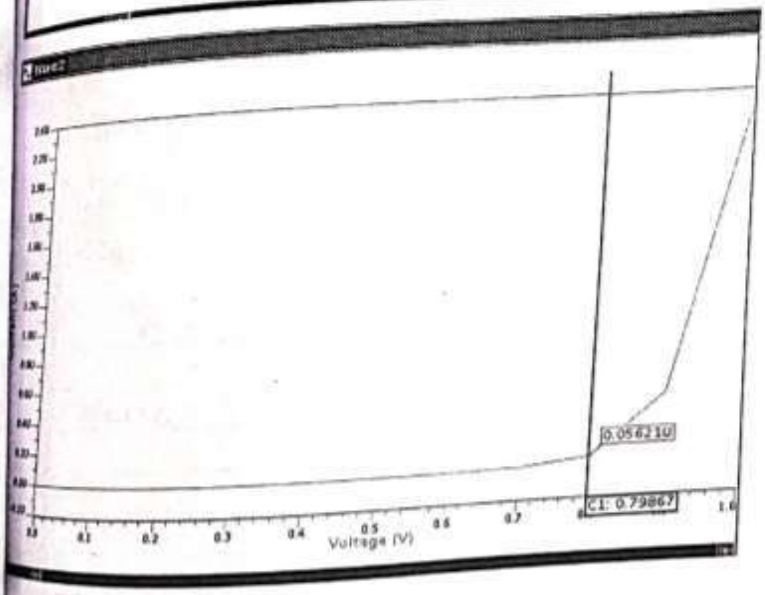


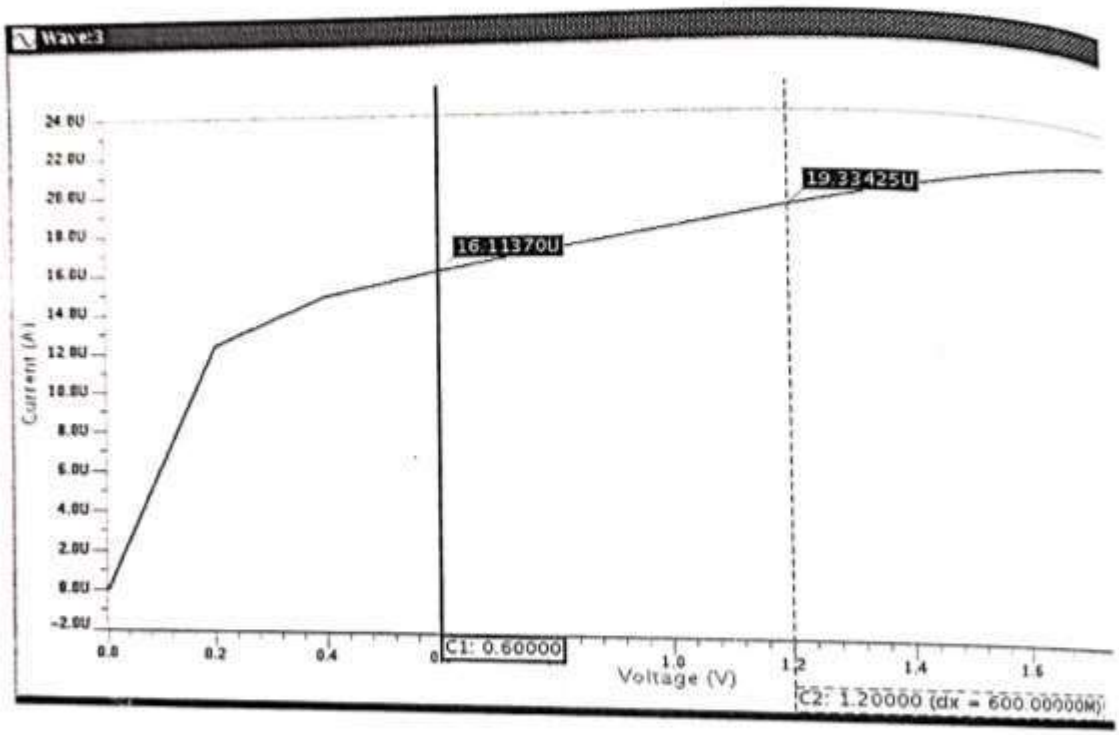
⇒ Fig 3: Two terminal MOS structure.

422

Experiment -1



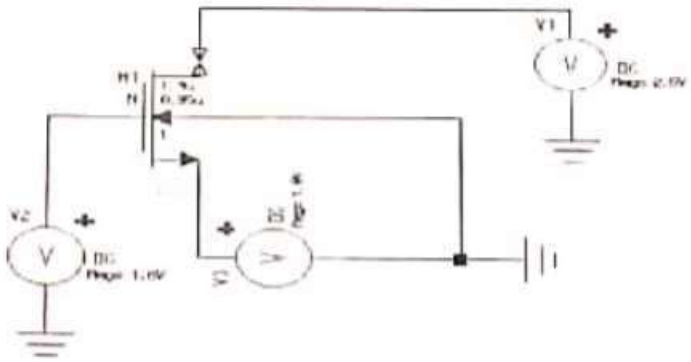



Wave:3
24.0U
22.0U
20.0U
18.0U
16.0U
14.0U
12.0U
10.0U
8.0U
6.0U
4.0U
2.0U
0.0U
-2.0U
Current (A)
0.0
0.2
0.4
0.6
0.8
1.0
1.2
1.4
1.6
Voltage (V)
16.11370U
19.33425U
C1: 0.60000
C2: 1.20000 (dx = 600.00000M)

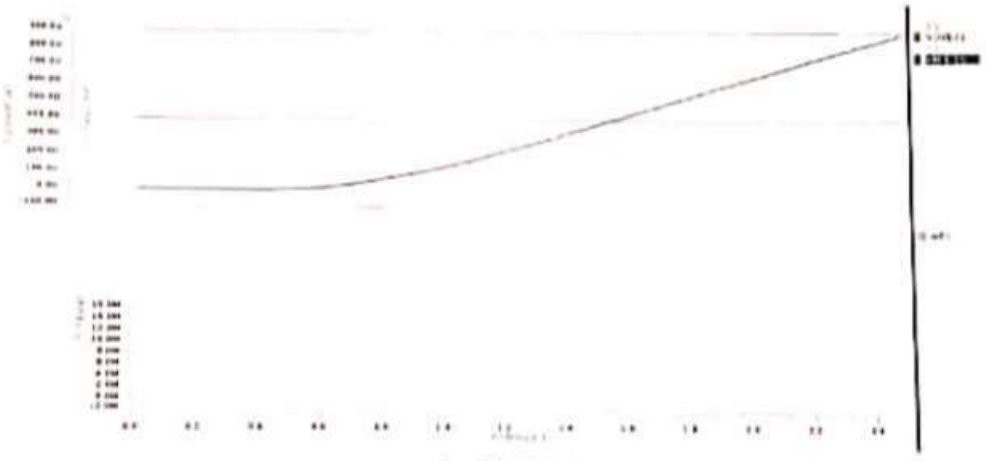
Experiment – 2

Experiment No 2

AIM: To design and study the DC characteristic of NMOS

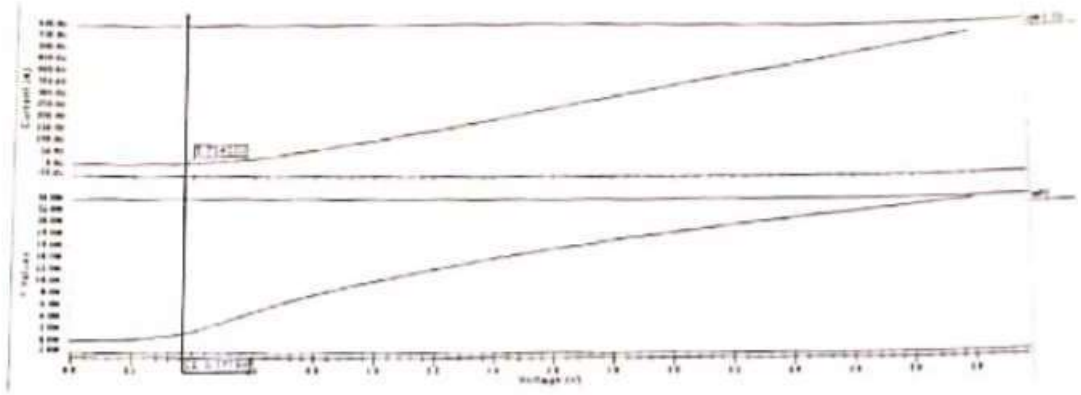


Id vs Vgs

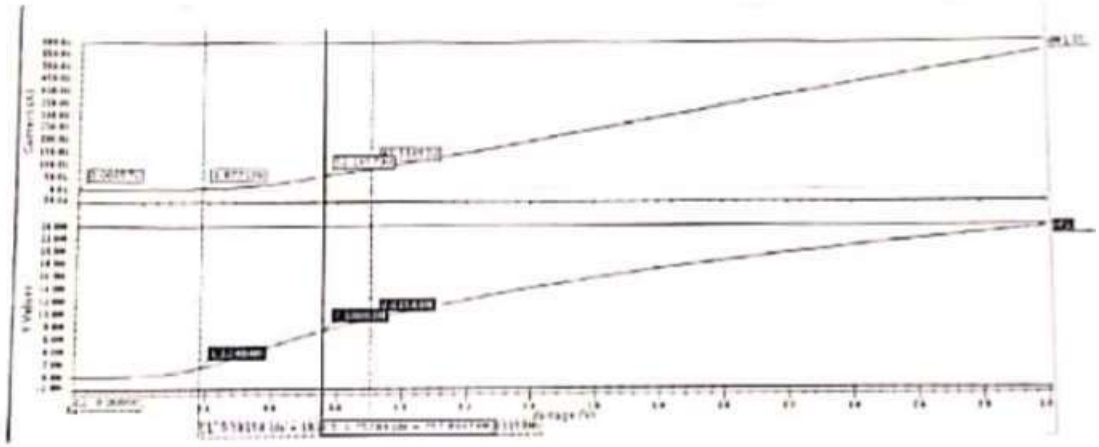


Sqrt(Id) vs Vgs

Id vs Vgs and sqrt(Id) vs Vgs (Vbs=1V)



Id vs Vgs and sqrt(Id) vs Vgs (Vbs=0V)



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Exp-2

Aim: To design and study the DC characteristic of NMOS

Theory: Mosfets are 3 terminal, unipolar, voltage controlled MOSFETS, impedance devices. These are of two types:-

i) Enhancement type
ii) Depletion type.

In MOSFET, the threshold voltage is given as when substrate is grounded

$$V_{T0} = \phi_{GC} - 2\phi_F - \frac{Q_{B0}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}}$$

When substrate is at some potential

$$V_T = V_{T0} - \frac{Q_B - Q_{B0}}{C_{ox}}$$

$$V_T = V_{T0} + \gamma\left(\sqrt{-2\phi_F + V_{SB}} - \sqrt{|2\phi_F|}\right)$$

where, C_{ox} → gate oxide capacitance = $\frac{\varepsilon_{ox}}{t_{ox}}$

Q_{B0} → Depletion region charge density

$= -\sqrt{2 q N_A \varepsilon_{si} |-2\phi_F + V_{SB}|}$

ϕ_{GC} → work func b/w gate & substrate.

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The drain current

$$I_D = \frac{K'}{2}\frac{W}{L}\left[2(V_{GS} - V_{TO})V_{DS} - V_{DS}^2\right]$$

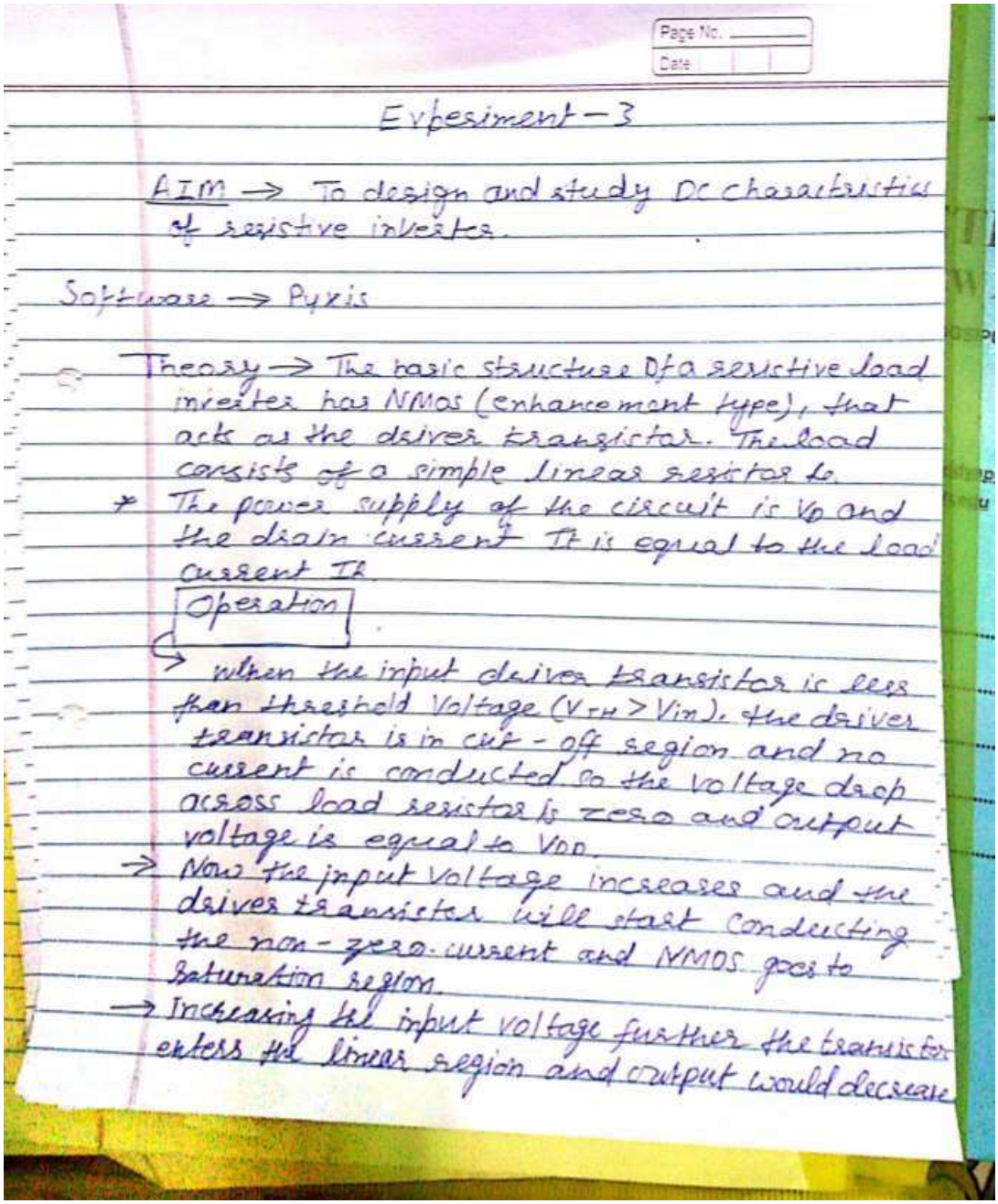
where $K' = \mu_n C_{ox}$

Result :-

All required parameters including transconductance parameters (K_n) substrate bias coefficient (γ), channel length modulation (λ), threshold voltage at zero and non-zero bias voltage. (V_{TN}, V_{TO}) etc are calculated & observed.

Parameters	Calculated	Observed
→ Threshold voltage		
⇒ V_{TO}	0.27 V	0.38 V
⇒ V_{TH}	0.25 V	0.372 V
→ K_n (Transconductance)	0.22 mA/V²	0.222 mA/V²
→ Substrate bias coefficient γ	0.1 $V^{1/2}$	0.29 $V^{1/2}$
→ Channel length modulation coefficient, λ	-	0.185

EXPERIMENT – 3



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Experiment – 3

AIM → To design and study DC characteristics of resistive inverter.

Software → Pyxis

Theory → The basic structure of a resistive load inverter has NMOS (enhancement type), that acts as the driver transistor. The load consists of a simple linear resistor RL.

* The power supply of the circuit is V_{DD} and the drain current I_t is equal to the load current I_L.

Operation

→ When the input driver transistor is less than threshold voltage ($V_{TH} > V_{in}$), the driver transistor is in cut-off region and no current is conducted so the voltage drop across load resistor is zero and output voltage is equal to V_{DD}.

→ Now the input voltage increases and the driver transistor will start conducting the non-zero current and NMOS goes to saturation region.

→ Increasing the input voltage further the transistor enters the linear region and output would decrease

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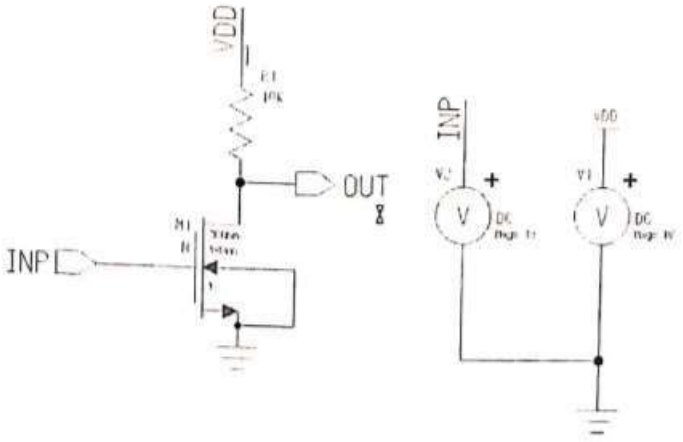
→ The result is plotted on a graph, between the relation of output and input voltage.

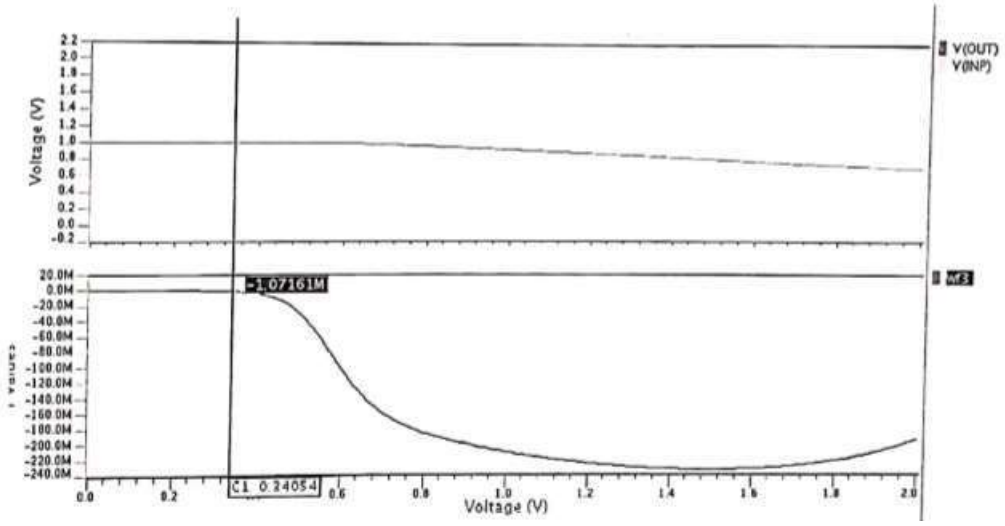
$$I_R = \frac{k_n}{2}\left(1/1 + \frac{V_{out}}{E_c L_n}\right)\left[2.(V_{in} - V_{TO})V_{out} - V_{out}^2\right]$$

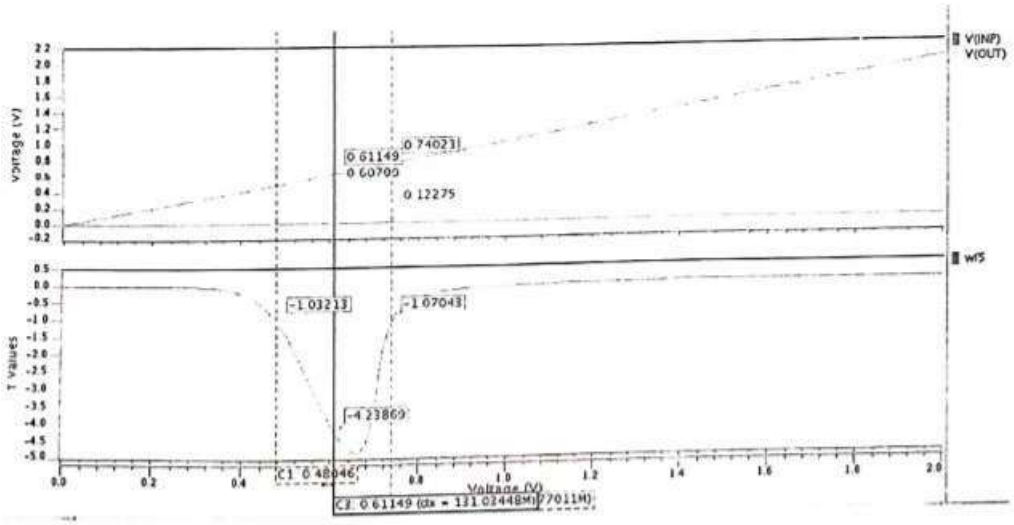
Result →

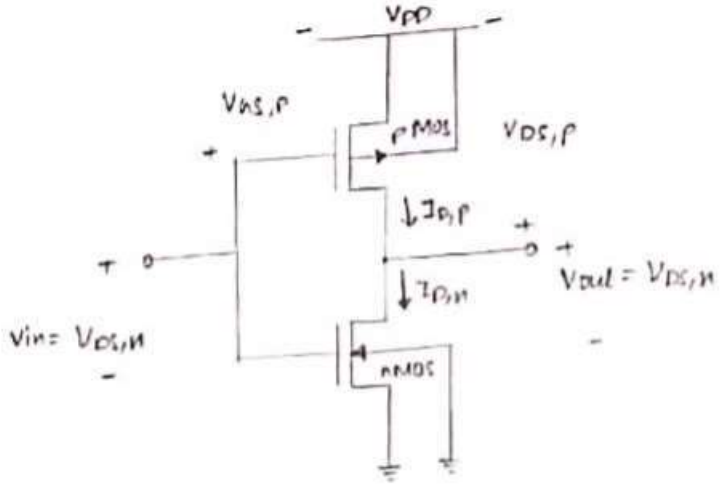
Dc characteristics of resistive load inverter were succesfully studied and verified.

EXPERIMENT-3

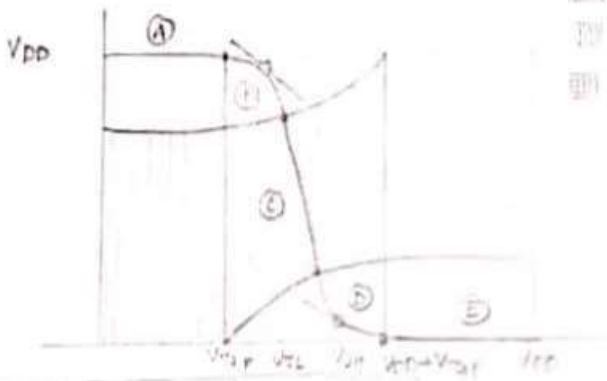





V(INP)
V(OUT)
Voltage (V)
0.61149
0.74023
0.60700
0.12275
W(5
T Values
-1.03213
-1.07043
-4.23869
Voltage (V)
C1 0.48046
C2 0.61149 (dx = 131.02448M)



→ cmos inverter circuit



nmos in saturation
pmos in saturation
both in saturation

Region	nMOS	pMOS
A	Cut off	Linear
B	Saturation	Linear
C	Saturation	Saturation
D	Linear	Saturation
E	Linear	Cut off

EXPERIMENT-4

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Experiment - 4

Aim: To design and study DC characteristics of CMOS inverter.

Software - Pyxis

Theory: Here both, nMOS and PMOS transistors work as driver transistors, when one is ON, the other is OFF. The setup is called as complementary MOS. The input is connected to gate terminal of both transistors, so that both can be taken directly without input voltages.

+ Operation in n-mos is saturation, if $V_{in} > V_{T0,n}$ and

$$V_{DS,n} \geq \frac{(V_{GS,n} - V_{Tn}) E_c L_n}{(V_{GS,n} - V_{T0,n}) + E_c L_n} = V_{DSAT,n} = V_{out}$$

+ operation in pmos is

$(V_{in} < V_{DD} + V_{T0,P})$ is saturation,

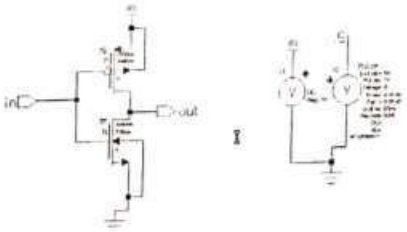
$$V_{DS,P} \geq \frac{(V_{SG,P} - |V_{T0,P}|) E_c L_P}{V_{SG,P} - |V_{T0P}| + E_c L_P} = V_{DSAT}$$

$P = V_{DD} = V_{out}$.

Region	V_{in}	V_{out}	nMOS	PMOS
A	$< V_{T,n}$	V_{OH}	cut-off	Linear
B	V_{IL}	High	Saturation	Linear
C	V_{th}	V_{th}	Sat	Saturation
D	V_{IH}	low	Linear	Sat
E	$> (V_{DD} + V_{T,p})$	V_{OL}	Linear	Cut-off

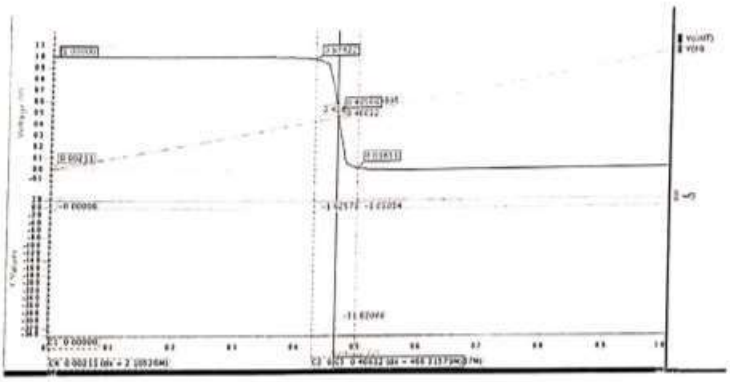
Result :-
Voltage transfer characteristics of CMOS inverter were studied and verified.

EXPERIMENT 4

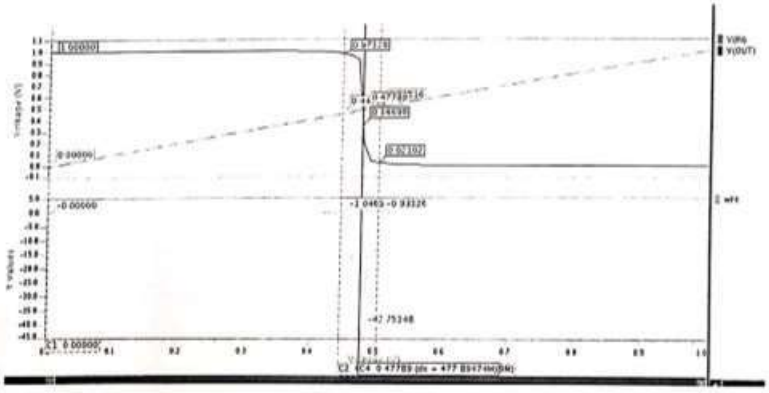


Dc Analysis

K=1

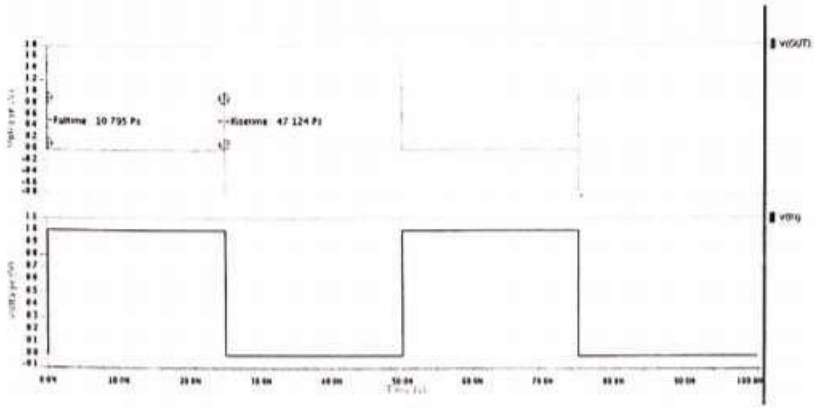


K=3

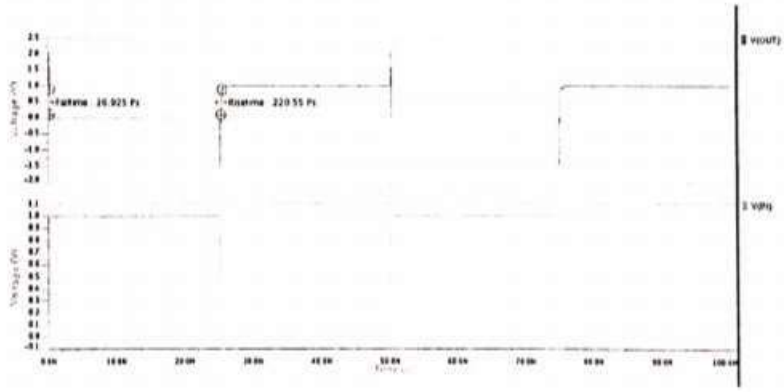


Transient Analysis

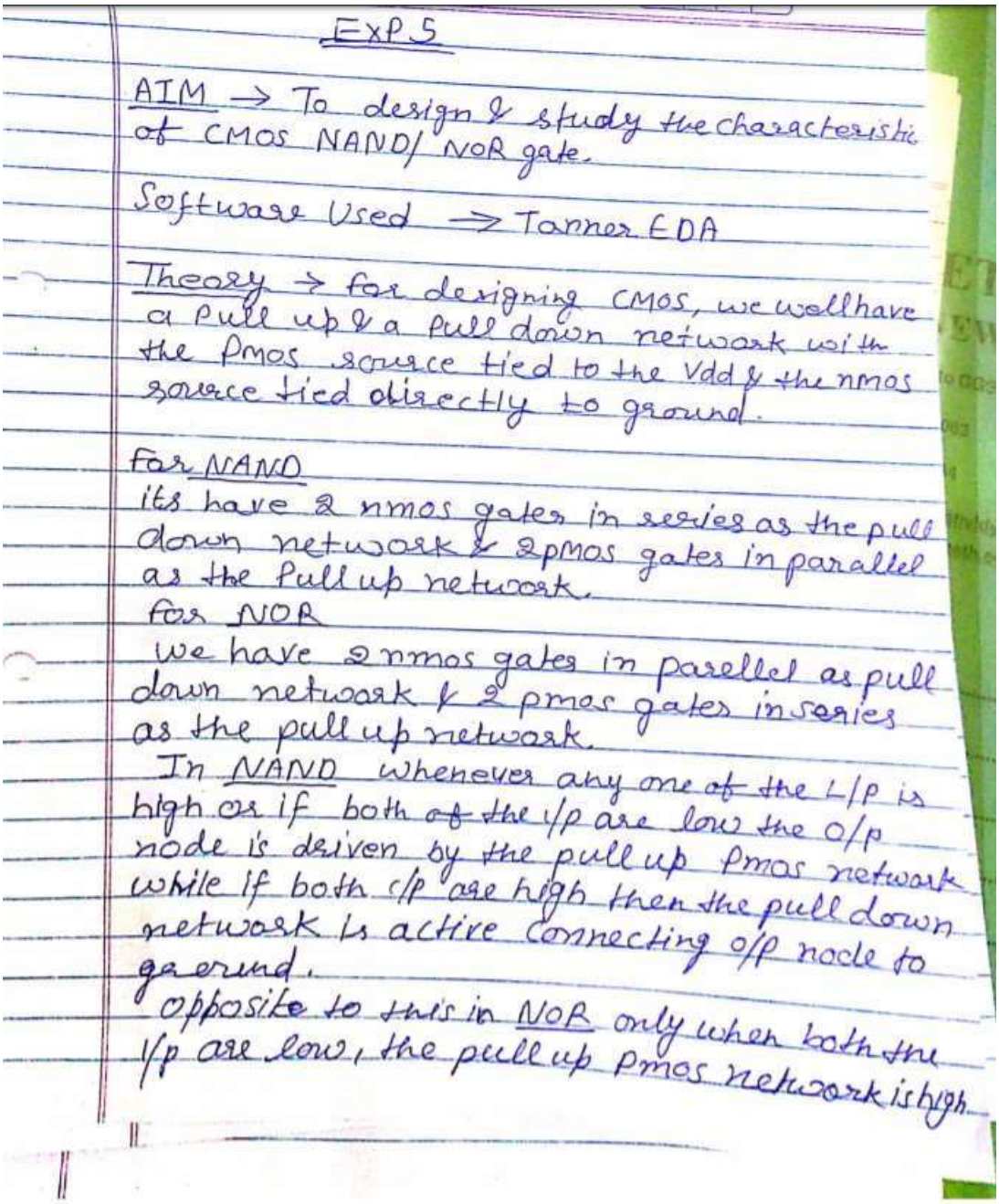
Kr =1



K=3



EXPERIMENT-5



EXP 5

AIM → To design & study the characteristic of CMOS NAND/ NOR gate.

Software Used → Tanner EDA

Theory → for designing CMOS, we will have a Pull up & a Pull down network with the Pmos source tied to the Vdd & the nmos source tied directly to ground.

For NAND
its have 2 nmos gates in series as the pull down network & 2pMos gates in parallel as the Pull up network.
for NOR
we have 2 nmos gates in parallel as pull down network & 2 pmos gates in series as the pull up network.
In NAND whenever any one of the I/P is high or if both of the i/p are low the O/P node is driven by the pull up Pmos network while if both c/p are high then the pull down network is active connecting o/p node to ground.
opposite to this in NOR only when both the I/p are low, the pull up Pmos network is high

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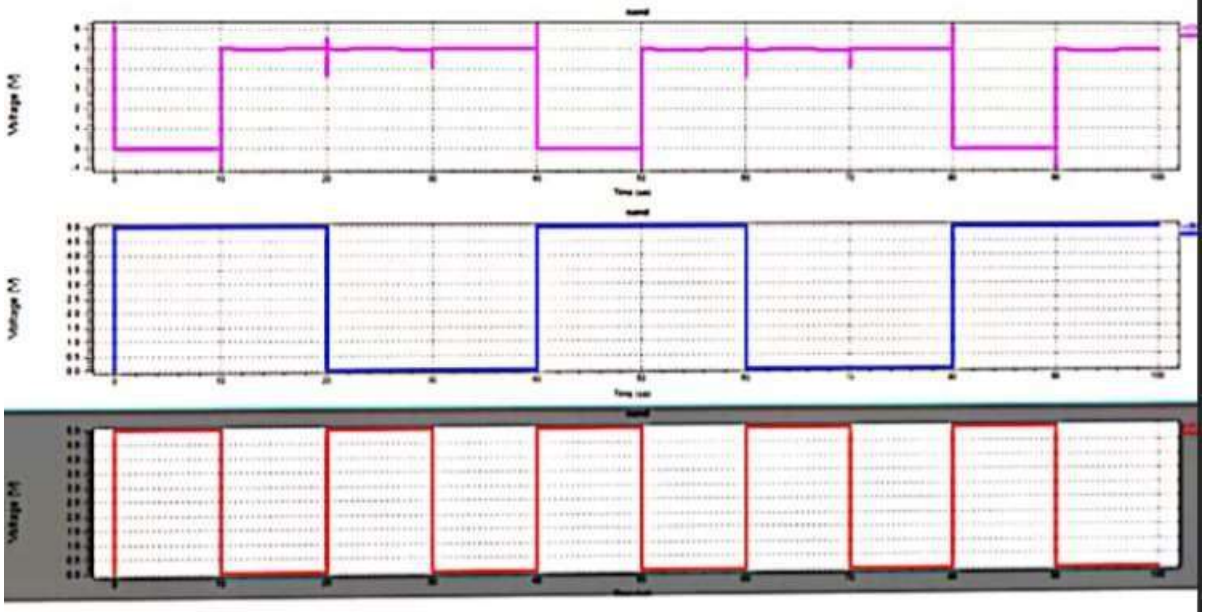
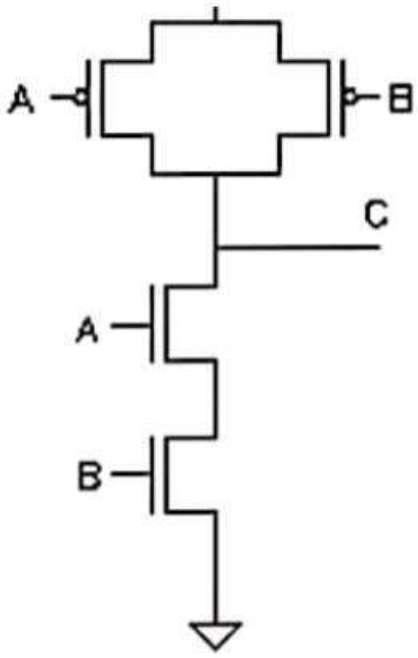
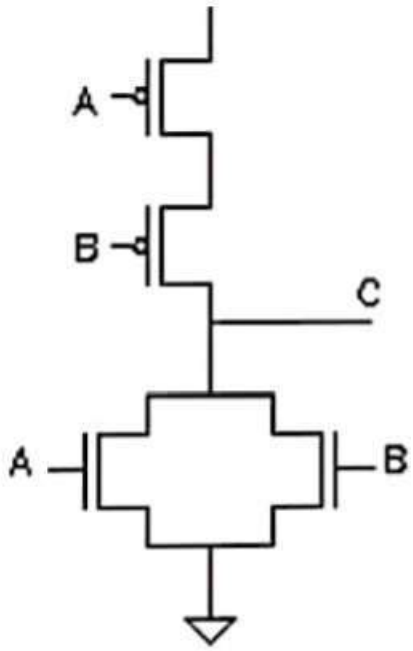
for all the other configurations o/p node is connected to ground & therefore low o/p.

Result : NAND/NOR CMOS circuits were designed & studied.


Voltage (V)
Time (us)
Voltage (V)
Time (us)
Voltage (V)



NAND



NOR

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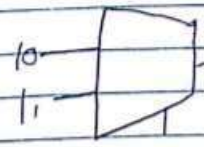
EXP 6

AIM → To design & study the characteristic of CMOS MUX (2:1)

Software Used → Tanner EDA

Theory – Multiplexer is a multiple input & single output digital circuit. It basically helps us to choose between multiple inputs on the basis of select lines & passes the appropriate input as the output line.

$Y = \bar{S} I_0 + I_1 S$



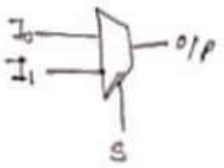
2:1 MUX

MUX can be build using transmission gate. Transmission gate acts as a bidirectional switch controlled by gate signal. When C=1 both the MOSFET are ON allowing the signal to pass through the gate. Similarly it can also be implemented using CMOS topology of pull up & down networks

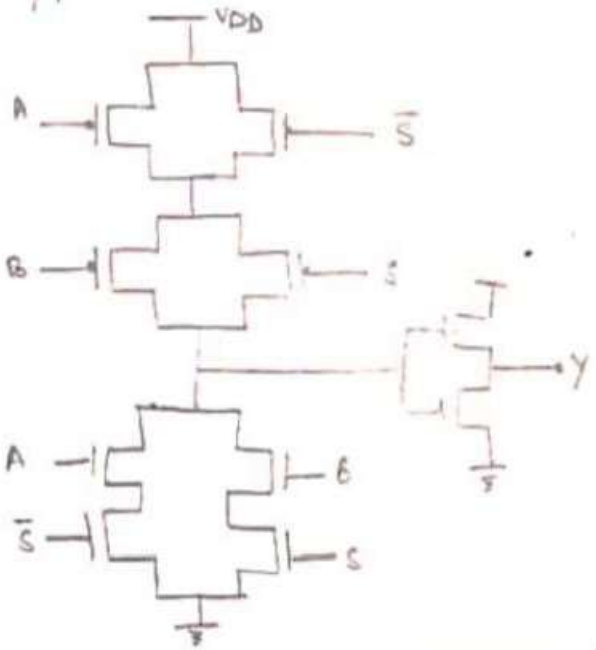
Result : A 2:1 CMOS MUX was implemented.

Truth Table

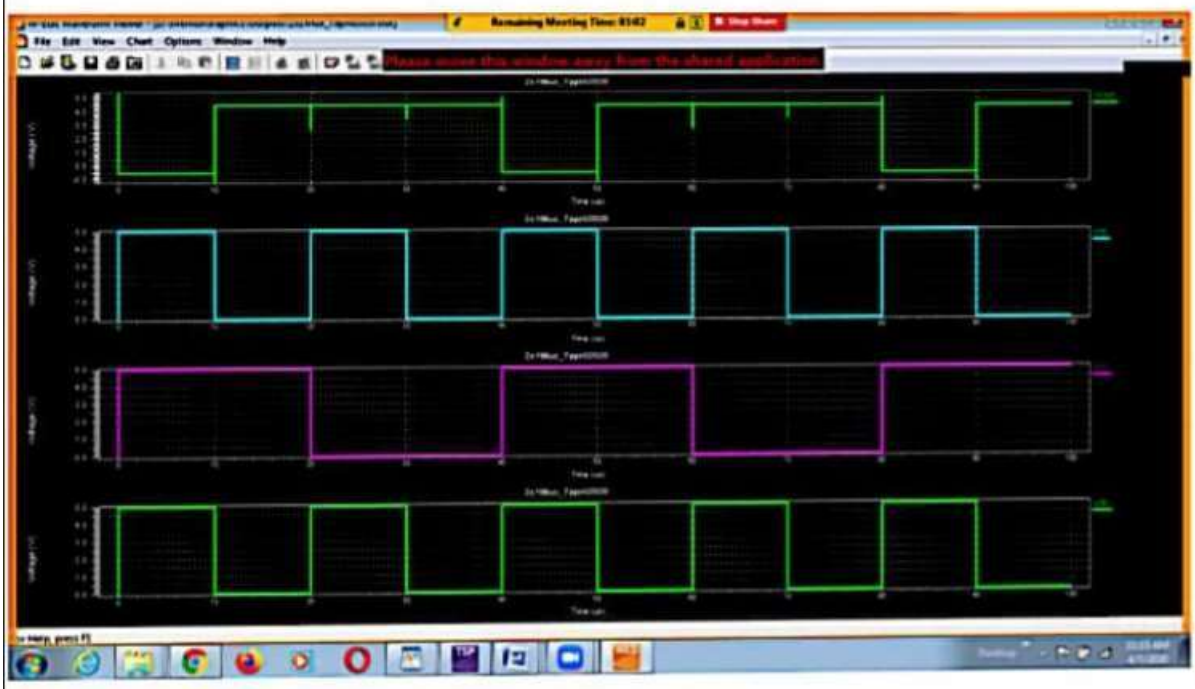
S	O/P
0	I_0
1	I_1



S	A	B	Z (or)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1



Circuit diagram for (2×1) MUX using CMOS


File Edit View Chart Options Window Help
Please move this window away from the shared application

EXPERIMENT 7

EXP- 7

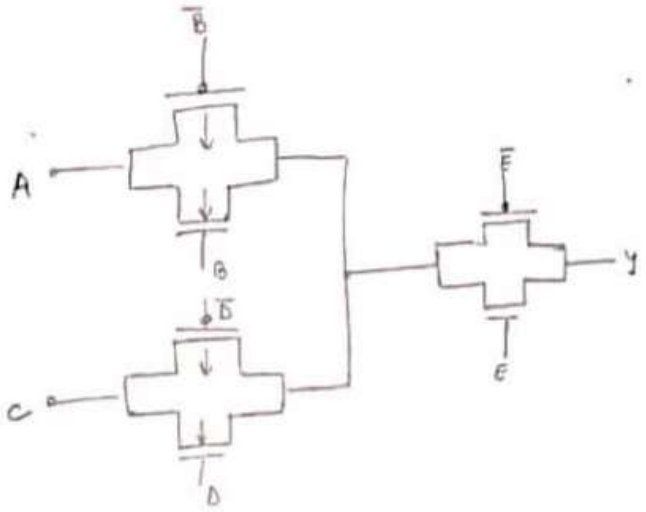
AIM → To design any boolean equation using transmission gate.

$$Y = (AB + CD)E$$

Software Used Tanner EDA

Theory Transmission gate is a bilateral switch with Nmos & Pmos. It is a CMos switch where P & N mos are in parallel & controlled by Complementary signals. Nmos switch passes a good 0 but poor 1. & Pmos passes good '0' & '1' in both directions.
TGs are efficient in implementing boolean functions.

Result → We used 3 TGs to implement given boolean equation.
→ TG is just implemented & observed.
→ Then using that TGs, we implement boolean eq & further their waveforms.



CMOS Transmission gate based implementation of
$Y = (AB + CD)\bar{E}$

EXP-8

AIM - To design & study the characteristics of CMOS D flip flop.

Software Used → Tanner EDA

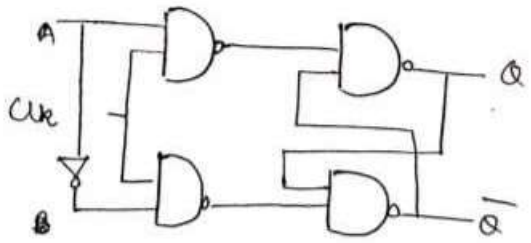
Theory → CMOS DFF is the cascading of 2D-latch circuits. The 1st stage is master, driven by clock signal & the 2nd stage is slave driven by the inverted clock signal. When clock changes to high, master follows D/p & slave holds the previous value. When clock changes from high to low, master ceases to sample the i/p & store the D value at the time the clock transition. When clock is changed from low to high slave locks in the master latch o/p & master samples the i/p again.

Result

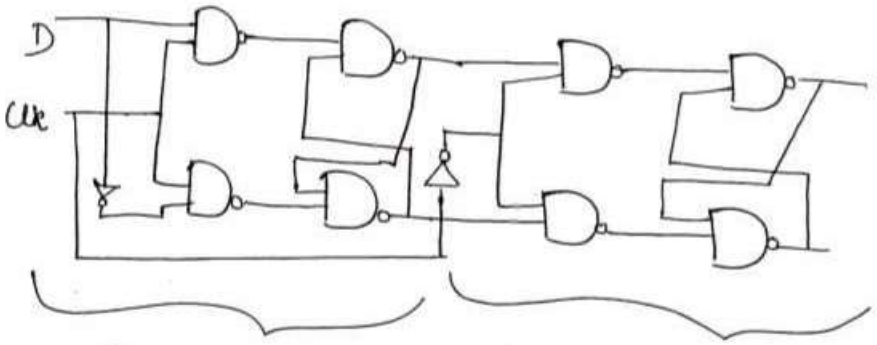
The o/p of the master stage latches applied i/p while clock signal is '1'

→ o/p of slave stage becomes valid when clock signals drops to '0'.

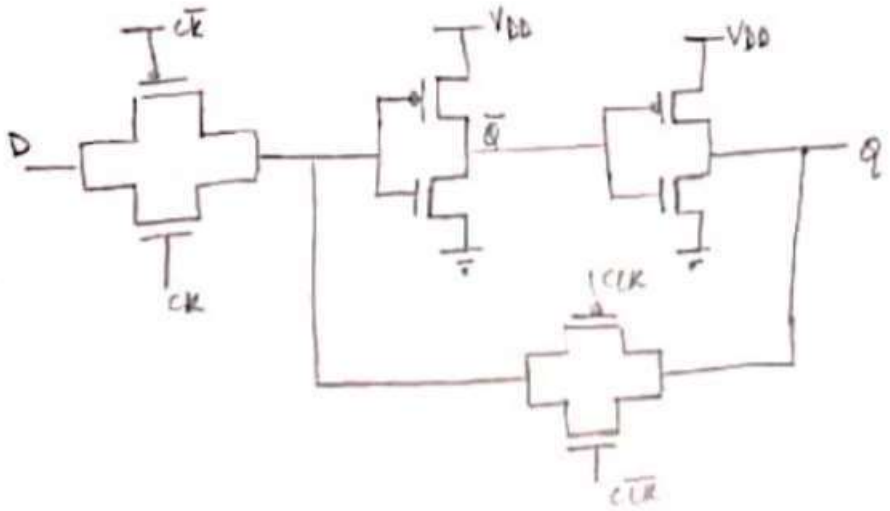
The DFF samples i/p at every falling edge of clock.



D - latch

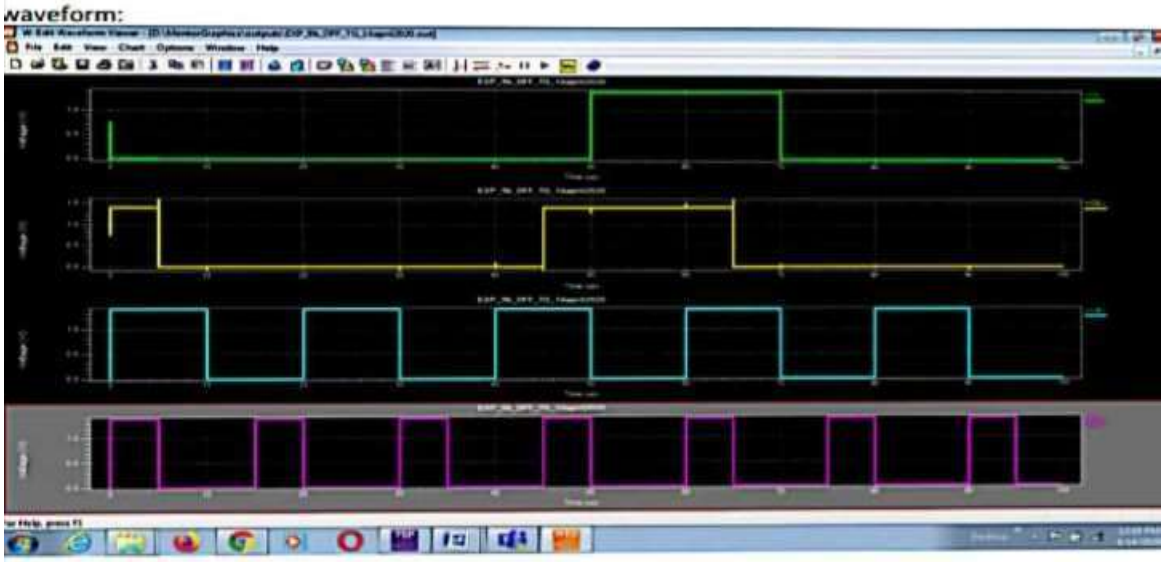


Master D-latch Slave D-latch



D latch using 2 inverters & 2 TG

waveform:



Innovation - 1

Aim

Design the 2:1 Multiplexer using cmos Logic.

Software Required

Tanner EDA

Theory

The expression for 2:1 MUX is given as

$$Y = S'A + SB$$

The transmission gate consists of parallel connection of nmos and pmos transistors such that drain of nmos is connected to source of pmos transistor and vice versa.

The truth table for 2:1 MUX is

Select	Inputs		Outputs
0	0	0	0
0	0	1	1
1	1	0	1
1	1	1	1

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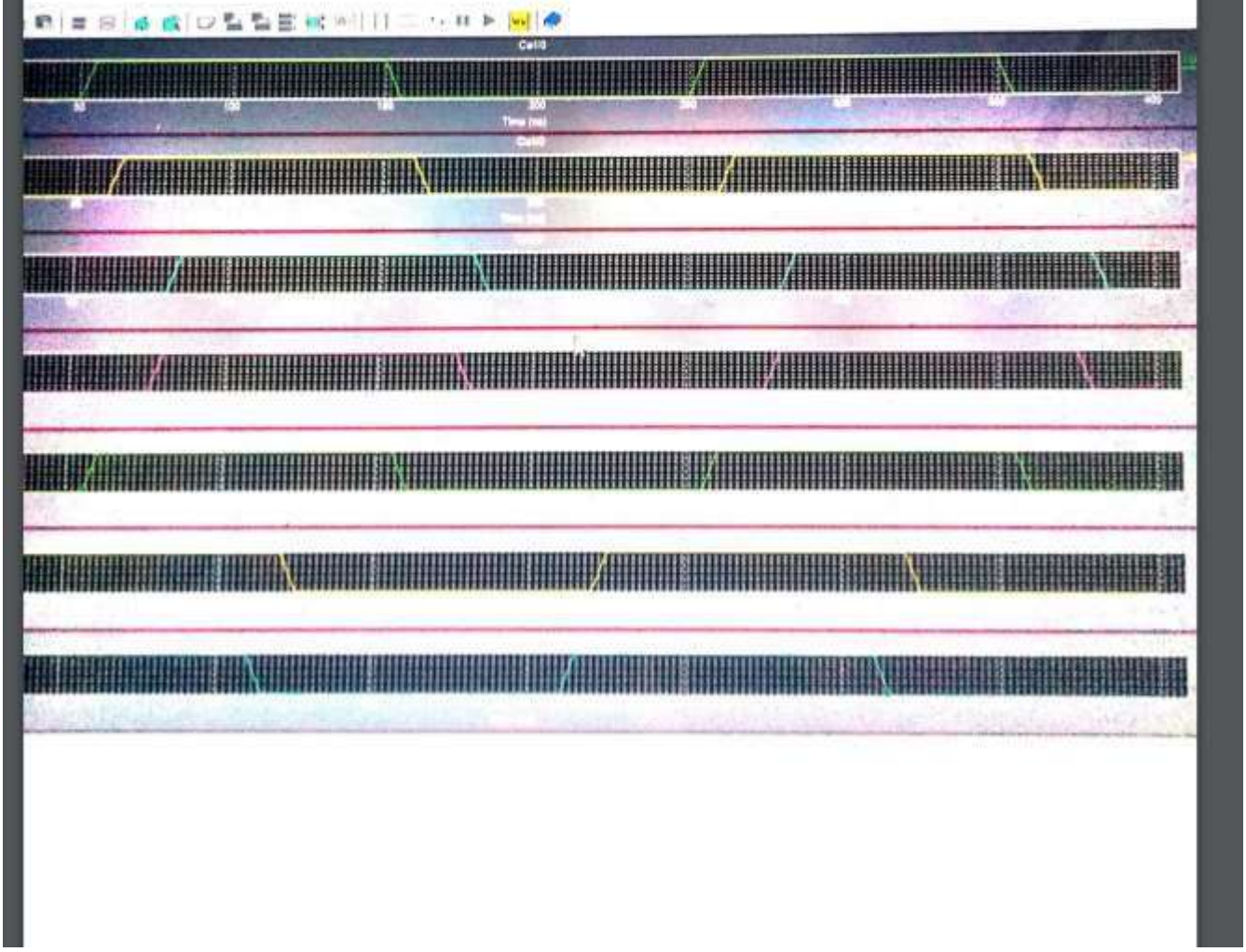
- Multiplexer is a device that selects one of several analog or digital inputs signals and forwards the select input into a single line.
- A multiplexer of 2^n inputs has 'n' select lines which are used to select which input line to send to the output.
- Multiplexer are mainly used to Increase the amount of data that can be sent over the network within a certain amount of time & bandwidth.
- A multiplexer is also called a data selector.
- Because they can "select" each input line are constructed from individual Analogue Switches encased in a single IC package as opposed to the "mechanical" type selectors such as normal conventional switches and relays.
- In 2:1 MUX, when the data select input, A is low at logic 0, input passes its data through the NAND gate multiplexer circuit to the output while other input is blocked.

When the data select A is high at logic 1, the reverse happens and now input passes data to the output.

So, by the application of either a logic "0" or a logic "1" at A we can select the appropriate input with the circuit acting a bit like a single pole double throw (SPDT) Switch.

Result

2:1 Multiplexer using CMOS logic is done successfully.


Ch10
Time (ms)
Ch10

Innovation - 2

Aim

Simulate the XOR and XNOR gate using either CMOS logic or transmission gate.

Software

Tanner Tools

Theory

XOR Gate

- An XOR gate pronounced as exclusive OR gate is a digital logic gate that gives a true (i.e, High or 1) output when the no. of true inputs is odd.

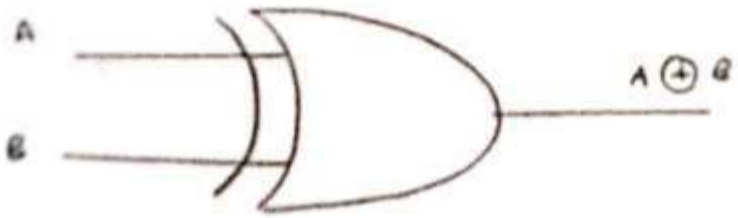
- An xor gate implements an exclusive or i.e, a true output results occurs if one & only one - of the inputs to the gate is true.

- If both the inputs are false (i.e, low or 0) or both are true, a false output results.

XOR Gate

Truth Table

Inputs		Output
A	B	x
0	0	0
0	1	1
1	0	1
1	1	0



- XOR represents the inequality function i.e., the output is true if the inputs are not alike otherwise the output is false.
- A common way to remember the XOR is "must have one or the other, but not both".

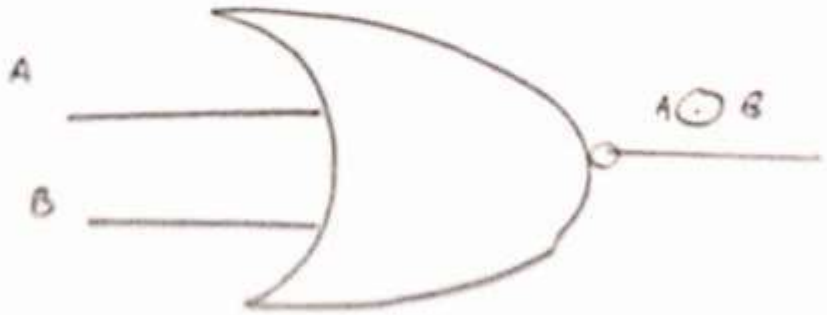
XNOR Gate

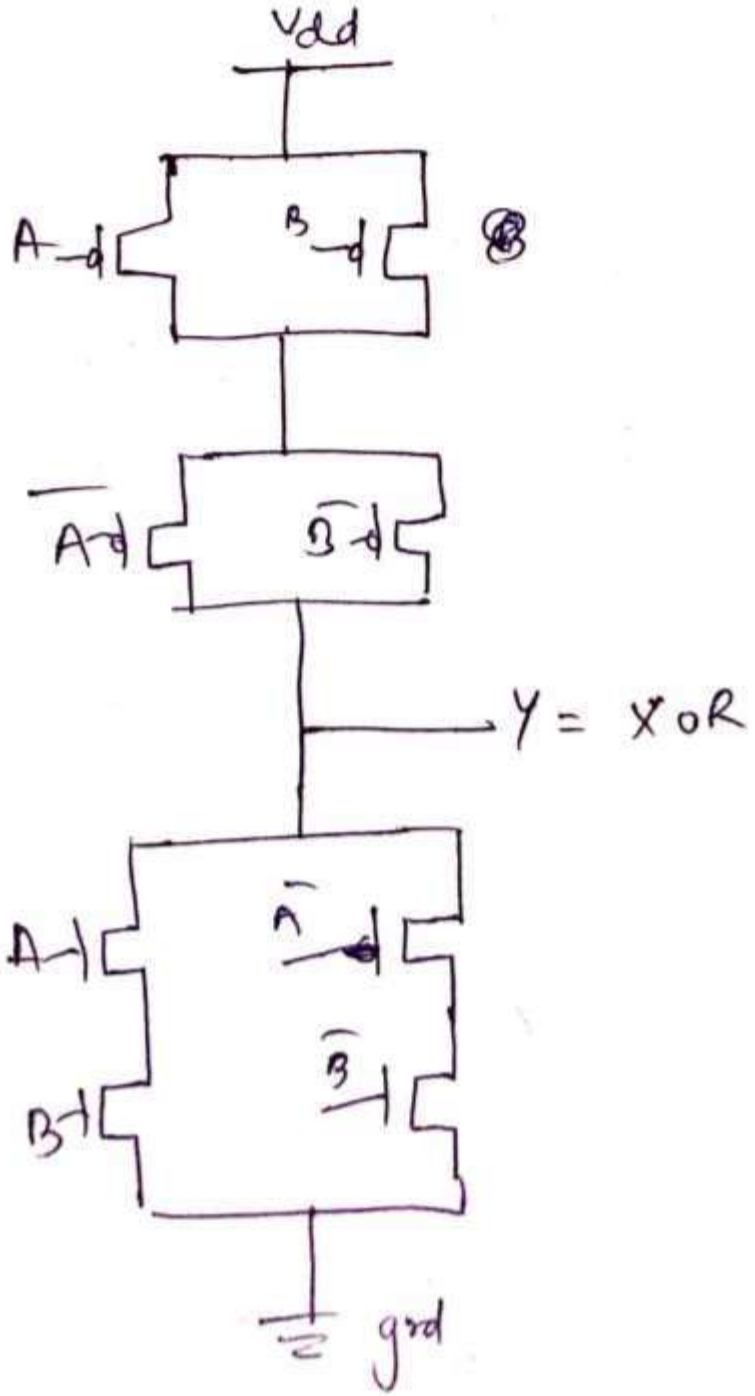
- The XNOR gate pronounced as exclusive nor is a digital logic gate whose function is the logical complement of the exclusive or gate.
- Logically an XNOR gate is a NOT gate followed by a XOR gate.
- The output is logical 0 when both inputs are same that means they are either 1 or 0. But in the case of XNOR gate, the output is 0 when only one input is 0 and the output is 1 when both inputs are same that is either both of them are 0 or 1.

XNOR gate

Truth Table

Input		Output
A	B	X
0	0	1
0	1	0
1	0	0
1	1	1





RESULT

Implementation of XOR & XNOR gate is successfully.