

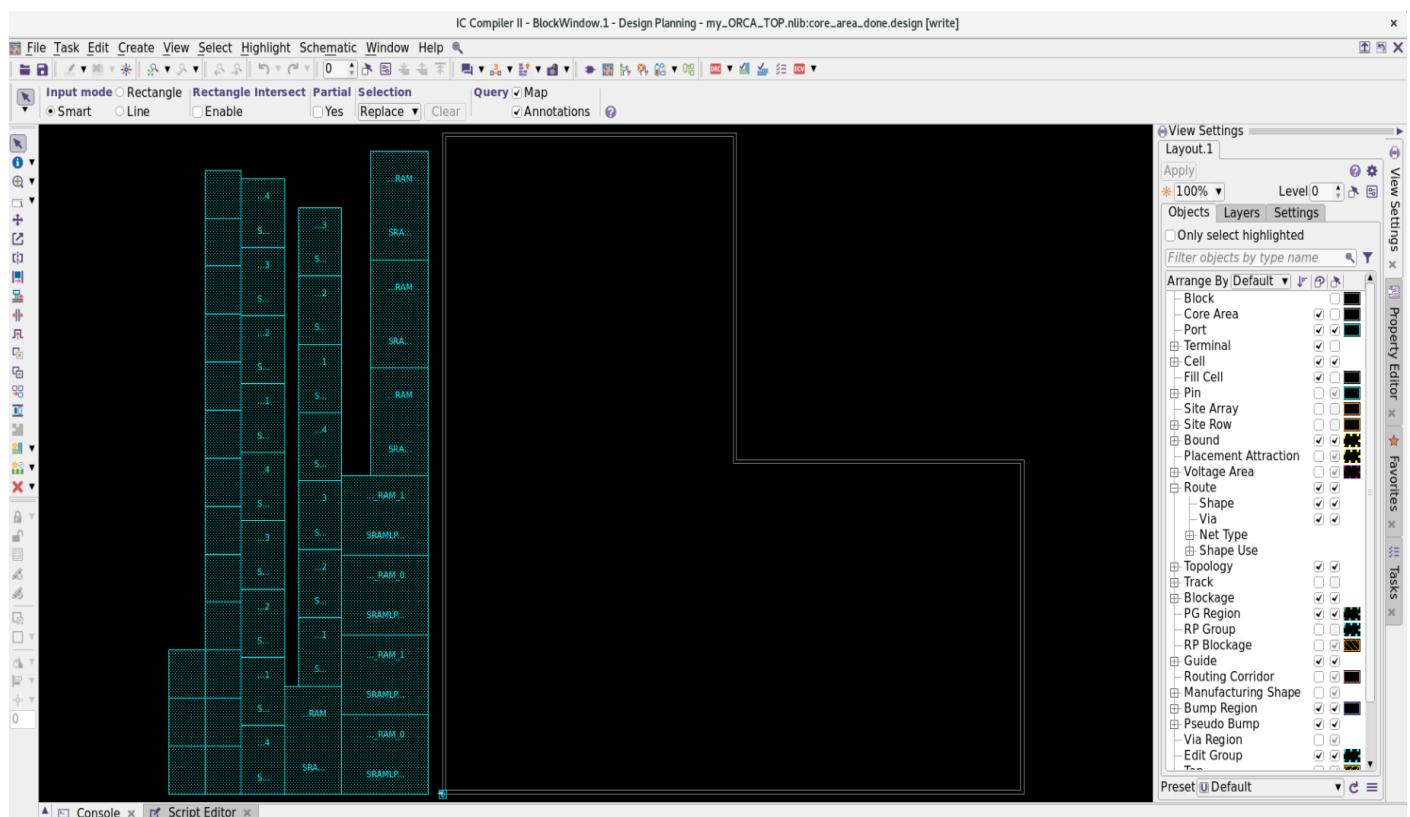
Project Name	: ORCA_TOP Multi-Voltage Block
Block Type	: Digital SoC Sub-Block with Multiple SRAM Macros
Technology Node	: 28 nm
Standard Cell Count	: ~ 60,000
Macro Count	: 40
Target Frequency	: 435 MHz

EDA Tools Used:

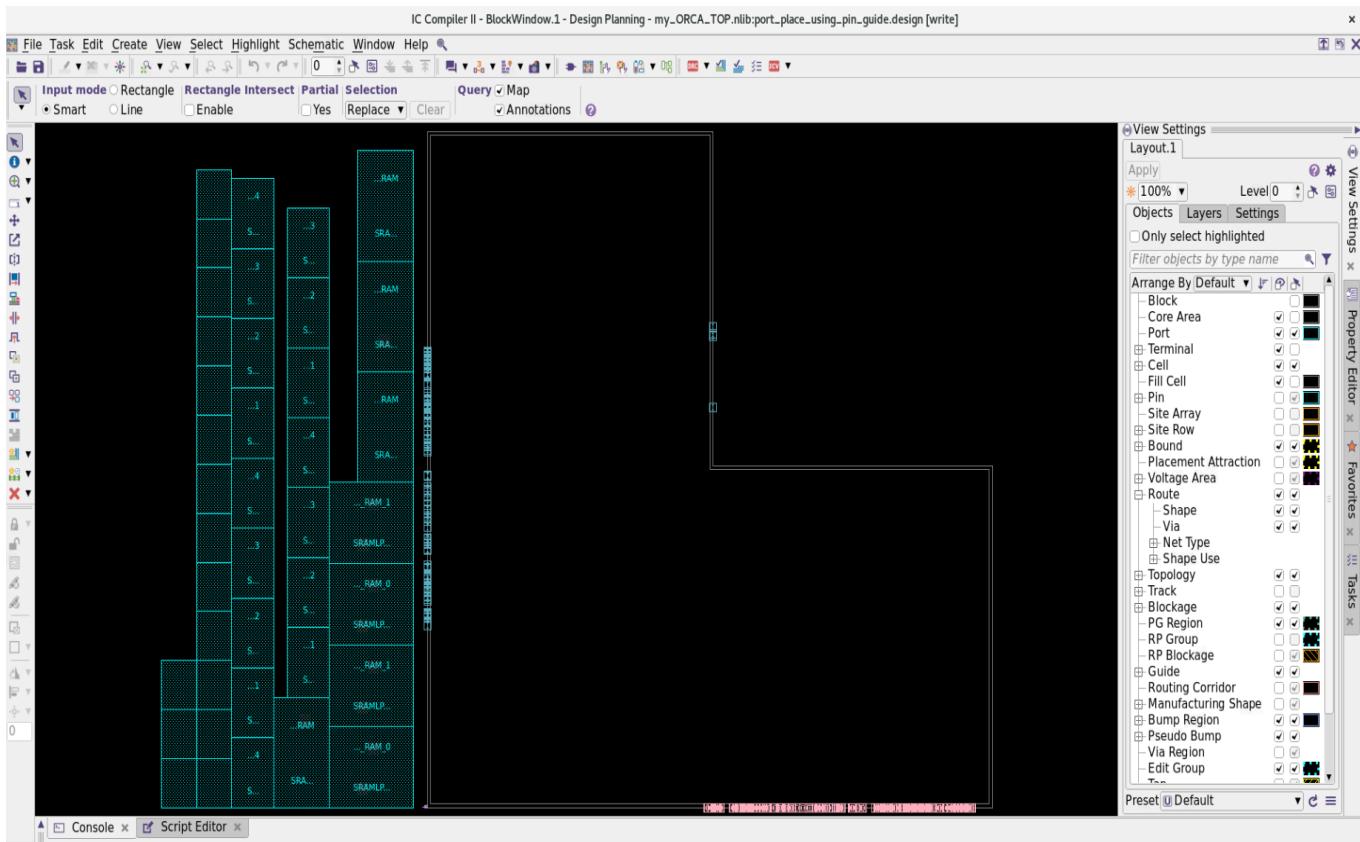
- Synopsys ICC2 (Place & Route)
- Synopsys PrimeTime (STA)
- Synopsys StarRC (Parasitic Extraction)

FLOORPLANNING

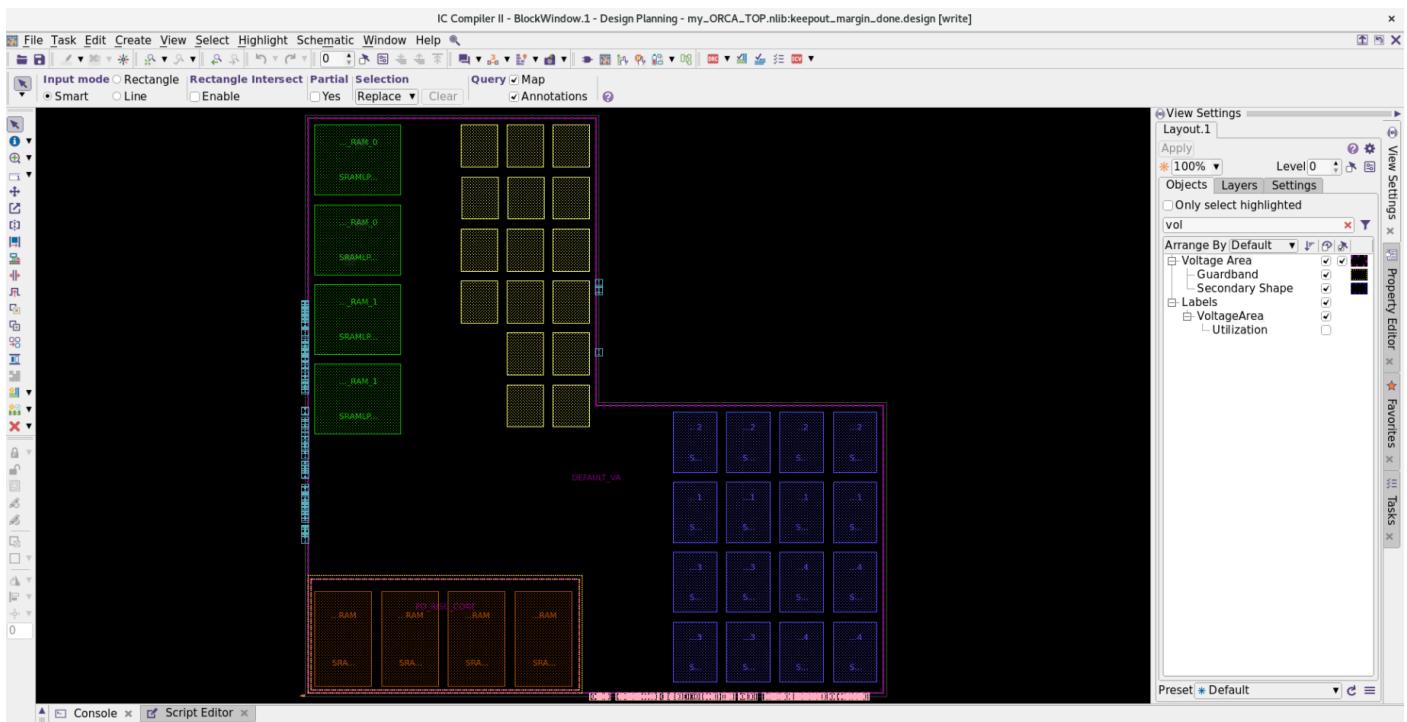
➤ Core Area using Utilization 0.75 and L shape



➤ Port placement

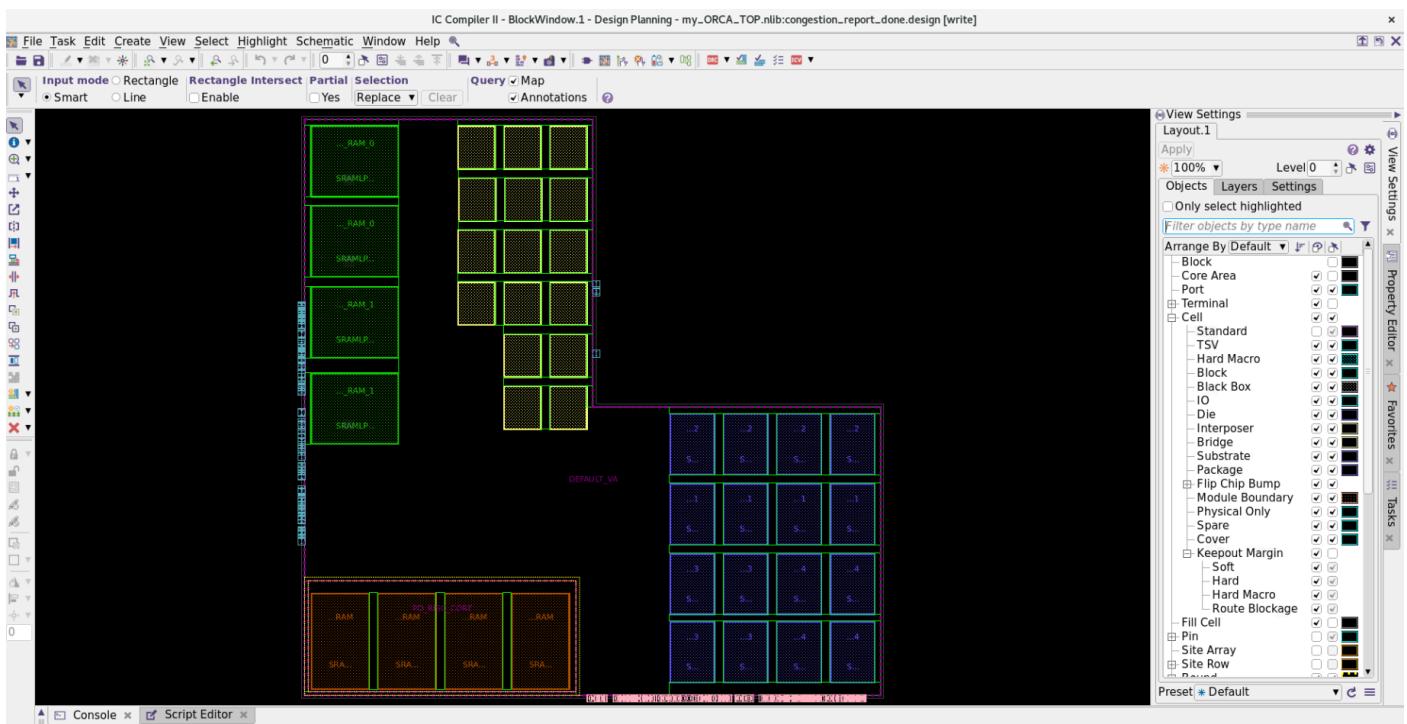


➤ Macro placement and voltage area creation

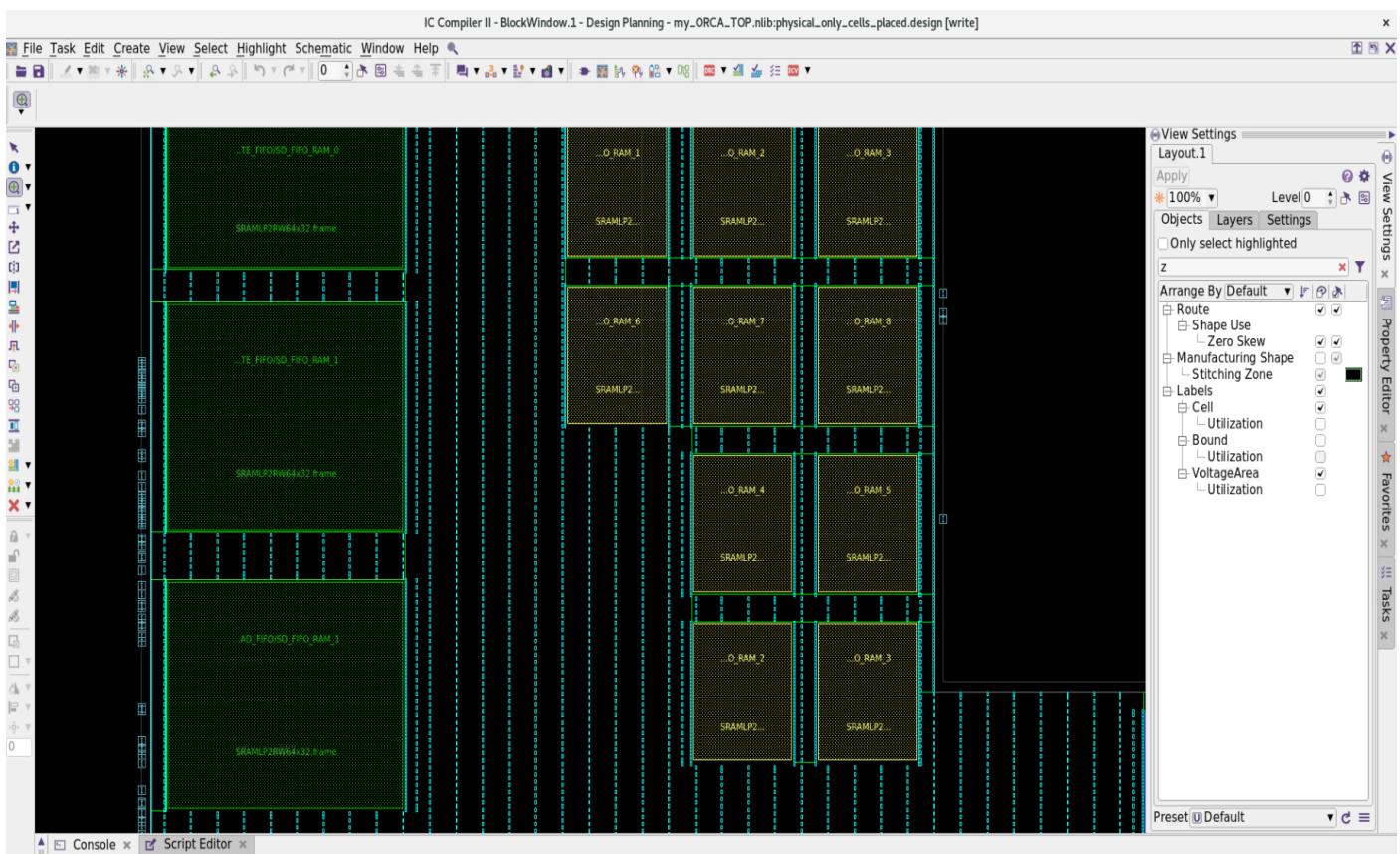


3 RTL to GDSII Implementation of ORCA_TOP Multi-Voltage Block

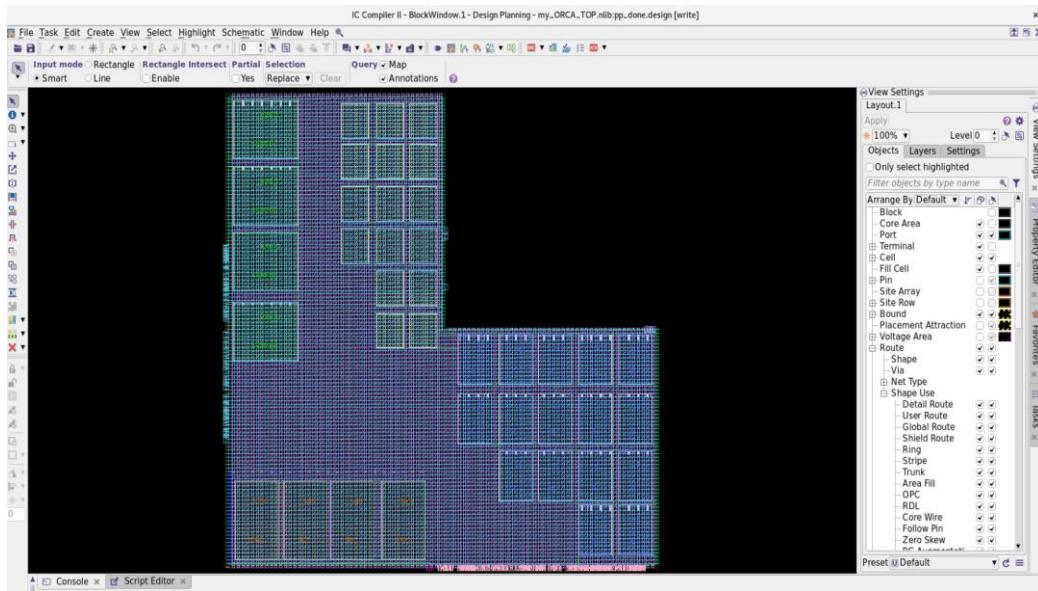
➤ Placement blockage



➤ Physical only cells



➤ Power planning



➤ Congestion report

```
icc2_shell> report_congestion
*****
Report : congestion
Design : ORCA_TOP
Version: S-2021.06-SP2
Date   : Tue Jan 13 09:20:35 2026
*****


Layer      |      overflow      | # GRCs has
Name       | total | max | overflow (%) | max overflow
-----+-----+-----+-----+-----+
Both Dirs |    26 |    1 | 26 ( 0.00%) |    26
H routing |    26 |    1 | 26 ( 0.01%) |    26
V routing |     0 |    0 |    0 ( 0.00%) |     0
-----+-----+-----+-----+-----+
```

1 -

➤ Check Pin Placement

```
icc2_shell> check_pin_placement -wire_track true
Warning: Didn't find any enabled planning block for check_pin_placement. (DPPA-268)
0 total number of pre-routes loaded
0 total number of vias loaded
0 total number of edges loaded
----- Start Of Missing Pin Check -----
----- End Of Missing Pin Check -----
```

```
----- Start Of Wire Track Check -----
----- End Of Wire Track Check -----
```

```
----- Start Of Technology Spacing Check -----
----- End Of Technology Spacing Check -----
```

```
----- Start Of Pin Short Check -----
----- End Of Pin Short Check -----
```

No violation has been found

Summary

Type of Violation	Count
Missing Pins	0
Pins Off Track	0
Pin Short	0
Technology Spacing	0
Total Violations	0

➤ Checking Boundary cells

```
icc2_shell> check_boundary_cells
*****
Report : check_boundary_cells
Design : pp_done
Version: S-2021.06-SP2
Date   : Tue Jan 13 09:30:24 2026
*****
Collecting design data...

Continuity report
=====
Information: No continuity violation. (CHF-024)
Continuity violations in design pp_done: 0

Redundant extra boundary cells report
=====
Information: No redundant extra boundary cells violation. (CHF-024)
Redundant extra boundary cell in design pp_done: 0

Corner and boundary cell report
=====
Information: No corner and boundary cell violation. (CHF-024)
Corner and boundary cell violations in design pp_done: 0

Orientation report
=====
Information: No orientation violation. (CHF-024)
Orientation violations in design pp_done: 0
1
```

➤ Checking tap cells legality

VIOLATIONS BY SUBCATEGORY:			
MOVABLE	APP-FIXED	USER-FIXED	DESCRIPTION
0	0	0	Two objects overlap.
0	0	0	Two cells overlap.
0	0	0	Two cells have overlapping keepout margins.
0	0	0	A cell overlaps a blockage.
0	0	0	A cell keepout margin overlaps a blockage.
0	0	0	A cell violates a pnet.
0	0	0	A cell is illegal at a site.
0	0	0	A cell violates pin-track alignment rules.
0	0	0	A cell is illegal at a site.
0	0	0	A cell violates legal index rule.
0	0	0	A cell has the wrong variant for its location.
0	0	0	A cell is not aligned with a site.
0	0	0	A cell is not aligned with the base site.
0	0	0	A cell is not aligned with an overlaid site.
0	0	0	A cell has an illegal orientation.
0	0	0	A cell spacing rule is violated.
0	0	0	A spacing rule is violated in a row.
0	0	0	A spacing rule is violated between adjacent rows.
0	0	0	A cell violates vertical abutment rule.
0	0	0	A cell violates metal spacing rule.
0	0	0	A layer rule is violated.
0	0	0	A layer VTH rule is violated.
0	0	0	A layer OD rule is violated.
0	0	0	A layer OD max-width rule is violated.
0	0	0	A layer ALL_OD corner rule is violated.
0	0	0	A layer max-vertical-length rule is violated.
0	0	0	A layer TPO rule is violated.
0	0	0	Filler cell insertion cannot satisfy layer rules.
0	0	0	A cell is in the wrong region.
0	0	0	A cell is outside its hard bound.
0	0	0	A cell is in the wrong voltage area.
0	0	0	A cell violates an exclusive movebound.
0	0	0	Two cells violate cts margins.
0	0	0	Two cells violate coloring.

check_legality for block design ORCA_TOP succeeded!

check_legality succeeded.

➤ Power and Ground Connectivity Check

```
icc2_shell> check_pg_connectivity -check_std_cell_pins none
Loading cell instances...
Number of Standard Cells: 0
Number of Macro Cells: 40
Number of IO Pad Cells: 0
Number of Blocks: 0
Loading P/G wires and vias...
Number of VDD Wires: 2096
Number of VDD Vias: 24138
Number of VDD Terminals: 189
*****Verify net VDD connectivity*****
    Number of floating wires: 0
    Number of floating vias: 0
    Number of floating std cells: 0
    Number of floating hard macros: 0
    Number of floating I/O pads: 0
    Number of floating terminals: 0
    Number of floating hierarchical blocks: 0
*****
Loading cell instances...
Loading P/G wires and vias...
Number of VDDH Wires: 396
Number of VDDH Vias: 1574
Number of VDDH Terminals: 76
*****Verify net VDDH connectivity*****
    Number of floating wires: 0
    Number of floating vias: 0
    Number of floating std cells: 0
    Number of floating hard macros: 0
    Number of floating I/O pads: 0
    Number of floating terminals: 0
    Number of floating hierarchical blocks: 0
*****
Loading cell instances...
Loading P/G wires and vias...
Number of VSS Wires: 4408
Number of VSS Vias: 53990
Number of VSS Terminals: 221
*****Verify net VSS connectivity*****
    Number of floating wires: 0
    Number of floating vias: 0
    Number of floating std cells: 0
    Number of floating hard macros: 0
    Number of floating I/O pads: 0
    Number of floating terminals: 0
    Number of floating hierarchical blocks: 0
*****
Overall runtime: 0 seconds.
```

➤ Check pg missing vias

```
icc2_shell> check_pg_missing_vias
Check net VDD vias...
Number of missing vias: 0
Checking net VDD vias took 0 seconds.
Check net VDDH vias...
Number of missing vias: 0
Checking net VDDH vias took 0 seconds.
Check net VSS vias...
Number of missing vias: 0
Checking net VSS vias took 1 seconds.
Overall runtime: 1 seconds.
```

➤ Check pg drc

```
icc2_shell> check_pg_drc -ig
ignore_clock_nets      ignore_keepout_margins ignore_std_cells
icc2_shell> check_pg_drc -ignore_std_cells
Command check_pg_drc started at Tue Jan 13 10:04:33 2026
Command check_pg_drc finished at Tue Jan 13 10:04:36 2026
CPU usage for check_pg_drc: 3.34 seconds ( 0.00 hours)
Elapsed time for check_pg_drc: 3.34 seconds ( 0.00 hours)
No errors found.
```

PLACEMENT

➤ Pre-Placement Mega Checks

```
icc2_shell> check_design -checks pre_placement_stage
*****
Report : check_design
Options: { pre_placement_stage }
Design : ORCA_TOP
Version: S-2021.06-SP2
Date   : Tue Jan 13 10:08:13 2026
*****  

Running mega-check 'pre_placement_stage':
  Running atomic-check 'design_mismatch'
  Running atomic-check 'scan_chain'
  Running atomic-check 'mv_design'
  Running atomic-check 'rp_constraints'
  Running atomic-check 'timing'
  Running atomic-check 'hier_pre_placement'  

*** EMS Message summary ***
-----  

Rule      Type    Count     Message
-----  

TCK-001    Warn    23620    The reported endpoint '%endpoint' is unconstrained. Reason: '%re...
TCK-002    Warn     45       The register clock pin '%pin' has no fanin clocks. Mode:'%mode'.
TCK-012    Warn     82       The input port '%port' has no clock_relative delay specified. Mo...
-----  

Total 23747 EMS messages : 0 errors, 23747 warnings, 0 info.  

-----  

*** Non-EMS message summary ***
-----  

Rule      Type    Count     Message
-----  

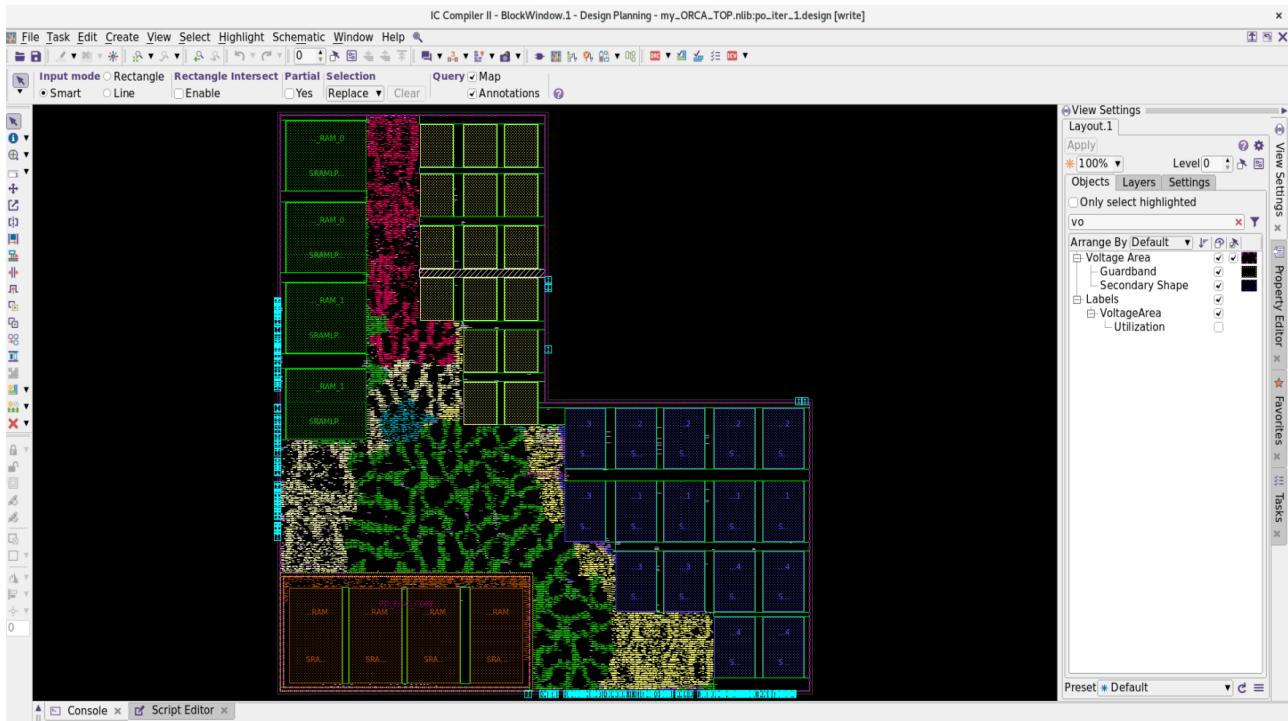
NDMUI-173        1       There are no relative placement groups in the design.
PVT-032         2       Corner %s: no PVT mismatches.
TIM-124         1       RDE mode is turned %s.
-----  

Total 4 non-EMS messages : 0 errors, 0 warnings, 4 info.  

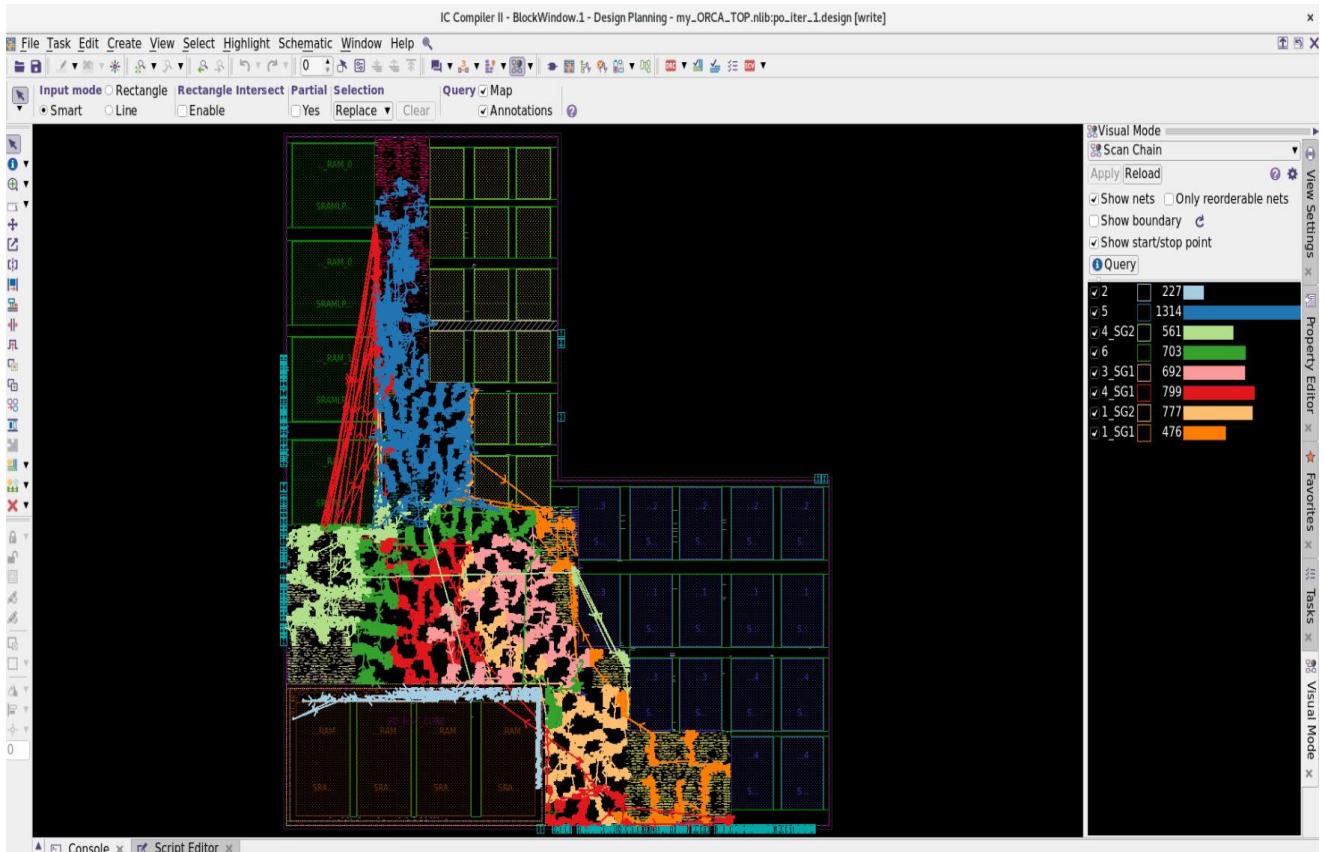
-----  

Information: EMS database is saved to file 'check_design.ems'.
Information: Non-EMS messages are saved into file 'check_design2026Jan13100813.log'.
1
```

➤ Placement of std cells



➤ Scan chain reordering



➤ Reports

Constraint	Cost
min_delay/hold	0.44 (VIOLATED)
max_delay/setup	0.00 (MET)
max_transition	8.52 (VIOLATED)
max_capacitance	1862.30 (VIOLATED)
min_capacitance	0.00 (MET)

```
icc2_shell> report_congestion
*****
Report : congestion
Design : ORCA_TOP
Version: S-2021.06-SP2
Date   : Tue Jan 13 10:18:18 2026
*****
```

Layer	overflow	# GRCs has		
Name	total	max	overflow (%)	max overflow
Both Dirs	762	7	457 (0.08%)	2
H routing	672	7	383 (0.13%)	2
V routing	90	4	74 (0.03%)	1

```
icc2_shell> report_utilization -config a
*****
Report : report_utilization
Design : ORCA_TOP
Version: S-2021.06-SP2
Date   : Tue Jan 13 10:19:26 2026
*****
Utilization Ratio: 0.7790
Utilization options:
- Area calculation based on: core_area of block po_iter_1
- Categories of objects excluded: None
Total Area: 585529.4776
Total Capacity Area: 585529.4776
Total Area of cells: 456132.2929
0.7790
```

```
icc2_shell> report_net_fanout -high_fanout
*****
Report : net_fanout
    -high_fanout
Design : ORCA_TOP
Version: S-2021.06-SP2
Date   : Tue Jan 13 10:26:07 2026
*****
```

NetName	Fanout Driver
I_BLENDER_0/net23067	747 I_BLENDER_0/clk_gate_rem_green_reg/latch/GCLK
I_BLENDER_1/net23049	851 I_BLENDER_1/clk_gate_rem_green_reg/latch/GCLK
I_SDRAM_TOP/I_SDRAM_IF/net23014	1345 I_SDRAM_TOP/I_SDRAM_IF/clk_gate_mega_shift_0_reg[0]/latch/GCLK
I_SDRAM_TOP/I_SDRAM_IF/net23031	1345 I_SDRAM_TOP/I_SDRAM_IF/clk_gate_mega_shift_1_reg[0]/latch/GCLK

```

icc2_shell> report_global_timing
*****
Report : global timing
  -format { narrow }
Design : ORCA_TOP
Version: S-2021.06-SP2
Date   : Tue Jan 13 10:21:52 2026
*****


Setup violations
-----
      Total    reg->reg    in->reg    reg->out    in->out
-----
WNS      -0.10      -0.10      0.00      0.00      0.00
TNS      -5.31      -5.31      0.00      0.00      0.00
NUM       146        146        0          0          0
-----


Hold violations
-----
      Total    reg->reg    in->reg    reg->out    in->out
-----
WNS      -0.08      -0.08      0.00      0.00      0.00
TNS     -12.50     -12.50      0.00      0.00      0.00
NUM       908        908        0          0          0
-----
```

CTS - Clock Tree Synthesis

➤ Pre CTS mega-check

```

icc2_shell> check_design -checks pre_clock_tree_stage
*****
Report : check_design
Options: { pre_clock_tree_stage }
Design : ORCA_TOP
Version: S-2021.06-SP2
Date   : Tue Jan 13 10:38:52 2026
*****


Running mega-check 'pre_clock_tree_stage':
  Running atomic-check 'design_mismatch'
  Running atomic-check 'scan_chain'
  Running atomic-check 'mv_design'
  Running atomic-check 'legality'
  Running atomic-check 'timing'
  Running atomic-check 'clock_trees'
  Running atomic-check 'hier_pre_clock_tree'

*** EMS Message summary ***
-----  

Rule      Type  Count   Message
-----  

CTS-012    Warn   1      Net %net in the clock network have a dont_touch constraint.  

CTS-013    Warn   35     Cell %inst in the clock network have a dont_touch constraint as ...  

CTS-019    Warn   34     Clock %clock traverse to pin %pin which is a output port because...  

CTS-904    Warn   4      Clock reference cell %libcell(cell %cell) have no LEQ cell speci...  

CTS-905    Warn   2      Clock %clock(%mode) with no sinks.  

TCK-001    Warn  23902   The reported endpoint '%endpoint' is unconstrained. Reason: '%re...  

TCK-002    Warn   181    The register clock pin '%pin' has no fanin clocks. Mode:'%mode'.  

TCK-012    Warn   82     The input port '%port' has no clock_relative delay specified. Mo...  

-----  

Total 24241 EMS messages : 0 errors, 24241 warnings, 0 info.

*** Non-EMS message summary ***
-----  

Rule      Type  Count   Message
-----  

CTS-101    1      %s will work on the following scenarios.  

CTS-107    1      %s will work on all clocks in active scenarios, including %d mas...  

LGL-130    1      Legalizer threading is enabled with %s effort  

LGL-150    3195   %s  

LGL-336    6      Adjusting %s to a multi-height library cell.  

NPLDRC-003  1      Reading PG structure for '%'.  

NPLDRC-007  5      Detected a sector %s on layer %s with %d metal and/or via shapes.  

PVT-032    2      Corner %s: no PVT mismatches.  

-----  

Total 3207 non-EMS messages : 0 errors, 5 warnings, 3207 info.

Warning: EMS database "check_design.ems" already exists, over-writing it. (EMS-040)  

Information: EMS database is saved to file 'check_design.ems'.  

Information: Non-EMS messages are saved into file 'check_design2026Jan13103852.log'.
1
```

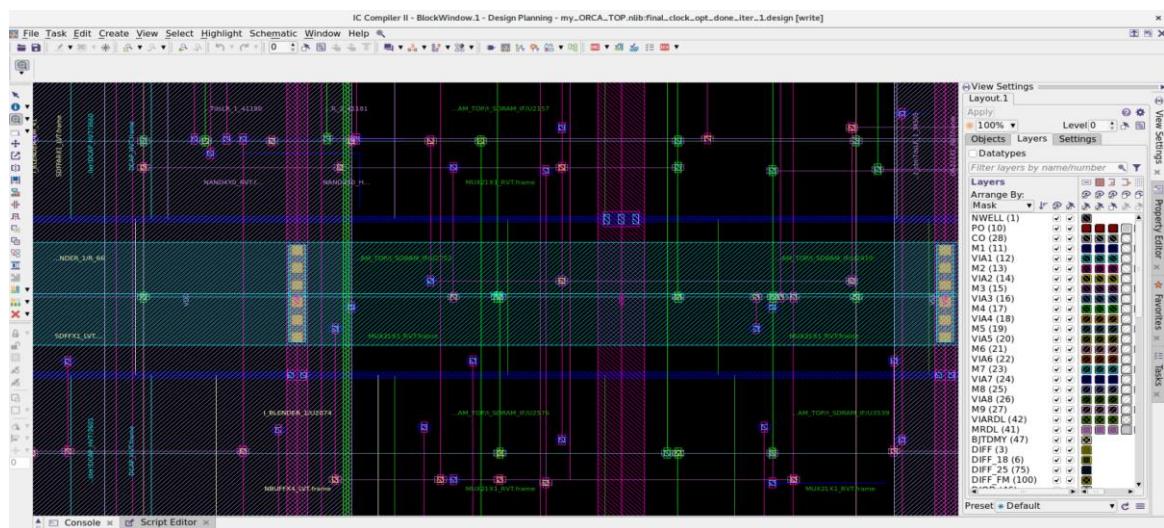
➤ CTS clock window overview

IC Compiler II - CTSWindow.1 - my_ORCA_TOP.nlb:final_clock_opt_done_iter_1.design

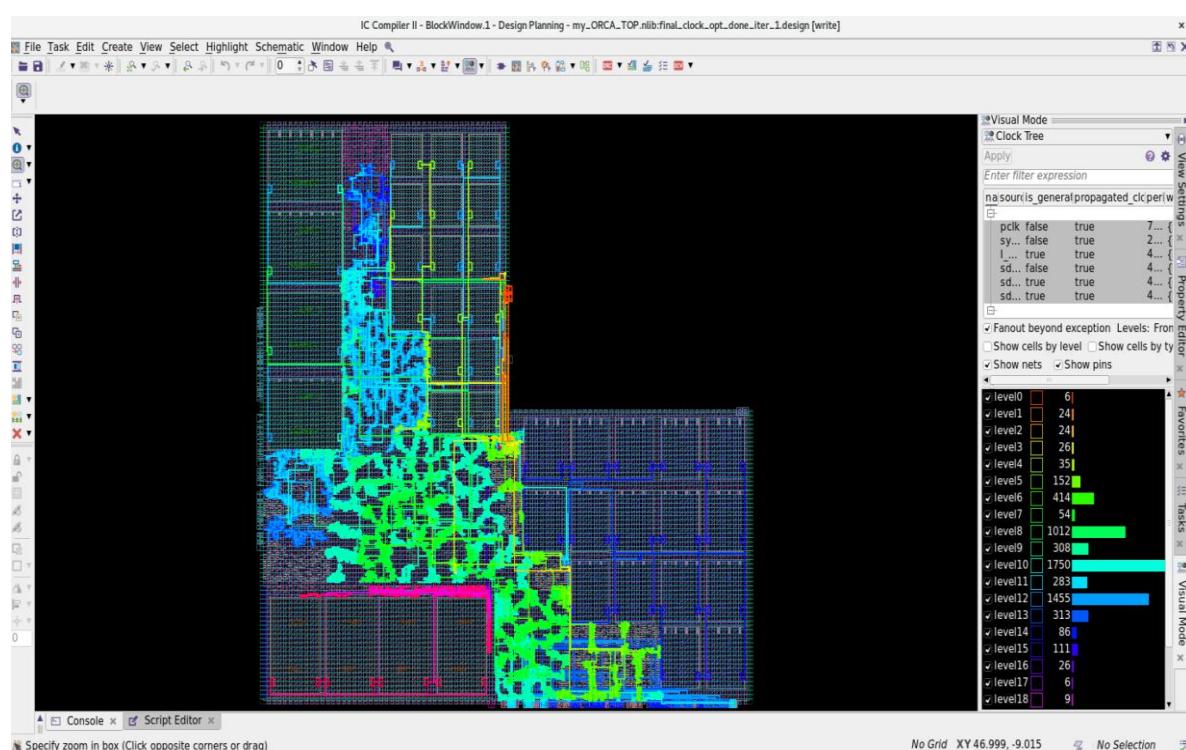
The screenshot shows the IC Compiler II interface with the title bar "IC Compiler II - CTSWindow.1 - my_ORCA_TOP.nlb:final_clock_opt_done_iter_1.design". The main window displays a table titled "Enter filter expression" with columns: name, sources, is_generated, propagated_clock, period, waveform, and skew_groups. The table lists various clock signals and their properties.

name	sources	is_generated	propagated_clock	period	waveform	skew_groups
func						
M PCI_CLK	pclk	false	true	7.500000 {0.000000 3.750000}		default_PCI_CLK
M SDRAM_CLK	sdram_clk	false	true	4.100000 {0.000000 2.050000}		default_SDRAM_CLK
G SD_DDR_CLK	sd_CK	true	true	4.100000 {0.000000 2.050000}		
G SD_DDR_CLKn	sd_CKn	true	true	4.100000 {0.050000 4.100000}		
M SYS_2x_CLK	sys_2x_clk	false	true	2.300000 {0.000000 1.150000}		default_SYS_2x_CLK
G SYS_CLK	I_CLOCKING/sys_clk_in_reg/Q	true	true	4.600000 {0.000000 2.300000}		
V v_PCI_CLK		false	false	7.500000 {0.000000 3.750000}		default_v_PCI_CLK
V v_SDRAM_CLK		false	false	4.100000 {0.000000 2.050000}		default_v_SDRAM_CLK
test						
M ate_clk	ate_clk	false	true	30.0000... {0.000000 15.000000}		default_ate_clk

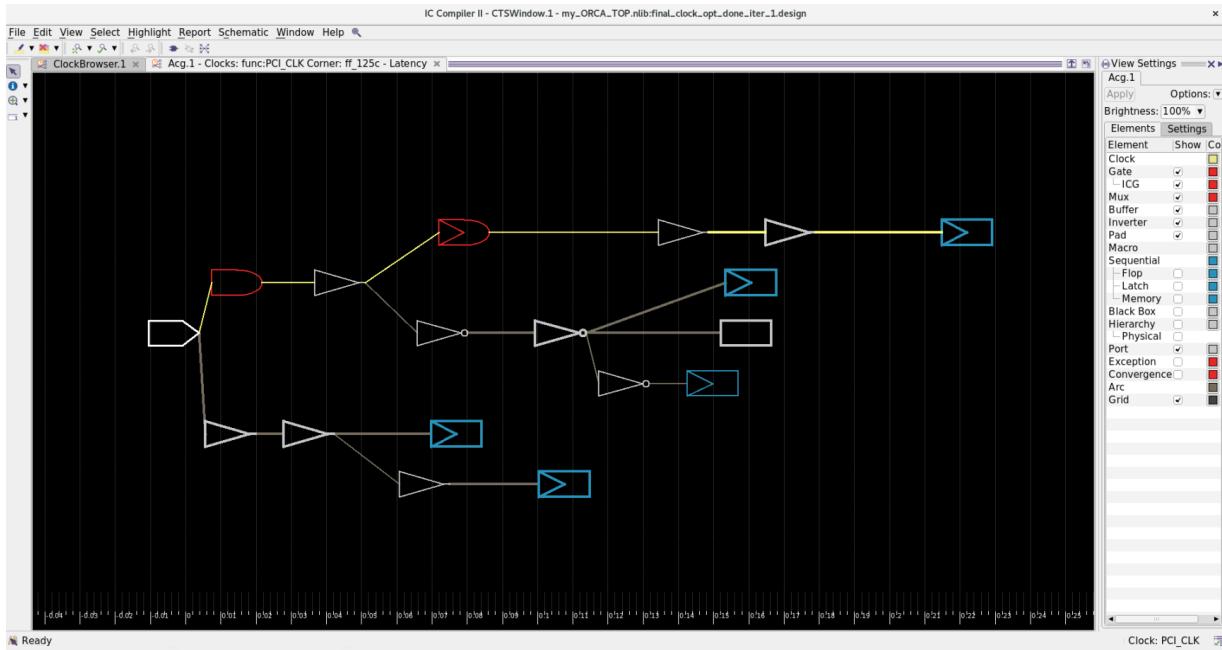
➤ Clock path routed



➤ CLOCK_TREE



➤ Leveled Clock Tree



➤ Report of global timing

```
icc2_shell> report_global_timing
Information: Timer using 'CRPR'. (TIM-050)
*****
Report : global timing
  -format { narrow }
Design : ORCA_TOP
Version: S-2021.06-SP2
Date   : Tue Jan 13 11:13:15 2026
*****
```

Setup violations

	Total	reg->reg	in->reg	reg->out	in->out
WNS	-0.06	-0.06	0.00	0.00	0.00
TNS	-1.70	-1.70	0.00	0.00	0.00
NUM	86	86	0	0	0

Hold violations

	Total	reg->reg	in->reg	reg->out	in->out
WNS	-0.04	-0.03	0.00	0.00	-0.04
TNS	-0.46	-0.17	0.00	0.00	-0.29
NUM	40	15	0	0	25

➤ Report of constraints

Constraint	Cost
min_delay/hold	0.00 (MET)
max_delay/setup	0.13 (VIOLATED)
max_transition	6.68 (VIOLATED)
max_capacitance	1360.54 (VIOLATED)
min_capacitance	0.00 (MET)

ROUTING

➤ Pre routing checks

```
icc2_shell> check_design -checks pre_route_stage
*****
Report : check_design
Options: { pre_route_stage }
Design : ORCA_TOP
Version: S-2021.06-SP2
Date   : Tue Jan 13 11:22:00 2026
*****


Running mega-check 'pre_route_stage':
  Running atomic-check 'design_mismatch'
  Running atomic-check 'scan_chain'
  Running atomic-check 'mv_design'
  Running atomic-check 'timing'
  Running atomic-check 'routability'
  Running atomic-check 'hier_pre_route'

*** EMS Message summary ***

Rule      Type     Count    Message
-----
TCK-001   Warn    23938   The reported endpoint '%endpoint' is unconstrained. Reason: '%re...
TCK-002   Warn    181     The register clock pin '%pin' has no fanin clocks. Mode:'%mode'.
TCK-012   Warn    82      The input port '%port' has no clock_relative delay specified. Mo...
-----


Total 24201 EMS messages : 0 errors, 24201 warnings, 0 info.
-----


*** Non-EMS message summary ***

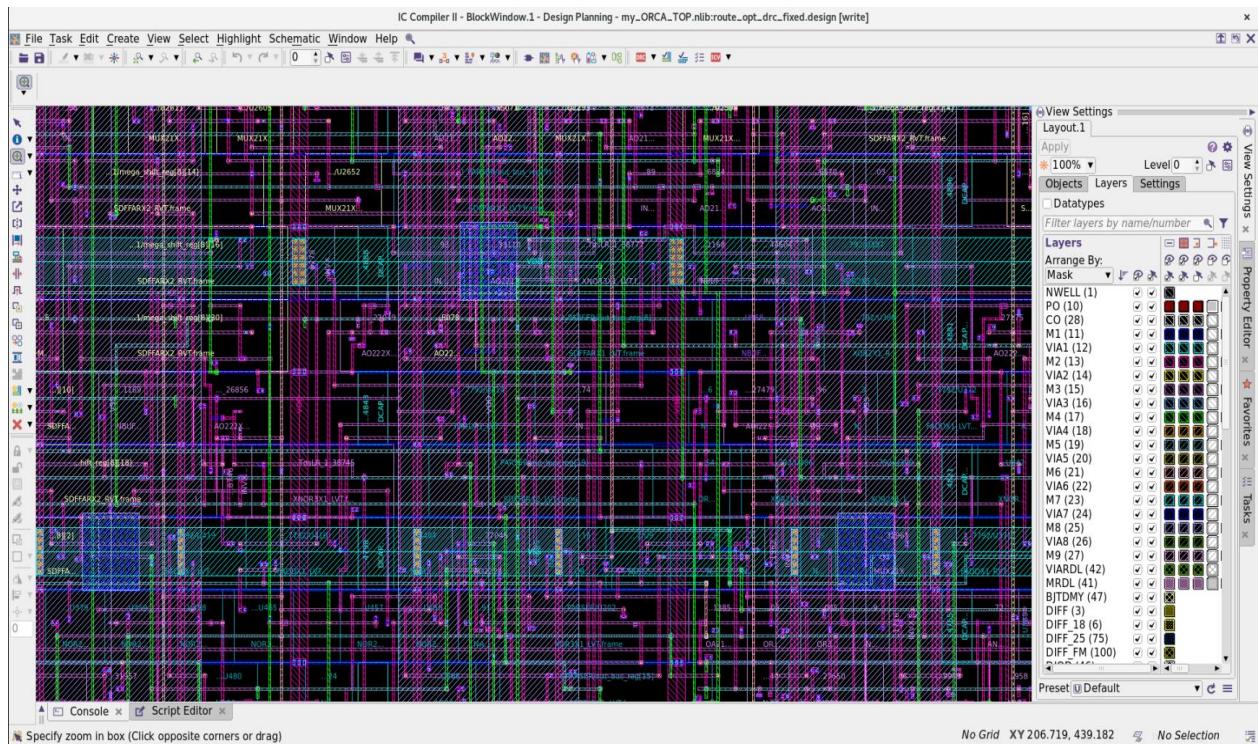
Rule      Type     Count    Message
-----
PVT-032    2       Corner %s: no PVT mismatches.
ZRT-022    1       Cannot find a default contact code for layer %s.
ZRT-044    3       Standard cell pin %s/%s has no valid via regions.
ZRT-703    1       Option route.detail.force_end_on_preferred_grid will be ignored ...
ZRT-706    1       When applicable layer based tapering will taper up to %.2f in di...
ZRT-707    1       When applicable Min-max layer allow_pin_connection mode will all...
-----


Total 9 non-EMS messages : 0 errors, 5 warnings, 4 info.
-----


Warning: EMS database "check_design.ems" already exists, over-writing it. (EMS-040)

Information: EMS database is saved to file 'check_design.ems'.
Information: Non-EMS messages are saved into file 'check_design2026Jan13112200.log'.
1
```

➤ Routed nets



➤ Check_routes

Verify Summary:

Total number of nets = 53784, of which 0 are not extracted

Total number of open nets = 0, of which 0 are frozen

Total number of excluded ports = 0 ports of 0 unplaced cells connected to 0 nets

0 ports without pins of 0 cells connected to 0 nets

0 ports of 0 cover cells connected to 0 non-pg nets

Total number of DRCs = 0

Total number of antenna violations = no antenna rules defined

Information: Routes in non-preferred voltage areas = 2073 (ZRT-559)

Total number of tie to rail violations = not checked

Total number of tie to rail directly violations = not checked

➤ Check_lvs

Total number of input nets is 53845.

Total number of short violations is 0.

Total number of open nets is 0.

Total number of floating route violations is 0.

Elapsed = 0:00:23, CPU = 0:00:23

TIMING CLOSURE

➤ Report global timing

```
*****
Report : global timing
    -format { narrow }
Design : ORCA_TOP
Version: S-2021.06-SP2
Date   : Mon Jan 12 13:37:16 2026
*****
```

No setup violations found.

Hold violations

	Total	reg->reg	in->reg	reg->out	in->out
WNS	-0.06	-0.06	-0.00	0.00	-0.06
TNS	-2.87	-1.20	-0.00	0.00	-1.66
NUM	111	78	1	0	32

1

➤ Report constraints

Constraint	Cost
min_delay/hold	0.00 (MET)
max_delay/setup	0.00 (MET)
max_transition	0.00 (MET)
max_capacitance	0.00 (MET)
min_capacitance	0.00 (MET)

➤ **Report_constraints -max_capacitance -max_transition -nosplit -max_delay -all_violators -scenarios ***

```

Information: Timer using 'SI, Timing Window Analysis, CRPR'. (TIM-050)
Endpoint          Path Delay      Path Required      CRP      Slack Group      Scenario
-----
No paths.

Mode: func Corner: ff_125c
Scenario: func_ff_125c
-----
Number of max_transition violation(s): 0

Mode: func Corner: ss_m40c
Scenario: func_ss_m40c
-----
Number of max_transition violation(s): 0

Mode: test Corner: ff_125c
Scenario: test_ff_125c
-----
Number of max_transition violation(s): 0

Mode: test Corner: ss_m40c
Scenario: test_ss_m40c
-----
Number of max_transition violation(s): 0

Mode: func Corner: ff_125c
Scenario: func_ff_125c
-----
Number of max_capacitance violation(s): 0

Mode: func Corner: ss_m40c
Scenario: func_ss_m40c
-----
Number of max_capacitance violation(s): 0

Mode: test Corner: ff_125c
Scenario: test_ff_125c
-----
Number of max_capacitance violation(s): 0

Mode: test Corner: ss_m40c
Scenario: test_ss_m40c
-----
Number of max_capacitance violation(s): 0

Total number of violation(s): 0
1

```