Title:

Performance study of two-level on-chip caches in a fixed area.

Abstract:

Memory hierarchy performance, specifically cache memory capacity, is a constraining factor in the performance of modern computers. This paper will present the results of twolevel cache memory simulations and examines the impact of exclusive caching on system performance. Exclusive caching enables higher capacity with the same cache area by eliminating redundant copies. The experiments will compare an exclusive cache hierarchy with an inclusive cache hierarchy utilizing similar L1 and L2 parameters. The performance differences will be illustrated using the L2 cache misses and execution time metrics. With equal size victim buffer and victim cache for exclusive and inclusive cache hierarchies respectively, some benchmarks show increased execution time for exclusive caches because a victim cache can reduce conflict misses significantly while a victim buffer can introduce worst-case penalties. Considering the inconsistent performance improvement, the increased complexity of an exclusive cache hierarchy needs to be justified based upon the specifics of the application and system.