SVKM's
D. J. Sanghvi College of Engineering

Program: B.Tech in Computer Science and Engineering (IOT and Cyber Security with Block Chain Technology **Academic Year: 2022** **Duration: 3 hours**
Date: 27.01.2023
Time: 09:00 am to 12:00 pm
Subject: Digital Logic Design and Applications (Semester III) **Marks: 75**

Instructions: Candidates should read carefully the instructions printed on the question paper and on the cover page of the Answer Book, which is provided for their use.
(1) This question paper contains two pages.
(2) All Questions are Compulsory.
(3) All questions carry equal marks.
(4) Answer to each new question is to be started on a fresh page.
(5) Figures in the brackets on the right indicate full marks.
(6) Assume suitable data wherever required, but justify it.
(7) Draw the neat labelled diagrams, wherever necessary.

Question No.		Max. Marks
Q1 (a)	(i) Convert $(1134.21)_{10}$ into octal and hexadecimal numbers (ii) Compute $(60)_{10} - (70)_{10}$ using 2's complement method (iii) Compute $(FB9F)_{16} - (C5D7)_{16}$ **OR** (i) Represent $(521)_{10}$ into excess-3, BCD, and gray code (ii) Write a short note on Hamming code.	[05] [02] [03] [05] [05]
Q1 (b)	With the help of Boolean laws, ~~prove that~~ simplify $F = A\,(B + C(AB + AC)')$	[05]
Q2 (a)	Minimize the following expression using k-map and implement using basic gates. F(A,B,C,D)=∑m(1,7,9,10,11,15)+ d(2,3,5) **OR** Realize the following logic function in SOP form using The Quine-Mc Cluskey method. f(A,B,C,D) = ΠM(2,7,8,9,10,12)	[10] [10]
Q2 (b)	Explain 2 to 4-line decoder by drawing suitable diagram and truth table. Write the Boolean expression and draw the logic diagram.	[05]

Q3 (a)	Explain with a neat diagram 4-bit binary subtractor. **OR** Implement a 32:1 multiplexer using 16:1 multiplexer. Write a truth table and draw the circuit.	[10] [10]
Q3 (b)	Design the full adder using a 1:8 demultiplexer. Write a truth table and draw the circuit.	[05]
Q4 (a)	Draw the circuit diagram of JK flip flop using NAND gates. Draw its characteristics equation and excitation table. What is the race condition in JK flip flop and how it can be avoided.	[10]
Q4 (b)	Convert a JK Flip-Flop to T Flip-Flop.	[05]
Q5 (a)	Design and implement MOD 6 Asynchronous counter using T flip-flops. **OR** With the help of a neat diagram explain the functioning of a 4-bit bidirectional shift register	[10] [10]
Q5 (b)	Compare PLA, PAL and PROM. **OR** Explain capacitive and magnetic sensors in detail.	[05] [05]