SVKM's
D. J. Sanghvi College of Engineering

Program: B.Tech in Computer Engineering **Academic Year: 2022** **Duration: 3 hours**
Date: 27.01.2023
Time: 09:00 am to 12:00 pm
Subject: Digital Electronics (Semester III) **Marks: 75**

Instructions: Candidates should read carefully the instructions printed on the question paper and on the cover page of the Answer Book, which is provided for their use.
(1) This question paper contains two pages.
(2) All Questions are Compulsory.
(3) All questions carry equal marks.
(4) Answer to each new question is to be started on a fresh page.
(5) Figures in the brackets on the right indicate full marks.
(6) Assume suitable data wherever required, but justify it.
(7) Draw the neat labelled diagrams, wherever necessary.

Question No.		Max. Marks
Q1 (a)	i. Perform following conversions. a) $(A\ 7\ 2\ E)_{16} = (?)_8$ b) $(6\ 5\ 5\ 3\ 5)_{10} = (?)_{16}$ c) $(0\ 7\ E\ 5)_{16} = (?)_{10}$ d) $(2\ 4\ 7\ .\ 3\ 6)_8 = (?)_{16}$	[04]
	ii. Represent decimal number 27 in binary form using a) Binary code b) Gray code c) BCD code d) Octal code e) Excess-3 code f) Hexadecimal code	[06]
	OR Perform following hexadecimal subtractions using 16's complement method. a) (6 9 A) – (C 1 3) b) (9 7 1) – (C B 1)	[10]
Q1 (b)	What is Hamming code? Generate 7 bit hamming code for given data bits 1011.	[05]
Q2 (a)	i. Prove the following using Boolean algebra. $(A + B)(\bar{A} + C) = AC + \bar{A}B$	[05]
	ii. Solve the following function using K-map and implement simplified expression using NAND gate only. $F = ABC\bar{D} + \bar{B}\bar{C} + \bar{B}D + AB\bar{C}\bar{D} + \bar{B}C$	[05]

	OR i. Simplify following logical expression using Boolean algebra and implement the simplified expression using logic gates. $(A+C+D)(A+C+\bar{D})(A+\bar{C}+D)(A+\bar{B})$ ii. Solve the following function using K-map and implement simplified expression using NAND gate only. $F = \sum m\ (0,1,2,3,7,8,9,10,11,12,13)$	[05] [05]
Q2 (b)	Implement Exclusive gates using NAND gates only.	[05]
Q3 (a)	Convert Y=A+BC′+AB+A′BC into canonical form.	[05]
Q3 (b)	i. What is Multiplexer? Implement given function using 8:1 Mux only. $F = \sum m\ (3,9,10,11,12,13,15)$ ii. Design a combinational logic circuit that checks for even parity of four bits. A logic 1 output is required when four bits do not constitute an even parity. **OR** Explain BCD addition with suitable example and design BCD adder circuit with neat diagram.	[05] [05] [10]
Q4 (a)	Enlist types of Flip-Flops. Draw and explain J-K Flip-Flop. **OR** i. Enlist types of Flip-Flops. Draw and explain S-R Flip-Flop ii. Write and explain excitation table of SR Flip-flop.	[10] [05] [05]
Q4 (b)	Design sequential logic circuit to generate sequence of bits 10110.	[05]
Q5 (a)	Design decade UP counter. Use JK FLIP-FLOPS.	[10]
Q5 (b)	i. Write a short note on PLA. **OR** ii. Write a short note on Sensors.	[05] [05]