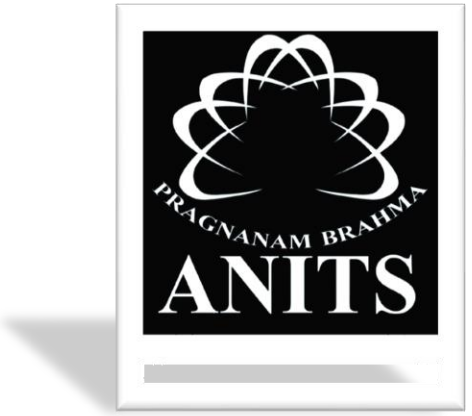
Course Name: Micro Processors and Micro Controllers

Topic Name: 8085 Microprocessor



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Course Objectives:

At the end of the course, students will be able to

- **CO1** (BL-2) Describe the architecture and various addressing modes of a typical 8085 microprocessor
- **CO2** (BL-4) Classify different memory devices to Discuss the interfacing between memory and 8085 microprocessor
- **CO3** (BL-3) Describe the architecture of a typical 8086 microprocessor to illustrate the general bus operations
- **CO4** (BL-3) Describe the various peripheral devices and show how the peripherals (8259,8251 & 8253) are interfaced with Microprocessor.
- **CO5** (BL-4) Use the architecture of 8051 microcontroller and illustrate how 8051 is interfaced with advanced applications.

Syllabus

UNIT 2

Memory Devices & Interfacing:

Introduction to memory device, Types of memory devices, Difference between SRAM and DRAM, Chip select signal generation, Memory interfacing with processor, I/O and peripheral device interfacing: Memory mapped and standard I/O mapped.

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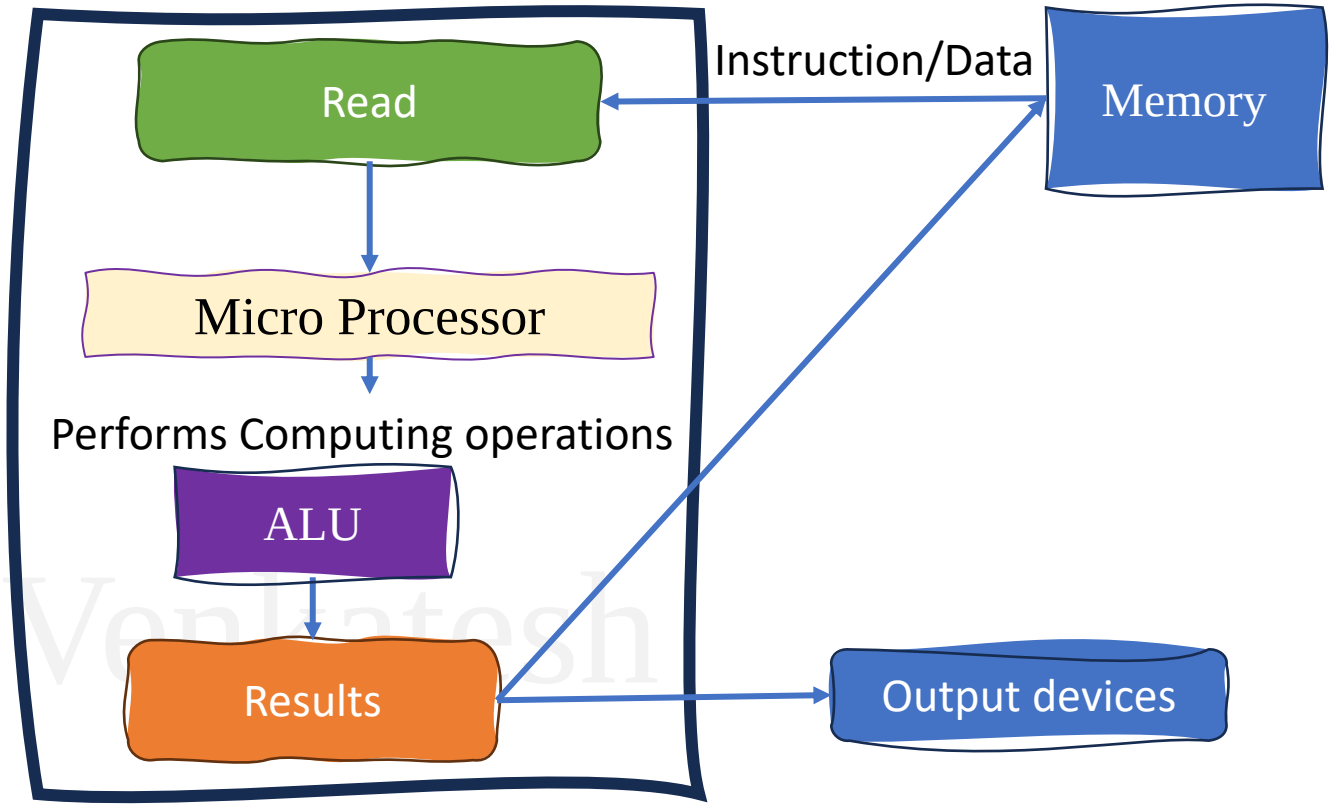
Introduction to Memory Devices

What is Memory?

Memory **stores the binary information as instructions, data** and provides that information to microprocessor whenever necessary.

The **no. of bits stored in a register** is called as "**Memory**".



Memory significance in executing a Program

The microprocessor → Reads instruction/data from memory → Computing operations are performed in ALU → Results are transferred to output devices or memory for later use.

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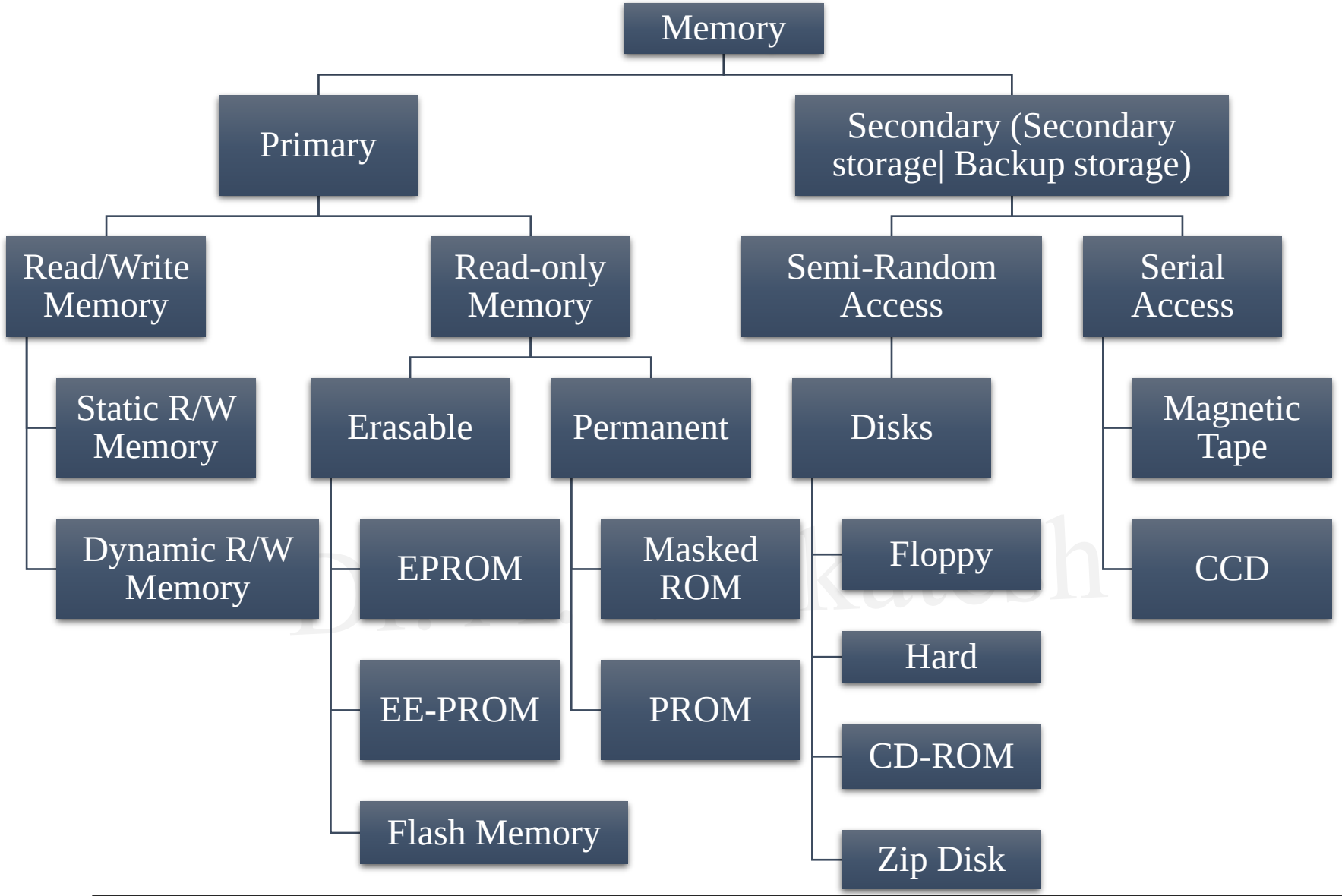
Memory Classification



Primary vs Secondary Memory

Primary(system or main) memory:

- Volatile
- Directly accessed by CPU
- High speed but low density.
- Expensive

- RAM
- Used for temporarily storing data and software that the CPU is actively using

Secondary(Storage) memory:

- Non-volatile
- Indirectly accessed by CPU (initially transferred to primary memory and the processed by CPU)
- Low speed but high density.
- Less Expensive than primary memory

- Hard drives and SSDs
- Used for long-term data storage, including the operating system, applications, and user files

Capacity of memory = Density*speed

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Primary Memory: R/W Memory (SRAM Vs DRAM)

R/W Memory:

- **RAM is a volatile memory** type used for **temporary storage of data** and **program instructions** that are actively being processed by a computer or electronic device.
- It allows fast read and write operations, making it suitable for quick data access.
- RAM used for **Running programs, holding the operating system, and storing data while applications are running**

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Static memory(SRAM):

- Made up of **Flip-flops.**
- Stores the bit as **Voltage**.
- Each memory cell requires 6 transistors.
- In high speed processors SRAM termed as **Cache Memory**
- In high speed processors SRAM connected externally to improve the performance.
- **Low density and high power consumption**, costlier

Dynamic memory(DRAM):

- Made up of **MOS transistor gates**.
- Stores the bit as **Charge.**
- **High density and low power consumption**, cheaper.
- **Charge(bit information) leaks** → So stored information needs to be **refreshed** every few milli seconds → So **extra circuit needed** → So more cost
- Use DRAM used for **small systems**.
- To increase the speed of DRAM various techniques Extended Data out(EDO), Synchronous DRAM and Rambus DRAM.

Difference between SRAM and DRAM

Parameter	SRAM	DRAM
Full Form	Static Random Access Memory.	Dynamic Random Access Memory.
Storage bits in the form of	SRAM stores bits as voltage.	DRAM stores bits as charge.
Made up of	SRAM memory cell design made up of Flipflops.	DRAM memory cell design made up of MOS transistor gates.
Storage capacity	Lower capacity	Higher capacity
Need to Refresh	In SRAM, capacitors are not used which means refresh is not needed.	In DRAM, contents of a capacitor need to be refreshed periodically.
Refreshing unit	It doesn't require refreshing unit	Separate refreshing unit is required.
Reliability	More Reliable	Less Reliable as data is refreshed frequently.
Data Transfer rate	It has faster speed of data read/write.	It has slower speed of data read/write.
Power Consumption	SRAM consumes more power.	DRAM consumes less power.
Data Life	Longer data life.	Shorter data life.
Cost	SRAM are expensive.	DRAM are less expensive.
Packaging Density	low packing density device.	High packing density device.
Latency	Lower latency when compared with DRAM	More latency when compared with SRAM
Application	SRAMs are used as cache memory in computer and other computing devices.	DRAMs are used as main memory in computer systems

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Primary Memory: Read Only Memory (ROM)

ROM:

- **ROM is a non-volatile memory**.
- ROM contains data or program instructions that **cannot be modified by regular software**.
- It stores **firmware, BIOS (Basic Input/Output System), and other critical software needed to boot** a computer or embedded system.

Masked ROM(MROM):

- Bit pattern is permanently recorded by masking and **Metalization process**.
- **Expensive** and specialized process but **economical for bulk productions**.
- If any wrong metalization done at any point leads to wastage in chip use

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Programmable Read only memory(PROM):

- Bit pattern is permanently recorded by wires functionally viewed as **diodes or fuses**
- **Fuses are burned according to bit pattern** to be stored. The process is called "**burning the PROM**".

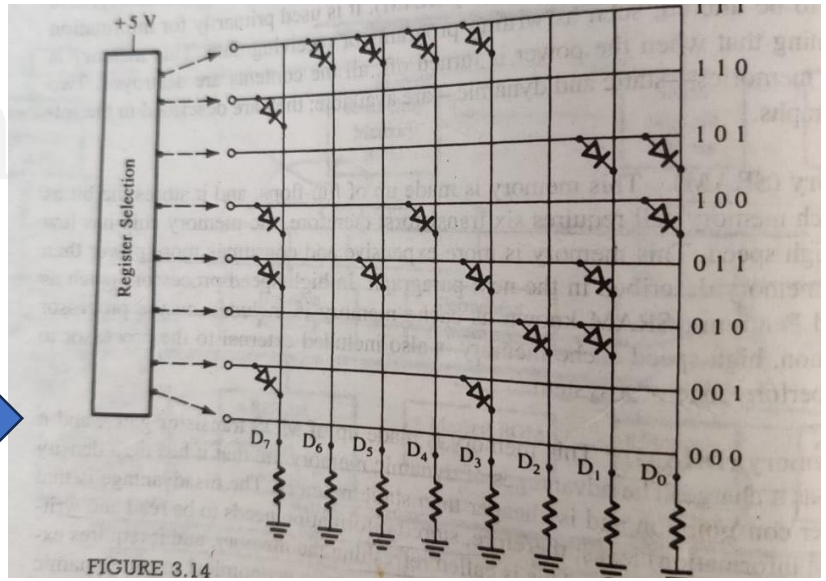

FIGURE 3.14

Primary Memory: Read Only Memory (ROM)

Erasable Programmable ROM(EPROM)

- Stores a bit by charging the floating gate of an FET.
- **Information is erased** by exposing the chip to **UV light and reprogrammed.**
- Disadvantages
  - It must be taken out of circuit to erase.
  - Entire chip must be erased.
  - **Erasing process takes 15 to 20minutes**.

Electrically Erasable Programmable ROM(EEPROM)

- Information is **erased** by using **electrical signals.**
- **Erasing at register level rather than erasing the entire information.**
  - Erasing process takes 10msec.

Flash Memory

- Information is **erased** by using **electrical signals.**
- **Erasing Block level**
  - Erasing process takes 10msec.

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Secondary Memory

Semi-Random Access

- **Data is accessed** in a somewhat ordered or partially predictable manner, but it is not strictly sequential or **entirely random**.
- In semi-random access, you may access data with a degree of regularity, possibly based on **some pattern, algorithm, or indexing mechanism**, but it doesn't strictly follow a specific sequence or order.
- An example of semi-random access could be **accessing data in a database using an index or key**, where the order of retrieval is determined by the keys but not strictly sequential. **Floppy disks, Hard Disk, CDROM disk, zip Disk.**

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Serial Access

- **Data is accessed in a specific order**, one item at a time, from the beginning to the end of a dataset or storage medium.
- In serial access, you must **process data items sequentially**, and **if you need to reach a specific item, you must go through all preceding items to get there**.
- An example of serial access is **Magnetic Tape**, where the tape must be physically moved to access data sequentially.
- **Charge-Coupled Device (CCD)** is an electronic device used for the **capture, storage, and transfer of electrical charge (photons or electrons) in the form of an electrical signal**. CCDs are widely used in **image sensors, digital cameras, camcorders, and various scientific instruments for capturing visual information**.

Chip Selection Signal generation

Also known as the Chip Enable (CE) signal, Slave Select (SS) signal

Purpose of Chip Select Signal $\overline{CS}$:

- The $\overline{CS}$ signal is used to **select a specific peripheral device or memory component among multiple devices** on a shared bus.
- When the $\overline{CS}$ signal for a particular device is active (low or high, depending on the logic level conventions), that device is allowed to communicate with the bus and respond to commands or data transfers

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Generation Methods:

- **Hardware Logic:** Using **digital logic gates (AND, OR, etc.)** to generate CS signals based on address decoding or other control signals.
- **Microcontroller/Microprocessor Control: Software running** on a microcontroller or microprocessor can directly control the $\overline{CS}$ signal based on specific conditions.
- **Programmable Logic:** In some cases, programmable logic devices like **FPGAs** can be used to generate CS signals.

Chip Selection Signal generation

Generation Methods:

- **Hardware Logic:** Using **digital logic gates (AND, OR, etc.)** to generate CS signals based on address decoding or other control signals.

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IO/M'	S1	S0	Data Bus Status
0	1	1	Opcode fetch
0	1	0	Memory read
0	0	1	Memory write
1	1	0	I/O read
1	0	1	I/O write
1	1	1	Interrupt acknowledge
0	0	0	Halt

$IO/\bar{M}$	$\overline{RD}$	$\overline{WR}$	$\overline{MEMR}$	$\overline{MEMWR}$	$\overline{IOR}$	$\overline{IOWR}$
0	0	0	0	0	1	1
0	0	1	0	1	1	1
0	1	0	1	0	1	1
1	0	0	1	1	0	0
1	0	1	1	1	0	1
1	1	0	1	1	1	0
1	1	1	1	1	1	1

When is IO/M high, both memory control signals are deactivated irrespective of the status of RD and WR signals.

Chip Selection Signal generation

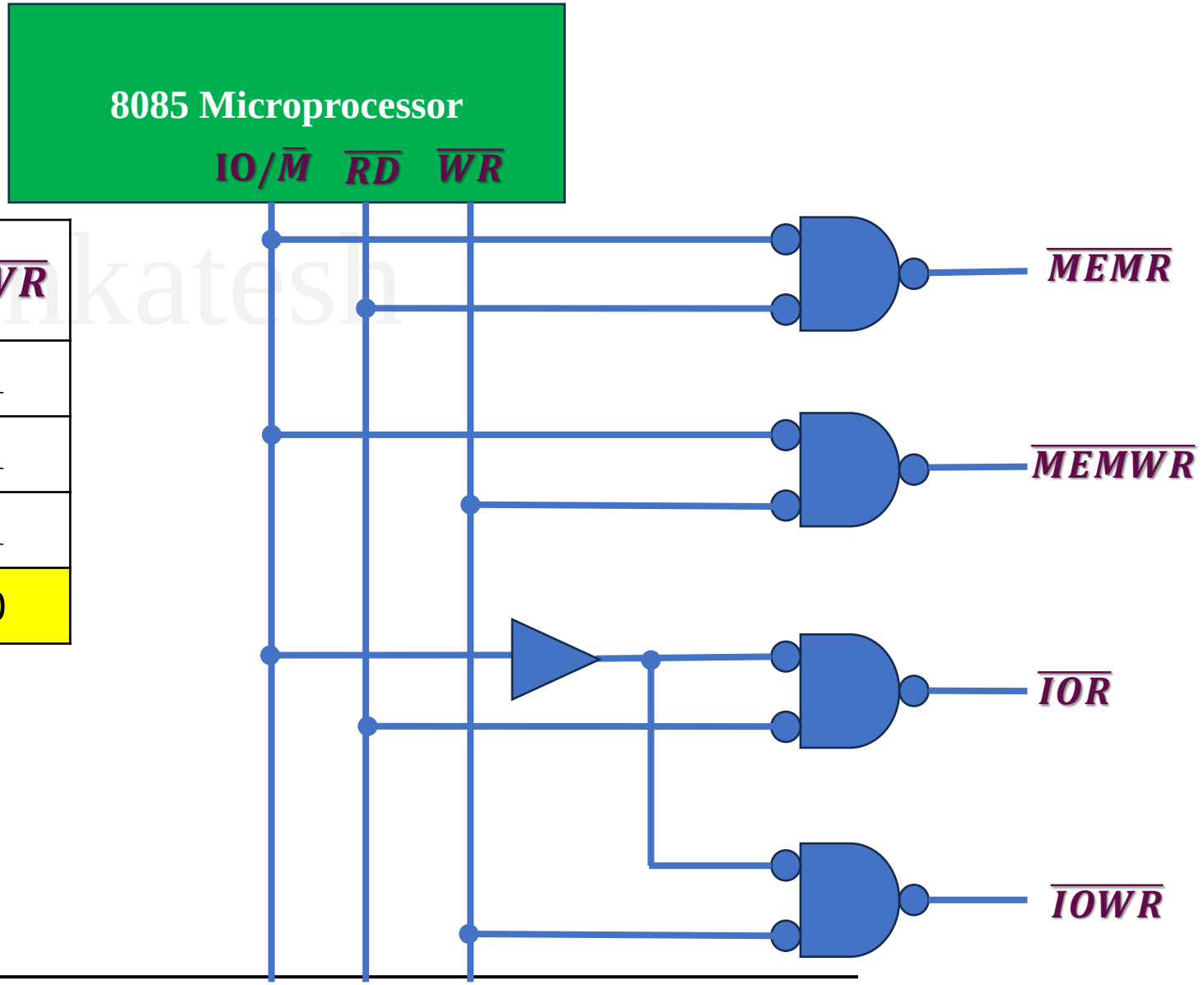
$IO/\bar{M}$	$\overline{RD}$	$\overline{WR}$	$\overline{MEMR}$	$\overline{MEMWR}$	$\overline{IOR}$	$\overline{IOWR}$
0	0	1	0	1	1	1
0	1	0	1	0	1	1
1	0	1	1	1	0	1
1	1	0	1	1	1	0

$\overline{MEMR} = \bar{M}\,\overline{RD}$

$\overline{MEMWR} = \bar{M}\,\overline{WR}$

$\overline{IOR} = IO\,\overline{RD}$

$\overline{IOWR} = IO\,\overline{WR}$



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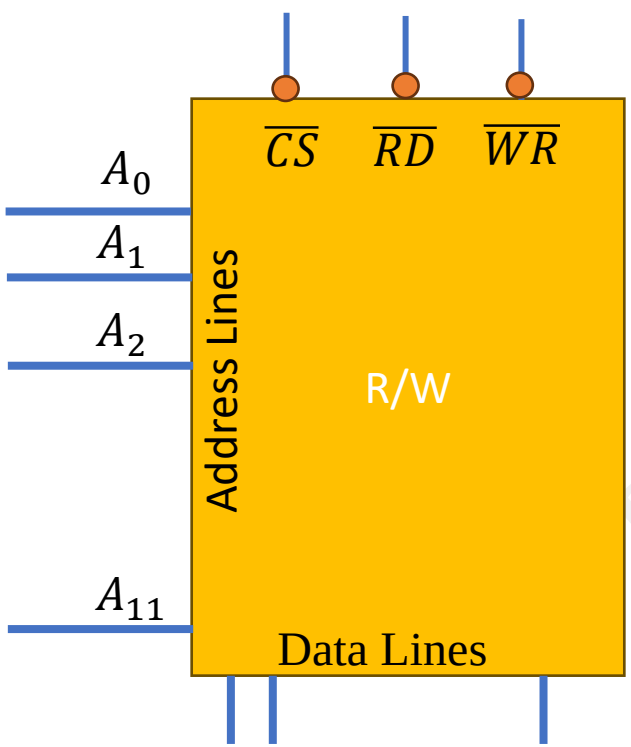
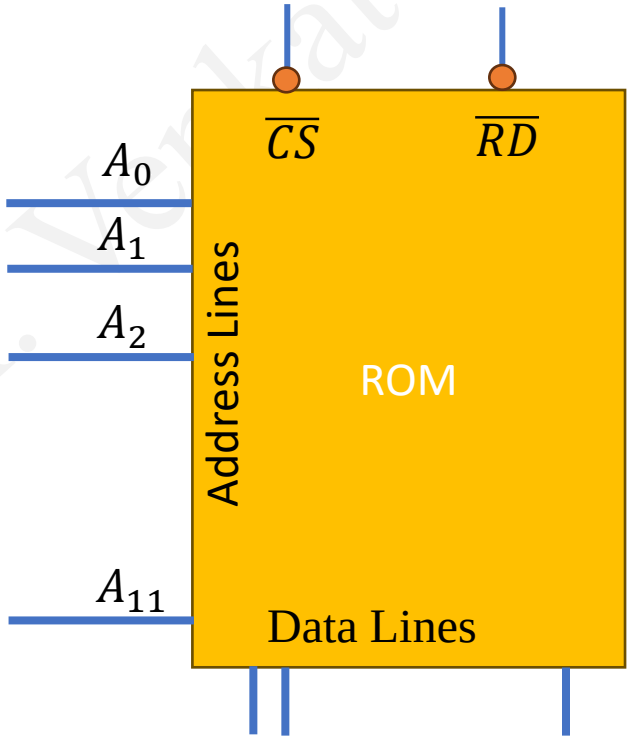
Memory Interfacing with Microprocessor

To communicate with Memory→ Microprocessors should be

- **Able to select the chip**
- **Identify the Register**
- **Enable the appropriate buffer**





Memory chip requires Address lines to identify a memory register

- 8085 microprocessor has 16 address lines.
- No. of Registers in 8085 = 2^n where n = no. of address lines.
- 12 address lines(A_0- A_{11}) are used.

Memory chip requires a chip select $\overline{CS}$ signal to Enable Chip

- The remaining address lines are used to select chip select signal.

Control Signal $\overline{RD}$ Enables Output Buffer

- The data from selected register are made available on output lines.

Control Signal $\overline{WR}$ Enables Input Buffer

- The data on input lines are written into memory.

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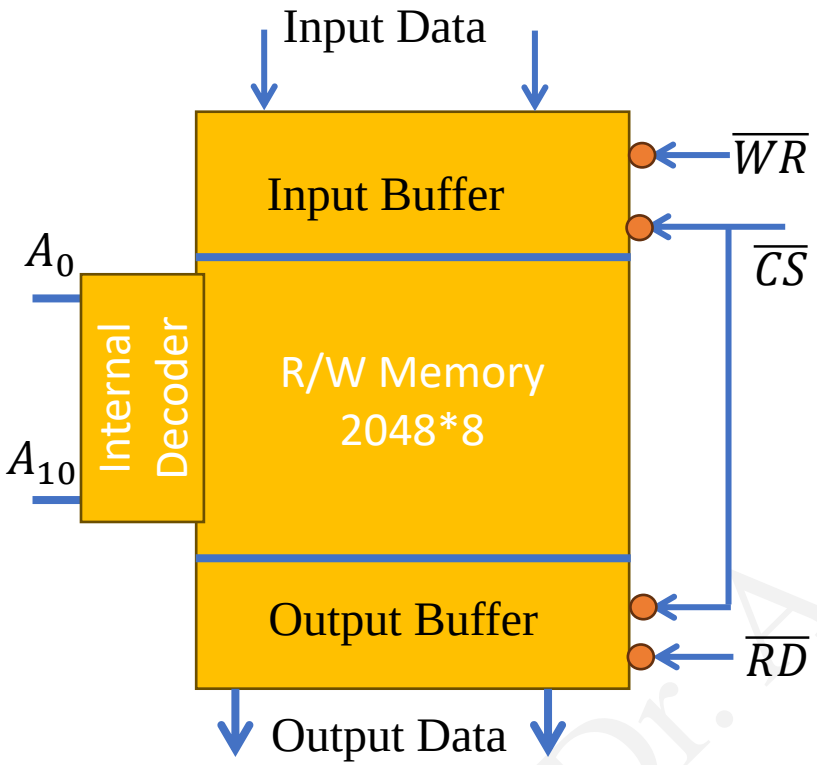
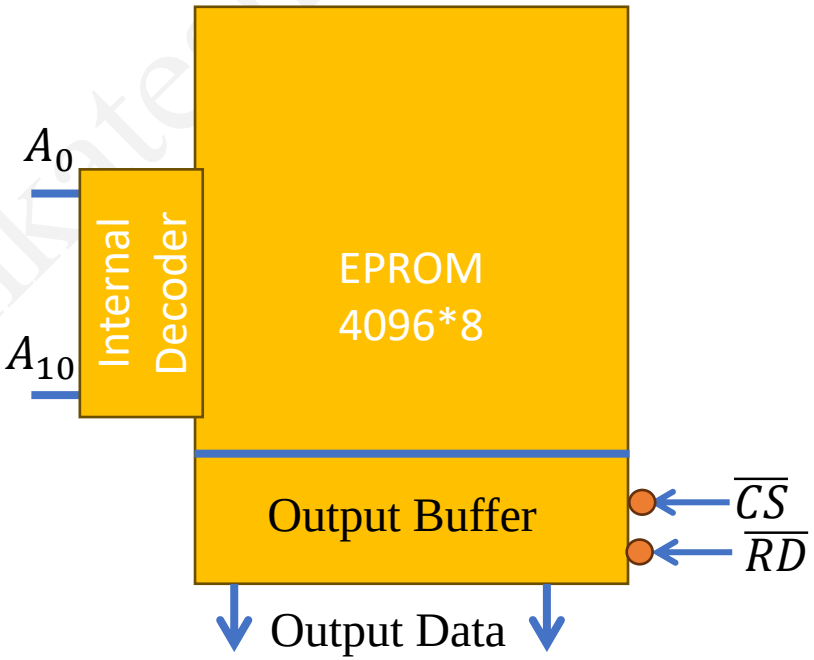
Memory Interfacing with Microprocessor





For Memory Interfacing in 8085, following important points are to be kept in mind.

1.Microprocessor **8085 can access 64Kbytes memory since address bus is 16-bit**. But it is not always necessary to use full 64Kbytes address space. The total memory size depends upon the application.

2.Generally **EPROM (or EPROMs) is used as a program memory** and **RAM (or RAMs) as a data memory**. When both, EPROM and RAM are used, the total address space 64Kbytes is shared by them.

3.The capacity of program memory and data memory depends on the application.

1.It is not always necessary to select 1 EPROM and 1 RAM. **We can have multiple EPROMs and multiple RAMs** as per the requirement of application.

2.We can place EPROM/RAM anywhere in full 64 Kbytes address space. **But program memory (EPROM) should be located from address 0000H since reset address of 8085 microprocessor is 0000H**.

3.It is not always necessary to locate EPROM and RAM in consecutive memory For example : If the mapping of EPROM is from 0000H to OFFFH, it is not must to locate RAM from 1000H. We can locate it anywhere between 1000H and FFFFH. Where to locate memory component totally depends on the application

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Example for Memory Interfacing

If a particular memory chip is capable of storing M words with each word having N-bits. Then the size of the memory will be M× N.

Consider a system in which the full memory space 64kb is utilized for EPROM memory. Interface the EPROM with 8085 processor. The memory capacity is 64 Kbytes. i.e 2^n = 64 x 1024 = 65536 bytes where n = address lines. So, n = 16.

In this system **16 address lines** of Microprocessor will be connected to the **address lines of the memory**.

and **D0 to D7** of the 8085 microprocessor will be connected to the **data bus of the memory**.

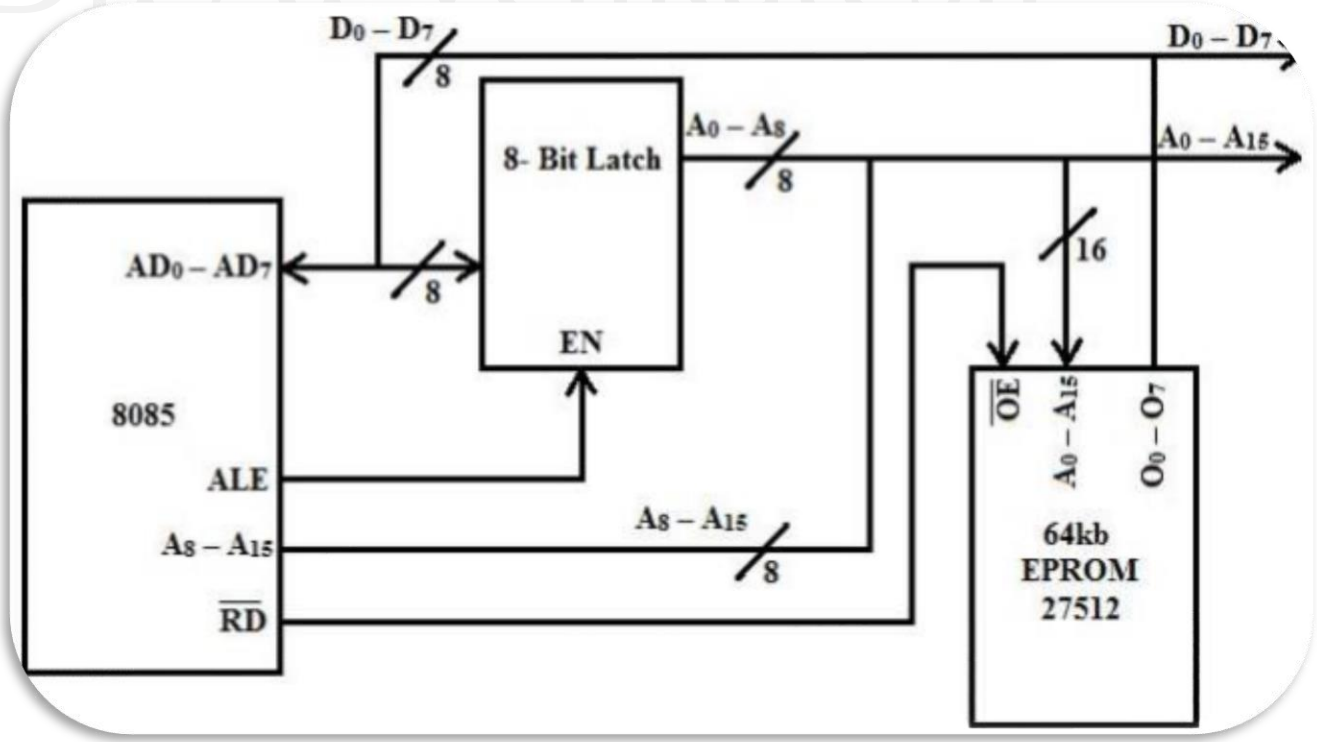
In order **to address the internal locations of memory**. **The chip select (CS) pin** of EPROM is permanently tied to logic low (i.e., tied to ground).

Since it is **ROM only read pin is presented, no write pin**.

Since the processor is connected to EPROM, the active low RD pin is connected to active low output enable pin of EPROM. The range of address for EPROM is 0000H to FFFFH.

Image reference

http://microprocessorforyou.blogspot.com/2011/12/memory-interfacing-in-8085.html



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I/O and peripheral device interfacing

In a microprocessor system, there are two methods of interfacing input/output (I/O) devices:

- ❖ Memory-mapped I/O(16 bit address)
- ❖ I/O mapped I/O(8 bit address)

In memory-mapped I/O, **input/output devices are mapped to the memory address** space of the microprocessor. This means that the I/O devices are treated like memory locations and can be accessed using the same read and write instructions as memory.

In I/O mapped I/O, **input/output devices are mapped to a separate I/O address** space that is different from the memory address space. The microprocessor uses special instructions to access the I/O devices using specific I/O address signals, which are separate from the memory address signals.

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Memory Mapped I/O

- In this Microprocessor **uses 16 address lines to identify the I/O device.**
- **I/O devices connected to memory register.**
- Microprocessor uses **same control signal(Memory read or Memory write) for I/O devices.**

Memory Address	Machine Code	Mnemonics	Comments
2050	32	STA 8000H	Store contents of accumulator in memory location 8000H
2051	00		
2052	80		

In above example, **If an output device is connected instead of memory Register** at this address(2050H) accumulator contents will be transferred to output device. This is called **Memory-Mapped I/O technique**.

Memory Address	Machine Code	Mnemonics	Comments
2050	3A	LDA 8000H	Load contents from memory location 8000H to accumulator

In above example, **If an input device is connected instead of memory Register** at this address(2050H) , the input device contents will be transferred to accumulator. This is called **I/O mapped-Memory technique**.

I/O Mapped I/O

- In this Microprocessor **uses 8 address lines to identify the I/O device.**
- I/O mapped I/O also known as Peripheral Mapped I/O
- **8 address lines** can have $2^8 = 256$ address combinations→ **So microprocessor can connect 256 I/O devices.**
- Microprocessor uses **I/O Read control signal for input devices and I/O Write control signal for output devices.**

IN instruction inputs data from input devices(such as key board) into accumulator
OUT instruction displays contents of accumulator at the output port(such as LED display).

OPCODE	OPERAND	Comments
OUT	8 bit port address	Transfers(copies) data from the accumulator to the output device.

Memory Address	Machine Code	Mnemonics	Comments
2050	D3	OUT 01H	Load contents from memory location 8000H to accumulator
2051	01		

In above example, **If an output device is LED display** then OUT instruction displays contents of accumulator at the port. This is called **I/O mapped-I/O technique**.

Difference between Memory-Mapped I/O Interfacing and I/O Mapped I/O Interfacing

Features	Memory Mapped IO	IO Mapped IO
Addressing	IO devices are accessed like any other memory location.	They cannot be accessed like any other memory location.
Address Size	They are assigned with **16-bit address** lines.	They are assigned with **8-bit address** values.
Instructions Used	The instruction used are **LDA and STA**, etc.	The instruction used are **IN and OUT**.
Cycles	Cycles involved during operation are Memory Read, Memory Write.	Cycles involved during operation are IO read and IO writes in the case of IO Mapped IO.
Registers Communication	**Any register** can communicate with the IO device.	**Only Accumulator** can communicate with IO device.
Space Involved	**2^{16} I/O ports** are possible to be used for interfacing.	Only **256 I/O ports** are available for interfacing.
IO/M`signal status	During writing or read cycles **(IO/M` = 0).**	During writing or read cycles **(IO/M` = 1).**
Control Signal	**No separate control signal** required.	**Special control signals** are used.
AL operations	Arithmetic and logical operations are **performed directly** on the data in the case of Memory Mapped I/O.	Arithmetic and logical operations **cannot be performed** directly on the data in the case of IO Mapped IO.
Hardware requirements	Only **one set of address and data buses are required** for memory and I/O devices	**Separate address and data buses are required** for memory and I/O devices
Instruction set	Uses the **same instructions** for accessing both memory and I/O devices	**Special instructions** are used for accessing I/O devices
Address range	**Limited number of memory locations** available for use by the microprocessor	**Dedicated address space** available for I/O devices
Design complexity	**Simple** to implement and design	**More complex** to implement and design
Examples of processors	Intel 8085, Motorola 6800	Intel 8255, Zilog Z80

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