ABHISHEK PARDHI
200026

End-Semester Examination 2021-22-II

Subject Name: Computer Organisation
Course Code: CS220

Total: 50 Marks
Duration: 1 Hour 30 Minutes

(This is not an open book examination)

1. (a) Let us have a cache memory of size 16 KB and a main memory of size 8 GB. The cache memory is 4-way set associate and every block is of size 8 words. Every word is 32 bits long. Calculate the number of bits for the TAG field. [5]
   (b) Let us assume a direct mapped cache policy. The physical address size is 5 bits. The cache memory can have 8 blocks where every block is of size 1 word. Show the status of the cache memory (in the form of Index, Valid Bit, Tag, Data) after the following memory references are made by the processor: 16,18,16,3,16,26,22,26,22.
   For such a cache, what is the total number of bits that can be stored? [4+1]

2. (a) Consider an instruction pipeline with five stages without any branch prediction: Fetch Instruction (FI), Decode Instruction (DI), Fetch Operand (FO), Execute Instruction (EI) and Write Operand (WO). The stage delays for FI, DI, FO, EI and WO are 5 ns, 7 ns, 10 ns, 8 ns and 6 ns, respectively. There are intermediate storage buffers after each stage and the delay of each buffer is 1 ns. A program consisting of 12 instructions I1, I2, I3, ..., I12 is executed in this pipelined processor. Instruction I4 is the only branch instruction and its branch target is I9. If the branch is taken during the execution of this program, what is the time (in ns) needed to complete the program? [Explain with Pipelining diagram] [6]
   (b) Let us assume a processor with the frequency of 4GHz and one level of SRAM cache where clock per instruction (CPI) is 1.0 if all accesses hit in L1 cache. The round trip DRAM access latency is 150 ns. The combined L1 miss rate per instruction is 3%. Now, calculate the speedup if an L2 cache is added with round trip access latency of 10 ns and 15% miss rate per L2 access. [4]

3. (a) What decimal number does the bit pattern 0X0C000000 represent if it is a two's complement integer and as an unsigned integer? What decimal number does the bit pattern 0X0C000000 represent if it is a floating point number? Use the IEEE 754 standard. [2+3]
   (b) Consider a processor that does not have a FPSQRT instruction and FPSQRT is emulated in software. The frequency of FP instruction is 20%. The average CPI of these instructions is 5.0. The average CPI for non-FP instructions is 1.53. The frequency of FPSQRT operation is 3%. CPI of FPSQRT operation is 25.0. One design alternative is to reduce the CPI of FPSQRT to 2. The other alternative is to reduce the CPI of all FP operations to 2.0. Which one is better? [5]

4. (a) For the MIPS assembly instructions below, what is the corresponding C statement? Assume that the variables f, g, h, i, and j are assigned to registers $s0, $s1, $s2, $s3, and $s4, respectively. Assume that the base address of the arrays A and B are in registers $s6 and $s7, respectively. [5]

```
sll $t0, $s0, 2
add $t0, $s6, $t0
sll $t1, $s1, 2
add $t1, $s7, $t1
lw $s0, 0($t0)
addi $t2, $t0, 4
```

```
lw $t0, 0($t2)
add $t0, $t0, $s0
sw $t0, 0($t1)
```

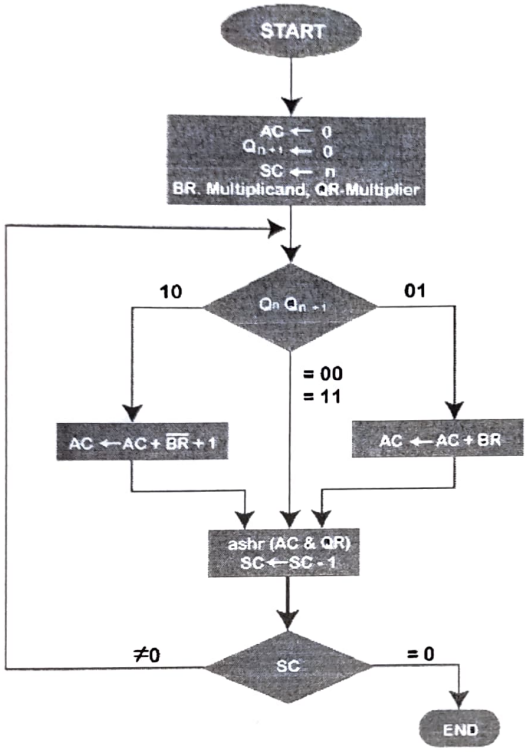
(b) Consider the following code snippet:

```
main
{
    int x = prompt("Enter a value for x: ");
    int y = 5 * x * x + 2 * x + 3;
    print("The result is: " + y);
}
```

The corresponding assembly instructions for the same are given below. Fill up the five blanks so that the code works correctly. [5]

```
.text
.globl main
main:
# Get input value, x
addi $v0, $zero, 4
la $a0, prompt
_______ [1]
addi $v0, $zero, 5
syscall
move $s0, _____ [2]

# Calculate the result of 5*x*x + 2* x + 3
mul $t0, $s0, $s0
___ $t0, $t0, 5 [3]
mul $t1, $s0, 2
add $t0, $t0, $t1
addi $s1, $t0, ___ [4]

# Print output
addi $v0, $zero, 4
la $a0, result
syscall
addi $v0, $zero, 1
move $a0, $s1
syscall

#Exit program
addi $v0, $zero, ___ [5]
syscall

.data
prompt: .asciiz "Enter a value for x: "
result: .asciiz "The result is: "
```

5. Below given the Booth's algorithm for multiplication.



(a) Multiply -4 with 7 with the given algorithm. [4]

(b) Draw a hardware architecture for the given algorithm clearly identifying the data path and the control unit. Mention the size of the registers and the signals used in the diagram. [3+3]