Assignment 4: CS220

3-bit Gray code counter and 8-bit Adder/Subtracter Using FSM

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Contents

1 3-bit Gray code counter

1.1 State Diagram

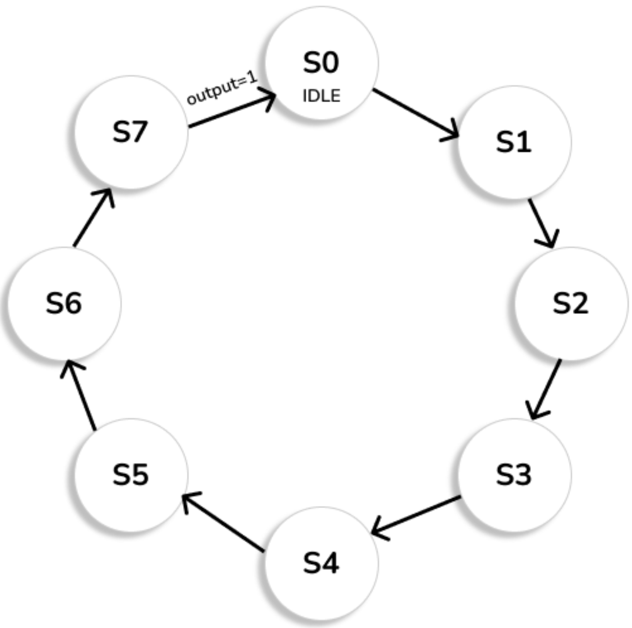


Figure 1: State diagram of sequence detector

1.2 State Assignment Table

State Assignment	
S_0	000
S_1	001
S_2	011
S_3	010
S_4	110
S_5	111
S_6	101
S_7	100

Table 1: State Assignment table

1.3 State Table

PS	NS
000	001
001	011
011	010
010	110
110	111
111	101
101	100
100	000

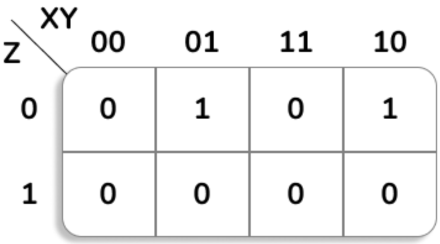
Table 2: State table

1.4 Excitation Table

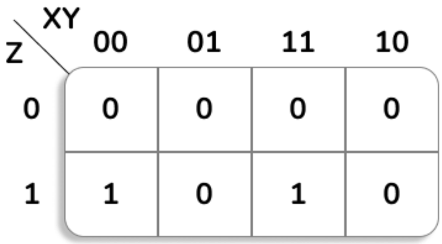
P.S. X	P.S. Y	P.S. Z	N.S. X'	N.S. Y'	N.S. Z'	FF's T_x	FF's T_Y	FF's T_Z	O/P
0	0	0	0	0	1	0	0	1	0
0	0	1	0	1	1	0	1	0	0
0	1	1	0	1	0	0	0	1	0
0	1	0	1	1	0	1	0	0	0
1	1	0	1	1	1	0	0	1	0
1	1	1	1	0	1	0	1	0	0
1	0	1	1	0	0	0	0	1	0
1	0	0	0	0	0	1	0	0	1

Table 3: Excitation table

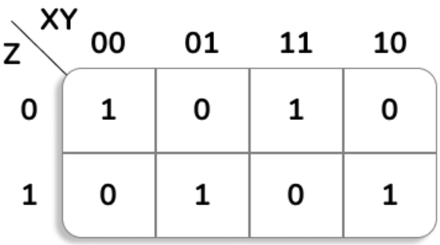
1.5 K-map



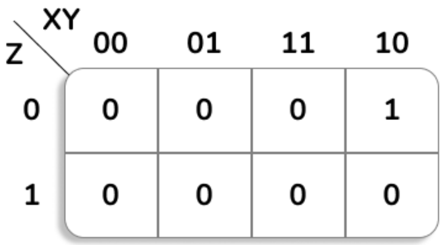
(a) T_x



(b) T_y



(c) T_z



(d) O

Figure 2: *K-maps*

$\Rightarrow T_x = \overline{Z}(X \oplus Y)$
$\Rightarrow T_y = Z(\overline{X \oplus Y})$
$\Rightarrow T_z = \overline{Z \oplus (X \oplus Y)}$
$\Rightarrow O = X\overline{Y}\,\overline{Z} \cdot T_x\overline{T_y T_z}$

1.6 Circuit Diagram

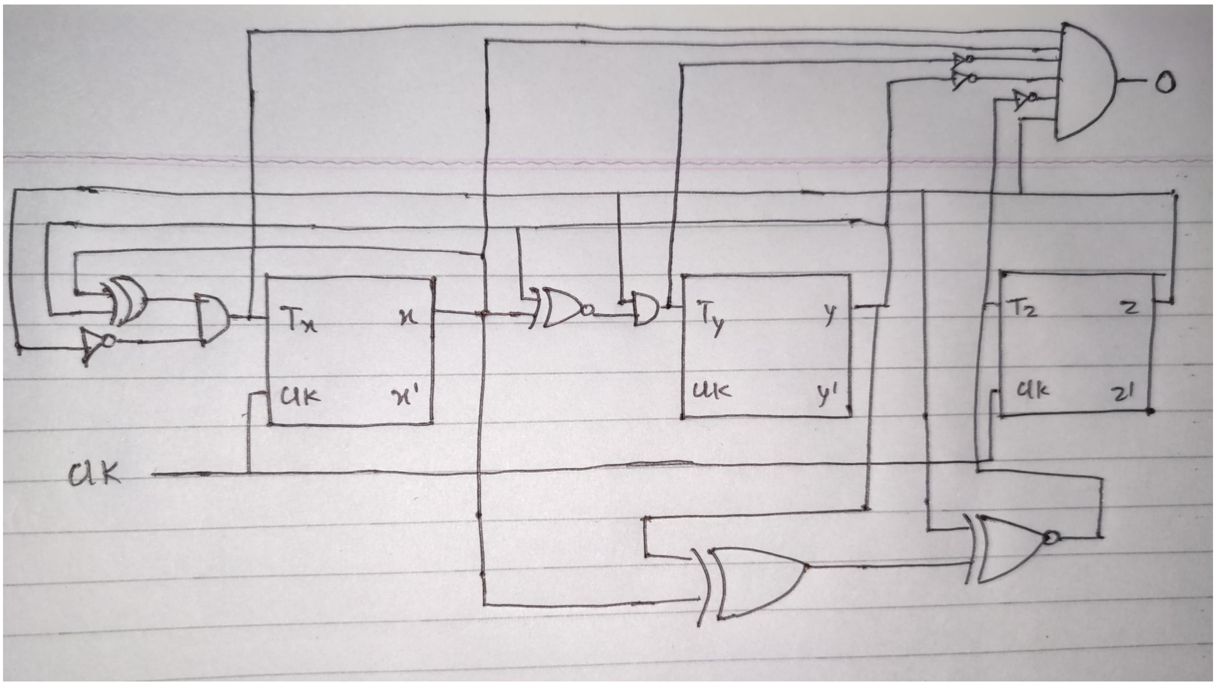


Figure 3: Circuit diagram of 3-bit Gray code counter

2 8-bit Adder/Subtracter

2.1 Description

The 8-bit adder/subtracter was made using eight 1-bit adder/subtracter. Each 1-bit adder/subtracter takes three 1-bit inputs **a**, **b**, **cin**, **opcode** and gives two 1-bit outputs sum and carry. We first made a full adder and then gave it **a** and $\mathbf{b} \oplus \mathbf{opcode}$ as input . Here, $\mathbf{b} \oplus \mathbf{opcode}$ gives us the 1's complement of **b** whenever **opcode** is **1'b1** (since XOR gate can invert or not invert a Boolean bit depending on input at other terminal). Also, we gave **opcode** as **cin** to the lower most significant bit's adder to convert the 1's complement of **b** to 2's complement of **b** (since 2's complement is obtained by flipping all bits of the binary number and adding 1).
The 8-bit adder/subtracter takes two 8-bit inputs **A** & **B** and one 1-bit input **opcode** and it gives one 8-bit output **Sum** if there's no overflow. The overflow is known from the value of $\mathbf{cout}[\mathbf{7}] \oplus \mathbf{cout}[\mathbf{6}]$ (since overflow occurs whenever the carry out of last bit is not equal to carry out of second last bit).

2.2 Circuit Diagram

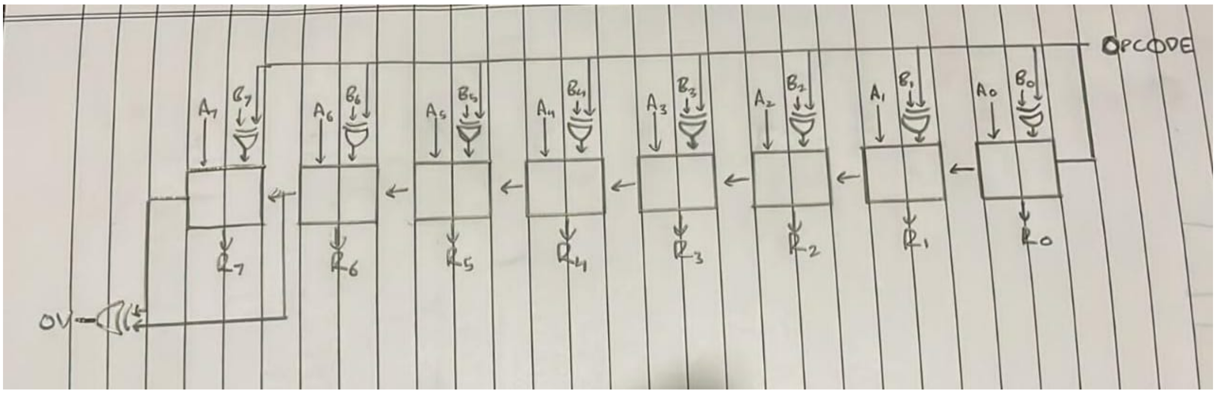


Figure 4: Circuit diagram of 8-bit Adder/Subtracter