project_3 - [/home/abhishek-revoor/Desktop/Thesis/rwu-rv64i-master/Vivado/project_3/project_3.xpr] - Vivado 2024.2

File Edit Flow Tools Reports Window Layout View Help Quick Access

write_bitstream Complete

Default Layout

Flow Navigator

PROJECT MANAGER
- Settings
- Add Sources
- Language Templates
- IP Catalog

IP INTEGRATOR
- Create Block Design
- Open Block Design
- Generate Block Design

SIMULATION
- Run Simulation

RTL ANALYSIS
- Run Linter
- Open Elaborated Design

SYNTHESIS
- Run Synthesis
- Open Synthesized Design

IMPLEMENTATION
- Run Implementation
- Open Implemented Design

PROGRAM AND DEBUG
- Generate Bitstream
- Open Hardware Manager

PROJECT MANAGER - project_3

Sources

- Design Sources (6)
  - as_top_mem (asTopMem.sv) (9)
  - ir_reg (ir_reg.sv) (8)
  - as_rv64i (asRV64I.sv) (2)
  - as_delay_reg (asDelReg.sv)
  - as_slave_bpi_mem (asSBpiMem.sv)
  - Memory File (1)
    - riscvtest.mem
- Constraints (1)
  - constrs_1 (1)
    - Zybo-Master.xdc (target)
- Simulation Sources (6)
- Utility Sources (1)

Hierarchy | Libraries | Compile Order

Properties

Select an object to see properties

Project Summary

Overview | Dashboard

Project name:	project_3
Project location:	/home/abhishek-revoor/Desktop/Thesis/rwu-rv64i-master/Vivado/project_3
Product family:	Zynq-7000
Project part:	Zybo Z7-10 (xc7z010clg400-1)
Top module name:	as_top_mem
Target language:	Verilog
Simulator language:	Mixed
Target Simulator:	Vivado Simulator

Board Part

Display name:	Zybo Z7-10
Board part name:	digilentinc.com:zybo-z7-10:part0:1.1
Board revision:	B.2
Connectors:	No connections
Repository path:	/home/abhishek-revoor/.Xilinx/Vivado/2024.2/xhub/board_store/xilinx_board_store
URL:	https://digilent.com/reference/programmable-logic/zybo-z7/start
Board overview:	Zybo Z7-10

Synthesis

Status:	✓ Complete
Messages:	36 warnings
Part:	xc7z010clg400-1
Strategy:	Vivado Synthesis Defaults
Report Strategy:	Vivado Synthesis Default Reports
Incremental synthesis:	Automatically selected checkpoint

Implementation Summary | Route Status

Status:	✓ Complete
Messages:	1 warning
Part:	xc7z010clg400-1
Strategy:	Vivado Implementation Defaults
Report Strategy:	Vivado Implementation Default Reports
Incremental implementation:	None

DRC Violations

Summary: 3 warnings

Implemented DRC Report

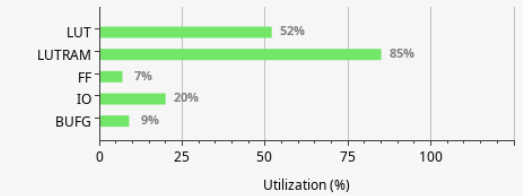
Timing Setup | Hold | Pulse Width

Worst Negative Slack (WNS):	2.879 ns
Total Negative Slack (TNS):	0 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	52016

Implemented Timing Report

Utilization Post-Synthesis | Post-Implementation

Graph | Table



Power Summary | On-Chip

Total On-Chip Power:	**0.096 W**
Junction Temperature:	**26.1 °C**
Thermal Margin:	58.9 °C (5.0 W)
Effective θJA:	11.5 °C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Medium

Implemented Power Report

Tcl Console | Messages | Log | Reports | Design Runs