Seminar on Topics in Electronic Design Automation
Seminar on Topics in Integrated Systems

Workshop on Scientific Writing
08.11.2021

Conrad Foik

Agenda

Introduction

Structure and Content

Style

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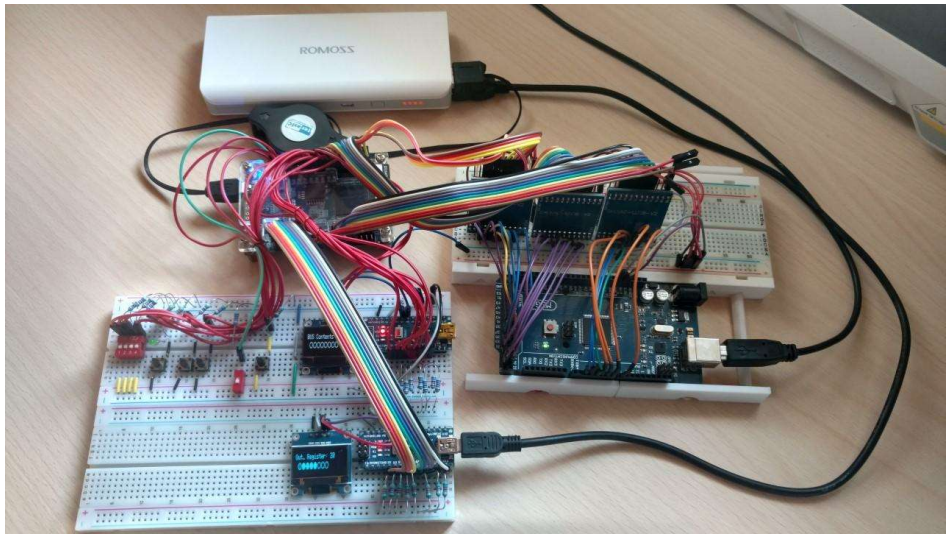
Technology and Communication

Main task of an engineer: Developing solutions for technical problems / tasks

```
case 0x0:
    // Check exception delegation
    if (((RISCV *)cpu)->CSR[CSR_MEDELEG] & (1 << (causeCode & 0x1f)))
    {
        // Pop MPIE to MIE
        etiss::log(etiss::VERBOSE, "Exception is delegated to supervisor mode");
        (((RISCV *)cpu)->CSR[CSR_MSTATUS]) ^=
            (((((RISCV *)cpu)->CSR[CSR_MSTATUS]) & MSTATUS_MPIE) >> 4) ^ ((((RISCV *)cpu)->CSR[CSR_MS
        ((RISCV *)cpu)->CSR[CSR_SCAUSE] = causeCode;
        // Redo the instruction encoutered exception after handling
        ((RISCV *)cpu)->CSR[CSR_SEPC] = static_cast<etiss_uint32>(cpu->instructionPointer - 4);
        ((RISCV *)cpu)->CSR[CSR_SSTATUS] ^= (((RISCV *)cpu)->CSR[3088] << 8) ^ (((RISCV *)cpu)->CSR[C
        ((RISCV *)cpu)->CSR[3088] = PRV_S;
        cpu->instructionPointer = ((RISCV *)cpu)->CSR[CSR_STVEC] & ~0x3;
    }
    else
    {
        ((RISCV *)cpu)->CSR[CSR_MCAUSE] = causeCode;
        // Redo the instruction encoutered exception after handling
        ((RISCV *)cpu)->CSR[CSR_MEPC] = static_cast<etiss_uint32>(cpu->instructionPointer - 4);
        (((RISCV *)cpu)->CSR[CSR_MSTATUS]) ^=
            (((RISCV *)cpu)->CSR[3088] << 11) ^ ((((RISCV *)cpu)->CSR[CSR_MSTATUS]) & MSTATUS_MPP);
        ((RISCV *)cpu)->CSR[3088] = PRV_M;
        // Customized handler address other than specified in RISC-V ISA manual
        if (addr)
        {
            cpu->instructionPointer = addr;
            break;
        }
        cpu->instructionPointer = ((RISCV *)cpu)->CSR[CSR_MTVEC] & ~0x3;
```



Communication is a crucial aspect of today‘s technical projects!

Source right picture: https://eecs.blog/8-bit-computer_in_an-fpga

Technical Documents

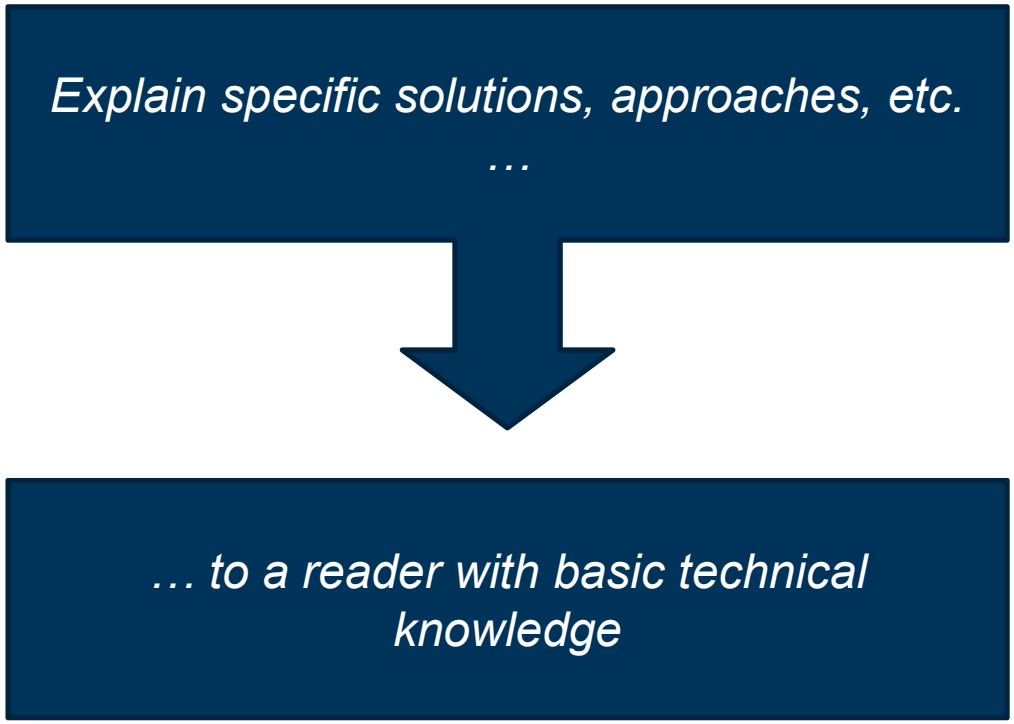
Writing technical documents is part of an engineer‘s job description

What? Why?

- Documentations
- Specifications
- Analytic reports, reviews

For whom?

- Colleagues
- Supervisor
- Customers
- Suppliers, project partners
- Peers



Scientific Publications

In seminar: Write a 4-page paper

What is the purpose of a scientific publication:

- Publish new scientific findings (knowledge)
  - Focus on single aspect: New concept, method, etc.
  - Survey: New point-of-view, comparisons, relations, etc.
- Publicity for the work and the authors
- Secures rights for the work

Focus on Key Message

The new (scientific) finding is the key message of the publication.

The ENTIRE publication serves this ONE key message

Structure & Content:

- Common thread
- Clear relevance / relation of every section towards the key message
- Not a cluster of losely related topics under a common title

Style:

- Clear and understandable presentation of the key message
- As simple as possible, as complex as necessary
- Precise and factual, but „readable“

Agenda

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Structure of a Scientific Paper

1. Title
2. Authors
3. Abstract
4. Keywords
5. Introduction
6. State of the art / related work
7. Main part: Scientific contribution
8. Experiments & results
9. Conclusion
10. References

Aging model for timing analysis at register-transfer-level

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ABSTRACT

Designing at higher levels of abstraction plays a key role in managing the complexity of today's and future VLSI circuits. Furthermore, performance degradation due to aging effects can no longer be neglected, especially in high performance technologies. Hence, timing models at higher abstraction levels are needed that take aging into account. For that purpose, we present an aging-aware timing model at register-transfer-level.
The delay of a circuit is defined by the critical timing path. For an aged circuit, multiple timing paths may exist that can be the critical one depending on the conditions the circuit operates at. The proposed timing model is a reduced timing graph that just contains those possible critical paths. It has a speed-up of up to 56× compared to an aging-aware timing analysis at gate level, without any loss of accuracy.

Keywords

Aging analysis, RTL, timing analysis, timing model, NBTI

1. INTRODUCTION

To keep pace with the unabatedly growing complexity of integrated circuits, circuit design begins at higher and higher levels of abstraction. New challenges evolve from ongoing miniaturization, on the one hand by process variation and on the other hand by performance degradation due to aging. Therefore, new models at higher abstraction levels are required that accurately describe the impact of process variation and aging. This paper proposes a new timing model at register-transfer-level (RTL) which considers the aging of integrated circuits. To the best of our knowledge it is the first aging-aware timing model above gate level.

Macro-cells, such as adders or multipliers, are used to represent a circuit at register-transfer-level. These logical/arithmetic blocks have a higher complexity than standard cells. A single value – the delay τ – is enough to specify the timing of a macro-cell if aging effects are not considered (e.g., adder with $\tau = 80ns$). By considering performance degradation due to aging, delay becomes dependent on the conditions

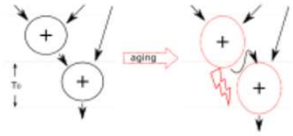


Figure 1: The dotted circles indicate the aged performances. The circuit fails because the second adder needs the result before the first adder has finished its calculation.

the macro-cell operates at over the lifetime – the so-called use profile UP.

If a model at higher abstraction levels is available, it is possible to:

- consider the impact of aging on a system early in the design process,
- determine the system performance quickly at the system level,
- perform an extensive exploration of the design space.

Timing models that take process variation into account have already been published [2,6]. In this work we propose an aging-aware timing model at RTL.

Such models can, for instance, be used in high-level synthesis (HLS). One important step in HLS is scheduling. During scheduling, arithmetic/logical operands are mapped on time slots of duration T_0 (see Fig. 1). Therefore, a pre-characterized library with different implementations of macro-cells is required. The individual implementations differ in their characteristics (delay, area, power). The schedule is generated by choosing optimal implementations from the pre-characterized library [1].

When a macro-cell ages, its delay increases. If this is not taken into account during synthesis, it is possible that the system fails before the end of its specified lifetime because the time of a macro-cell for performing a calculation is no longer sufficient. At the moment a macro-cell is characterized for the library, it is unknown how the cell will be utilized. Therefore, a timing model is needed which provides the delay τ of a macro-cell as a function of the use profile.

The remainder of this work is organized as follows: In Sec. 2, the requirements for such an aging-aware timing model are defined. In Sec. 3, the proposed approach is described. It is based on a strongly reduced timing graph that only contains those timing paths that might become the critical ones. The timing graph reduction process is based on

Task of Sections

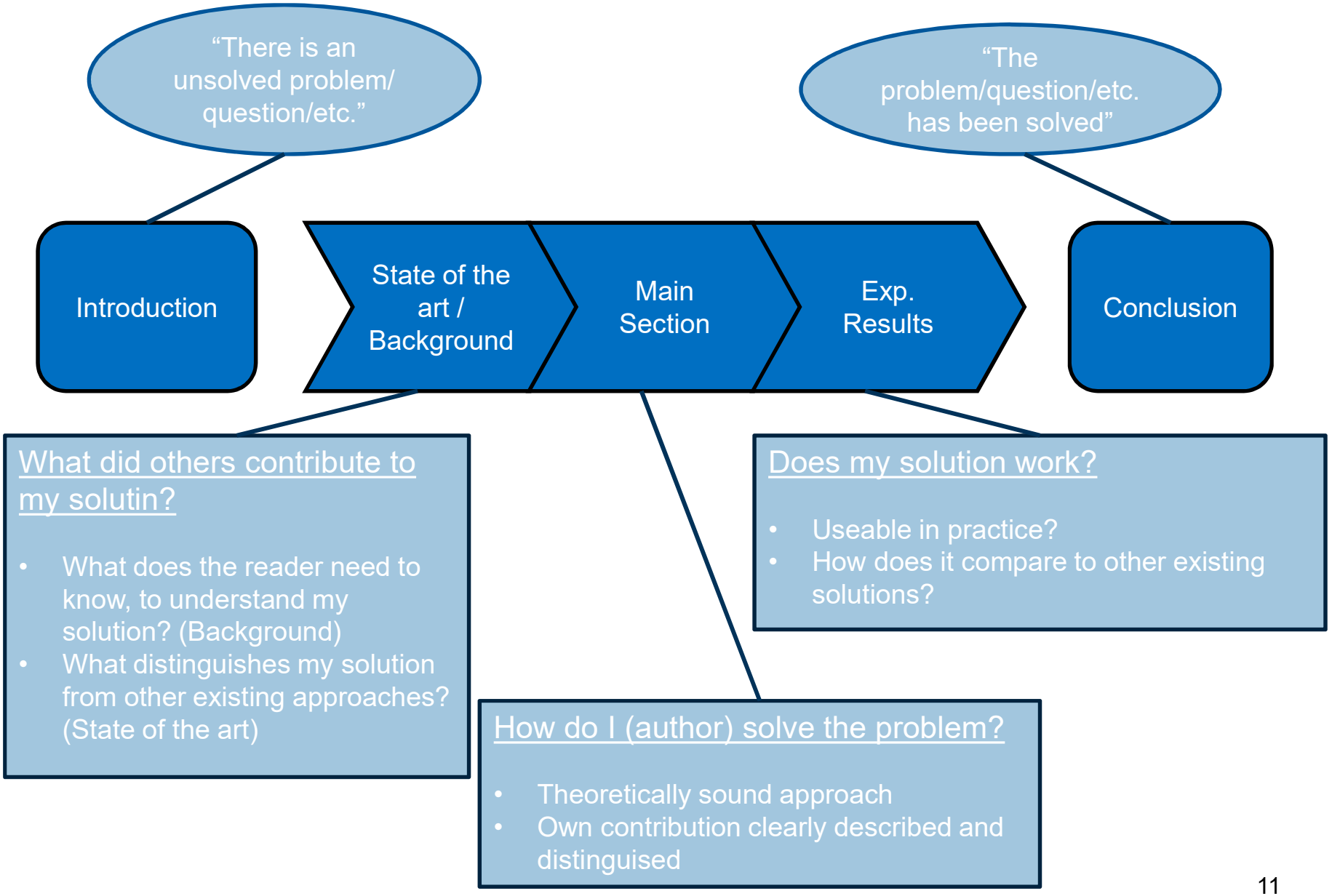
- Arise interest of the reader
  (Title, Abstract, Introduction, Conclusion)

- Clarify related context and state of the art
  (State of the art / Introduction)

- Full and precise (theoretical) description of the key topic
  (Main section, graphic illustrations)

- Evidence of practical significance
  (Experimental results)

Structure Supports the Key Message



Present the Structure

Author knows structure/context („top view“)
Reader unfamiliar with topic and structure („line by line“)

Well chosen, expressive titles (chapters/ sections)

- „Main Part“ vs. „Extending PSL for Co-Verification“ [1]

Cross references to earlier and later sections

- „As mention earlier, …“ vs. „As mentioned in Section I, …“
- „This will be further discussed in Section III“

Explicitly formulated overview

- Standard at end of introduction
- Possibly at beginning of chapter/section
  - Recommended for longer reports (e.g. master thesis)
  - Paper: Consider „space-benefit“ equation

1) Text example from: “Unified Property Specification for Hardware/Software Co-Verification”, Xie et al., IEEE

Present the Structure (Examples)

Section II introduces the relevant background. In section III, our novel approach is presented. Experimental results, using our approach, are discussed in section IV. Section V concludes this paper.

In this section, we first introduce […] PSL in the hardware domain. We then present a hardware semantics that PSL already supports [and afterwards] two representative software semantics that we will extend PSL to support […]

Second text example from: “Unified Property Specification for Hardware/Software Co-Verification”, Xie et al., IEEE

Purpose of Title and Abstract

- Typically only title and abstract are accessible free of charge
- Must arise the interest of the reader for the whole paper

What Is a good Title?

Examples:

Enable the inherent omni-directionality of an absolute coupled dark state magnetometer for e.g. scientific space applications

[Pollinger et al.; IEEE International Instrumentation and Measurement Technology Conference]

Exploring the use of a test automation framework

[Cervantes, A.; Aerospace conference, 2009 IEEE]

Security of TMN

[Johannessen, K.; IEEE Network Operations and Management Symposium]

Exercise:

- What are good/bad aspects of these titles?
- Proposal for improvements!

Requirements for the Title

- As short as possible, as long as necessary
- Clearly describes the content of the paper (Key message!)
- Abbreviations only in rare exceptional cases (*FPGA vs. DFT*)

Requirements for the Abstract

Following questions must be answered in the abstract:

- WHAT is the unique selling point of the paper?
- WHY is this research important? WHY should I read this paper?
- WHAT has been done?
- HOW has the improvement been achieved (e.g. new methods)?
- WHICH main results have been obtained?

Usually the number of words or characters is limited.
(Rule of thumb for the seminar: ~100 words)

1 – 2 Introdcuing sentences
2 – 3 Sencences about contribution
1 – 2 Sentences about results

Exercise: Abstract

Exercise:
Read the example abstracts.

Have all questions been answered?
Is all the needed information provided?
Is unnecessary information provided?

Abstract Example 1

Example :

> MOS analog circuit sizing is considered a highly complex task that requires experience and skills. Many methods proposed in the literature have arguable merits and limitations; none of them has become a widely recognized method being adopted in the design practice. This paper attempts to use a simply computable metric called the finite difference sensitivity computed mainly in the ac domain for the purpose of device sizing. Multiple design goals are formulated as a weighted optimization objective function and a gradient search is developed for optimizing the objective function. All constraints are subsumed in the objective function in the form of penalty functions. Experimental results show that such a simple formulation of circuit optimization is capable of finding satisfactory suboptimal sizing results which can be used for subsequent manual tuning or layout reference. The automated sizing procedure is compared to manual sizing and is demonstrated that the auto-sizing scheme has a better capability in balancing the multiple design objectives.
>
> *[B. Weng et al.; Design optimization of MOS operational amplifiers using finite difference sensitivity IEEE ISIC 2011]*

What is good / bad?

Points of criticism:
- Information content & level of detail (very extensive)
- Too generalized (impression of universality of the experiments)

Abstract Example 2

Example:

> Optimizing Gain of an RF Amplifier using Design of Experiments (DOE), is presented. The constraints of keeping minimum deviations in both frequency and Noise Figure (NF) is taken in to account by ANOVA and nominal-the-best approach of Taguchi Methods. Gain of the amplifier is improved by 2.4 dB with frequency and NF deviations of 0% each.
>
> *[J.N. Tripathi et al.; Optimizing Gain of 5 GHz RF amplifier keeping minimum deviation in center frequency and noise figure; IEEE ISIC 2011]*

What is good / bad?

Points of critisim:
- Why has this work been done?
- What is special about this paper?

Introduction

Leads to the actual topic:

1. „Pick up“ reader: From common knowledge to the specific topic
2. Motivate the reader: Why is the topic important?
3. Establish the problem/question: Leads to key message
4. Short overview of the solution/approach

Important:

- Provide enough background knowledge to reader to understand the following sections
- References to proof statements in the introduction (e.g. problems with other approaches, necessity of the own work)

Typical: Short outline of the paper‘s structure (context)

Conclusion

Summarizes the main results of the paper:

- Which improvements could be achieved?
- Which conclusions can be drawn?
- Take-away points

Important:

- Link to introduction and thus to the original problem statement

Main Content (1)

Every paper has a key message!

- The paper solves a relevant technical problem
- **Every section** of the paper supports this message
- Do not get off track or describe unnecessary details (**short, but complete**)
- Keep track of the common thread (clarify connections)

You write the paper for the reader (not for yourself)!

- The goal is to **explain the topic** to the reader
- Reader has common technical knowledge. Unfamiliar with the specific topic
- Every aspect relevant to the reader must be explained

Main Content (2)

You do not do any research (in the seminar)

- Your paper is a summary of other papers
- Your task:
  - No raw listing of summaries
  - Find another level of detail / your own description
  - Explain correlations (Is one paper based on another? Do they complement each other? Are they in contradiction?)

Agenda

Introduction

Structure and Content

Style

References

Style of Writing (1)

As simple as possible,… (Understandable for reader)

- Clear and simple formulations (No novel)
- Avoid unnecessary fillers
- Write active and not passive

... as complex as necessary (technical depth)

- Use relevant technical terminology
- Specific statements (often vs. about 1000 times)
- Use meaningful verbs

Style of Writing (2)

- Highlight universal validity
  - Avoid „I“ and „we“ (only used to emphasize something you uniquely did)
  - Use present tense (present perfect) instead of past tense

- Correct abbreviations (e.g. „Fig.“, „Tab.“ …)

- Do not try to build suspense

- Follow common rules for good style (e.g. varied choice of words)

Goal: Present the key message precisely and objectively, without boring or overburdening the reader.

Style of Writing (3)

It is shown by the experiment that the computation time is slightly improved by the used algorithm.

The experimental results show that the used algorithm decreases the computation time by 3%.

I investigated a number of test circuits using this method (see Fig. 6).

With this method a number of test circuits have been investigated (see Fig. 6).

The network list is passed through from the primary inputs to the primary outputs by the proposed algorithm in order to identify those gates which have to be removed.

The algorithm passes through the network list from the primary inputs to the primary outputs. Thereby gates to be removed are identified.

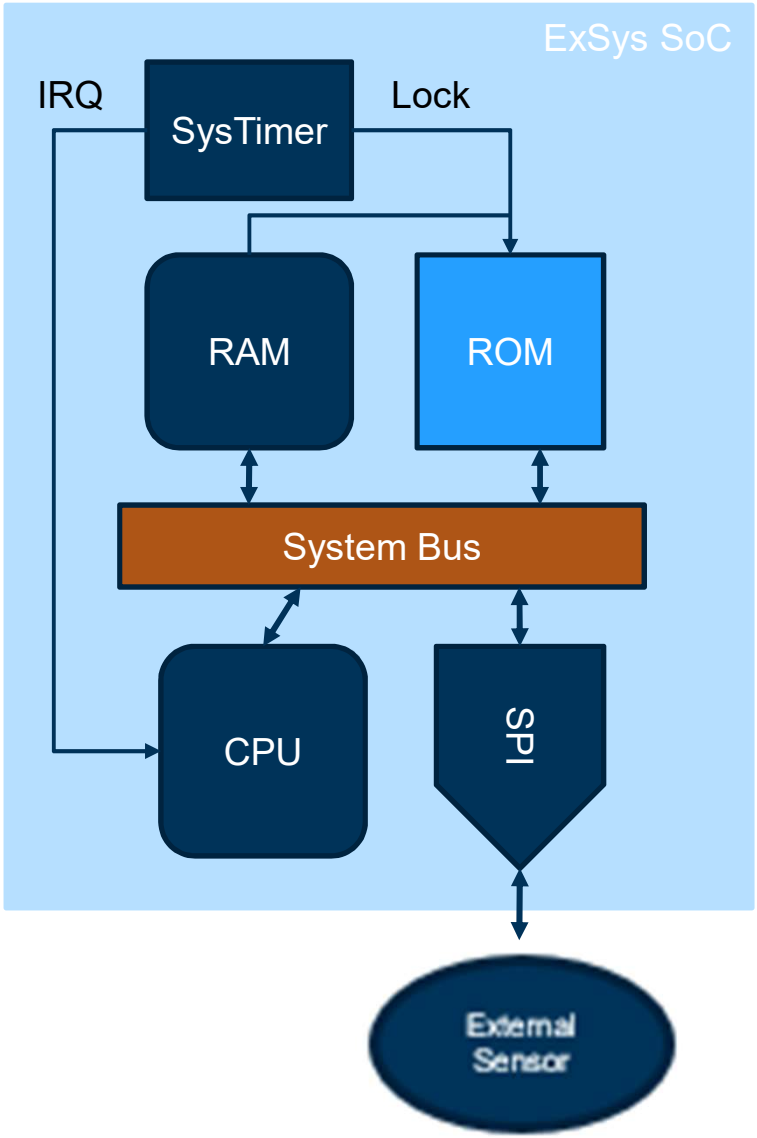
Structuring the Content

- Divide the text into meaningful parts
- First sentence summarizes paragraph, followed by details
- Sensible transitions between sentences, paragraphs, sections, etc.
- Rule-of-thumb:
  Reading (only) the first sentences of every paragraph should clearly outline the „story“ of the paper

Exercise - Figures

DISCLAIMER: Made-up example

Fig. 1: ExSys



The ExSys System-on-chip (SoC) contains a microprocessor core (CPU), data memory, program memory and a watch-dog timer. The components are connected through a system bus.
On a timeout, the watchdog timer sends an interrupt request (IRQ) to the CPU. In addition, the watch-dog timer locks the memory blocks.

Exercise: Improve the figure (and text).

Figures (1)

„A picture is worth more than 1000 words“ – but only if it is used right!

Goal:

- Assistance on interpretation of (e.g.) formulas
- Present relationships
- Present experimental setup
- Depict results

Tips:

- Make your own figures
- Use figures as starting point for writing
  - First, describe the figure
  - Then, expand text

Figures (2)

„A picture is worth more than a thousand words“ – but only if it is well done!

- Every figure must be referenced in the text
- Content of figure needs to match the text
  - Do not overload
  - Do not leave out important details
- Formally correct
  - Captions and labels must be present and correct (Label axes!)
  - Unambiguous use of symbols (e.g. arrows)
- Consider the quality
  - Size
  - Sharpness
  - Take care on usage of colors (usually printed gray-scaled)
- Consistent representations (if multiple figures are used)
  - Purposeful use of shapes
  - Color coding
- Reference sources (if necessary)

Same considerations apply for tables, (pseudo-) code, etc.

Agenda

Introduction

Structure and Content

Style

References

References

To build on the existing pool of knowledge is the only way to progress
➔ Use of external sources is desirable!

- Ideas, texts, statements, pictures, tables, etc. which are reused must be clearly referenced
- Source must be citable (published)

<u>You *have* to reference sources:</u>
- Academic honesty
- **Not marking a source = Plagiarism!**

<u>You *want* to reference sources:</u>
- Sources support/confirm statements
- A high number of references indicates a thorough investigation
- Sources should meet scientific standard

Copyright

"Copy-and-Paste" without marking the source **Plagiarism**

But: even if the source is marked, **copyright has to be considered**:

- Copyright covers every type of creation (i.e. text, graphics, music, etc.)
- You have to ask for the right to use materials owned by others in your own work
- Exceptions: Citations for the purpose of discussion in your own work (§51 UrhG; "fair use": 17 U.S.C. §107)

e.g.: Website: **Requesting Permission to Reuse IEEE Material**

http://www.ieee.org/publications_standards/publications/rights/reqperm.html

References

- **Journals**: Authors, title, journal, year
  - F. N. Najm, “A Survey of Power Estimation Techniques in VLSI Circuits,” IEEE Transactions on VLSI Systems, vol. 2, no. 4, pp. 446 – 455, Dec. 1994.

- **Book**: Authors or editors, title, publisher, year
  - P. Coussy and A. Morawiec, High-Level Synthesis from Algorithms to Digital Circuits. Springer, 2008

- **Conference contribution**: Authors, title, name of the conference, year
  - Y.-C. Ju, et al., “Incremental techniques for the identification of statically sensitizable critical paths,” in ACM/IEEE Design Automation Conference (DAC) , 1991

- **Website:** Name, URL, date

Example Text Citation (1)

Source: Mollick, E., "Establishing Moore's Law," *Annals of the History of Computing, IEEE* , vol.28, no.3, pp.62,75, July-Sept. 2006

> The seemingly unshakeable accuracy of Moore's law - which states that the speed of computers; as measured by the number of transistors that can be placed on a single chip, will double every year or two - has been credited with being the engine of the electronics revolution, and is regarded as the premier example of a self-fulfilling prophecy and technological trajectory in both the academic and popular press.

Example Text Citation (2)

Copy&Paste without source

Moore’s law has been driving the electronic industry for centuries. The seemingly unshakeable accuracy of Moore's law - which states that the speed of computers; as measured by the number of transistors that can be placed on a single chip, will double every year or two - has been credited with being the engine of the electronics revolution, and is regarded as the premier example of a self-fulfilling prophecy and technological trajectory in both the academic and popular press.
Due to Moore’s law complexity of integrated circuits is rising constantly. In this paper we will discuss an algorithm to (…)

Plagiarism, source not identifiable

Example Text Citation (3)

Copy&Paste with source

Moore’s law has been driving the electronic industry for centuries. The seemingly unshakeable accuracy of Moore's law - which states that the speed of computers; as measured by the number of transistors that can be placed on a single chip, will double every year or two - has been credited with being the engine of the electronics revolution, and is regarded as the premier example of a self-fulfilling prophecy and technological trajectory in both the academic and popular press [1].
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[1] Mollick, E., "Establishing Moore's Law," *Annals of the History of Computing, IEEE* , vol.28, no.3, pp.62,75, July-Sept. 2006

Plagiarism: Not identifiable that direct quote is used

Example Text Citation (4)

Copy&Paste with source and identification as direct quote

Moore's law has been driving the electronic industry for centuries. As is formulated in [1]: "*The seemingly unshakeable accuracy of Moore's law - which states that the speed of computers; as measured by the number of transistors that can be placed on a single chip, will double every year or two - has been credited with being the engine of the electronics revolution, and is regarded as the premier example of a self-fulfilling prophecy and technological trajectory in both the academic and popular press.*"
Due to Moore's law complexity of integrated circuits is rising constantly. In this paper we will discuss an algorithm to (…)

[1] Mollick, E., "Establishing Moore's Law," *Annals of the History of Computing, IEEE* , vol.28, no.3, pp.62,75, July-Sept. 2006

No plagiarism, but also no real own contribution

Citing Figures and Tables (1)

Example:

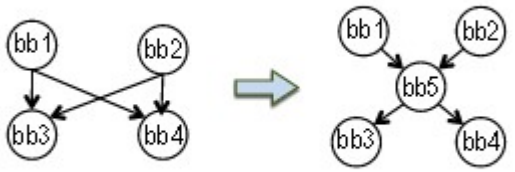


Fig. 7. Control node reconstruction for optimized branch.

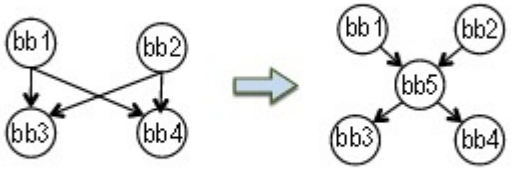
TABLE I
COMPARISON OF SIMULATION ACCURACY AND SPEED

	crc	edgeDetect	prime	lzw	select
#. divsion	2	3	3	5	3
#. instr. (ISS)	21533	34552254	2409307	1585488	1992
#. instr. (SLS)	22305	34966371	2410509	1592424	1996
error(%)	3.6	1.2	<0.1	0.4	0.2
exe.time (ISS)	3.4ms	4.85s	314ms	265ms	343us
exe.time (SLS)	3.3us	5.6ms	270us	345us	0.5us
speedup	1020	870	1162	770	685

Source: Kun Lu; Muller-Gritschneder, D.; Schlichtmann, U., "Hierarchical control flow matching for source-level simulation of embedded software," *System on Chip (SoC), 2012 International Symposium on* , vol., no., pp.1,5, 10-12 Oct. 2012

Citing Figures and Tables (2)

No source:



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Plagiarims and possible copyright infringement

Citing Figures and Tables (3)

With source:

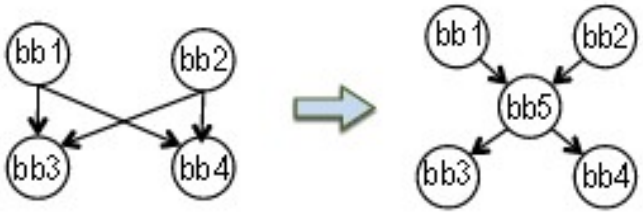

Fig. X: Control Node Reconstruction for optimized branch [1]

Table X: Simulation Results [1]

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speedup	1020	870	1162	770	685

- No plagiarism but possible copyright infringement
- In addition: No own contribution

[1] Kun Lu; Muller-Gritschneder, D.; Schlichtmann, U., "Hierarchical control flow matching for source-level simulation of embedded software," *System on Chip (SoC), 2012 International Symposium on* , vol., no., pp.1,5, 10-12 Oct. 2012

Citing Figures and Tables (4)

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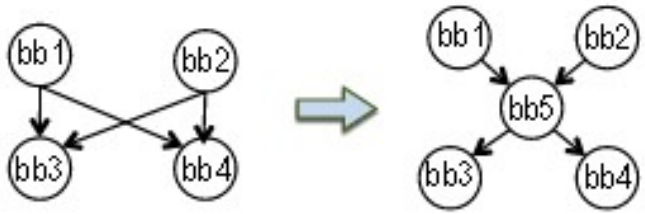

Fig. X: Control Node Reconstruction for optimized branch [1]
* With permission by IEEE

Table X: Simulation Results [1]
* With permission by IEEE

	crc	edgeDetect	prime	lzw	select
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speedup	1020	870	1162	770	685

- No plagiarism
- No copyright infringement
- Still: No own contribution

→Tip: Find your own representation!

[1] Kun Lu; Muller-Gritschneder, D.; Schlichtmann, U., "Hierarchical control flow matching for source-level simulation of embedded software," *System on Chip (SoC), 2012 International Symposium on* , vol., no., pp.1,5, 10-12 Oct. 2012

Citing Figures and Tables (5)

Example: Graphs are often better suited to present comparisons than tables

Table X: Simulation Results [1]
* With permission by IEEE

	crc	edgeDetect	prime	lzw	select
#. divsion	2	3	3	5	3
#. instr. (ISS)	21533	34552254	2409307	1585488	1992
#. instr. (SLS)	22305	34966371	2410509	1592424	1996
error(%)	3.6	1.2	<0.1	0.4	0.2
exe.time (ISS)	3.4ms	4.85s	314ms	265ms	343us
exe.time (SLS)	3.3us	5.6ms	270us	345us	0.5us
speedup	1020	870	1162	770	685

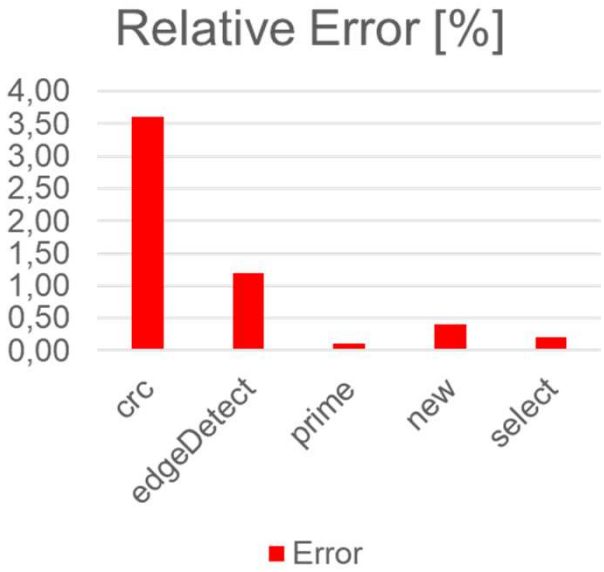

Fig. X: Simulation Results [1]

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Thank you for your attention and enjoy working on your topic!