



Name : .....

Roll No. : .....

Invigilator's Signature : .....

**CS/B.TECH (CSE)(N)/(IT)(N)/SEM-3/CS-301/2012-13**

**2012**

**ANALOG & DIGITAL ELECTRONICS**

Time Allotted : 3 Hours

Full Marks : 70

*The figures in the margin indicate full marks.*

*Candidates are required to give their answers in their own words  
as far as practicable.*

**GROUP – A**

**( Multiple Choice Type Questions )**

1. Choose the correct alternatives for any *ten* of the following :

10 × 1 = 10

- i) A 2-transistor class B power amplifier is commonly called
- |                 |                   |
|-----------------|-------------------|
| a) push-pull    | b) dual           |
| c) differential | d) none of these. |
- ii) A stable multivibrator has
- |                      |                     |
|----------------------|---------------------|
| a) no stable state   | b) one stable state |
| c) two stable states | d) none of these.   |
- iii) Schmitt trigger circuit generates
- |                    |                   |
|--------------------|-------------------|
| a) triangular wave | b) square wave    |
| c) saw tooth wave  | d) none of these. |
- iv) A Wien-bridge oscillator has a frequency
- |                              |                          |
|------------------------------|--------------------------|
| a) $\frac{1}{2\pi\sqrt{RC}}$ | b) $\frac{1}{\sqrt{RC}}$ |
| c) $\frac{1}{2\pi RC}$       | d) none of these.        |



- v) Which of the following oscillators is used at audio frequency ?
- Crystal oscillator
  - Hartley oscillator
  - RC phase-shift oscillator
  - Colpitts oscillator.
- vi)  $A + A'B + B'$  is equal to
- A
  - $B'$
  - 1
  - 0.
- vii) Negative feedback in an amplifier is
- reduced gain
  - increased noise
  - increased frequency & phase
  - reduced bandwidth.
- viii) How many minimum NOR gates is required to implement NAND gate ?
- 3
  - 4
  - 5
  - 2.
- ix) The digital logic family which has minimum power dissipation is
- TTL
  - RTL
  - DTL
  - CMOS.
- x) If the input to T-flip-flop is 100 Hz signal, the final output of the three T-flip-flops is cascade is
- 1000 Hz
  - 500 Hz
  - 300 Hz
  - 12.5 Hz.
- xi) Which one is the sequential circuit ?
- Multiplexer
  - Decoder
  - Encoder
  - Counter.



xii) 8421 is a

- a) weighted code                      b) non-weighted code  
c) complementary code              d) none of these.

**GROUP – B**

**( Short Answer Type Questions )**

Answer any *three* of the following                       $3 \times 5 = 15$

2. Implement Full-adder circuit using two Half-adders. Write the truth table of Half-subtractor.                       $3 + 2$
3. What is Multiplexer ? Why is it called 'data selector' ? Write the important characteristics of digital IC.                       $2 + 1 + 2$
4. Implement the function  $F(A, B, C) = \sum m(1, 3, 5, 6)$  using decoder. What is the difference between combinational circuit and sequential circuit ?                       $3 + 2$
5. Draw and explain the operation of Monostable multivibrator using 555 Timer.
6. Draw and explain the Schmitt trigger circuit.

**GROUP – C**

**( Long Answer Type Questions )**

Answer any *three* of the following.                       $3 \times 15 = 45$

7. a) Write truth table, circuit diagram and timing diagram of SR flip-flop using NOR gate.                       $8 + 7$   
b) Convert D flip-flop to JK flip-flop.
8. a) Design a 2-bit Asynchronous up counter using negative edge trigger JK flip-flop and draw timing diagram.                       $6 + 9$   
b) Design a MOD-6 Synchronous counter using JK flip-flop.
9. Write short notes on any *three* of the following :                       $3 \times 5$   
a) Johnson counter  
b) TTL family  
c) Serial input parallel output shift register  
d) BCD adder  
e) 8 : 3 encoder.



10. a) What are the advantages of negative feedback ?  
b) Explain the operation of a phase shift oscillator with circuit diagram.  
c) Derive an expression for its frequency of oscillation.

3 + 6 + 6

11. a) Explain the working of a R-2R Ladder type DAC with a neat circuit diagram.  
b) Explain the working of a successive approximation register (SAR) type ADC.

7 + 8

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