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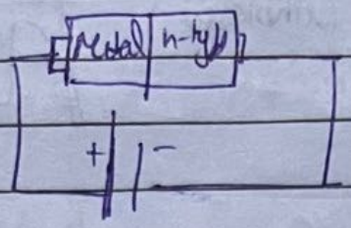
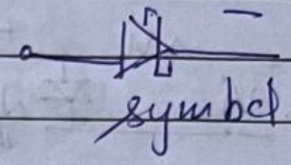
2.3 Schottky diode

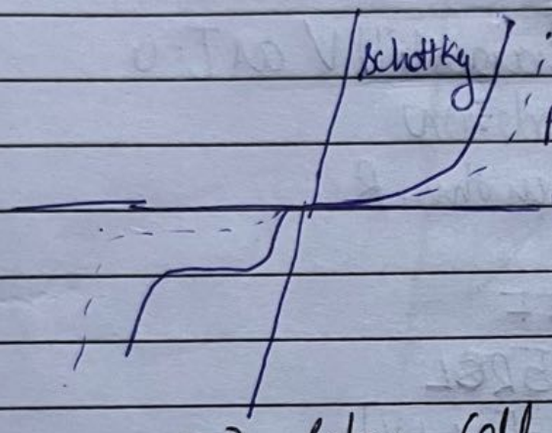
hot carrier diode





→ Construction (metal instead of p-type)

→ Working (no minority carrier, only e^-, high kinetic energy to overcome negative wall)



Unipolar

→ application

fast switching

Power rectifier

→ Solar Cell

→ LED

2.4 Zener & avalanche breakdown diff

2.5 Clipper & clamper

Answer

2

Ruhanika105

506 answers • 550.2K people helped

Since there are no minority carriers in the junction, the 'storage' time (the time required for the minority carriers to recombine with the majority carriers in the junction) is zero.
The only time required for the diode to turn off is the transit time of the majority carriers across the junction.
Thus schottky diode helps in reducing storage time.

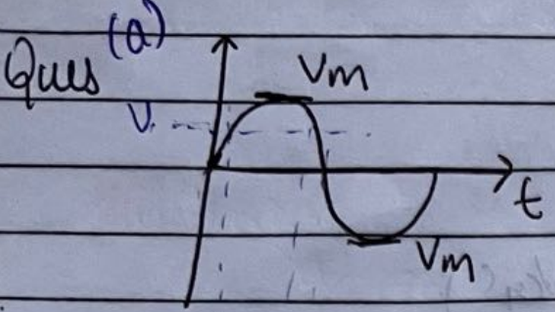
hope it helps....

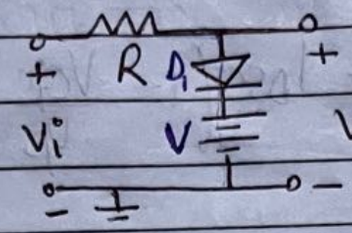
quarterfreelp and 2 more users found this answer helpful

THANKS 2 ☆☆☆☆☆ 0.0 (0 votes)

mod-1 (Prev Year)

Ques (a)



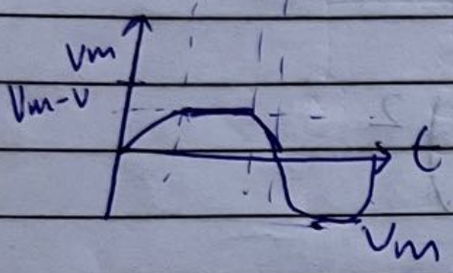


for +ve half cycle

(a) when $V_i < V$

D_1 will be O.B. (O.C) open circuit

output will follow input



(b) when $V_i > V$

replace Di with 0V (ideal)

$V_o = V_i - V$

for -ve half

input = output

(b)

What is Gray Code?

This code belongs to a class of codes called minimum change code in which only one bit in the code group changes when going from one step to the next.

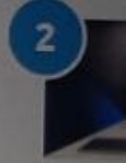
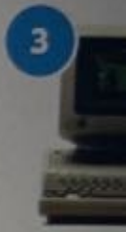
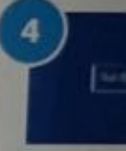
This is an un-weighted code which means that there are no specific weights assigned to the bit positions. Because of this the Gray code is not suited for arithmetic operations but finds applications is input/output devices and some types of analog to digital converters (ADCs)

Advantages of Gray Code

In Gray code, if we go from one decimal number to next, only one bit of the gray code changes. Because of this feature, an amount of switching is minimized and the reliability of the switching systems is improved.

Advantage of grey code over binary is only one-bit changes for each step. This will be useful in circuits that are sensitive to glitches. Example: When you use grey code to trim the output impedance of IO blocks, their won't be a huge jump in codes momentarily that would cause reflection.

The reflected binary code was originally designed to prevent spurious output from electromechanical switches. Today, Gray codes are widely used to facilitate error correction in digital communications such as digital terrestrial television and some cable TV systems.


Categor

› C Progra
› What is &
› Advantag

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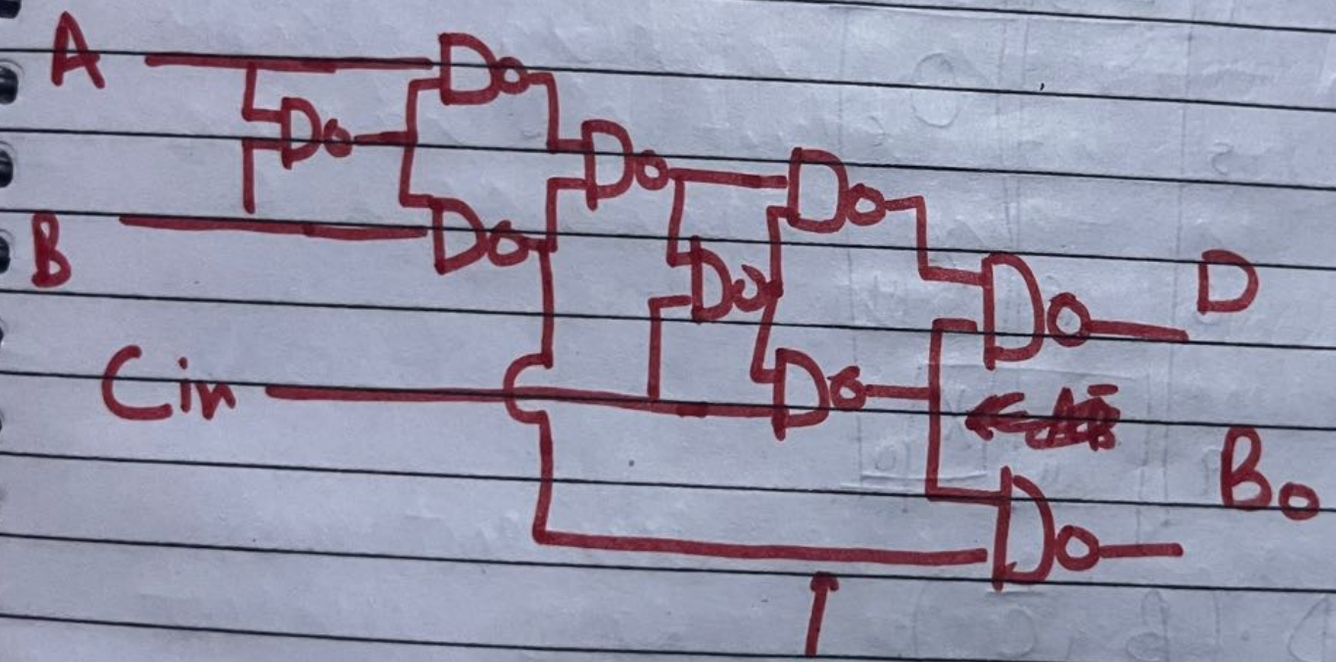
full subtractor using nand

$diff = A \oplus B \oplus C$ $\quad borrow = A\bar{B} + BC_{in}$

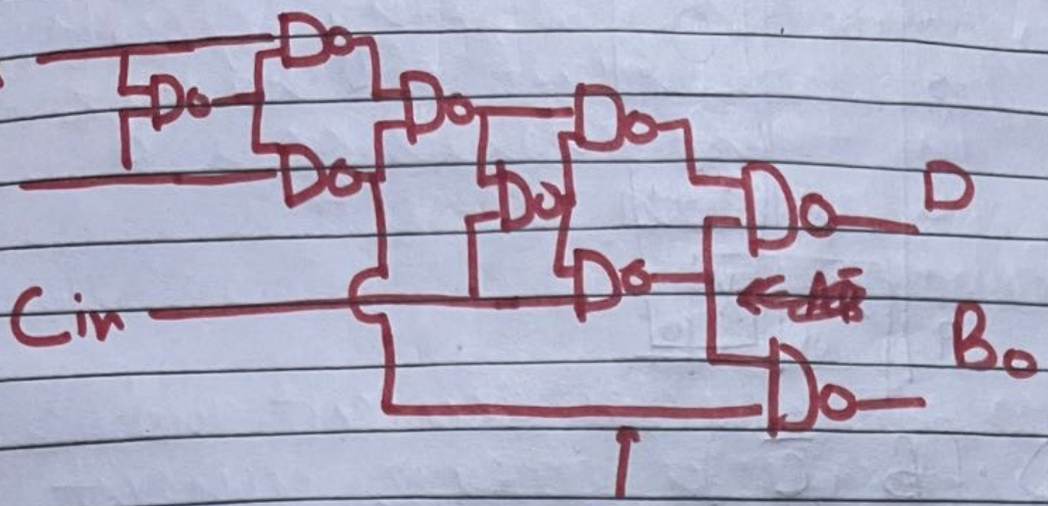
$(A \overline{\oplus} B)$



→ CMRR

Common mode rejection ratio

It is the ratio of differential mode voltage gain (A_d) to common mode voltage



→ CMRR

Common mode rejection ratio

It is the ratio of differential mode voltage gain (Ad) to common mode voltage gain

$$CMRR = \frac{Ad}{Ac}$$

Ideally $CMRR = \frac{\infty}{Ac = 0}$

numerical

$Ac = 0.2$ $CMRR = 3250$

Ans = 4.55 V rms

$$CMRR = \frac{Ad}{Ac}$$

$$Ad = \frac{0.2 \times 3250}{650}$$

$$= 650$$

$Vo = Ad(Vd)$ $Ad = \frac{Vo}{Vd}$

$650 \times 7\,mV = Vd$ $4550\,mV = 4.55\,V$ rms

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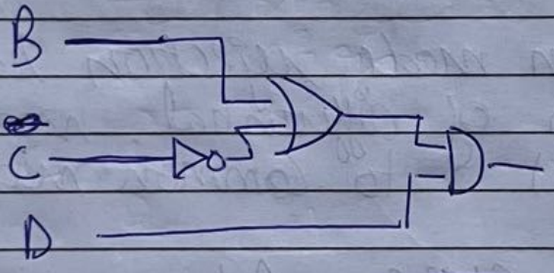
Ques $F(A,B,C,D) = \pi(0,2,3,4,6,12) + d(8,10,11,14)$

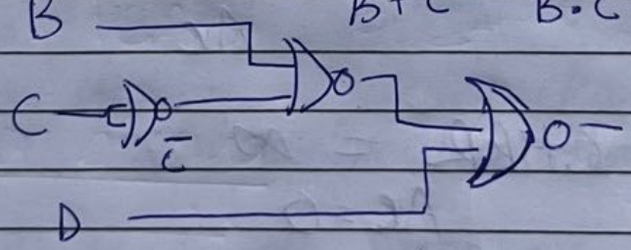
POS

AB \ CD	00	01	11	10
00	0 (0)	1	0 (3)	0 (2)
01	0 (4)	5	7	0 (6)
11	0 (12)	13	15	X (14)
10	X (8)	9	X (11)	X (10)

$F = D \cdot (B + \bar{C})$



$\overline{B+\bar{C}}$ $\overline{B \cdot \bar{C} + D}$ $(B+\bar{C})D$



Ans I_{CBO} and I_{CEO}

Good Write

→ I_{CBO} & I_{CEO}

↓

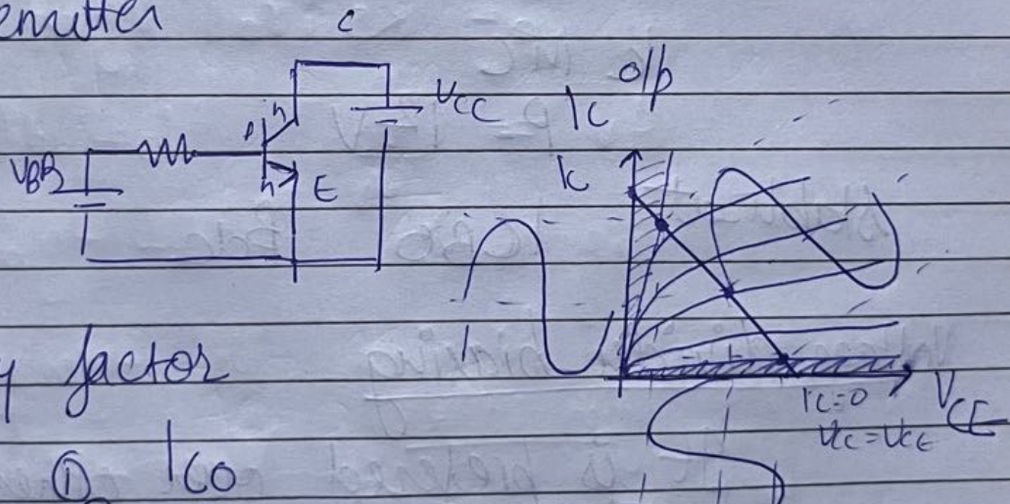
Both of these are leakage currents

I_{CBO} → current flows through collector Base in reverse bias them emitted is open circuit
(Happen in common base)

I_{CEO} → Current that flows through collector emitter in Revers bias when base is open circuited
(Happens in common emitter)

$$I_{CEO} = \frac{I_{CBO}}{1-\alpha}\Big|_{I_B=0}$$

Common emitter



Stability factor

Temp ① I_{CO}
② β
③ V_{BE}

① Saturation
② cutoff
③ center

Good Write

$I_{CEO} = (1+\beta) I_{CBO}$

$I_C = I_{EO} + \beta I_B$

V_{BE} changes 2.5 V/°C

β_{dc} varies with temp so I_C also varies as $I_C = \beta I_B$

Stabilization - process of making operating pt independent of change in temp changes or variation

Thermal Runaway

Flow of collector current and also the collector leakage current cause heat dissipation in unstabilized circuit which leads to self destruction

I_C inc

$P = I^2 V$

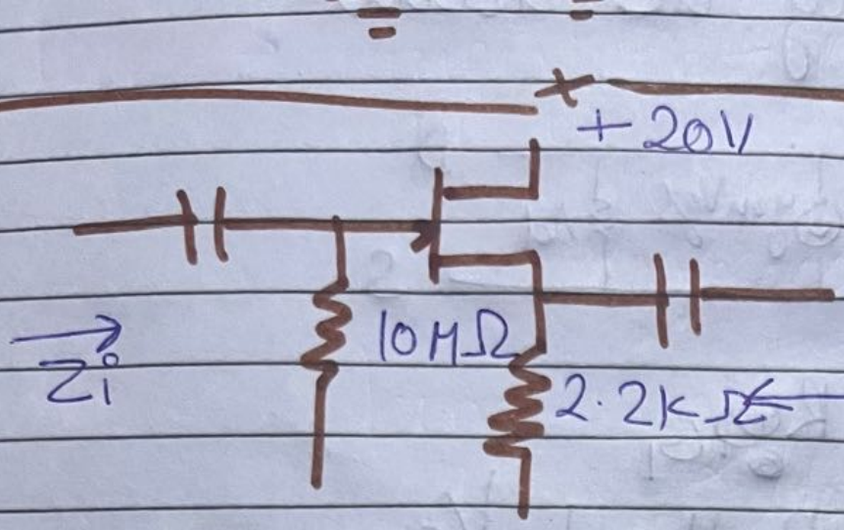
Stabilize I_{CBO} β_{dc} V_{BE}

Voltage divider biasing

It is prefered over other biasing as it gives complete control over current & voltage each component receives in the transistors.

Also R_E helps stabilize the value of β gain dispite fluction in β

Good Write



$I_{DSS} = 9mA$

$V_p = -4.5V$

$r_d = 40k\Omega$

Z_i, Z_o, A_v

$Z_i = R_G$

$Z_o = r_d \| R_s \| 1/g_m$

$$A_V = \frac{V_o}{V_i} = \frac{g_m(r_d \| R_s)}{1 + g_m(r_d \| R_s)}$$

$Z_i = R_G = 10M\Omega$

$Z_o = 40 \| 2.2 \| \frac{1}{2.28}$

$$g_m = -\frac{2 I_{DSS}}{V_p}\left(1 - \frac{V_{GS}}{V_p}\right)$$

$$A_v = \frac{V_o}{V_i} = \frac{g_m(r_d \| R_s)}{1 + g_m(r_d \| R_s)}$$

Good Write

$\frac{V_{in}}{R_1} = -\frac{V_o}{R_f}$ $V_o = 1 + \frac{R_f}{R_1}$

$\frac{V_o}{V_{in}} = -\frac{R_f}{R_1}$

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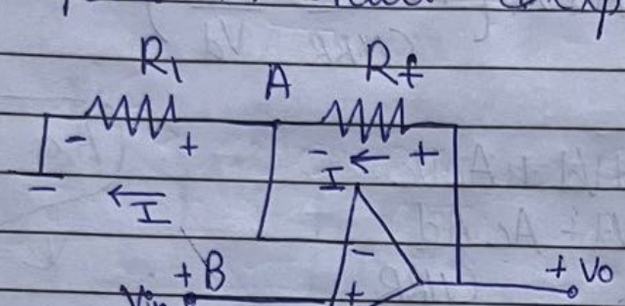
Ques Draw circuit diagram of closed loop non-inverting op-amp. and deriv the expression for it's voltage gain. Locate virtual ground point in circuit & explain significance

Ans →



from eq -① & ②

$\frac{V_o - V_{in}}{R_f} = \frac{V_{in}}{R_1}$

$\frac{V_o}{R_f} = \frac{V_{in}}{R_1} + \frac{V_{in}}{R_f}$

$\frac{V_o}{R_f} = V_{in}\left(\frac{R_1 + R_f}{R_1 R_f}\right)$

$A_{VF} = \frac{V_o}{V_{in}} = \frac{(R_1 + R_f) R_f}{R_1 R_f}$

$= \frac{R_1 + R_f}{R_1} = 1 + \frac{R_f}{R_1}$

$V_A = V_B = V_{in}$

from output side

$I = \frac{V_o - V_A}{R_f}$

$I = \frac{V_o - V_{in}}{R_f}$ -①

at inverting terminal

$I = \frac{V_A - 0}{R_1}$ -②

$I = \frac{V_{in}}{R_1}$

Practical op amp

① very high vol gain
② " " input impedence
③ very low output "
④ wide bandwidth

~~Dont~~ Calculating virtual ground

$I = \frac{V_o}{R_f}$ $V_{in} = 0$

$\frac{0}{R_1} =$

Good Write

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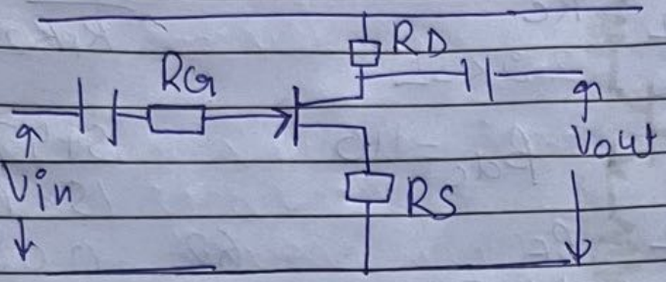
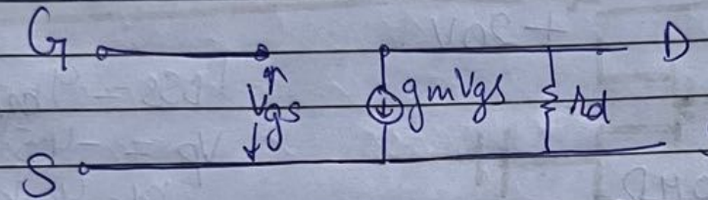
→ Common source JFET



Low frequency ac. circuit



$Z_i = R_G$

$Z_o = R_S \| r_d \| 1/g_m$

$A_v = \frac{V_o}{V_i}$ $V_o = I_d(r_d \| R_S)$

putting eqn $I_d = -g_m V_{gs}$

$V_o = -g_m V_{gs}(r_d \| R_S)$

$A_v = \frac{g_m(r_d \| R_S)}{1 + g_m(r_d \| R_S)}$

$V_{in} = -V_{gs} + V_o$

$= -V_{gs}(1 + g_m(r_d \| R_S))$