Final Assessment Test – November 2019

VIT
Vellore Institute of Technology

Course: ECE2002 - Analog Electronic Circuits

Class NBR(s): 0853 / 0861 / 0864 / 0866 / 0870 / 0880 / 6877 Slot: D1

Time: Three Hours Max. Marks: 100

KEEPING MOBILE PHONE/SMART WATCH, EVEN IN 'OFF' POSITION, IS EXAM MALPRACTICE

Answer ALL Questions

(i) How the diode will behave when a small low frequency signal and high frequency signal are applied to it? Draw the ac equivalent circuit for the two cases mentioned in the question. [10]

(ii) A PN junction operating in the forward-bias region with a current I of 1 mA is found to have a diffusion capacitance of 10pF. What diffusion capacitance do you expect this junction to have at I = 1mA? What is the mean transit time for this junction?

1. b) Derive the expression for voltage gain (A_M) and upper cutoff frequency f_H using hybrid π model of BJT with a neat diagram. [10]

[OR]

2. Given $I_C = 0.8$ mA, $R_1 = 68$ KΩ, $R_2 = 27$ KΩ, $R_C = 4.7$ KΩ, $R_E = 2.2$ KΩ, $R_{sig} = 10$ KΩ, $R_L = 10$ KΩ, $\beta_0 = 200$, $C_\mu = 0.8$ pF, $f_T = 1$ GHz. Neglect the effect of r_x and r_o. Find the midband gain and upper-3dB frequency of the CE amplifier. Also calculate the value of R_L that reduce the midband gain to half the value, and hence find the upper-3dB frequency of the CE amplifier for the reduced gain. [10]

3. Find the C_{C1}, C_{C2} and C_S for a CS amplifier for which $R_G = 4.7$ MΩ, $R_D = R_L = 5$k Ω, $R_{sig} = 100$k Ω, $r_o = 70$ Ω and $g_m = 1$mA. It is required to have f_L at 100Hz. [10]

4. For a N-channel MOSFET with $t_{ox} = 25$ nm, $L = 2$ μm; $W = 20$ μm, $L_{ov} = 0.07$ μm, $V_O = 0.55$ V, $C_{sbo} = C_{dbo} = 15$ fF, $V_{SB} = 1.2$ V and $V_{DS} = 2.5$ V. Determine a) Oxide capacitance, b) Overlap capacitance, c) Gate-Source capacitance, d) Gate-Drain capacitance, e) Source-Bulk capacitance and f) Drain-Bulk capacitance. [10]

5. a) The class-A amplifier shown in Fig.1 is biased at $V_{CE} = 12$ V. The output voltage is the maximum possible without distortion. Find [10]

(a) the average power from the dc supply,
(b) the average power delivered to the load,
(c) the efficiency,
(d) Draw the transfer characteristics of the amplifier showing the load lines and locate the Q-point.

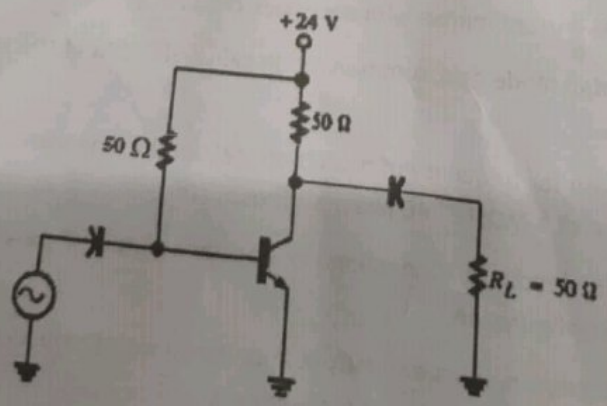

Fig.1

[OR]

5. b) For an PMOS differential pair with a common-mode voltage v_{CM} applied, as shown in Fig.2., let $V_{DD} = V_{ss} = 2.5$ V, $k'_nW/L = 3$ mA/V^2, $V_{th} = 0.7$ V, $I = 0.2$ mA, $R_D = 2$ kΩ, and neglect channel-length modulation. [10]

(a) Find V_{OV} and V_{GS} for each transistor.

(b) For $V_{CM} = 0$, find v_s, i_{D1}, i_{D2}, V_{D1}, and V_{D2}.

(c) Repeat (b) for $V_{CM} = +1$ V.

(d) Repeat (b) for $V_{CM} = -1$ V.

(e) What is the highest value of V_{CM} for which Q_1 and Q_2 remain in saturation?

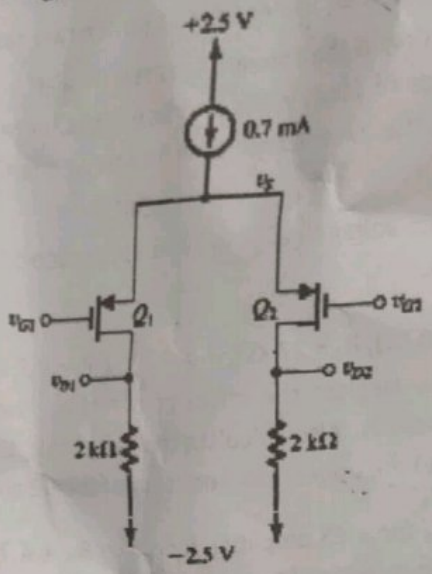

Fig.2

6. At an instance, consider a class B amplifier provides a 10 V peak signal to a 4 Ω load and a power supply of 12 V, [10]

a) Determine the input power, output power and efficiency of the amplifier.

b) What will be the peak output voltage when the class B amplifier provides efficiency of 78.54%?

c) Compute the maximum input power, maximum output power and maximum efficiency of the amplifier.

d) Estimate the maximum power dissipated by each transistors of the amplifier.

7. Explain Wilson MOS current mirrors with necessary circuit diagrams. [5]

8. Derive the differential mode gain, common mode gain and CMRR of the MOS differential pair, with neat sketch. [10]

9. Derive the expression for frequency of oscillation, gain of the amplifier and feedback gain to obtain sustained oscillation of a MOSFET RC phase shift oscillator. [10]

10. Explain the effect of feedback connection on input and output impedance for voltage series and voltage shunt and configuration. [5]

11. Determine the voltage gain, input and output impedance with feedback for voltage series feedback having A = -100, R_i=10kΩ and R_o = 20kΩ for feedback of $\beta = -0.5$. [5]

12. Explain the recent trends and techniques used in analog electronic circuits. [5]

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