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Continuous Assessment Test – I

Programme Name & Branch: B.Tech. IT **Exam Duration:** 90 mins **Slot:** G1+TG1

Course Code: ITE2001 **Course Title:** Computer Architecture and Organization

Faculty Name: Dr. Swarna Priya RM, Dr S. Subha **Maximum Marks:** 50

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1. a. Write an Assembly Language Program for implementing the expression
$Z=(X-Y)/((A+B)-(C/D))$
Consider that the data values are stored in memory location starting from 600 onwards and the program is stored from memory location 200 onwards. **(5 Marks)**

b. An instruction is stored at location 300 with its address field at location 301. The address field has the value 600. A processor register R1 contains the number 200 and another register R2 contains 210. Evaluate the effective address if the addressing mode of the instruction is (a) direct; (b) immediate (c) relative (d) register indirect; (e) index with R1 as the index register (f) base with R2 as the base register. **(5 Marks)**

2. Compute the memory traffic, total memory for encoding and storing code that implements the expression evaluation for the following code. Assume that opcode occupy one byte, address occupy three bytes, and data values also occupy three bytes and 1 byte word length for 0,1,2,3 address machines. Give proper justifications wherever required. (Use the template)

3-addr	2-aadr	1-aadr	0-addr

ADD A,B,C
MPY A,A,D
SUB A,A,E
	LOAD A,B
	ADD A,C
	MPY A,D
	SUB A,E
		LOAD B
		ADD C
		MPY D
		SUB E
		STA E
			PUSH B
			PUSH C
			ADD
			PUSH D
			MPY
			PUSH E
			SUB
			POP A

Template: (Follow for all types)

3-addr Instruction

Instruction	Memory to Store	Memory to Encode	M/A's to Fetch	M/A's to Execute	Total Memory Traffic
ADD A,B,C					
MPY A,A,D					
SUB A,A,E					
				Total	

After computation for each case, give the comparison in the following template.

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Instruction Type	Memory To Store in Bytes	Memory to Encode in Bytes	MAT to fetch an Instruction	MAT to Execute an Instruction	Memory Traffic

3. Show step by step multiplication process using Booth Algorithm when the following numbers are multiplied. Assume eight bit registers that hold signed numbers. (Use the following template)
(+15) * (-13)

A	Q	Q_{n-1}	Operation/ Action	Count/Iteration Number

4. a. Design the following set of instructions using a 5 stage instruction pipeline. If any hazards occur, identify those hazards and redesign the pipeline for rectifying each hazard. **(5 Marks)**
ADD R3,R1,R2
SUB R3,R2,R1
NAND R4, R3, R1
OR R0,R3,R4
XOR R1,R4,R3

b. Calculate the time taken (for the above set of instructions) by the pipelined processor with and without hazard if each instruction takes a cycle time of 10 ns and the time is evenly distributed among the stages. Compare the throughput of this pipelined processor with the unpipelined processor. Assume that there is no latency delay in the pipeline system. Use the following template for comparing the performance. **(5 Marks)**

Time taken in Unpipelined	Time taken in Pipelined (Without Hazard)	Time Taken in Pipelined (With Hazard Rectification)

5. a. Represent the following in Sign-Magnitude, 1's complement and 2's complement representation using 6 bits. **(3 Marks)**
-12

b. Consider that the processor accepts 2's complement data representation. Identify the original data. **(3 Marks)**
(i) 110110101
(ii) 010101010

c. Perform the following operation and identify if there is Overflow condition using 1's complement and 2's complement Addition Subtraction using 4 bits. **(4 Marks)**
(+7) + (-1)
(-1) + (-6)