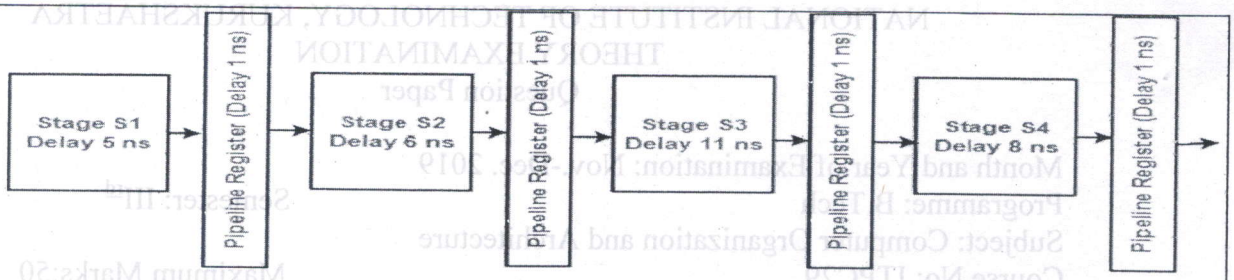
NATIONAL INSTITUTE OF TECHNOLOGY, KURUKSHAETRA
THEORY EXAMINATION
Question Paper

Month and Year of Examination: Nov.-Dec. 2019
Programme: B.Tech
Semester: III[rd]
Subject: Computer Organization and Architecture
Course No: ITPC29
Maximum Marks:50
Number of Questions to be attempted: 5
Time Allowed: 3 hrs
Total no of Questions: 5
Total No of Pages Used:2

Note: All questions are compulsory. Marks are indicated against each question. There is internal choice within Question 2 and Question 4

Q1	(i)What do you understand by Von Neumann type computation? Explain the organization of Von Neumann Computer using a schematic diagram. Point out the shortcomings of the Von Neumann Architecture. (5 marks) (ii) Discuss a few issues concerning computer architecture and organization (5 marks)
Q2	(i) Consider a pipeline having 4 phases with duration 60, 50, 90 and 80 ns. Given latch delay is 10 ns. Calculate-Pipeline cycle time, Non-pipeline execution time, Speed up ratio, Pipeline time for 1000 tasks, Sequential time for 1000 tasks, throughput? (5 marks) (ii)Show the hardware that implements the following statement. Include the logic gates for control function and a block diagram for binary counter with a count enable input (5 marks) $x\,yT_0 + T_1 + y'T_2$: AR<— AR+1 **OR** (iii) Consider an instruction pipeline with four stages (S1, S2, S3 and S4) each with combinational circuit only. The pipeline registers are required between each stage and at the end of the last stage. Delays for the stages and for the pipeline registers are as given in the figure. What is the approximate speed of the pipeline steady state under ideal condition compared to the corresponding non-pipeline implementation? (5 marks)

	
Q3	(i) What is difference between a direct and indirect address instruction? How many references to memory are needed for each type of instruction to bring an operand in to a processor register? (4 marks) (ii) A computer uses a memory unit with 256K words of 32 bits each. A binary instruction code is stored in one word of memory. the instruction has four parts: an indirect bit, an operation code, a register code part to specify one of 64 registers and an address part. (6 marks) a. How many bits are there in the operation code, the register code part and address part? b. Draw the instruction word format and indicate the number of bits in each part c. How many bits are there in the data and address inputs of the memory?
Q4	(i) A block-set associative cache memory consists of 128 blocks divided into four block sets. The main memory consists of 16,384 blocks and each block contains 256 eight-bit words. a) How many bits are required for addressing the main memory? c) How many bits are needed to represent the TAG, SET and WORD fields? (5 marks) (ii) How is write through method is different from write back method (5 marks) **OR** (iii) Consider a direct-mapped cache with 8 cache blocks (0-7). If the memory block requests are in the order-3, 5, 2, 8, 0, 6, 3, 9, 16, 20, 17, 25, 18, 30, 24, 2, 63, 5, 82, 17, 24. Which of the following memory blocks will not be in the cache at the end of the sequence? a)3 b)18 c)20 d)30. Also, calculate the hit ratio and miss ratio.
Q5	(i) Why does a DMA have priority over the CPU when both request a memory transfer? (4 marks) (ii) Establishing the priority of simultaneous interrupts can be done by hardware and software methods. What are these methods? (6 marks)