VR20
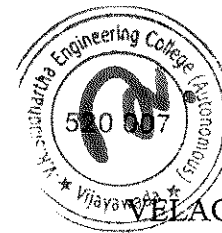
Reg. No:

VELAGAPUDI RAMAKRISHNA
SIDDHARTHA ENGINEERING COLLEGE
(AUTONOMOUS)

II/IV B.Tech. DEGREE EXAMINATION, JANUARY, 2023

Third Semester

ELECTRONICS AND INSTRUMENTATION ENGINEERING

20EI3303 DIGITAL CIRCUITS AND SYSTEMS

Time: 3 hours   *Max. Marks: 70*

Part-A is compulsory

Answer One Question from each Unit of Part - B

Answer to any single question or its part shall be written at one place only

PART-A

10 x 1 = 10M

1.   a.   Convert Decimal Number $(675)_{10}$ to Hexadecimal.   **(CO1 K2)**

   b.   Classify binary codes.   **(CO1 K1)**

   c.   Define Multiplexer.   **(CO1 K2)**

   d.   Write the truth table, characteristic equation of Full Subtractor.

                                                                     (CO2 K2)

   e.   Draw the Truth table, circuit diagram of JK flip flop.   **(CO2 K2)**

   f.   List the applications of counters.   **(CO3 K2)**

   g.   Define Flip Flop.   **(CO3 K2)**

   h.   What is full form of VHDL?   **(CO3 K2)**

   i.   Define Fan In and Fan Out.   **(CO4 K2)**

   j.   Define ROM.   **(CO4 K2)**
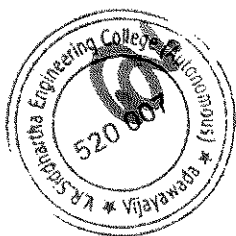
PART-B

4 x 15 = 60M

UNIT-I

2. a. Simplify the following Boolean function using tabulation method
        $Y(A,B,C,D)=\sum (0,1,3,7,8,9,11,15)$ **(CO1 K3) 8M**

    b. Express the following functions in sum of minterms and product of
        maxterms
        i) $(AB + C)(B + C'D)$
        ii) $x' + x(x + y')(y + z')$ **(CO1 K3) 7M**

(or)

3. a. What are universal gates? Realize AND, OR, NOT, XOR gates using
        universal gates. **(CO1 K3) 8M**

    b. Using the k-map method, obtain the minimal sum of products expression
        of the following function $Y = \sum (0, 2, 3, 6, 7, 8, 10, 11, 12, 15)$
        (CO1 K3) 7M

UNIT-II

4. a. Design a 32-to-1 MUX using 8-to-1 multiplexers. **(CO2 K5) 9M**

    b. Design a 4-bit Gray code to binary code converter. **(CO2 K3) 6M**

(or)

5. a. What is encoder? Design octal to binary encoder. **(CO2 K2) 8M**

    b. Design BCD to 7-segment decoder using logic gates. **(CO2 K2) 7M**

UNIT-III

6. a. What is race-around problem in JK flip-flop? Explain how it is
        eliminated in Master-Slave J-K flip-flop. **(CO2 K3) 8M**

    b. What is a shift register? Explain the working of serial in-serial out shift
        register with logic diagram and wave forms. **(CO2 K2) 7M**

(or)

7. a. Draw the circuit diagram of 4-bit ring counter using D flip flops and
        explain its operation with the help of bit pattern. **(CO2 K3) 8M**

    b. Convert a JK flip flop to a D flip-flop. **(CO2 K4) 7M**

UNIT-IV

8. a. Illustrate Basic Digital Design Process. **(CO4 K2) 6M**

    b. Draw the circuit diagram of CMOS NAND gate and explain its
        working. **(CO4 K2) 9M**

(or)

9. a. Write VHDL Program for logic gates. **(CO5 K3) 7M**

    b. Discuss briefly about various Read Only Memories. **(CO3 K2) 8M**

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