VIT
Vellore Institute of Technology

# Final Assessment Test – April 2019

Course: ITE1001 - Digital Logic and Microprocessor
Class NBR(s): 4376/4383/4389
Time: Three Hours

Slot: A2+TA2
Max. Marks: 100

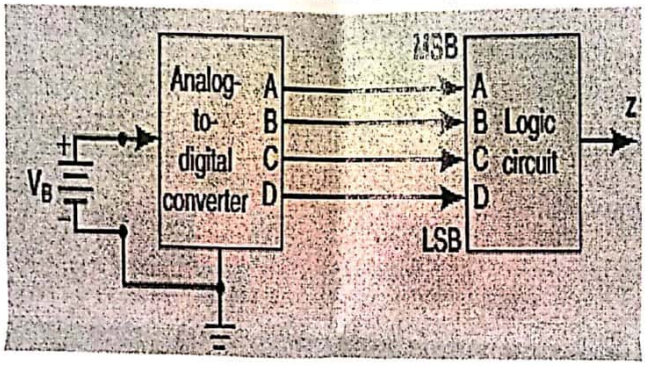
**Answer any TEN Questions**
**(10 X 10 = 100 Marks)**

1. a) Simplify the following Boolean Expression using K-Map. **[2.5]**
   $F(a,b,c,d) = \prod(2,4,9,12,15) + d(3,5,6,13)$

   b) Draw the logic circuit for the derived expression and find the NOR equivalent for the same. **[2.5]**

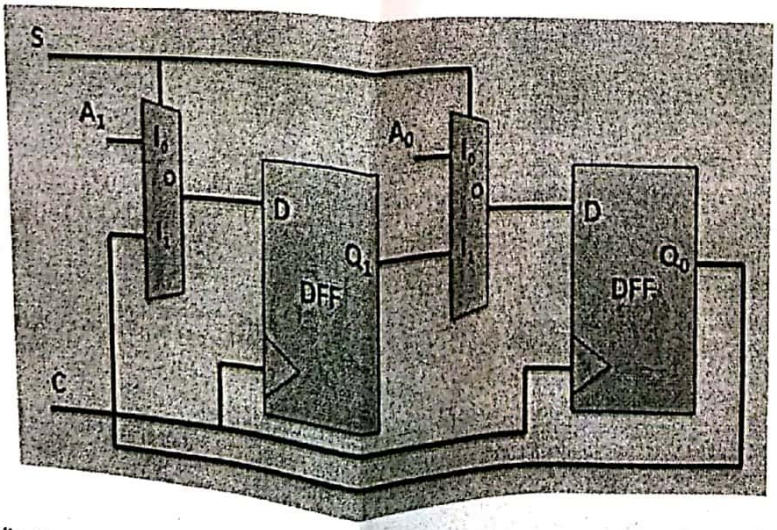
   c) Represent the following expression in Sum of minterms and Product of maxterms. **[5]**
   $A' + B' + A'C + ABCD$

2. Refer to Figure below, where an analog-to-digital converter is monitoring the dc voltage (VB) of a 12-V storage battery on an orbiting spaceship. The converter's output is a four-bit binary number, ABCD, corresponding to the battery voltage in steps of 1 V, with A as the MSB. The converter's binary outputs are fed to a logic circuit that is to produce a HIGH output as long as the binary value is greater than 01102=610; that is, the battery voltage is greater than 6 V. Design this logic circuit using 4*1 multiplexer. **[10]**




3. In digital systems it is often necessary to have circuits that can shift the bits of a vector by one or more bit positions to the left or right. Design a combinational circuit using decoder and external OR gates that can shift a four-bit vector W=w3w2w1w0 one bit position to the right when a control signal Shift is equal to 1. Let the outputs of the circuit be a four-bit vector Y=y3y2y1y0 and a signal k, such that if Shift=1 then y3=0, y2=w3, y1=w2, y0=w1, and k=w0. If Shift=0 then Y=W and k=0. **[10]**

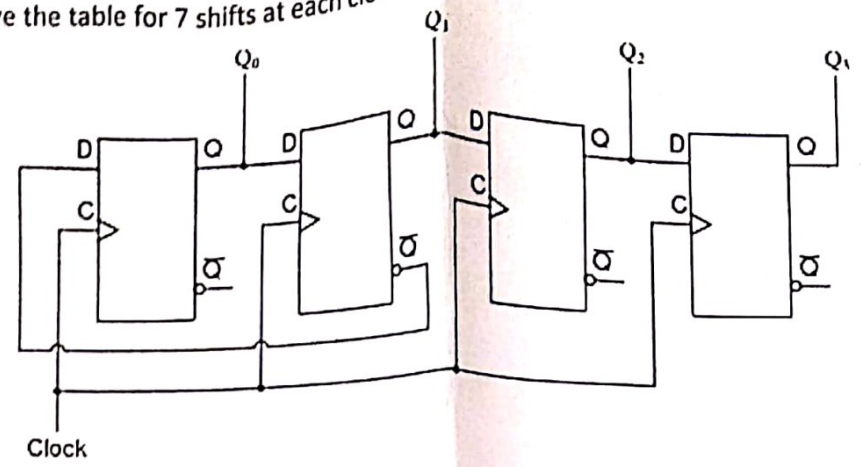
4. The below circuit shows a sequential circuit that uses two D-flip flops and two multiplexers. There are three inputs to the circuit, namely A0, A1 and S. The input C is the clock and the state variables Q1 and Q0 are the output of the circuit. At time t0, the output values Q1= 0 and Q0= 1. Show the timing diagram for the state variables Q1 and Q0. Also derive the state diagram and state table. **[10]**






Possession of Mobile Phone in the exam hall even in switched off condition is a malpractice.

5. Draw the timing diagram for this circuit until 10 clock pulses, assuming all Q outputs begin in the low state. Also give the table for 7 shifts at each clock pulse. [10]




6. Design an Asynchronous counter which counts in the sequence 001, 011, 101, 110, 010, 111, 000, 001 ... using JK Flip Flop. Remodify the same for working as a down counter. [10]

7. a) Analyse the following instructions and specify the content of flag registers, general purpose register and accumulator at the end of execution of every instruction. [5]

```
MVI A, #29H
MVI B, #30H
MOV C, B
ADC B
MOV D, A
SBB C
MOV E, A
HLT
```

b) Calculate the execution time for each Machine cycle and the instruction if the clock frequency f=7 MHz. [5]

i) MVI B, #09H
ii) CMA
iii) ADI #07H

8. Analyse the use of the following instructions and specify the Addressing modes used. [10]

i. MOV AX, DX
ii. MOV BX, [1345H]
iii. MOV CX, [BX]
iv. MOV DX, [BX + SI + 0AH]
v. MOV SI, [1234H]

9. a) Write an assembly language program using 8086 instructions for finding the LCM for two numbers stored in memory location 2034H and 2035H. Store the result in the memory location 1034H. [5]

b) Elucidate an assembly language program for finding the factorial of a number in 8086. [5]

10. Illustrate how the serial data communication could be carried out by the microprocessor using peripheral chip with a neat architectural diagram. [10]

11. a) Analyse the need of FPGA in digital design. [5]

b) Discuss how Internet of Things could be helpful in Industrial Automation. [5]

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