



VIT

Vellore Institute of Technology
(Deemed to be University under section 3 of UGE Act, 1956)

Continuous Assessment Test – II

Programme Name & Branch: B.Tech and ECE

Course Code&Name: ECE1006-Introduction to Nanoscience and Nanotechnology

Class Number: VL2019201001488, 1492, 1496

Slot: A1

Exam Duration: 90 mins

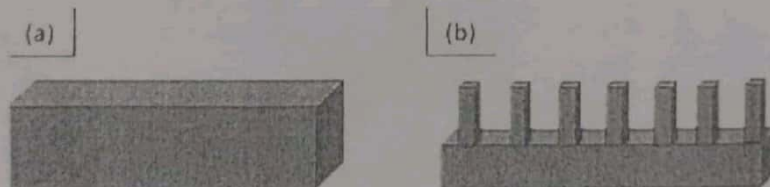
Date: 29-09-2019

Maximum Marks: 50

General instruction(s):

- Calculators are allowed!
- Answer should be specific to the questions.
- Point by point answer is highly recommended instead of writing paragraphs

1. The diagram below shows a rectangular silicon substrate (a) which needs to be patterned as shown in figure (b) using a cost-effective technique. The diameter of pillar (in figure b) is about 250 nm. Propose a suitable fabrication technique and discuss its process in detail with neat diagrams. (12)



2. (a) A high quality material of 'X' needs to be deposited on a suitable substrate for opto-electronics applications. The lattice constant of 'X' is about 5.5 \AA . Propose a suitable substrate from the below table and identify the fabrication process and discuss it in detail with suitable diagrams. (12)

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Substrate Materials	Lattice constant (Å)
GaAs	5.65
Glass (SiO ₂)	4.93
Alumina (Al ₂ O ₃)	4.78

(OR)

(b) Discuss a suitable scanning probe technique which can be utilized to image as well give information about the local electronic structure of an assembly of gold nanowire pattern in a copper substrate. Comments about the density of state plot. (12)

3/ Calculate the diameter and chiral angle of CNT with the following lattice vectors.

(a) (5, 5) (b) (5, 0) (c) (6, 3) (d) (6, 4)

Based on the calculation, identify the structures and explain about their electronic properties. (16)

4. Propose a suitable technique to synthesis multi-walled and single-walled CNTs for industrial applications. (10)

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