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VELAGAPUDI RAMAKRISHNA SIDDHARTHA ENGINEERING COLLEGE

(AUTONOMOUS)

II/IV B.Tech. DEGREE EXAMINATION, DECEMBER - 2023 Third Semester

ELECTRONICS AND INSTRUMENTATION ENGINEERING

20EI3303 DIGITAL CIRCUITS AND SYSTEMS

Time: 3 hours Max. Marks: 70

Part-A is compulsory

Answer One Question from each Unit of Part - B

Answer to any single question or its part shall be written at one place only

PART-A

 $10 \times 1 = 10M$

1.	a.	Convert $(10101)_2$ into decimal number system.	(CO1 K1)
	1	W1 4 1 DCD0	(CO1 T71)

b. What do you mean by BCD? (CO1 K1)

c. Write the carry expression for half subtractor. (CO2 K1)

d. Define Demultiplexer. (CO2 K1)

e. Write the characteristic equation of SR Flip-Flop. (CO3 K1)

f. Define register. (CO3 K1)

g. List various types of ROMs. (CO4 K1)

h. Mention any two characteristics of digital IC's. (CO4 K1)

i. List data types used in VHDL. (CO5 K1)

j. What are the basic uses of EDA tools. (CO5 K1)



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UNIT-III

- a. Design a JK flip flop using AND gates and NOR gates. Explain the operation of the JK flip flop with the help of characteristic table and characteristic equation.
 (CO3 K3) 8M
 - b. Explain the D flip-flop with the help of truth table and excitation table.

 (CO3 K3) 7M

(or)

- 7. a. With suitable logic diagram explain a 4-bit bidirectional shift register? (CO3 K2) 8M
 - b. What are the different types of registers? Explain the Serial Input Serial
 Output shift register. (CO3 K2) 7M

UNIT-IV

- 8. a. Write a VHDL code for Half adder and full adder. (CO5 K3) 5M
 - Explain the functional diagram and operation of various memory devices.
 (CO4 K2) 10M

(or)

9. a. Write the VHDL code for Implementation of logic gates.

(CO5 K3) 6M

Write a detailed note on logic families. (CO4 K2) 9M

UNIT-I

2. a. List various logic gates and explain.

(CO1 K2) 8M

 $4 \times 15 = 60M$

b. Convert the following to Octal then hexa decimal. (CO1 K2) 7M (i) (568), (ii) (1100110011), (iii) (23.45), (23.45)

(or)

- 3. a. Explain Quine-Mcklusky method of minimization with suitable example. (CO1 K2) 9M
 - b. Explain the generation of 4-bit Gray code.

(CO1 K2) 6M

UNIT-II

4. a. Design BCD to 7 segment decoder.

(CO2 K3) 8M

b. Design Full adder using two half adders and required gates.

(CO2 K3) 7M

(or)

- 5. a. A certain logic circuit has four inputs A, B, C, and D. The output X of the circuit is logic 1 if two or more inputs are logic 1. Implement by using decoder with active low output. (CO2 K3) 8M
 - b. Implement the function $F(A,B,C,D) = \sum (1,3,4,11,12,13,14,15)$ using 8×1 Multiplexer. (CO2 K3) 7M