MAULANA ABUL KALAM AZAD UNIVERSITY OF TECHNOLOGY, WEST BENGAL

Paper Code : IT-502

COMPUTER ARCHITECTURE

Time Allotted : 3 Hours *Full Marks* : 70

The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable.

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for the following : $10 \times 1 = 10$

i) Size of virtual memory is equivalent to the size of

a) main memory

b) secondary memory

c) cache memory

d) totality of (a) and (b).

ii) The branch type instructions in program cause

a) data hazard b) structural hazard

c) control hazard d) none of these.

iii) In which category of Flynn's classification of computers do the array processors fall ?

a) SISD b) SIMD

c) MISD d) MIMD.

iv) Code sharing is possible in

a) paging b) segmentation

c) both (a) and (b) d) none of these.

v) The pre-fetching is a solution for

a) data hazard b) structural hazard

c) control hazard d) none of these.

vi) Several switch boxes are used in

a) single stage networks

b) multi-stage networks

c) multi-port memory networks

d) cross-bar switch networks.

vii) The instruction execution flow in the pipeline processor is represented by

a) reservation table b) data-flow diagram

c) time-space diagram d) flow chart.

viii) A no. of pipelines that are working in parallel are used in

a) pipelining b) super-pipelining

c) superscalar d) VLIW processor.

ix) The no. of operating system that controls a multiprocessor system is

a) one

b) two

c) three

d) equal to the no. of processor attached to the system.

x) The protection against unauthorized access can be achieved by

a) any single stage network

b) any multi-stage network

c) multi-port memory network

d) cross-bar switch network.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following $3 \times 5 = 15$

2. What is VLIW processor ? How it is differ from superscalar architecture ? How will you design a VLIW processor ? 1 + 2 + 2

3. What are in-order issue and out-order issue in superscalar pipeline ? Describe with an example.

4. Describe the Shuffle-Exchange and Omega network of SIMD interconnection network.

5. What is cache coherence problem ? What are the several protocols to solve this problem ? 1 + 4

6. What is Flynn's taxonomy ? Compare RISC and CISC machines.

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. $3 \times 15 = 45$

7. a) What is the difference between computer organization and computer architecture ?

b) What is meant by pipeline architecture ? How does it improve the speed of execution of a processor ?

c) Consider the following reservation table for a 4-stage pipeline with a clock cycle t = 20 ns :

1	2	3	4	5	6	
×					×	S1
	×		×			S2
		×				S3
			×	×		S4

i) What are the forbidden latencies and the initial collision vector ?

ii) Draw the state transition diagram for scheduling the pipeline.

iii) Determine the MAL associated with the shortest greedy cycle.

iv) Determine the pipeline throughput corresponding to the MAL and given t.

v) Determine the lower bound on the MAL for this pipeline. 2 + 5 + 8

8. a) What is the arithmetic pipeline ? Describe with an example.

b) What do you mean by pipeline hazards ? What is a data hazard ? What are several types of data hazards and the solutions of these ?

c) What is register tagging or data forwarding ? Describe several methods of it. 4 + 7 + 4

9. a) What is virtual memory ? Why is it called virtual ? What are the advantages of it ?

b) what is locality of reference ? Explain the concept of cache memory with it.

c) What are the advantages of split cache memory ?

d) Given the following, determine the size of sub-fields in the address for several mapping schemes of cashe memory.

Main memory size : 512 MB, Cache memory size : 1 MB, Address space of processor : 512 MB, Block size : 128 B, 8 blocks in cache set.

4 + 3 + 2 + 6

10. Write short notes on any *three* of the following : 3 × 5

a) Array processor

b) Cluster computer

c) Data flow computer

d) Systolic architecture

e) Vector processor.