VIT
Vellore Institute of Technology

Final Assessment Test – November 2018

Course: CSE2001 - Computer Architecture and Organization
Class NBR(s): 5001 / 5002 / 5005 / 5007 / 5008 / 5009 / 5010 / 5011 / 5012 / 5013 / 6956 / 6968
Slot: B1+TB1
Time: Three Hours
Max. Marks: 100

PART – A (8 X 5 = 40 Marks)
Answer ALL Questions

1. Program execution normally follows sequential order as per Von Neumann Model – Analyze its pros and cons. Discuss the impact of program order and storage locations for parallel execution.
2. Describe data representation format for the following entities with an example for each:
   - Signed Integer value
   - Decimal or Binary point mixed value
   - Too Larger and smaller value
   - Characters
3. Give the register transfer notations for the typical multiplication operation on IAS machine: **LOAD MQ, M(100) MUL M(101)**
4. Design a cache memory unit with the capacity of 8KB, word size is 32-bits and block size is 8 words by using 4-way set associative mapping. Give the size of TAG memory as well as the data memory if the main memory capacity is 4 GB.
5. What is the need for an IO Interface? Compare and contrast Memory mapped IO and IO mapped IO approaches for interfacing IO devices.
6. Illustrate the physical structure of magnetic disk with necessary components.
   Calculate the average disk access time of a disk with average seek time of 5ms, 10000 RPM, 512 bytes per sector, 500 sectors per track, having transfer rate of 50MB/sec with controller overhead of 0.1ms.
7. *Give the expression for ideal pipeline* speedup. Justify the expression for a six stage pipeline with 9 tasks.
   A non-pipeline system takes 50ns to process a task. The same task can be processed in a six stage pipeline with a clock cycle of 10ns. Find the speedup ratio of the pipeline for 100 tasks. What is the maximum speedup that can be achieved?
8. Explain with suitable diagrams
   - Flynn's Taxonomy of parallel models
   - Shared Vs Distributed Memory model
   - Techniques for parallel execution of programs

PART – B (6 X 10 = 60 Marks)
Answer any SIX Questions

9. Discuss the following parameters for assessing the performance of CPU
   - Relative performance
   - Instruction Performance
   - Average Instruction CPI
   - CPU Performance
   - MIPS and MFLOPS rate

Consider the execution of a program which results in the execution of 2 million instructions on a 400 MHz processor. The program consists of four major types of instructions. The instruction mix and the CPI for each instruction type are given below based on the result of a program trace experiment:

Instruction Type	CPI	Instruction Mix
Arithmetic and logic	1	60%
Load/store with cache hit	2	18%
Branch	4	12%
Memory reference with cache miss	8	10%

Calculate the CPI, MIPS rate and CPU Time.

10. Suggest an algorithm with flowchart for the multiplication of signed 2's complement numbers. Solve **(-9) X (-13)** by using modified Booth's algorithm.

11. Extend the instruction set of von Neumann IAS machine with the following additional instructions – AND, OR, NOT, NEG, CMP. Characterize the enhanced instruction set for type, opcode and symbolic representation.

Write an assembly program using enhanced instruction set of IAS to find largest among the list of numbers.

12. Illustrate address translation using Paging system for a Virtual Address of 32b, 4GB Physical Memory, Physical Page of size 4KB and Page table of 4MB. Explain how the use of TLB cache can make the virtual address translation faster.

A Virtual Memory system has an address space of 8k words, memory space of 4k words and Page & Block size of 1k words. The following page reference changes occur during a given time interval. 4, 2, 0, 1, 2, 6, 1, 4, 0, 1, 0, 2, 3, 5, 7. Determine the four pages that are resident in main memory after each Page reference change if the replacement algorithm used is (i)FIFO (ii) LRU.

13. Define an Interrupt and categorize. Discuss the pros and cons of interrupt initiated IO over programmed IO. Suggest an approach for prioritizing and handling multiple simultaneous interrupts.

14. a. Write short notes on various storage technologies with an example each.
    b. Compare and contrast various RAID architecture levels to improve throughput and reliability of storage systems by using multiple disks.

15. Illustrate timing diagram for a typical 5-stage pipeline for 9 instructions.
Analyze the effect of conditional branch on pipeline if the instruction 3 branches to instruction 15 with the necessary branch penalty.
Derive the logic needed for pipelining to account for branches and interrupts.

16. Investigate how following factors impose practical limitations on pipeline:
    - Additional stage and delay between stages
    - Dependency on registers between instructions
    - Branches in program
    - Hazards or pipeline stalling – Structural, Data and Control
    - Memory bandwidth and conflicts