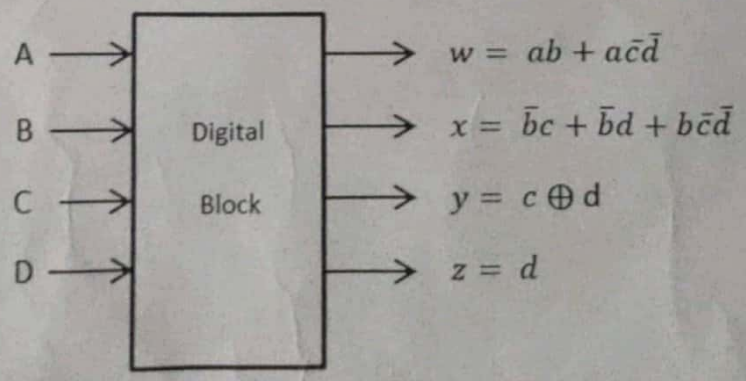
VIT
Vellore Institute of Technology

Continuous Assessment Test – II

Programme Name & Branch: B.Tech – ECE
Course Name & Code: Digital Logic Design & ECE2003 **Slot:** B1
Class Number:
Exam Duration: 2.00 PM – 3.30 PM **Date:** 30.9.18
Maximum Marks: 50

Answer ALL Questions.

Q. No	Ques	Marks
1.	Using a active low output decoder and external gates, design the combinational circuit defined by the following three Boolean functions: $f_1 = \bar{x}y\bar{z} + x\bar{y}, f_2 = \bar{x}\bar{y}z + x\bar{z}, f_3 = xy\bar{z} + xy$	10
2.	Design the following using only one 4:1 Digital Switch, in which K and M are the data inputs. $Z(K,L,M,N) = K\overline{LN} + KL\overline{M} + LMN + \overline{KL}M\overline{N}$, with don't care condition $(\overline{K}L\overline{M}N, K\overline{L}MN)$	10
3.	Draw the hardware logic that get infer for the following Verilog code. Rewrite the Verilog code using conditional operator. module que3 (e ,l , a, b, c, d); output a, b, c, d; reg a, b, c, d ; input e; input [1:0] l ; wire [1:0] l ; always @ (e or l) begin case (l) 2'd0: begin a = e; b = 0; c = 0; d = 0; end 2'd1: begin a = 0; b = e; c = 0; d = 0; end 2'd2: begin a = 0; b = 0; c = e; d = 0; end 2'd3: begin a = 0; b = 0; c = 0; d = 0; end endcase end endmodule	10
4.	Draw the circuit diagram with the truth table and write the structural level Verilog code. 	10
5.	Design a code converter to convert BCD to 7421 code.	10