Final Assessment Test – November 2019

VIT
Vellore Institute of Technology

Course: ITE2001 - Computer Architecture and Organization
Class NBR(s): 2674/2677
Slot: G1+TG1
Time: Three Hours
Max. Marks: 100

KEEPING MOBILE PHONE/SMART WATCH, EVEN IN 'OFF' POSITION, IS EXAM MALPRACTICE

Answer ALL Questions
(10 X 10 = 100 Marks)

1. a) Consider the expression Z = X*Y + Z. Assume multiplication has higher precedence than addition. Express Z in three address, one address notation. Assume each variable is integer of four bytes. What is the total memory access of your code? Can you generalize the total memory accesses for the three address and one address notation? [5]

   b) Consider the following program segment. Write the pipeline execution of the instructions assuming five stage pipeline. Identify the hazards if any in the code. Suggest one method to overcome the identified hazards. Assume there is one adder/subtractor unit available in the system. [5]

```
Add r1, r2, r3
Sub r3, r1, r4
If (r4>0) go to label1
Mul r3, r4, r5
Label1: Add r6, r1, r8
```

   Where add, sub, mul have the format
   Opcode operand1, operand2, destination

2. Perform 125/5 using non-restoring division. Suggest a method to improve the division performance.

3. a) Is floating point addition associative? Give an example. [5]

   b) Find the square root of 445 in binary. [5]

4. You are provided with RAM chip of size 128 x 8 and ROM chip of 256x8. Design memory system with 1024x8 RAM and 1024x8 ROM chips. Show the address map.

5. Compare the hit ratio of the following trace in direct mapped memory of 16 sets and 2-way set associative cache of 8 sets. Assume line size of 32B.

```
10101 1000 01010
10101 1000 01010
11001 1010 10101
11001 1010 10101
01011 1100 10101
11101 1100 10101
01110 0101 01010
10101 0100 01010
```


6. a) The following are the page references for main memory with four frames. [5]
   3, 4, 5, 3, 4, 5, 9, 10, 11, 12, 6, 7, 8, 10
   What is the page faults for FIFO and LRU algorithm?

   b) Given the data 10101 find the hamming code for it. [5]

7. What is DMA? Explain the features of DMA process if data of block sizes 1024B are to be transferred from disk to main memory. Can a computer have more than one DMA controller?

8. What is RAID? List the differences of various RAID level from level 1 to level 6. Can you have nested RAID? Give one example.

9. What is SMART? List any five parameters used in SMART.

10. Briefly describe the application of computer architecture in artificial intelligence.

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