VIT

Vellore Institute of Technology

(Deemed to be University under section 3 of UGC Act, 1956)

Continuous Assessment Test – 1

Programme Name & Branch: B. Tech (ECE)

Course Name & Code: Computer Organization & Architecture (ECE3004)

Class Number: 5035,5036

Slot: C1+TC1

Exam Duration: 90 min **Maximum Marks: 5X10=50**

ANSWER ALL QUESTIONS

1. **a) Draw the structure of the CPU (Central Processing Unit) and Control Unit of a computer with neat diagram.**

   b) Compare Von-Neumann vs. Harvard architectures with neat diagram.

SCAN ME

2. **a) Draw the expanded structure of IAS computer and explain the function of each block.**

   b) Assume a ROM memory chip of 5 GB (Giga byte) and PROM memory chip of 2 TB (Tera byte) are interfaced with CPU. Calculate the address lines required by the CPU to access the ROM and PROM memory chips.

3. **With neat flow chart perform the following multiplication using Booth's Algorithm for multiplicand $(-5)_{10}$ and multiplier $(-3)_{10}$**

   [OR]

   Illustrate how division is taking place in processor for the data $(-16)_{10}$ / $(-5)_{10}$ with suitable flow chart.

4. ***Using 2's complement arithmetic perform the following***
   - ***a) -18 + 21***
   - ***b) -17 – 22***
   - ***c) 19 + 23***
   - ***d) 16 - 24***

5. Assume a 16-bit registers are holding the values R_1=2000 and R_2=4000. The initial value of PC (Program Counter) is 1000 and each instruction occupies 2 bytes in ROM (Read Only Memory). The values stored in RAM memory is given below.

Memory Address(in decimal)	Value (in decimal)
2000	3000
3000	4000
4000	5000
5000	6000

Mention the addressing mode used in each of the following instruction and also specify the value of R1, R2, PC after the execution of every instruction.

1. MOV R_2, 2000
2. ADD R_1 , 2000
3. MOV R_2, [2000]
4. MOV R_1, R_2
5. MOV R_2, @ R_1
