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Paper Code : PE-EC603C CMOS VLSI Design

UPID : 006751

Time Allotted : 3 Hours *Full Marks :70*

The Figures in the margin indicate full marks.
Candidate are required to give their answers in their own words as far as practicable

Group-A (Very Short Answer Type Question)

1. Answer *any ten* of the following : [1 x 10 = 10]

(I) What is ASIC ?

(II) In a MOS, current becomes invariable with Drain to Source voltage in _____ region.

(III) Stick diagram carries out the information about _____ area of the device.

(IV) How Pseudo NMOS logic provides less no. of transistor count in comparison with Static CMOS logic?

(V) What is Iterative Placement?

(VI) Define Moore's Law.

(VII) When $V_{GS}>V_T$, pMOS operates in Cut-Off region. True or False ?

(VIII) Positive photoresist becomes insoluble in Developer solution , if exposed to UV-light. True or False?

(IX) The equivalent (W/L) of two nMOS transistors with (W_1/L) and (W_2/L) connected in parallel is
(a) $(W_1/L) + (W_2/L)$ (b) $(W_1/L).(W_2/L)$ (c) $1/(L/W_1 + L/W_2)$ (d) $(W_1/L)/(W_2/L)$

(X) What is netlist in vlsi?

(XI) The design flow of VLSI system is
1. Architecture design 2. market requirement 3. logic design 4. HDL coding.
Arrange in proper order.

(XII) Electron drift velocity saturation is a Short Channel Effect. True or False ?

Group-B (Short Answer Type Question)

Answer *any three* of the following : [5 x 3 = 15]

2. Discuss the working principle of nMOS. [5]
3. State the reasons for which Silicon is preferred over Germanium as wafer material. [5]
4. Design a Static CMOS Full adder circuit. [5]
5. Explain the differences between Slicing and Non Slicing Floorplan. [5]
6. Explain Drain Induced Barrier Lowering as a short channel effect. [5]

Group-C (Long Answer Type Question)

Answer *any three* of the following : [15 x 3 = 45]

7. (a) State Moore’s Law with the help of a graphical representation. [5]
   (b) Differentiate between PAL and PLA. [5]
   (c) Compare in between Channeled and channel less gate array based ASIC. [5]
8. (a) Compare I-V characteristics of NMOS and PMOS with mathematical equations valid for different modes of operation. [6]
   (b) Draw and explain cross sectional view of NMOS during Pinch-Off. [6]
   (c) State the advantages of Constant Voltage Scaling. [3]
9. (a) Show the difference between Isotropic and Anisotropic Etching with diagram. [5]
   (b) What is Annealing ? Discuss Rapid Thermal Annealing. [5]
   (c) 'A class 10 clean room in British System is equivalent to M 2.544 in Metric System.' Justify the statement. [5]
10. (a) A proximity printer operates with a 10 µm mask-wafer gap, and a wavelength of 430 nm. Another printer uses a 40 µm gap with wavelength 250 nm. Which offers higher resolution? [5]
    (b) Show that to grow an oxide layer of thickness x, a thickness of 0.44× of Si is consumed (Molecular weight of Si and SiO2 are 28.09 g/cm3 and 2.21 g/cm3) [5]

(c) Draw Stick Diagram of F= (AB+CD)'. [5]

11. (a) Design an AOI based S-R latch using Static CMOS logic. [5]

(b) Design a 2 input XOR and XNOR gate using Pass Transistor Logic. [5]

(c) NMOS is efficient is passing 'Strong 0' but not efficient is passing 'Strong 1'. Explain. [5]

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