

Vellore - 632 014, Tamil Nadu, India

SCHOOL OF ELECTRICAL ENGINEERING WINTER SEMESTER 2023-2024

CAT-II SLOT: E1

Programme Name & Branch : B.Tech.

Course Code: BEEE102L

Course Name

: Basic Electrical and Electronics Engineering

Faculty Members

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Class Number (s)

: VL2023240504548,4566,4569,4572,4577

Date of the Examination

: 05.04.2024

Duration: 90 minutes

Max. Marks: 50

General instruction(s): Answer ALL the questions. Q. No Question Marks a) Convert the octal number a) 321 and b) 1024 to its equivalent hexadecimal. 5 b) Determine, the POS and SOP form of $Z = \Sigma$ m (0, 1, 3, 6, 7, 8, 9, 13, 15). 5 a). A mild steel ring has a radius of 50 mm and a cross sectional area of 400 mm². A current of 0.5 A flows 2. in a coil wound uniformly around the ring and the flux produced is 0.1 mWb. If the relative permeability 5 at this value of current is 200 find (a) the reluctance of the mild steel and (b) the number of turns on the b). A solenoid of 800 turns is wound on an iron core of relative permeability 600. The length and radius of the solenoid are 20 cm and 3 cm respectively. Calculate the average emf induced in the solenoid if the 5

current in it changes from 0 to 6 A in 0.8 second. Using k-map realize the following expression using minimum number of gates $Y = \overline{A} \ \overline{B} \ \overline{C}D + \overline{A} \ \overline{B}CD + \overline{A}B\overline{C}D$ 3. $+\overline{A}BCD + A\overline{B}\overline{C}D + A\overline{B}CD + AB\overline{C}D + ABCD.$ 10

A magnetic circuit with a single air gap is shown in Figure 1. The core dimensions are: Cross-sectional area Ac = 1.8×10^{-3} m², Mean core length $l_c = 0.6$ m, air gap length $g = 2.3 \times 10^{-3}$ m, N = 83 turn. Assume that the core is of infinite permeability and neglects the effects of fringing fields at the air gap and leakage flux. (a) Calculate the reluctance of the core R_e and that of the gap R_g . For a current of i = 1.5 A, calculate (b) the total flux ϕ , (c) the flux linkages λ of the coil, and (d) the coil inductance L.

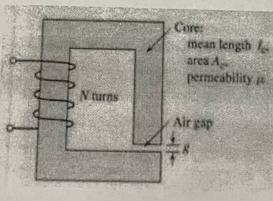


Fig. 1.

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Sketch the logic circuit using universal gate for expression F=((C'.B.A)'(D'.C.A)'(C.B'.A)')'. Use suitable gates such as NAND or NOR gate based on the expression given.