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VIT

Vellore Institute of Technology

School of Computer Science and Engineering
Continuous Assessment Test II – September – 2018

B.Tech Computer Science and Engineering- III Semester

CSE2001 –Computer Architecture and Organization

Answer all the questions (5 x10 = 50Marks)

1. A computer employs RAM chips of 512 x 8 and ROM chips of 128 x 8. The computer system needs 1024 *16 of RAM, 256 x 16 of ROM, and two interface units with 256 registers each.
   a. Compute the number of chips required to realize the required memory
   b. Compute total number of decoders are needed for the above system?
   c. Design a memory-address map for the above system
   d. Show the chip layout for the above design

2. Suppose an 8-bit data word stored in memory is 10111001. Using the Hamming algorithm, determine how many check bits & what check bits would be stored in memory along with the data word. Illustrate how check bits helps to detect and correct single bit error with an example.

3. (a) Explain the single precision format for floating point numbers and give the ranges for precision and significant. Represent the number $\mathbf{36.5625_{10}}$ in IEEE single precision format.

   (b) Perform binary floating point addition on the numbers 0.5_{10} and -0.4375_{10} and represent the result in 32 bit single precision format.

4. Assuming a computer memory system with following specifications:
   - Address size = 32b
   - Word size = 32b
   - Block size = word size
   - Cache size = 16KB
   a. Give the address format for Direct Mapping, 4-way Set Associative Mapping and Fully Associative Mapping.
   b. Analyse the size of Tag Versus Associativity.
   c. Total no. of comparators required for each mapping.
   d. Impact of multi word cache block on cache hit and miss ratio.
   e. Identify the optimal mapping function with respect to Tag size

5.
   a. Investigate key characteristics of computer memory systems for improving the overall system performance.
   b. List out the motivations for virtual memory. Frame a system to illustrate virtual to physical address translation mechanism with an example.