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Paper Code : PCC-CS402 Computer Architecture

UPID : 004442

Time Allotted : 3 Hours *Full Marks :70*

The Figures in the margin indicate full marks.
Candidate are required to give their answers in their own words as far as practicable

Group-A (Very Short Answer Type Question)

1. Answer *any ten* of the following : [1 x 10 = 10]

   (I) The process of converting a program written in a high-level language into machine code is known as _____.

   (II) The process of copying data from main memory to cache memory is known as _____.

   (III) In _____ processors, the entire vector is processed in a single instruction cycle.

   (IV) In a centralized shared-memory architecture, _____ is used to ensure that multiple processors do not attempt to access the same memory location simultaneously.

   (V) In pipelining, a _____ hazard occurs when an instruction depends on the result of a previous instruction that has not yet completed.

   (VI) The _____ property of cache memory refers to the fact that when a block is placed in a cache, all the blocks from higher levels of the memory hierarchy that contain that block are also present in the cache.

   (VII) What are the basic techniques for increasing ILP?

   (VIII) What is the main emphasis of dataflow architecture?

   (IX) What is pipelining?

   (X) What is virtual memory?

   (XI) What are vector processors used for?

   (XII) What is the purpose of a systolic architecture?

Group-B (Short Answer Type Question)

Answer *any three* of the following : [5 x 3 = 15]

2. What is the purpose of virtual memory in computer architecture? [5]
3. What is the purpose of loop unrolling ? How does it increase instruction-level parallelism (ILP) in processor architectures? [5]
4. Explain the concept of a systolic array and give an example of an application that could benefit from this architecture. [5]
5. Explain the concept of branch prediction in computer architecture. What are the different techniques used for branch prediction? [5]
6. What is cache coherence? Explain its importance in multiprocessor systems. [5]

Group-C (Long Answer Type Question)

Answer *any three* of the following : [15 x 3 = 45]

7. Compare and contrast the working of Direct Mapped, Set Associative and Fully Associative cache mapping techniques, highlighting their advantages and disadvantages. [15]
8. What are vector processors and how are they used in modern computing applications? [15]
9. What is distributed shared-memory architecture and how does it differ from centralized shared-memory architecture? [15]
10. (a) Explain the concept of exception handling in computer architecture. [4]
    (b) What are the different types of exceptions that can occur? [4]
    (c) How can exceptions be handled efficiently in a pipelined processor? [7]
11. Consider a processor architecture that implements both pipelining and out-of-order execution. Assume that the processor has four functional units and a pipeline depth of eight stages. Each functional unit has a latency of two clock cycles and the processor can issue up to four instructions per clock cycle. Assume that the processor uses a branch predictor with a 90% accuracy rate.
    (a) What is the maximum instruction-level parallelism (ILP) that can be achieved by this processor? [8]

(b) Assume that the program being executed contains a loop with a 10% taken branch. How many cycles are required to execute the loop, assuming that it contains 200 instructions and that the branch is taken every 10 iterations? [4]

(c) What is the impact of the branch on the performance of the processor and how could this be mitigated? [3]

*** END OF PAPER ***