DCS LAB- MAJOR (Set-1)

Name:

Roll No:

1. A 4-input multiplexer can be used to implement

(A) Four combinational functions of 2- variables each

(B) Two combinational functions of 4- variables each

(C) One combinational function of 4- variables

(D) One combinational function of 3- variables

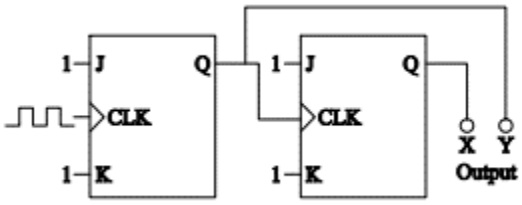
2. Which of the following circuits come under the class of sequential logic circuits?

1. Full adder 2. Full subtractor 3. Half adder 4. J-K flip-flop 5. Counter

Select the correct answer from the codes given below:

(A) 1, 2 and 4 (B) 2 and 3 (C) 3 and 4 (D) 4 and 5

3. The circuit shown in the figure below uses ideal positive edge-triggered synchronous JK flip flops with outputs X and Y. If the initial state of the outputs is X = 0 and Y = 0 just before the arrival of the first clock pulse, the state of the output just before the arrival of the second clock pulse is :



(A) X = 0, Y = 0 (B) X = 0, Y = 1

(C) X = 1, Y = 0 (D) X = 1, Y = 1

4. The result of $(45)_{10}$ - $(45)_{16}$ expressed in 2's complement representation is

(A) 011000 (B) 100111

(C) 101000 (D) 101001

5. What is the IC number of MUX used in the lab?

(A) 74151 (B) 74253 (C) 7400 (D) 7402

6. The output Qn+1 of a J-K flip-flop for the input J=1, K=1 is

(A) 0 (B) 1 (C) Qn (D) Q

7. A master slave flip-flop has the characteristic that

(A) change in the input immediately effected in the output

(B) change in the output occurs when the site of the master is affected

(C) change in the output occurs when the state of the slave is affected

(D) both the master and the slave states are affected at the same time.

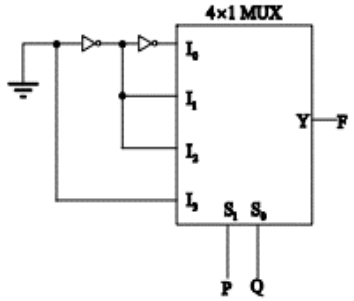
8. The output Y of a 2-bit comparator is logic 1 whenever the 2-bit input B is greater than or equal to the 2-bit input A. The number of combinations for which the output is logic 1, is

A. 4 B. 6 C. 8 D. 10

9. Which pin of LED used in the lab is positive side?

A. the shorter one B. the larger one C. both are positive D. none of these

10. The logic function implemented by the circuit below is (ground implies a logic "0")



(A) F = AND (P, Q) (B) F = OR (P, Q) (C) F = XNOR (P, Q) (D) F = XOR (P, Q)

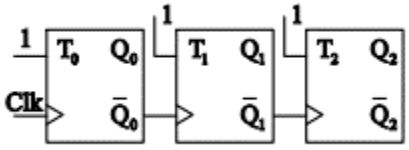
11. Convert RS Flip Flop to T Flip Flop?

12. In signed magnitude representation, the binary equivalent of 22.5625 is (the bit before comma represents the sign)

(A) 0, 10110.1011 (B) 0, 10110.1001

(C) 1, 10101.1001 (D) 1, 10110.1001

13. The given figure shows a ripple counter using positive edge triggered flip-flops. If the present state of the counter is Q2 Q1 Q0 = 011, then its next state Q2 Q1 Q0 will be



(A) 010 (B) 100

(C) 111 (D) 101

14. Identify the IC?

- 7404 …….
- 7402 …….
- 7432 …….
- 7486 …….

15. A full-adder can be implemented with half-adders AND OR gates. A 4-bit parallel full adder without any initial carry requires

(a) 8 half-adders 4-or gates

(b) 8 half-adders 3-or gates

(c) 7 half-adders 4-or gates

(d) 7 half-adders 3-or gates