Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS/B.TECH(ICE)/SEM-6/EI-602/2012

2012

MICROPROCESSOR BASED SYSTEM

Time Allotted : 3 Hours Full Marks : 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for any *ten* of the following :

10 × 1 = 10

i) What is the output of DL after execution of the following instructions ?

MOV DL, 36H

AND DL, 0FH

a) 06H b) 60H

c) 36H d) 0FH.

ii) $\overline{RQ}$ / $\overline{GT}$ signal used in

a) minimum mode only

b) maximum mode only

c) both maximum and minimum mode

d) none of these.

iii) When port *A* is used as input, port *B* and port *C* are used as output, the control word of 8255 is

a) 80H b) 90H

c) 85H d) 86H.

iv) What is the vector location of INT21 ?

a) 0084 b) 0054

c) 0064 d) 0021.

v) Which of the following signal should be provided to dynamic RAM ?

a) Refresh b) DMA request

c) Write enable d) Interrupt request.

vi) Which of the following segments is used by the CMPSB string instruction for the destination ?

a) CS b) ES

c) DS d) SS.

vii) The output frequency of OSC pin of 8284 clock generator is

a) same as crystal frequency

b) $\frac{1}{3}$ of the CLK pin

c) $\frac{1}{2}$ of the CLK pin

d) $\frac{1}{2}$ of crystal frquency.

viii) The INTR input is sensitive for

a) positive edge b) negative edge

c) edge & level d) only level.

ix) The refresh interval of DRAM is

a) 1 ms-2ms b) 2 ms-3ms

c) 3 ms-4ms d) 4 ms-5ms.

x) Scanned keyboard mode of 8279 interface keyboard in encoded scan

a) 4 × 8 b) 8 × 4

c) 8 × 8 d) 4 × 4.

xi) Function of ISR of 8259

a) store the interrupts

b) interrupt request being served

c) interrupt request served latter

d) interrupt request have been served.

xii) In 8259, which is the lowest priority interrupt ?

a) IR0 b) IR3

c) IR4 d) IR7.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. 3 × 5 = 15

2. Draw and discuss the internal block diagram of 8086.

3. What are the advantages of having segmentation ? How does the 8086 microprocessor support segmentation ? 2 + 3

4. Describe the function of the following instructions

$\overline{DEN}$, READY, LOCK, $\overline{TEST}$, $\overline{BHE}$.

5. Describe the different addressing modes of 8086 Microprocessor with proper example.

6. Discuss the memory organisation of 8051 micro controller.

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. 3 × 15 = 45

7. i) What is the difference between RET and IRET instructions in 8086 microprocessor.

   ii) Explain how bidirectional communication can be done between two computers using 8255A.

   iii) The content of SS is 5000H and the content of the stack pointer be 2050H. Find out the current stack-top address.

   iv) Explain the function of ISR during Interrupt operation in 8086. 3 + 6 + 3 + 3

8. i) Write down the procedure to determine physical address for the following Instruction as given below :

   a) MOV AX, [SI + 03]

   b) MOV AL, CS : [BX + 0400]

   c) MOV AX, [3000]

   d) MOV AL, [BX + SI + 22].

ii) From memory location 00490H successively 0AH, 9CH, B2H and 78H are stored respectively. What does AX contain after execution of each following instructions. Assume that SI contains 0490H and BP contains 0002H.

a) MOV AX, SI

b) MOV AX, (SI + 1)

c) MOV AX, (SI + BP) .

iii) What is instruction format ? What are the types of instructions of 8086 microprocessor ? 6 + 6 = 3

9. i) Design an interface between 8086 CPU and two chips of 32K × 8 EPROM and two chips of 16K × 8 RAM. Select the starting address of EPROM suitably. The RAM address must start at 00000H.

ii) Compare between the refresh cycle of DRAM & memory read cycle.

iii) Write down the RESET and INITIALIZATION procedure of 8086 processor. 8 + 3 + 4

10. i) Explain the register organization of 8237A DMA Controller.

ii) What is the function of HOLD HLDA signal ?

iii) Draw the internal architecture & explain the signals Keyboard/Display controller 8279. 6 + 3 + 6

11. Write short notes any *three* of the following : 5 + 5 + 5

i) BIU & EU of 8086 Microprocessor

ii) Register organization of 8051

iii) Interfacing of A/D converter with 8086

iv) OCW of 8259A.

v) I/O mapped I/O & Memory mapped I/O.