

## Communuous Assessment Leve

Frogramme Name & Branch & Fort & Co.

Course Name & Code

WEST Systems Design & Res was

Slot: A1+TA1

Exam Duration: 90 Minutes

Maximum Marks 56

(Answer all the questions)

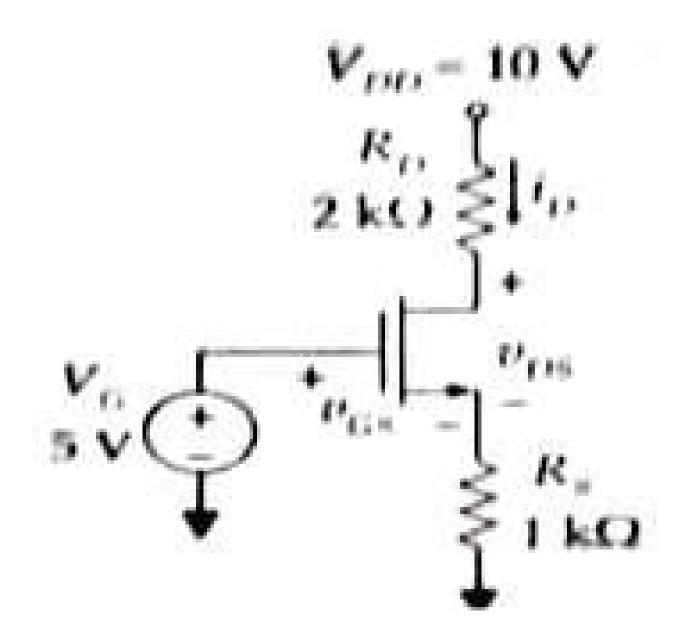
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- La Explain the following second order effects
  - a) Body effect

b) Channel length modulation

1.b For the circuit shown, use the the NMOS equations to find to and Voice Considering V<sub>10</sub> as 1 V.

[3]



2.a Implement the function F = ac'd'+acd+a'cb'+a'c'b using NMOS pass transistor.

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2.b Implement the CMOS Logic for the following expression

 $\mathbf{x} = \mathbf{u}\widetilde{\mathbf{x}} + \widetilde{\mathbf{n}}_{1}(\widetilde{\mathbf{r}} + \widetilde{\mathbf{D}} + \widetilde{\mathbf{D}} + \widetilde{\mathbf{r}}_{1}) + \widetilde{\mathbf{r}}_{1}\widetilde{\mathbf{G}}$ 

3.a Design a 4x1 Multiplexer using three 2x1 Multiplexer and implement the [5] 2 same using PMOS pass transistor logic.

- 3.b Discuss the capacitance associated with each terminal of the MOSFET. [5] 1
- 4.a Consider the nMOS transistor in a 0.6 µm process with gate oxide thickness of 100 A. The doping level is Na = 2 = 10<sup>17</sup> cm<sup>-1</sup> and the nominal threshold voltage is 0.7 V. The body is fied to ground with a substrate contact. How much does the threshold change at room temperature if the source is at 4 V instead of 0?
- 4.b Design a positive edge triggered the flop using 1Gs and explain its
  operation.
- 5.a Implement the function  $S = ABC + \overline{ABC} + \overline{ABC} + \overline{ABC}$  using [5] 2 Transmission gates
- Determine  $V_{\rm o}$  for each of the circuits shown below. Assume that  $V_{\rm in} = |V_{\rm spl}| = 0.5 V$ , that there is no subthreshold conduction, that the capacitor is initially discharged and that there are no body effects.

