# MAULANA ABUL KALAM AZAD UNIVERSITY OF TECHNOLOGY, WEST BENGAL

**Paper Code : EC302 Digital System Design**

**UPID : 003461**

*Time Allotted : 3 Hours* *Full Marks :70*

*The Figures in the margin indicate full marks.*
*Candidate are required to give their answers in their own words as far as practicable*

## Group-A (Very Short Answer Type Question)

1. Answer *any ten* of the following : [ 1 x 10 = 10 ]

(I) Which language can describe the hardware?

(II) Write the Gray code of $(1011)_2$ .

(III) What are the values of J and K of JK FF in the toggle state ?

(IV) Which logic gate family needs least power consumption?

(V) A D/A converter has a _____ input and _____ output.

(VI) 2's complement of which 5-bit binary number is the same number?

(VII) The S-R, J-K and D inputs are called _____ inputs.

(VIII) S-R type flip-flop can be converted into D type flip-flop if S is connected to R through _____ gate.

(IX) What do VHDL stand for?

(X) 1000 is a 2's complement number. Write the sign and magnitude of this number.

(XI) Which gates having output logic '1'when all its inputs are at logic '0'?

(XII) The resolution of 8 bit A/D converter is ..... %.

## Group-B (Short Answer Type Question)

Answer *any three* of the following : [ 5 x 3 = 15 ]

2. Define the following terms: [5]
i) Noise margin ii) Fan-in iii) Fan-out iv) Power dissipation v) Figure of Merit

3. Compare VHDL and verilog. [5]

4. Design a combinational circuit using all discrete logic gates to convert BCD-to-excess-3 Code. [5]

5. Draw diagram and explain the working principle of 3 bit synchronous Up-Down counter. [5]

6. Minimize the following expression using K-map. $Y(A,B,C,D)=\Sigma$ m (1,2,5,6,9) + d(10,11,12,13,14,15) [5]

## Group-C (Long Answer Type Question)

Answer *any three* of the following : [ 15 x 3 = 45 ]

7. (a) Briefly explain the operation of any one fast adder. [5+6+4]
(b) Design 4 bit composite adder in such a way that when external control signal='1' it will behave as adder otherwise subtractor.
(c) Implement a full adder using half adder and additional logic gates if required.

8. (a) Draw the diagram for a MOD -10 Johnson counter using J-K flip-flops and determine its counting sequence. Draw the decoding circuit needed to decode each of the 10 states. [10+5]
(b) Draw and explain the operation of J-K Master Slave flip flop.

9. (a) Draw an inverter circuit using CMOS and explain the operation. [5+5+5]
(b) Implement a full adder circuit using a suitable PROM type PLD.
(c) A 4-bit binary ladder D/A converter with R= 10 KΩ uses a reference of 5V. Find
(i) The analog output corresponding to the binary input 0110 (ii) Resolution in % (iii) Full scale output

10. (a) With neat sketch explain the digital system design approach using VHDL. [5+5+5]
(b) Differentiate concurrent and sequential assignments used in VHDL. Give suitable example.
(c) What are the various sequential statements in VHDL? Explain the behavioral description of Wait Statement with relevant example.

11. (a) Design synchronous counter with a repeated sequence of states as follows: [10+5]
(ABC) – (000 →001 →011 →010 →111 →101 →100→110→000 ..... )
Use D flip flop. Assume an input x, which control the forward and reverse transitions between the states.
(b) Draw the circuit diagram for a MOD-64 parallel counter.