END SEMESTER EXAMINATION : NOVEMBER-DECEMBER, 2023

BASIC ELECTRONICS ENGINEERING

Time : 3 Hrs. *Maximum Marks : 60*

Note: ***Attempt questions from all sections as directed. Use of scientific calculator is allowed.***

SECTION – A (24 Marks)

Attempt any **four** *questions out of* **five**.

Each question carries **06** *marks.*

1. Explain the two different types of capacitances across a P-N junction? Which of these is more important in case of forward bias?

2. Design a full subtractor using half subtractor and gates. Draw the truth table and expressions for difference and borrow

3. (a) A JFET has a drain current of 5mA. If I_{DSS} = 10 mA and $V_{GS\ off}$ = -6V, Find the value of V_{GS} and V_p. (4)

(b) Explain the significance of virtual ground in basic inverting amplifier. (2)

4. Sketch the Common Base (CB) configuration of BJT. Draw the input and output characteristics of Common Base (CB) configuration of BJT. In the output characteristics, which region is useful for voltage amplification and why?

5. Determine the output voltage of an OP-AMP for the input voltage of V_{i1} = 150μV, V_{i2} = 140 μV. The

amplifier has a differential gain of A_d = 5000 and the value of CMMR = 200.

SECTION – B (20 Marks)

Attempt any **two** *questions out of* **three**.

Each question carries **10** *marks.*

6. Determine v_o for the network of Fig. 1 for the input shown in Fig.2

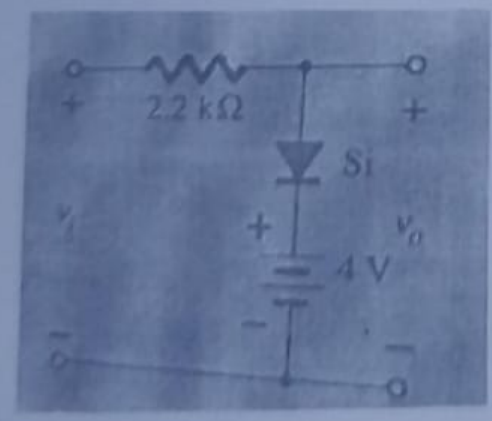


Fig.1

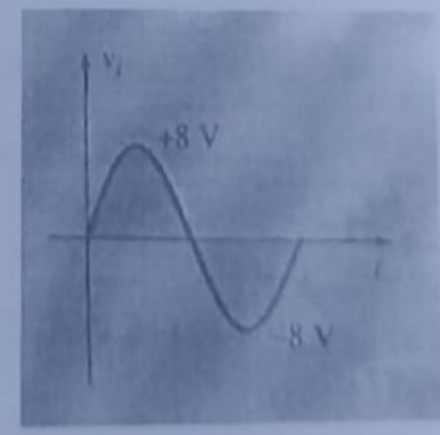


Fig.2

(5)

P.T.O.

(b) Minimize the following boolean function using Karnaugh Map and implement the minimized expression using gates: $F(A,B,C,D) = \Sigma(0,4,8,12) + d(1,2,3)$ (5)

7. (a) Draw the basic inverting amplifier with an input resistance R_i and feedback resistance R_f. Assuming the OP-AMP to be ideal, calculate the voltage gain ofthe inverting amplifier. (5)

(b) (i) For the Zener diode network of Fig 3 , determine V_L, V_R, I_Z, P_Z

(ii) Repeat part (i) with $R_L = 3k\Omega$

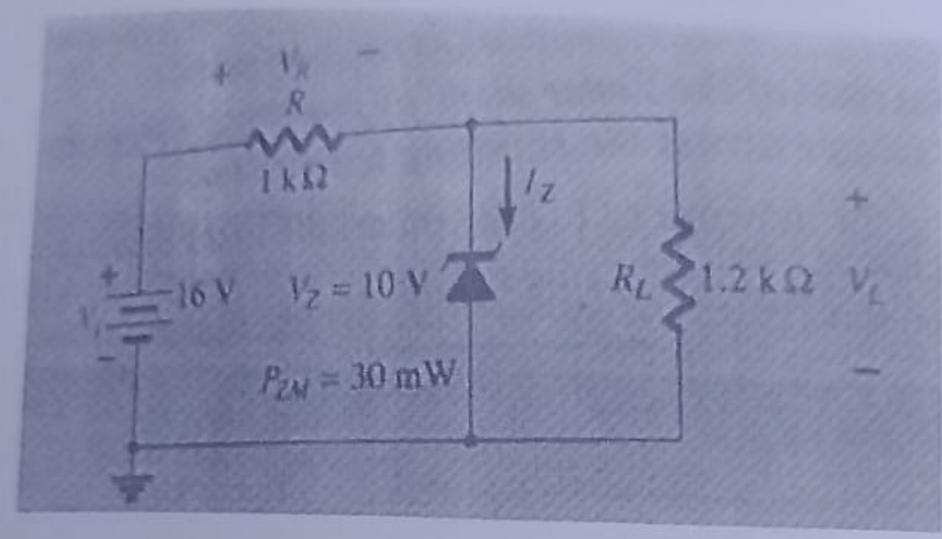


Fig.3

(5)

8. (a) Given an Enhancement - type MOSFET

(i) Given $V_{GS(Th)} = 4V$ and $I_{D(on)} = 6mA$ at $V_{GS(on)} = 6V$, determine k and write the general expression for I_D.

(ii) Sketch the transfer characteristics for the device of Part(a)

P.T.O.

(iii) Determine I_D for the device of part (a) at V_{GS} =2.5 and 10V (6)

(b) AC Voltage of 230 V is applied to a halfwave rectifier circuit through a transformer of turn ratio 10:1 . The load resistance value is 1 kΩ and diode internal resistance is 2Ω. Determine

(i) I_m, I_{dC} I_{rms}

(ii) D.c power output

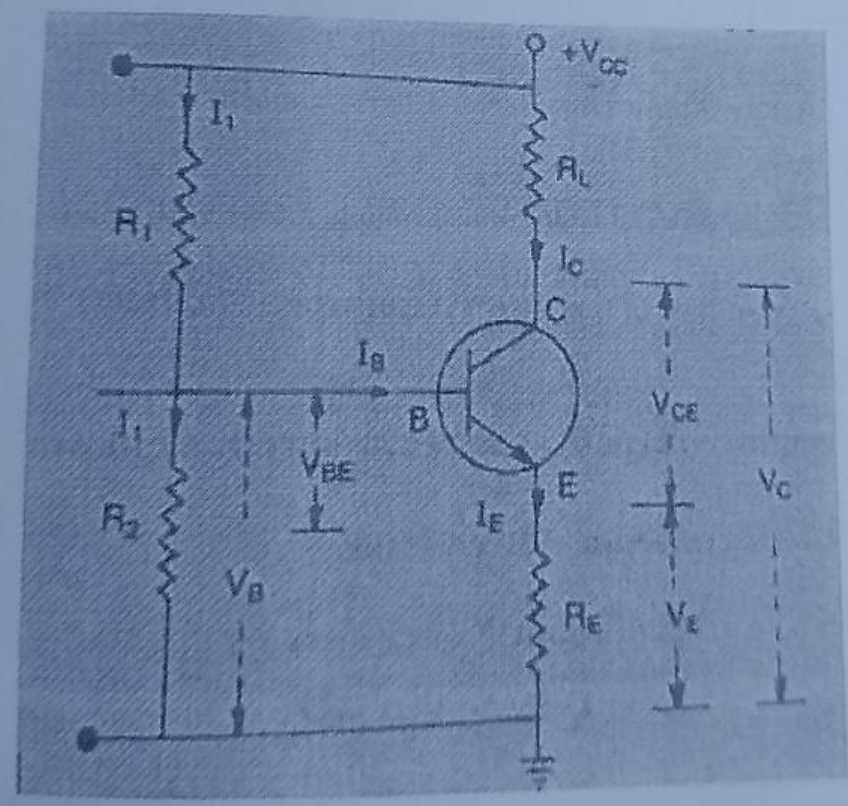
(iii) A.c power input

(iv) Efficiency of rectification (4)

SECTION – C (16 Marks)

(Compulsory)

9. (a) A Silicon transistor uses potential divider method of biasing V_{CC} = 12 V, R_1 = 10kΩ, R_2 = 5kΩ, R_L=1kΩ and R_E=3kΩ in fig below. Determine the operating point using Thevenin's theorem



(8)

P.T.O.

(b) Determine the value of transconductance ofa FET when drain current changes from lmA to 1.5 mA with a change in gate voltage from -2.125V to -2V. (5)

(c) Convert the following :

(i) $(11011)_2$ into decimal

(ii) $(243)_{10}$ into excess 3

(iii) $(10110110)_2$ into gray code (3)