Continuous Assessment Test – II

FALL Semester 2019-2020

Programme Name & Branch: M.Tech(SE) **Exam Duration:** 90 mins **Slot:**A2+TA2

Course Code: SWE 1003 **Course Title:** Digital Logic and Microprocessor

Faculty Name: Dr. Neelu Khare **Maximum Marks:** 50

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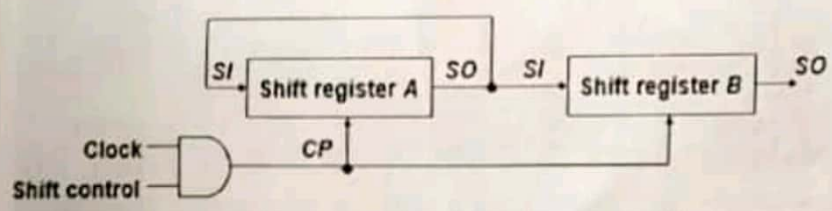
1. Consider the following set of shift registers. Let A contains 1100 and B contains 1111. What are the contents of A and B after eighth shift? (10 Marks)

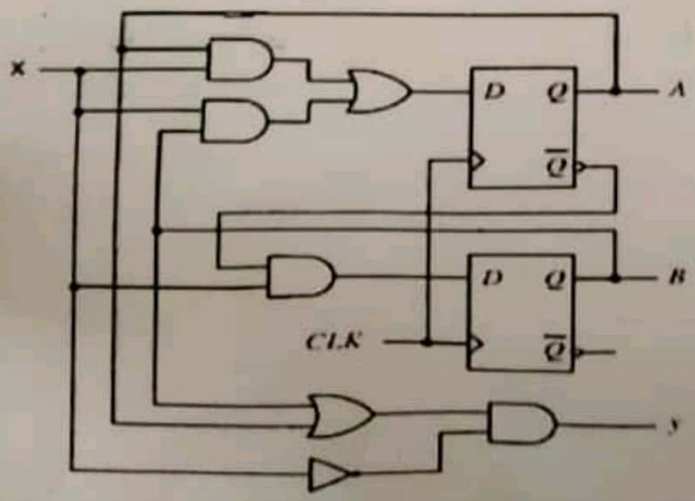


2. Design a sequential logic circuit with two D flip flops (X,Y) and one input A. When A=0, the state of the circuit remains the same. When A=1, the circuit goes through the state transitions from 00 to 11 to 10 to 01 back to 00 and then repeats. Derive the following: (15)
   - i) State Diagram
   - ii) State Table
   - iii) Input equations
   - iv) Logic circuit

   (15 Marks)

3. Design a Synchronous counter which counts the following sequence 1,3,5,7,1,... using the positive edge triggered JK flip flops. Draw the State table and logic circuit. (10 Marks)

4. Analyze the following sequential circuit and find its input-output equations, state table and state diagram. (15 Marks)



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