Name : ....

Roll No. : ....

Invigilator's Signature : ....

CS/B.Tech (CSE/IT)(NEW)/SEM-3/CS-303/2011-12
2011
COMPUTER ORGANIZATION

Time Allotted : 3 Hours   *Full Marks :* 70

The figures in the margin indicate full marks.

*Candidates are required to give their answers in their own words
as far as practicable.*

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for the following : 10 × 1 = 10

    i)   How many address bit are required for a 1024 × 8 memory ?

    a)   1024   b)   5

    c)   10   d)   none of these.

    ii) Micro instructions are kept in

    a)   Main memory   b)   Cache memory

    c)   Control memory   d)   None of these.

    iii) Booth's algorithm for computer arithmetic is used for

    a)   multiplication of numbers is signed magnitude form

    b)   division of numbers inn signed magnitude form

    c)   multiplication of numbers in 2's complement form

    d)   division of numbers in 2's complement form.

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iv) In a microprocessor, address for the next executable instruction is stored in the

    a) stack pointer   b) program counter

    c) instruction register   d) none of these.

v) A single bus structure is primarily found in

    a) Mini and micro computers

    b) Large mainframe computers

    c) Super computers

    d) Analog computers.

vi) Cache memory is used to

    a) increase performance

    b) increase machine cycles

    c) decrease performance

    d) none of these.

vii) Instruction cycle is

    a) Fetch-decode-execution

    b) Fetch-execution-decode

    c) Fetch-encode-execution

    d) Fetch-execution-encode.

viii) Equivalent hexadecimal of $(76575372)_8$ will be

    a) FAFAFF   b) FAFAFA

    c) FFFAAA   d) FAAFAF.

ix) Associative memory is

    a) a very cheap memory

    b) pointer addressable memory

    c) content addressable memory

    d) all of these.

x) Which of the following addressing mode is used for the instruction "Push B" ?

    a) Register   b) Register indirect

    c) Direct   d) Immediate.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. 3 × 5 = 15

2. Explain the difference between full associative and direct mapped cache mapping approaches ? Explain "write through" and "write back" policies in cache ? 3 + 2

3. Differentiate between three, two, one and zero address instructions with suitable examples. Explain base index addressing with example. 3 + 2

4. What is interrupt ? Differentiate vectored and non-vectored interrupts ? 1 + 4

5. Compare and contrast RISC and CISC architecture in brief.

6. What are the advantages of micro programming control over hardwired control ? Explain the role of an operating system in brief. 3 + 2
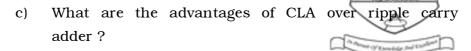
GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. 3 × 15 = 45

7. a) Describe the major components of a digital computer with a suitable block diagram.

   b) What are von Neumann concept and its bottleneck ?

   c) Explain and draw a binary decrement unit.

   d) Represent the decimal value – 7·5 inn IEEE – 754 single precision floating point formats. 5 + 4 + 3 + 3

8. a) Compare parallel adder with serial adder.

   b) With a suitable block diagram discuss the construction and working principles of an 8-bit carry-look-ahead adder.

    c)   What are the advantages of CLA over ripple carry adder ?

    d)   Explain the importance of a common bus system in a computer.   4 + 5 + 4 + 2

9.   a)   Explain Booth's multiplication algorithm with a suitable flowchart.

    b)   Using Booth's algorithm multiply (– 12) and (+ 6).

    c)   What do you mean by 'guard bit' ?   8 + 5 + 2

10.   a)   Explain instruction cycle, machine cycle and T-states with suitable example.

    b)   What are the advantages of relative addressing mode over direct address mode ?

    c)   Draw and explain the timing diagram for memory write operation.

    d)   Evaluate the arithmetic statement $X = (A * B) / (C + D)$ in one, two and three address machine.   5 + 4 + 3 + 3

11.   Write short notes on any *three* of the following : 3×5

    a)   IAS computer

    b)   Concept of hand shaking in IO operation

    c)   Static and dynamic memory

    d)   DMA controller

    e)   Classify MRI and non-MRI instructions.