

Name :

Roll No. :

Invigilator's Signature :

CS/B.Tech(CSE)(O)/IT(O)/SEM-3/EC-312/2012-13

2012

DIGITAL ELECTRONICS AND LOGIC DESIGN

Time Allotted : 3 Hours

Full Marks : 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for any *ten* of the following :

$$10 \times 1 = 10$$

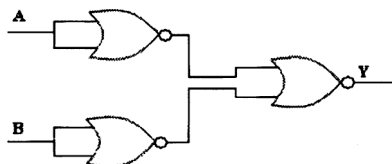
i) The octal equivalent of the binary number 11010111 is

- a) 656 b) 327
- c) 653 d) D7.

ii) A minterm is nothing but

- a) Standard sum terms
- b) Standard product terms
- c) May be standard sum term or product term
- d) None of these.

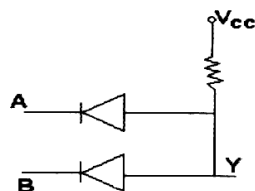
iii) Identify the operation of the following logic gate circuit :



- a) OR gate b) AND gate
- c) NOT gate d) none of these.



- iv) The fastest logic gate family is
- CMOS
 - ECL
 - TTL
 - RTL.
- v) The memory, which is ultraviolet erasable and electrically programmable is
- RAM
 - EEROM
 - EPROM
 - PROM.
- vi) A ring counter consists of 5 flip-flops will have
- 5 states
 - 10 states
 - 32 states
 - none of these.
- vii) The flip-flop, which is free from race around problem is
- R-S flip-flop
 - Master-slave JK flip-flop
 - J-K flip-flop
 - None of these.
- viii) Identify the carry expression of full adder circuit :
- $X'Y + ZX'$
 - $XY + YZ + ZX$
 - $XY' + YZ' + ZX$
 - $X'Y' + XZ' + YZ$.
- ix) Identify the operation of the circuit in the negative level logic system. :



- AND
- OR
- NAND
- NOR.



- x) The counter which requires maximum number of flip-flops for a given MOD number is
- Ripple counter
 - BCD counter
 - ring counter
 - programmable counter.
- xi) What is the minimum number of two-input NAND gates used to perform the function of two-input OR gate ?
- One
 - Two
 - Three
 - Four.

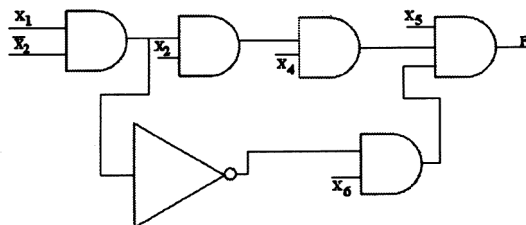
GROUP – B

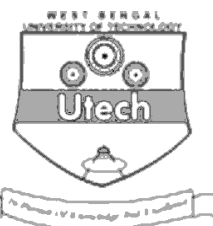
(Short Answer Type Questions)

Answer any *three* of the following. $3 \times 5 = 15$

- Draw Ex-OR gate circuit using minimum number of NAND gates and NOR gates.
- Implement a 16 : 1 MUX using only 4 : 1 MUX. Show block diagram only.
- What are the Schottky diode and schottky transistor ? What are the advantages of ECL logic family ?
- Simplify the following function using K-Map.

$$F(W, X, Y, Z) = W'X'Y' + X'YZ' + W'XYZ' + WX'Y'$$
- Converter the following circuit into a multilevel circuit using all NAND gates. Assume that the three and complement of all variables are available to the circuit.





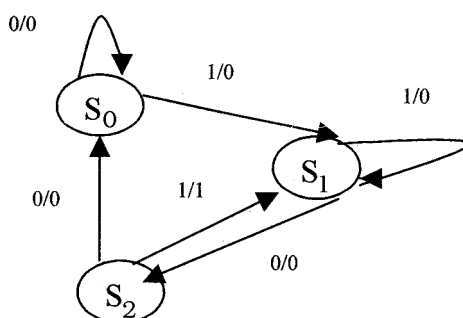
GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following.

3 × 15 = 45

7. a) Design a clocked synchronous sequential network whose state diagram is given below : 8



- b) Design a combinational circuit, which converts excess – 3 number to its corresponding BCD number. 7
8. a) Implement the following Boolean expressions using PAL.
 $F_1(A, B, C, D) = \sum (1, 2, 5, 7, 8, 10, 12, 13).$ 5
- b) Implement a full adder circuit using minimum number of NOR gates only. 5
- c) An 8 : 1 MUX has inputs A, B, C connected to select lines S_2, S_1, S_0 respectively. The data inputs I_0 to I_7 are connected as, $I_1 = I_2 = I_7 = 0, I_3 = I_5 = 1, I_0 = I_4 = D, I_6 = D'$. Determine the Boolean expression of the MUX output. 5
9. a) Design a MOD-6 synchronous counter using J-K flip-flop. 10
- b) (i) $F = AB + (AC)' + AB'C(AB + C)$
(ii) $F = ((XY' + XYZ)' + X(Y + XY'))'$ 5
10. a) What is the race around condition of J-K flip-flop ? How can it be avoided ? 5
- b) Design a BCD to 7-segment decoder using multiplexers. 10