ABV- Indian Institute of Information Technology & Management, Gwalior
Semester-II (BCCS-1203)

Course Title: Digital Circuit System (Major)

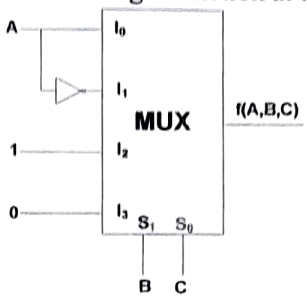
MM: 50 **Duration: 3:00 Hours**

Note:

1. All parts of a question should be answered consecutively.
2. Question paper has two sections and all the sections are compulsory.

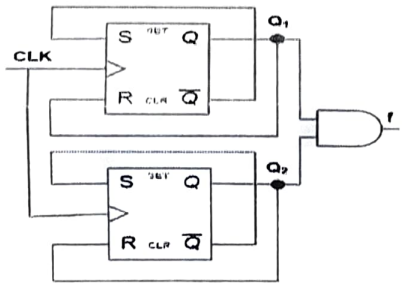
SECTION A

(1) For MUX shown in the figure below derive the logic function at the output terminal. **[2]**



(2) Design X-OR using 2:1 MUX. **[2]**

(3) What will be the duty cycle of waveform generated at "f". **[3]**



(4) Differentiate between combinational and sequential logic design. **[2]**

(5) $F(A,B,C) = \pi\ (0,2,4,7)$. Implement the given function using 4:1 MUX for given conditions (i) use BC as a select line and (ii) use AC as a select line. **[3]**

(6) Design 3:8 decoder using 2:4 decoders. **[2]**

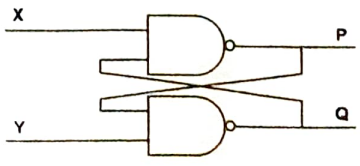
(7) An XY flip flop whose truth table is given is to be implement using JK flip flop. **[3]**

X	Y	Q_{n+1}
0	0	1
0	1	Q_n
1	0	$\bar{Q}_n$
1	1	0

(8) Given $F(w,x,y,z) = \Sigma(0,1,2,3,7,8,10) + \Sigma d(5,6,11,15)$. What is the minimum POS form of F(w,x,y,z)? Further, design a logical circuit using CMOS logic. **[3]**

(9) Derive the characteristic equation for the JK and SR flip flop (with proper steps). **[3]**

(10) The following binary values were applied to the X and Y inputs of the NAND latch shown in the figure in the sequence indicated below. X=0, Y=1; X=0, Y=0; X=1, Y=1. Find the corresponding stable P, Q outputs. **[2]**

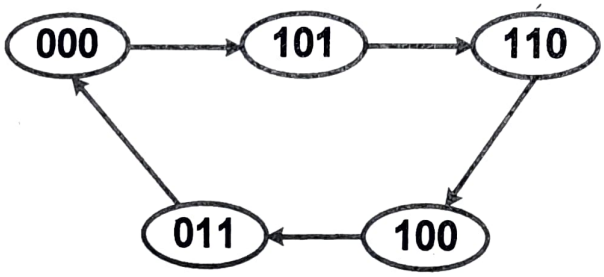


SECTION B

(1) Design a 4 bit look ahead carry adder. Explain the advantage of look ahead carry adder over parallel adder. **[5]**

(2) Design the given Boolean expression using (i) 2:1 MUX (ii) 4:1 MUX and (iii) 8:1 MUX.
$F(A,B,C) = \Sigma m(0,1,3,6,7)$ **[5]**

(3) Design a counter using T-FF that goes through following states. **[5]**



(4) Design 3-stage negative edge asynchronous UP/Down counter. The mode control; "M" decides the pattern of counting operation. When M=0 counter counts UP and when M=1, counter counts DOWN (Hint: Use MUX). **[5]**

(5) Consider the circuit given below. All J and K input are high and logic levels presents at each input and output prior to the occurrence of the first clock edge is mentioned in the circuit. Draw the timing diagram and tell after the occurrence of 6th negative going trigger of clock pulse the logic levels at X, Y, and Z. **[5]**