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Paper Code : PC-EE 602/PC-EEE-602 Micro processor & micro controller

UPID : 006608

Time Allotted : 3 Hours *Full Marks :70*

The Figures in the margin indicate full marks.
Candidate are required to give their answers in their own words as far as practicable

Group-A (Very Short Answer Type Question)

1. Answer any ten of the following : [1 x 10 = 10]

(I) What is the size of the queue in Intel 8086 microprocessor?

(II) How many bus cycles are used by the Intel 8086 processor to read a word from an odd address in memory?

(III) If an Intel 8086 based system has a total 64 K bytes of ROM memory in it then what should be one of the ROM memory location addresses available in this system?

(IV) Amongst the two possible architectures, Von Neumann architecture and Harvard architecture, which one is followed by Intel 8051 microcontroller?

(V) How many 8-bit parallel I/O ports are available in Intel 8051?

(VI) The instruction JE NEXT , where NEXT is a label, causes the processor to jump in which condition?

(VII) What is the addressing mode in the instruction ADD BL, DS:23H[BP][SI] ?

(VIII)
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MOV SP, 3012H
PUSH AX
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What will be the new value in SP register after the above two instructions?

(IX) What will be the control word that should be sent to 8255A to configure Port A as input in mode 0, Port B as output in mode 1 and remaining lines of Port C as output in mode 0?

(X) Which bit of the flag register is set when output overflows to the sign bit?

(XI) PIC 18 is a 8-bit microcontroller or 16-bit microcontroller?

Group-B (Short Answer Type Question)

Answer any three of the following : [5 x 3 = 15]

2. Explain with diagrams the IO mode control word Intel 8255A. [5]
3. With a neat diagram discuss the memory structure of Intel 8051 microcontroller. [5]
4. Write an ALP using 8051 instruction set, to load 25H and 34H in R2,R7 register respectively and store the Multiplication result of contents of R2 and R7 register in external RAM 0005H. [5]
5. Draw the timing diagram of a memory read cycle by Intel 8086 processor. Explain the signals. [5]
6. Describe Mode 3 in 8253 with timings diagram. [5]

Group-C (Long Answer Type Question)

Answer any three of the following : [15 x 3 = 45]

7. a) List the sequence of steps that the 8086 processor will go through when it will receive an interrupt signal on the INTR line. Assume a 8259A is connected to the system. [5+10]
b) Show how three 8259A s can be connected to the system where one is master and other two are slaves. Show only the connections of INTR, INTA' signals from the microprocessor side and IR signals and INT signals from 8259A side. No need to show the address decoding for chip select and connections of the data bus.

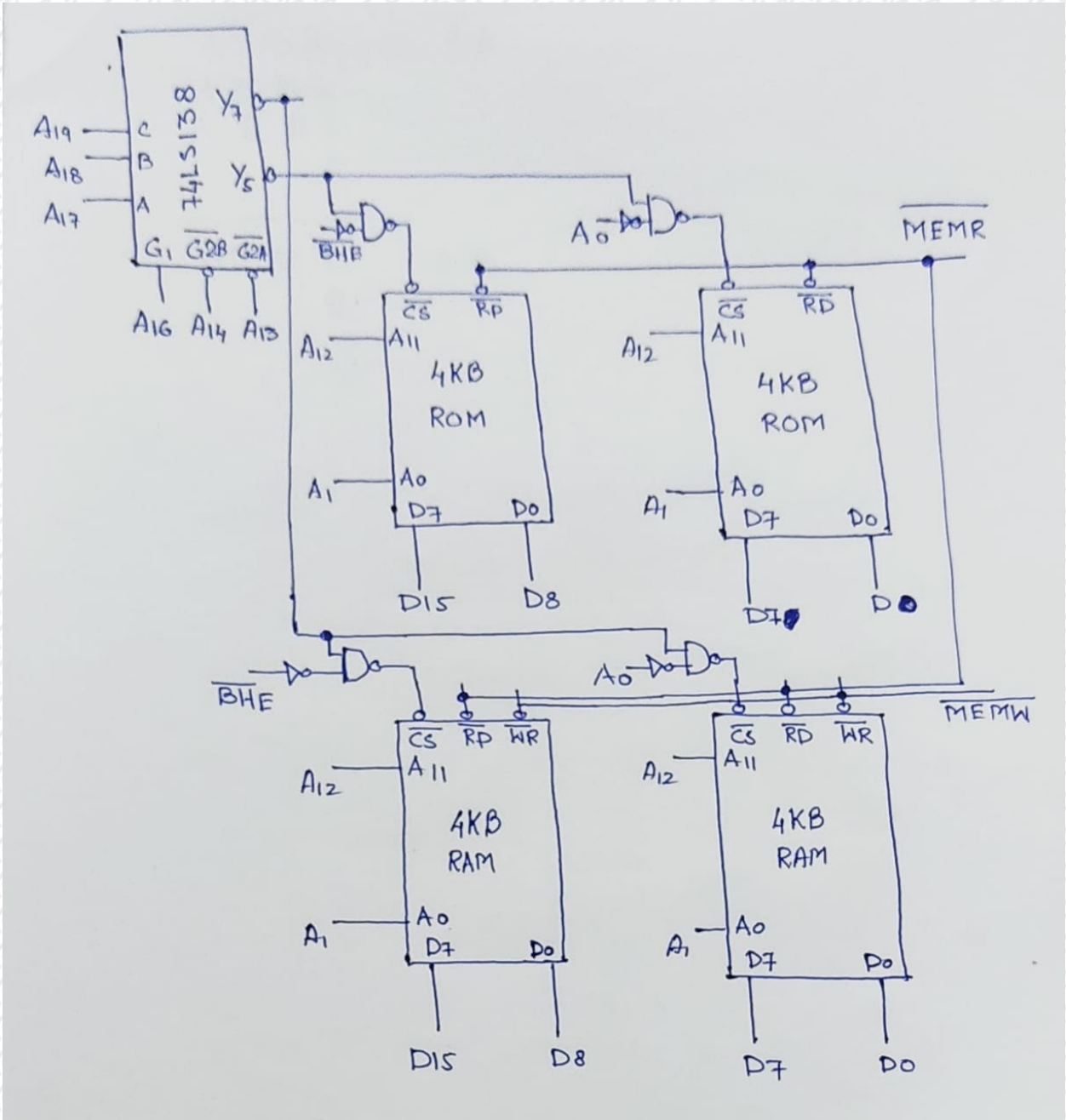
8. a) What operation will be performed by the Intel 8086 processor when it will execute ADD AL, 23H[BP][SI] instruction? Assume some arbitrary values for the contents of the internal registers involved in the operation. [3+2+10]
b) If (AL) = 23H and (BL) = 43H then what will be the new contents of these registers and state of CF after the execution of CMP AL,BL instruction. Explain your answer.
c) Two arrays of 8-bit numbers are present in memory at offsets 1012H and 3A97H respectively in the logical segment starting at 0A2B0H in memory. Length of both array is 20. Write a program for the 8086 processor which will add each element of the first array with the corresponding element of the second array and store the result in a third array in memory from offset A24BH. Assume that always the result of addition will be within 8-bits.

You can write the program using assembler directives or without using assembler directives as per your choice. If you are using assembler directives, then no need to include statements to declare or define data items for the program.

9. a) What is the purpose of the instruction register? [5+5+5]
   b) State the purpose of ALE/PROG signal.
   c) State the difference between program memory and data memory.

10. a) Write a program for 8051 to save the status of bits p1.2 and p1.3 on ram bit locations 6 and 7 respectively. [5+5+5]
    b) Two packed 2-digit BCD numbers are there in memory locations 30H and 31H of the internal RAM. Write a program for 8051 to add these numbers. Store the result at address 50H of the internal RAM and the carry (if any) at 51H.

11. a) Describe what happens on external bus signals when 8086 reads a word of data from an even address and odd address. [5+10]
    b) See the following figure showing interfacing of two 4 Kbytes ROM ICs and two 4 Kbytes RAM ICs with Intel 8086 processor. 74LS138 is a 3-8 decoder having three inputs A,B,C, seven active low outputs Y7-Y0, active high G1 enable signal and active low G2B', G2A' enable signals. Calculate all possible addresses of the resulting 8 Kbytes of ROM memory and 8 Kbytes of RAM memory present in the system.



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