Reg. No. : | E | N | G | G | T | R | E | E | . | C | O | M |

Question Paper Code : 40979

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2024.

Third Semester

Electronics and Communication Engineering

EC 3352 – DIGITAL SYSTEMS DESIGN

(Common to : Electronics and Telecommunication Engineering)

(Regulations 2021)

(Also common to PTEC 3352 for B.E. (Part-Time) for Electronics and Communication Engineering – Regulations 2023)

Time : Three hours | Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. How to represent a positive and negative sign in computers?
2. State Duality principle.
3. Differentiate multiplexer and de-multiplexer.
4. What is the need for parity checker?
5. Differentiate latches and flipflops?
6. What are ring counters? List the types of ring counters.
7. What is clock skew?
8. When does the race around condition occur in asynchronous sequential circuits?
9. Why RAM is called as Volatile memory?
10. List the classification of logic families based on category.

PART B — (5 × 13 = 65 marks)

11. (a) (i) Simplify the following Boolean function, $f(W,X,Y,Z) = WX'Y' + WY + W'YZ'$ using K-map and write the prime implicants and essential prime implicants. (7)

(ii) Convert the following Boolean expression into standard POS form:

$(A + B' + C)(B' + C + D')(A + B' + C + D')$. (6)

Or

(b) (i) Consider the boolean function $f(A,B,C,D) = \sum(0, 1, 2, 3, 5, 7, 8, 10, 12, 13, 15)$, simplify using Tabulation method and draw the logic diagram for the simplified boolean equation. (9)

(ii) Convert the SOP expression to an equivalent POS expression: (4)

$A'B'C' + A'BC' + A'BC + AB'C + ABC$

12. (a) (i) Design the combinational circuit for *BCD* to excess-3 code. (7)

(ii) Design a full adder using logic gates. Draw the truth table and explain its operation. (6)

Or

(b) (i) Design a 2-bit magnitude comparator and draw the logic diagram. (7)

(ii) Design a 3-bit priority encoder and draw the logic diagram. (6)

13. (a) (i) Design and implement a synchronous decade counter using T-flip flop and construct the timing diagram. (7)

(ii) Explain the operation of master-slave JK - flip flop with a suitable logic diagram. (6)

Or

(b) (i) Design a 4-bit binary counter with parallel load in detail. (7)

(ii) What are shift registers? Design a 4-bit universal shift register and explain the modes of operation. (6)

14. (a) Design a negative edge triggered asynchronous sequential circuits using T-FF. The circuit has two inputs, T(toggle) and C (Clock) and one output, Q. The output state is complemented if T = 1 and the clock changes from 1 to 0. Otherwise, under any other input condition, the output Q remains unchanged.

Or

(b) What are hazards? List and explain the types of hazards. Identify the ways in reducing hazards in sequential circuits?

15. (a) (i) Draw the TTL inverter circuit and explain the operation of TTL circuit. (6)

(ii) Design the PLA for the sum of products, $F = \Sigma\ (1, 6, 7, 8, 10, 14, 15)$. (7)

Or

(b) (i) Differentiate RAM and ROM. List and explain the various types of ROM. (7)

(ii) Implement the function $F1\ (A_1, A_2, A_3) = \Sigma(1, 2, 5, 7)$ and $F2\ (A_1, A_2, A_3, A_4) = \Sigma(3, 4, 8, 9, 10, 11, 15)$ using PAL. (6)

PART C — ($1 \times 15 = 15$ marks)

16. (a) Design an 8-bit arithmetic logic unit (ALU) which operates on two 8-bit input buses based on selection inputs. The ALU performs common arithmetic (addition and subtraction) and logic (AND, INV, XOR, and OR) functions.

Or

(b) (i) Design PAL for a combinational circuit that squares a 3 bit number. (7)

(ii) Using 8 to 1 multiplexer, realize the Boolean function $T = f(w, x, y, z) = \Sigma\ (0, 1, 2, 4, 5, 7, 8, 9, 12, 13)$. (8)