DIGITAL SYSTEMS DESIGN
(ECEN 2002)

Time Allotted: 3 hrs   **Full Marks : 70**

Figures out of the right margin indicate full marks.

*Candidates are required to answer Group A and
<u>any 5 (five)</u> from Group B to E, taking <u>at least one</u> from each group.*

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

    (i)   The binary number 10101 is equivalent to decimal number ....
              (a) 19   (b) 12   (c) 27   (d) 21.

    (ii)   The inputs of a NAND Gate are connected together. The resulting circuit is ....
              (a) OR Gate   (b) AND Gate
              (c) NOT Gate   (d) None of the above.

    (iii)   The only function of NOT Gate is to ....
              (a) Stop signal   (b) Invert input signal
              (c) Act as a Universal Gate   (d) None of the above.

    (iv)   A device which converts BCD to seven segments is called ....
              (a) Encoder   (b) Decoder
              (c) Multiplexer   (d) None of these.

    (v)   In the expression $A + BC$, the total number of Minterms will be ....
              (a) 2   (b) 3   (c) 4   (d) 5.

    (vi)   A Full Adder can be made out of ....
              (a) Two Half Adders
              (b) Two Half Adders and an OR Gate
              (c) Two Half Adders and a NOT Gate
              (d) Three Half Adders.

(vii) The basic storage element in a digital system is ....
    (a) Flip Flop   (b) Counter
    (c) Multiplexer   (d) Encoder.

(viii) Don't care conditions can be used for simplifying Boolean expressions in_____
    (a) Registers   (b) Terms
    (c) K-maps   (d) Latches

(ix) The speed of conversion is maximum in
    (a) Successive-Approximation A/D Converter
    (b) Parallel-Comparative A/D Converter
    (c) Counter Ramp A/D Converter
    (d) Dual-Slope A/D Converter.

(x) Which of the following is the fastest logic?
    (a)TTL   (b)ECL   (c)CMOS   (d)LSI

Group – B

2. (a) (i) State the distributive property of Boolean algebra.
    (ii) Prove that ABC + ABC' + AB'C + A'BC = AB + AC + BC

(b) (i)   Design XNOR Gate using NAND Gates only.
    (ii) Design a full subtractor circuit using logic gates.

5 + 7 = 12

3. (a) Draw the logic diagram of full adder and explain its operation.

(b) Using 8 to 1 multiplexer, realize the Boolean function
T = f(w, x, y, z) = Σ(0,1,2,4,5,7,8,9,12,13)

6 + 6 = 12

Group – C

4. (a) Implement a 2-Bit Comparator Circuit.

(b) Explain the BCD number and Implement a BCD Adder Circuit.

5 + 7 = 12

5. (a) Implement a 9-Bit Odd/Even Parity Generator-cum-Checker Circuit.

(b) Briefly describe the design of SRAM and DRAM.

4 + 8 = 12

Group – D

6. (a) (i) Distinguish between a combinational logic circuit and a sequential logic circuit.

(ii) Define Flip flop.

(b) Realize a JK flip flop using SR flip flop.

4 + 8 = 12

7. (a) Design a 4-Bit Synchronous Up and Down Counter.

(b) Design a Four-bit register using D Flip Flop.

6 + 6 = 12

Group – E

8. (a) Design a 4-Bit R-2R Ladder Type Digital-to-Analog Converter.

(b) Design a 4-Bit Flash Type Analog-to-Digital Converter.

6 + 6 = 12

9. (a) Explain the point/points of Superiority of CMOS Logic over other Logic Families.

(b) Design a PMOS NOR and a NAND gate.

4 + 8 = 12

Department & Section	Submission Link
IT	https://classroom.google.com/c/MTg0NTYwNzA0ODUy/a/Mjc0MDY4MTk1MzAy/details

Department & Section	Submission Link (Backlog)
IT	https://classroom.google.com/c/Mjg2Mjg3Njl1MDg2?cjc=ueqyxmy