Department of Computer Science and Engineering

UIET, CSJM University, Kanpur

Digital Logic Design (CSE-S202)

B.Tech. (CSE)

Semester: 2023 -24 (Odd Semester) **Year: IInd Year/ IIIrd, Semester**

Mid Semester Examination

Time: 1.5 H **Maximum Marks: 30**

All Questions are compulsory

Section A

(1 Mark each)

1. List out all neighbours of 29 in a 6 variable K-Map.
2. How many maximum number of don't care cases can be in a four variable Boolean function.
3. How many variables are in a minterm generated on pairing of 8 adjacent cells in 6 Variable K-Map.
4. What is the major limitation of K-Map?
5. Why we prefer K-Map instead of Boolean algebra to minimize a Boolean function?
6. Prove that OR is distributed over AND.
7. Express Boolean expression A+ B'C+ B'CD+ABC'D' in form of SOP (Σ).
8. Generate equivalent Boolean expression in POS form for Boolean expression given in previous question.
9. State and prove De Morgan's Theorem.

Section B

(3 Mark each)

10. Find prime implicants and essential prime implicants in Boolean function $f(A,B,C,D)= \Sigma(0,2,3,5,7,8,9,10,11,13,15)$
11. Draw circuit diagram of full subtractor using minimum number of NOR gates only.
12. Simplify Boolean expression f=ACD+A'B+D'

Section C

(6 Mark each)

13. Implement following Boolean functions using half adders.

    $F1=A \oplus B \oplus C$

    F2=A'BC+AB'C

    F3=ABC'+ (A'+B')C

    F4=ABC

14. Simplify the following five variable Boolean function using tabulation method.

    $F(A,B,C,D,E))= \Sigma(0,1,9,15,24,29,30)$

    $d(A,B,C,D,E) = \Sigma(8,11,31)$

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Section A
(1 Mark each)

1. $(32022132103)_4 = (?)_2$
2. $(A7692DF)_{16} = (?)_4$
3. $(51234)_6 + (31254)_6 = (?)_6$
4. $(5342)_6 - (4543)_6 = (?)_6$
5. If $(5436)_9 = (A02)_r$ where value of A is 10, find value of base r.
6. Consider the equation $(43)_x = (y3)_8$ where x and y are unknown. Find possible values of unknowns.
7. The 16 bits 2's complement representation of an integer is 1111111111110101, find its value in decimal.
8. Find the smallest and largest integer that can be represented by a 10-bit number in 2's complement form.
9. Give the name of logic gate(s) which is/are commutative but not associative.

Section B
(3 Mark each)

10. Solve $(345)_7 - (112)_7$ using r's complement subtraction method, show all the steps.
11. What will be the result of -25000-20000, if numbers are represented in 16 bits using 2's complement?
12. Implement Boolean function f=a'b + c'd' + ac using minimum number of NOR gates.

Section C
(6 Mark each)

13. Let x and y are two successive digits in base r number system such that,

    $(xy)_r = (101)_6$ & $(yx)_r = (112)_6$, find the value of x,y and r?

14. Draw neat and clean internal diagram of AND gate using any logic family and explain its working.

Department of Computer Science and Engineering

University Institute of Engineering and Technology, CSJM University, Kanpur

Digital Electronics (CSE-S202)

B.Tech (CSE)

Semester: III[rd] Year: 2[nd]

End Semester Examination

Time: 3 Hour M.M.: 50

All Questions are compulsory

Section A

Note: In this section, each question carries 1 mark. **(1X10)**

1. How many minimum bits are required to assign a binary sequence to each and every student of your class?
2. What is duality principle in Boolean algebra?
3. List the numbers from 8 to 28 in base 12.
4. Determine the base in which expression 24+17=40 is correct.
5. If f=wx+yz, show that f + f' = 1.
6. Draw circuit of JK flip flop using NAND gates.
7. If A and B are two 8 bit binary numbers, write Boolean expression for A>B.
8. How many and which size binary parallel adders are required to implement a 4 bit binary multiplier?
9. A Boolean expression in SOP form is f=A'B'C'+A'BC'+AB'C', write the equivalent expression in POS form.
10. Write Boolean expression for C_3 in the circuit of binary lookahead adder.

Section B

Note: In this section, each question carries 4 marks. **(4X5)**

11. Discuss some circuits in which truth table-based approach is not suitable for its implementation, implement circuit of 6-bit binary magnitude comparator.
12. Implement circuit of 4-bit binary multiplier and show the output in circuit on the multiplication of 7 with 8.
13. What is key problem in the implementation of parallel adder using half/full adders? Implement circuit of 4-bit binary look ahead adder.
14. Implement equivalent circuit of figure given on next page (Fig1) using only one 4X1 multiplexer and use a & b as selection lines.
15. Implement equivalent circuit of figure given on next page (Fig1) using 2X4 decoders.

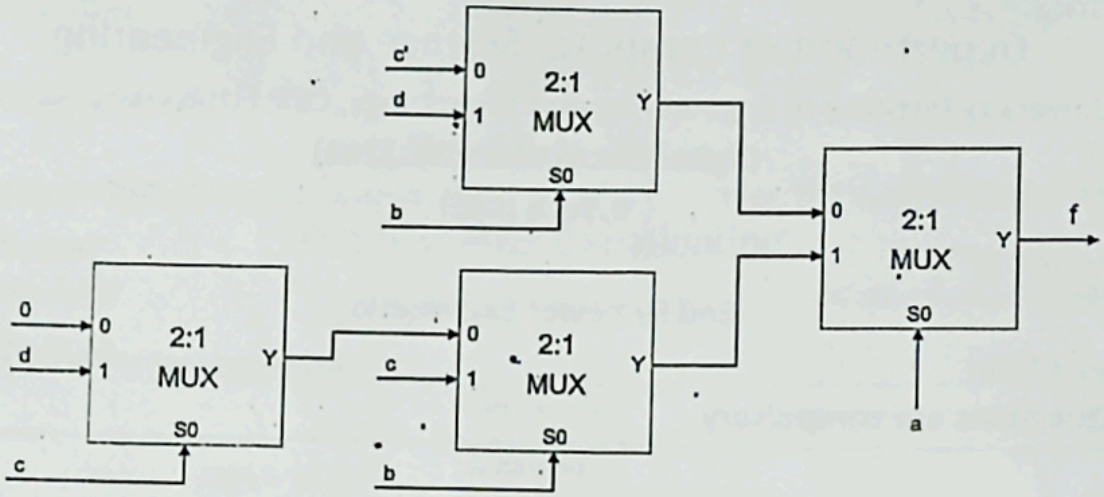

Fig1

Section C

Note: In this section, each question carries 10 marks. **(2X10)**

16a. What do you mean by counter? Implement circuit of four bit up counter using JK flip flops.

16b. What do you mean by registers? Discuss different type of registers used in computer with proper explanation.

17a. Find output (Q_2,Q_1,Q_0) of following circuit on next six clock pulses.

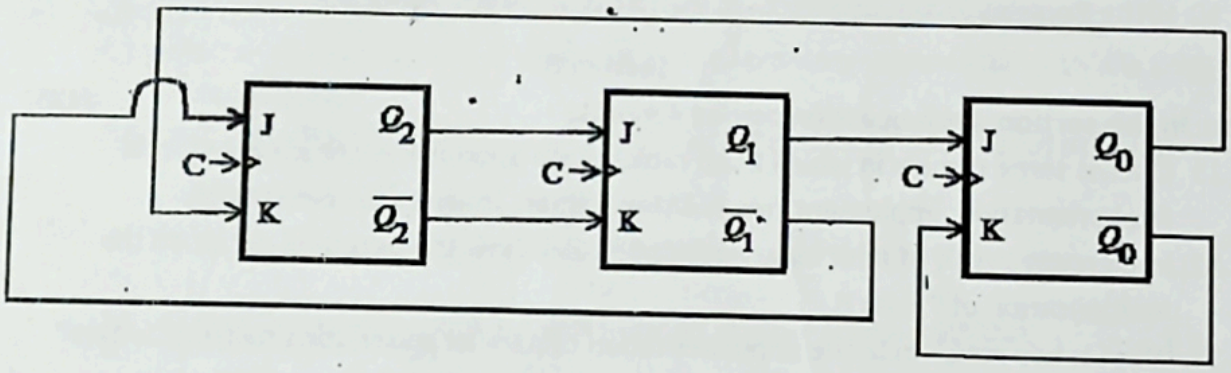

Fig2

17b. Let A,B,C,D are BCD digits, Draw circuit to add AB+CD where AB are two digit BCD number formed by combining A & B, similarly CD is formed by combining C & D. For example (23+49).