Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS/B.Tech (EEE/ICE)/PWE/EE(O)/SEM-4/EC-402/2010

2010

DIGITAL ELECTRONICS & INTEGRATED CIRCUITS

Time Allotted : 3 Hours *Full Marks* : 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for any *ten* of the following : $10 \times 1 = 10$

i) The binary equivalent number of $(25{\cdot}75)_{10}$ is

a) 11001·110 b) 11001·011

c) 11001·111 d) 11001·000.

ii) The hexadecimal equivalent number of $(348{\cdot}35)_{10}$ is

a) 15C.688 b) 15C.599

c) 15B.599 d) 15A.599.

iii) Which one of the following is a weighted code ?

a) 2421 b) Excess-3

c) Grayd) None of these.

iv) The characteristic equation of T flip-flop is given by

a) $Q+ = T'Q + TQ'$ b) $Q+ = TQ' + T'Q$

c) $Q+ = TQ'$ d) $Q+ = TQ$.

v) Daul form of $A\ (B + C)$ is

a) $A + BC$ b) $AB + AC$

c) $AB + C$ d) none of these.

vi) A latch is a

a) 1-bit memory cell b) 2-bit memory cell

c) 3-bit memory cell d) none of these.

vii) The functional difference between *S-R* nad *J-K* flip-flop is that

a) *J-K* flip-flop has a feedback path

b) *J-K* flip-flop does not have an external clock pulse

c) *J-K* flip-flop is faster than *S-R* flip-flop

d) *J-K* flip-flop can accept both inputs at 1.

viii) The output of a logic gate is 1 when all its inputs are at logic zero. The gate is either

a) a NAND or an EX-OR

b) an OR or an EX-OR

c) an AND or an EX-OR

d) a NOR or an EX-NOR.

ix) Gray code of 1011 (binary) is

a) 0101 b) 1101

c) 1110 d) 1011.

x) An example of reflected code is

a) BCD b) ASCII

c) Gray d) Hamming code.

xi) If a 10 MHz signal is applied to a MOD-5 counter followed by a MOD-8 counter then the o/p frequency will be

a) 10 kHz b) 2·5 kHz

c) 5 kHz d) 250 kHz.

xii) If $(212)_x = (23)_{10}$, where x is base ($+ve$ integer) then the value of x is

a) 2 b) 3

c) 4 d) 5.

xiii) Full form of FPGA is

a) Full Programmable Gated Array

b) Field Programmable Gated Array

c) Full Peripheral Gated Array

d) Field Peripheral Gated Array.

xiv) The resolution of 8 bit A/d converter is

a) 0·62% b) 0·38%

c) 0·39% d) 1·25%.

xv) If the following quadratic expression is solved it results the decimal roots 8, 5. $X^2 - (10)_r X + (31)_r = 0$.

What is the value of r ?

a) 10 b) 12

c) 13 d) 8.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. $3 \times 5 = 15$

2. a) Consider the following logic circuit whose inputs are $f_1(x, y, z)$, $f_2(x, y, z)$ & $f_3(x, y, z)$ and the output is $f(x, y, z)$ given that $f_1(x, y, z) = \Sigma(0, 1, 3, 5)$, $f_2(x, y, z) = \Sigma(6, 7)$ and $f(x, y, z) = \Sigma(1, 4, 5)$. What is $f_3(x, y, z)$?

Dia.

b) What will happen when a bit-string is X-ORed with itself n times ?

3. Design a *J-K F/F* using a *D F/F*, a 2 : 1 MUX and one inverter.

4. Design a 2-input NAND gate using MOS inverter.

5. Minimize the following expression using *K*-map and realize the simplified function using NOR gates only :

$F(A, B, C, D) = \Pi m(0, 1, 3, 5, 8, 10, 15). \Pi d(11, 13, 14)$.

6. Implement the following function using 4 : 1 MUX only :

$F = \Sigma m(0, 2, 3, 6, 8, 9, 12, 14)$.

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. 3 × 15 = 45

7. a) Implement a 16 : 1 MUX using 4 : 1 MUX only. Design 8 : 1 multiplexer using 3 : 8 decoder.

   b) Define the following terms :

      i) Noise margin

      ii) Fan-in

      iii) Fan-out

      iv) Power dissipation

      v) Floating inputs. (6 + 4) + 5

8. a) With the help of necessary circuit diagram explain the operation of dual slope ADC.

   b) A 4-bit binary ladder D/A converter with R = 10 kΩ uses a reference of 5V. Find

      i) the ideal scale factor in V/step

      ii) the analog output corresponding to the binary input 0110

      iii) resolution in %

      iv) full sale output

      v) the maximum deviation in volts from the best straight line in order to meet standard linearity.

      9 + 6

9. a) Design a sequential circuit that implements the following state diagram. Use all *D*-type *F*/*F* for the design.

dia.

b) Draw and explain the 4-bit bidirectional shift register using mode control (*M*), when *M* is logic zero then left shift and right shift for *M* is logic one. 9 + 6

10. a) Design a BCD adder using 4-bit binary full adder units and a few NAND gates.

b) Design a BCD to 7 segment decoder using basic gates.

5 + 10

11. Write short notes on any *three* of the following : 3 × 5

a) Priority encoder

b) Even parity generator and checker

c) PLD

d) Johnson counter

e) Parallel In Serial Out (PISO) shift register.