Sub Code: BECT303/BECT304 **ROLL NO……..……..**

ODD SEMESTER EXAMINATION, 2024 – 25

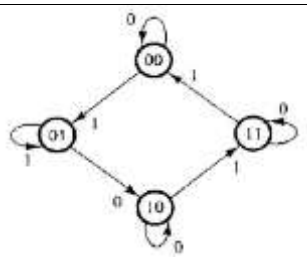
2nd Year (III Sem) B.Tech.: E&CE/CS&E/IT

NAME OF SUBJECT: Digital Electronics

Duration: 3:00 hrs **Max Marks: 100**

Note: - Attempt all questions. All Questions carry equal marks. In case of any ambiguity or missing data, the same may be assumed and state the assumption made in the answer.

Q 1.	Answer any two parts of the following.	(10x2= 20)
	a) Convert the following numbers with the indicated bases to binary	
	(i) $(41.6875)_{10} = (\quad)_2$	(5 marks)
	(ii) $(306.D)_{16} = (\quad)_2$	(5 marks)
	b) Simplify the following expression using Quine-Mc Cluskey Method.	
	$F(A,B,C,D) = \sum m(1,4,6,7,8,9,10,11,15)$	(10 marks)
	c) What are Error detection & correcting codes? Explain their significance in sending a signal. What are Parity bits and how are they used to detect error in codes?	(10 marks)
Q 2.	Answer any two parts of the following.	(10x2= 20)
	a) (i) What is a Priority Encoder? Describe its function using Truth Table and Block diagram.	(5 marks)
	(ii) Write down the Truth Table and logic design of a 1x8 Multiplexer.	(5 marks)
	b) Explain the working of a Full Adder using the Truth Table and derive the simplified SoP expression for the sum and carry of a Full Adder and draw the logic diagram.	(10 marks)
	c) Design a 4-bit magnitude comparator circuit. Explain the functioning and draw the logic diagram for the same.	(10 marks)
Q 3.	Answer any two parts of the following.	(10x2= 20)
	a) (i) Write down the truth table, excitation table, characteristic equation and logic diagram of SR Flip Flop.	(5 marks)
	(ii) List down the major limitations of an asynchronous/ripple counter.	(5 marks)
	b) What is race around condition in a JK Flip Flop? Explain the working of a Master-Slave Flip Flop with diagram.	(10 marks)
	c) Design a Mod-5 synchronous UP counter using a JK Flip Flop.	(10 marks)
Q 4.	Answer any two parts of the following.	(10x2= 20)
	a) (i) State and discuss the difference between Mealy and Moore machines?	(5 marks)
	(ii) Describe the operation of TTL logic circuit working as NAND gate.	(5 marks)
	b) Compare TTL and CMOS logic families on the basis of following: i) Propagation delay ii) Power dissipation iii) Fan-out iv) Basic gate	(10 marks)
	c) Design a sequential circuit using T Flip Flop for the following state diagram.	(10 marks)

	
Q 5.	Answer any two parts of the following. (10x2= 20) a) Compare the following. (i) Volatile with Non-Volatile memory. (5 marks) (ii) SRAM with DRAM memory. (5 marks) b) Explain the different types of Hazards that exist in asynchronous sequential circuits and discuss the techniques to determine hazards in combinational circuits. (10 marks) c) Explain the structure of PAL and PLA. How a combinational logic function is implemented in PAL and PLA? Explain with an example for each. (10 marks)

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