ABV-INDIAN INSTITUTE OF INFORMATION TECHNOLOGY & MANAGEMENT GWALIOR

Batch B (First Year)

Digital Electronics

Minor-1 Exam

Semester - II

Duration: 2 hour

Max. Marks: 40

Date: 26/02/2024
Time: 10AM-12Noon

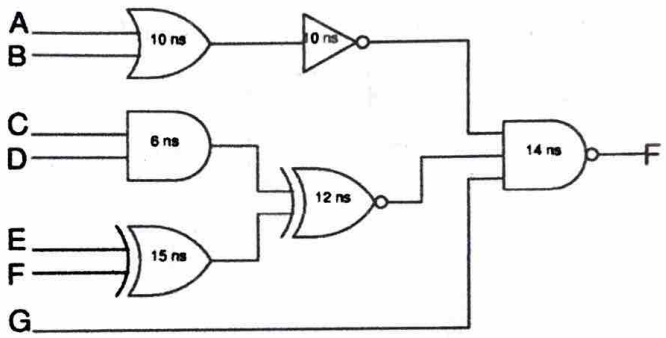
Important Instructions:

- This is a closed book, closed notes examination.
- This question paper comprises total 14 questions printed on three pages.
- **All the questions are compulsory and attempt all questions in sequence.**
- Maximum marks that can be obtained for a particular question are indicated in the brackets [ ] on the extreme right of the corresponding question

---

Q1. If X = 1 in the logic equation $[X + Z\{\bar{Y} + (\bar{Z} + X\bar{Y})\}]\{\bar{X} + \bar{Z}(X + Y)\} = 1$ then find the value of Z. **[2]**

Q2. In the digital circuit given below, delay of each gate is shown. What is the minimum time required for the output to reflect any transitions at the input? **[2]**



Q3. The following Boolean expression BE + B'DE' is a simplified version of the expression A'BE + BCDE + BC'D'E + A'B'DE' + B'C'DE'. Are there any don't care conditions? If so, what are they? **[2]**

Q4. Implement the following Boolean expression by using switches. **[2]**

Y= A.B. (C+D+E) F'

Q5. Perform the following operations using 2's complement and find there is an overflow or not. **[2]**

(a) -16-13

(b) 5+4

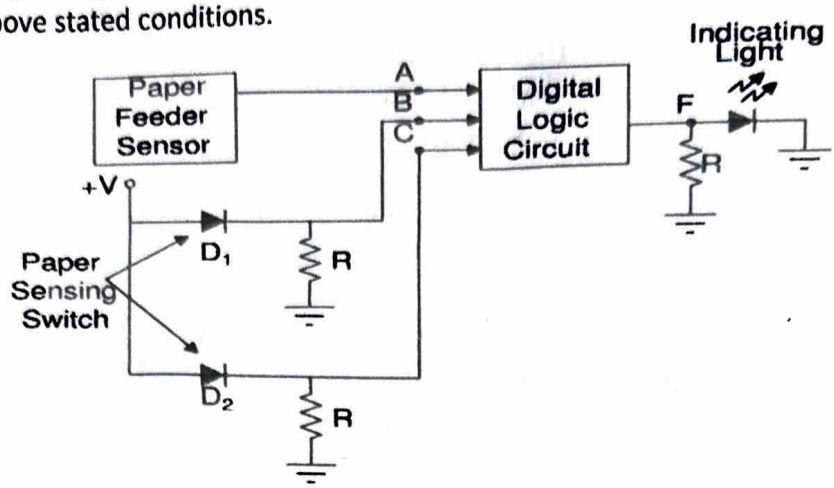
Q6. Implement Ex-NOR gate using minimum number of NOR gates. **[2]**

Q7. Refer to figure shown below. In a simple copier machine, a stop signal 'F' is to be generated to stop the machine operation and energize an indicator light whenever either of the following conditions exists:

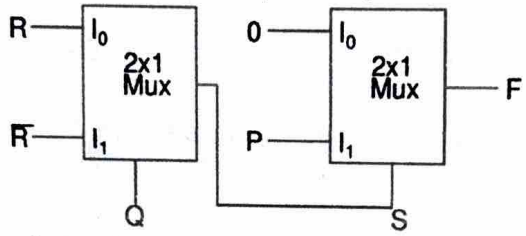
a. There is no paper in paper feeder tray or
b. The two micro switches in the paper path are simultaneously activated, indicating a paper jam.

The presence of paper in the paper feeder tray is indicated by a high at logic signal 'A' and each of the micro switches produce a logic signal (B and C) that goes high whenever paper is passing over the switch to activate it.

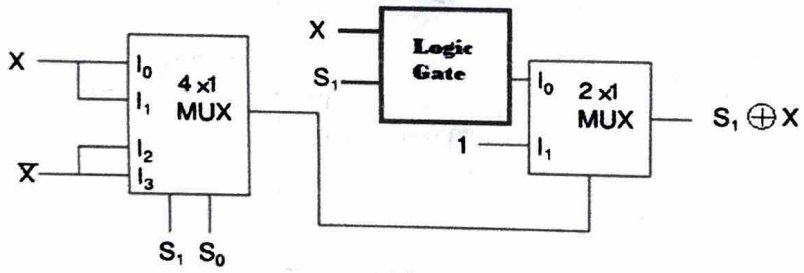
Design the digital logic circuit block shown in the figure below to produce a high at output signal (F) for the above stated conditions. [2]



Q 8. For the circuit given below, give the output expression, F. [2]



Q 9. The circuit shown in figure below has a missing 'logic gate', Identify this logic gate? [2]

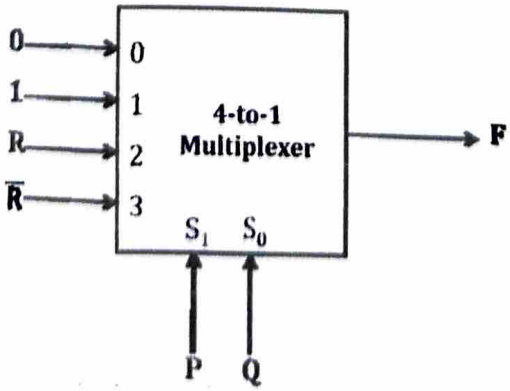


Q 10. $\sqrt{41} = 5$ is correct in some given number system. What is the base of this number system? [2]

Q 11. In a carry look ahead adder if the propagation delay of carry generator logic is 10 ns and propagation delay of each full adder is 20 ns. Then total propagation delay required to generate sum (S3) of 4-bit adder is? [2]

Q 12. If 2's compliment representation of a 12-bit number (with one sign bit and 11 magnitude bits) is FBF, then the magnitude of the number in decimal system should be: [2]

Q 13. Consider a 4-to-1 multiplexer with two select lines S1 and S0, given below. Find the minimal sum-of-products form of the Boolean expression for the output F of the multiplexer. [2]



Q 14. How many BCD code bits and how many straight binary bits would be required to represent the decimal number 643? **[2]**

Q 15. Find the simplified expression, Implicates, Prime Implicates, d1 cells, and Essential Prime Implicates of the following function. **[4]**

$\prod M$ (0,1,3,7,8,14)

Q 16. A 4-bit carry look ahead adder, which adds two 4-bit numbers, is designed using AND, OR, NOT, NAND, NOR gates only. Assuming that all the inputs are available in both complemented and uncomplemented forms and the delay of each gate is one time unit, what is the overall propagation delay of the adder (explain in detail)? Assume that the carry network has been implemented using two-level AND-OR logic. **[4]**

Q 17. Consider the Karnaugh map given below, where X represents "don't care" and blank represents 0.

dc \ *ba*	00	01	11	10
00		X	X	
01	1			X
11	1			1
10		X	X	

Assume for all inputs (a, c, d) the respective complements (a', b', c', d') are also available. The above logic is implemented 2-input NOR gates only. Fin the minimum number of gates required.

[4]