9. (a) What is virtual memory? Why is it called virtual? What are the advantages of it? 4

(b) What is locality of reference? Explain the concept of cache memory with it. 3

(c) What are the advantages of split cache memory? 2

(d) Given the following, determine the size of sub-fields in the address for several mapping schemes of cache memory. 6

Main memory size: 512 MB,

Cache memory size: 1 MB,

Address space of processor: 512 MB,

Block size: 128 B, 8 blocks in cache set.

10.(a) Draw the block diagram of a typical vector processor. 4

(b) What are the differences between a scalar instruction and a vector instruction? 3

(c) What do you mean by vector stride? 2

(d) State and explain different types of vector instructions. 6

11. Write short notes on any *three* of the following: 3×5

(a) Array processor

(b) Cluster computer

(c) Data flow computer

(d) Systolic architecture

(e) ILP

IT-502

COMPUTER ARCHITECTURE

Time Allotted: 3 Hours Full Marks: 70

The questions are of equal value.
The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable.

GROUP A
(Multiple Choice Type Questions)

1. Answer *all* questions. 10×1 = 10

(i) ENIAC stands for

(A) electronic numerical integrator and circulation
(B) electronic numerical integrator and calculator
(C) electronic numerical integrator and calculation
(D) electronic number integrator and calculator

(ii) Array processors are put under these categories

(A) SISD (B) SIMD
(C) MISD (D) MIMD

(iii) An architecture in which data is sent in a rhythmic fashion is known as

(A) systolic array (B) linear array
(C) chordal ring (D) none of these

(iv) An n-dimensional hypercube has

(A) n^n nodes (B) n nodes
(C) 2^n nodes (D) $2n$ nodes

(v) RISC has

(A) unified cache (B) I and D cache
(C) L_1 cache (D) none of these

(vi) In which of the following policies, Belady's anomaly occurs?

(A) FIFO (B) LRU
(C) LFU (D) NRU

(vii) When block size equals the entire cache size, the hit ratio becomes

(A) 1 (B) 2
(C) 0 (D) 4

(viii) If clock t = 20 ns, efficiency = 1 and MAL = 3, what will be the throughput of the pipeline?

(A) 10.23 MIPS (B) 12.56 MIPS
(C) 14.50 MIPS (D) 16.67 MIPS

(ix) The distance between the vector elements is known as

(A) stride (B) hamming distance
(C) zero distance (D) euclidean distance

(x) A mesh is an example of

(A) dynamic network (B) static network
(C) switch (D) omega network

GROUP B
(Short Answer Type Questions)

Answer any *three* questions. 3×5 = 15

2. State and explain Flynn's classification of computer architecture. 5

3. Show that the maximum speed-up of a pipeline is equal to its number of stages. 5

4. Discuss about the performance of VLIW processor. 5

5. What is cache coherence problem? What are several protocols to solve this problem? 1+4

6. Explain various types of shared memory multiprocessor architecture. 5

GROUP C
(Long Answer Type Questions)

Answer any *three* questions. 3×15 = 45

7. (a) What is the difference between computer organization and computer architecture? 2

(b) What is meant by pipeline architecture? How does it improve the speed of execution of a processor? 5

(c) Consider the following reservation table for a 4-stage pipeline with a clock cycle t = 20 ns. 8

1	2	3	4	5	6	
×					×	S1
	×		×			S2
		×				S3
			×	×		S4

(i) What are the forbidden latencies and the initial collision vector?
(ii) Draw the state transition diagram for scheduling the pipeline.
(iii) Determine the MAL associated with the shortest greedy cycle.
(iv) Determine the pipeline throughout corresponding to the MAL and given t.
(v) Determine the lower bound on the MAL for this pipeline.

8. (a) What is the arithmetic pipeline? Describe with an example. 4

(b) What do you mean by pipeline hazards? What is a data hazard? What are several types of data hazards and the solutions of these? 7

(c) What is register tagging or data forwarding? Describe several methods of it. 4