DCS LAB- MAJOR (SET-2)

Name:

Roll No:

1. Which one of the following statements is not correct?

(A) An 8 input MUX can be used to implement any 4 variable function.

(B) A 3 line to 8 line DEMUX can be used to implement any 4 variable function.

(C) A 64 input MUX can be built using nine 8 input MUXs .

(D) A 6 line to 64 line DEMUX can be built using nine 3 line to 8 line DEMUXs.

2. What is the number of EXOR gate IC required to implement 4 bit binary to gray conversion?

(A) 1 (B) 2 (C) 3 (D) 4

3. Consider the following statements regarding registers and latches :

1. Registers are temporary storage devices, whereas latches are not

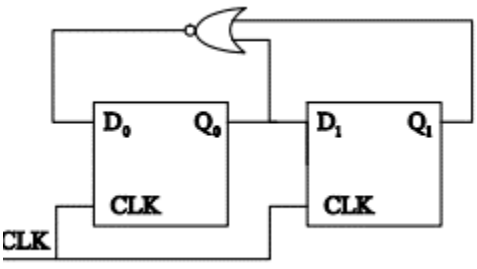
2. A latch employs cross-coupled feedback connections.

3. A register stores a binary word, whereas a latch does not.

The correct statement(s) is/are

(A) 1 only (B) 2 only (C) 1 and 3 (D) 2 and 3

4. For the circuit shown below the counter state (Q1 Q0) follows the sequence



(A) 00,01,10,11,00 ..... (B) 00,01,10,00,01 .....

(C) 00,01,11,00,01 ..... (D) 00,10,11,00,10 .....

5. The number of 1's in 8-bits representation of - 127 in 2's complement form is m and that in 1's complement form is n. What is the value of m : n ?

(A) 2 : 1 (B) 1 : 2 (C) 3 : 1 (D) 1 : 1

6.What is the IC number of EXOR gate used in lab ?

(A) 7432 (B) 7408 (C) 7485 (D) 7486

7. The present output Qn of an edge triggered JK flip-flop is logic 0. If J = 1, then Qn+1

(A) cannot be determined (B) will be logic 0 (C) will be logic 1 (D) will race around

8. A master slave configuration consists of two identical flip-flops connected in such a way that the output of the master is input to the slave. Which one of the following is correct?

(A) Master is level triggered and slave is edge triggered

(B) Master is edge triggered and slave is level triggered

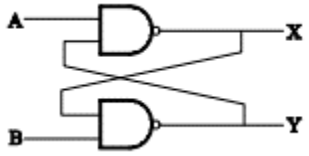
(C) Master is positive edge triggered and slave is negative edge triggered

(D) Master is negative edge triggered and salve is positive edge triggered

9. The output Y of a 2-bit comparator is logic 1 whenever the 2-bit input A is greater than the 2-bit input B. The number of combinations for which the output is logic 1, is

A. 4 B. 6 C. 8 D. 10

10. In below figure, A = 1 and B = 1. The input B is now replaced by a sequence 101010 ..... the outputs x and y will be



(A) fixed at 0 and 1, respectively (B) x = 1010 ------- while y = 0101 ----

(C) x = 1010 ------- and y = 1010 ------- (D) fixed at 1 and 0, respectively

11. Convert JK to T FF?

12. A full-adder can be implemented with half-adders AND OR gates. A 4-bit parallel full adder without any initial carry requires

(a) 8 half-adders 4-or gates

(b) 8 half-adders 3-or gates

(c) 7 half-adders 4-or gates

(d) 7 half-adders 3-or gates

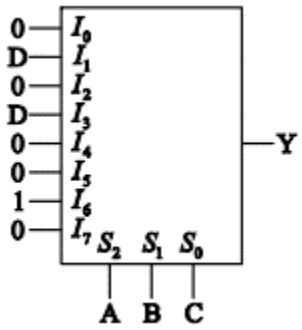
13. What is the voltage supply that is normally used to power IC's in lab?

(A) 3.8v (B) 5v (C) 7v (D)12v

14. The minimum number of 2-input NAND gates required to implement a 2-input XOR gate is :

(A) 4 (B) 5 (C) 6 (D) 7

15. An 8-to-1 multiplexer is used to implement a logical function Y as shown in the figure. The output Y is given by



(A) $Y = A\overline{B}C + A\overline{C}D$

(B) $Y = \overline{A}BC + A\overline{B}D$

(C) $Y = AB\overline{C} + \overline{A}CD$

(D) $Y = \overline{A}\overline{B}D + A\overline{B}C$