Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS/B.TECH (EEE/ICE/PWE) (OLD)/SEM-4/EC-402/2012

2012

DIGITAL ELECTRONICS AND INTEGRATED CIRCUITS

Time Allotted : 3 Hours *Full Marks* : 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for the following :

$10 \times 1 = 10$

i) The binary equivalent number of $(25.75)_{10}$ is

a) 11001.110 b) 11001.011

c) 11001.111 d) 11001.000.

ii) The hexadecimal equivalent number of $(348.35)_{10}$ is

a) 15C.688 b) 15C.599

c) 15B.599 d) 15A.599.

iii) The decimal equivalent number of $(1101.11)_{2}$ is

a) 13.25 b) 13.75

c) 13.5 d) 13.00

iv) The decimal equivalent number of $(427.35)_8$ is

a) 279.456732 b) 279.4567789

c) 279.432167 d) 279.453125

v) The decimal equivalent number of $(6ABC.2A)_{16}$ is

a) 27324.125 b) 27325.678

c) 27324.164 d) 27324.654.

vi) The binary equivalent number of $(155.52)_8$ is

a) 001101101.101010 b) 001101101.101101

c) 001101101.110000 d) 001101101.110011

vii) The binary equivalent number of $(1CEF.2B)_{16}$ is

a) 1110011101111.00101011

b) 1110011101111.00111011

c) 1110011101111.1101011

d) 1110011101111.1001001

viii) The hexadecimal equivalent number of $(7324.456)_8$ is

a) ED4.87 b) ED4.47

c) ED4.57 d) ED4.97.

ix) The result of subtraction of the binary bits 11101 – 1101 is

a) 00001 b) 10000

c) 10001 d) 10011.

x) The result of addition of the binary bits 1101 + 11101 is

a) 00001 b) 10000

c) 10001 d) 10011.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. 3 × 5 = 15

2. Simplify the Boolean function
$F(A, B, C, D) = \sum_m (1, 3, 7, 11, 15) + \sum_d (0, 2, 5)$ using *K*-map.
3. What are meant by SOP and POS from Boolean expression ? Give examples.
4. Design a 4 bit binary adder / subtractor using IC 7483.
5. Design a full adder circuit using two half adder circuits.
6. Design a binary full adder using a few 4 : 1 MUX and other necessary logic gates.

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. 3 × 15 = 45

7. a) Define universal gate. Explain how the basic gates can be realized using NAND gates.
   b) State and explain De Morgan's theorems which convert a sum into a product form and vice versa.
   c) If $A'B + CD' = 0$, then prove that
   $AB + C'(A' + D') = AB + BD + B'D' + A'C'D$.
   6 + 4 + 5
8. a) Design 5 : 32 decoder using one 2 : 4 and four 3 : 8 decoder ICs.
   b) Design the logic circuitry for the *A* and *C* output of a *BCD*-to-7 segment decoder with active low outputs.
   c) Implement the following function using IC 74138 and gates :
   $F(A, B, C) = \prod (0, 1, 3, 7)$ 5 + 6 + 4

9. a) Explain the function of basic flip-flop. Draw and explain the logic diagram of Master slave *D* flip-flop using NAND gates.

   b) Show how SR flip-flop can be converted into a *D* flip-flop.

   c) Give the difference between edge triggering and level triggering. 5 + 6 + 4

10. a) What is modulus counter ? Design MOD 10 synchronous counter using JK flip-flop and implement it.

   b) Design a 4-bit unit distance Up-Down counter.

   c) Explain the working of serial-in-parallel-out shift register with logic diagram and waveforms. 5 + 5 + 5

11. a) Describe the operation of successive approximation type analog to digital converter. How many clock pulses are required in worst case for each conversion cycle of an 8-bit SAR type analog to digital converter. Define quantizing error for an analog to digital converter.

   b) Draw a neat diagram for a R-2R ladder type digital to analog converter and explain its operation.

   c) Explain the working of a shift register. 6 + 5 + 4

12. Write short notes on any *three* from the following : 3 × 5

   a) EEPROM

   b) Odd parity generator

   c) Quine McCluskey method

   d) Johnson counter

   e) Serial-in-parallel-out shift register.