VIT

Vellore Institute of Technology

(Deemed to be University under section 3 of UGC Act, 1956)

SCHOOL OF ELECTRONICS ENGINEERING

CAT- II

Course: ECE2003Digital Logic Design — B.Tech(ECE)

Time: 90 mins — Slot: B2 — Max.Marks:50

Answer **ALL** Questions

1. Write a Verilog program in Behavioral modeling for a ALU which does the following operation: [10 marks]

S2	S1	S0	Output
0	0	0	A + B
0	0	1	A x B
0	1	0	$A + \overline{B} + 1$
0	1	1	A + A
1	0	0	A – 1
1	0	1	A
1	1	0	$A + B^2$
1	1	1	A – B

2. a.Design a 4x2 Priority encoder with the priority order as 3,1,2,0. [5 marks]

b.Design a 3-bit comparator circuit using logic gates. [5 marks]

3. A combinational circuit has three inputs, A, B, and C, and three outputs, W, X, and Y. When the binary input is 0, 1, 2, or 3, the binary output is one greater than the input. When the binary input is 4, 5, 6, or 7 the output is two less than the input. Design "W" using 2x4 Decoder, design "X" using 3x8 Decoder and design "Y" using 1:8 De-mux. [10 marks]

4. Design a 8 x 3 Encoder using 4:1 MUX. [10 marks]

5. Write a Verilog program for the following block diagram. Full Adder (FA) should be in dataflow modeling and 4:1 MUX should be in structural modeling. [10 marks]