Final Assessment Test – April 2019

VIT
Vellore Institute of Technology

Course: CSE1003 - Digital Logic and Design
Class NBR(s): 2389/2391/2392/2395/2397/2400/2401/ 2402 / 2406 / 2407 / 2408 / 2409
Slot: B2+TB2
Time: Three Hours
Max. Marks: 100

Answer ALL Questions
(10 X 10 = 100 Marks)

1. i. Convert to base 6: 3BA.2514 [2]
   ii. The 16-bit 2's complement representation of an integer $(1111\ 1111\ 1111\ 0101)_2$. What is its decimal representation? [2]
   iii. Convert $(12)_{10}$ to Gray code [2]
   iv. Show how a 16 bit computer using a two's complement number system would perform the operation : $-(2925)_{10} - (16850)_{10} = (?)_{10}$ [2]
   v. Find the 10's complement of the number $(935)_{11}$ [2]

2. a) Concisely describe the following problem using a Boolean equation. We want to fire a football coach (by setting F = 1) under at least one of two conditions: [5]
   a. if he is mean (represented by M = 1)
   b. if he is not mean but has a losing season (represented by L = 1).
   b) Solve the following: [5]
   a. Draw a circuit using AND, OR and NOT gates for the following equation:
   F(a,b,c) = (ab) (b' + c)
   b. Convert the circuit using only NAND gates (INV are ok)
   c. Convert the circuit using only NOR gates (INV are ok)

3. Given F(a, b, c, d) = ∑m(0, 3, 4, 5, 10, 14) + ∑d(1, 7):
   a. Derive a minimal expression for F [5]
   b. implement the function using a minimal network of 2:1 multiplexers and minimum number of inverters. Do not use any other logic gates. [5]

4. Simplify the logic circuit shown in Figure:1

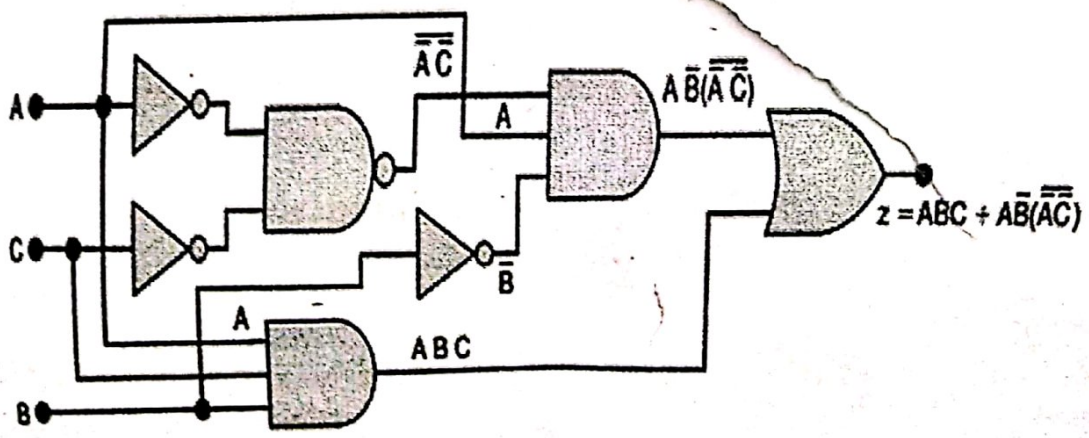


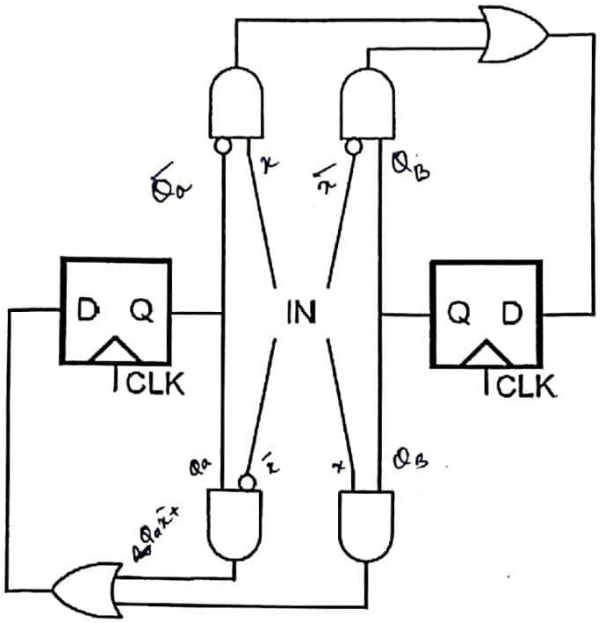
Figure:1

5. a) Design a circuit which reduces the propagation delay time in the binary parallel adder. [5]
   b) Design a 3-bit magnitude comparator, Which compares two numbers A and B having of three bits each and find out A > B, A < B and A = B. [5]

Possession of Mobile Phone in the exam hall even in switched off condition is a malpractice.

Scanned by CamScanner

6. Draw a state transition diagram for the circuit below. Succinctly describe what the circuit does. Signal IN is an input to the circuit.

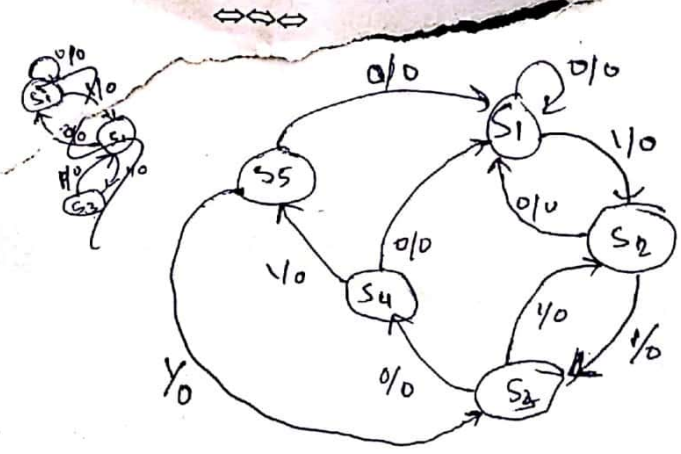


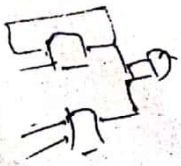
7. Design 11011 Sequence Detector using D flip flop. Assume overlap is allowed.

8. Draw the Logic Diagram of Universal Shift Register Using D flip-flop and Multiplexer. Mention the role of S0 and S1 pins and explain the four possible modes of transfer.

9. Draw the state diagram of 4bit Twisted Ring Counter (Johnson Counter) and design logic circuit for the same, using D flip-flop.

10. a) Draw the architecture of FPGA, show the internal logic block and explain its elements in detail. [5]
b) Design any four operations of ALU. [5]





JOIN
VIT QUESTION PAPERS
ON TELEGRAM

Scanned by CamScanner