Roll No. 2409031202 40

311202

May-2025

BCA (DS)/BCA-IInd SEMESTER

Digital Electronics-II

(BCG-104-V/BCA-23-106)

Time : 3 Hours

Max. Marks : 75

Instructions :

1. *It is compulsory to answer all the questions (1.5 marks each) of Part-A in short.*
2. *Answer any four questions from Part-B in detail.*
3. *Different sub-parts of a question are to be attempted adjacent to each other.*

PART–A

1. (a) What is tri-state logic, and how does it facilitate efficient signal management? (1.5)

   (b) Define a parity bit and analyze its significance in error detection mechanisms. (1.5)

   (c) What are self-complementary codes? (1.5)

   (d) Explain the operational advantages of a carry look-ahead adder. (1.5)

   (e) Perform the subtraction 8–3 in BCD. (1.5)

   (f) Differentiate between asynchronous and synchronous counters, highlighting their design principles. (1.5)

(g) Compare ring and Johnson counter. (1.5)

(h) Define the term resolution with respect to ADC. (1.5)

(i) A successive approximation ADC has a clock frequency of 1 MHz and 8-bit resolution. Determine the conversion time. (1.5)

(j) Explain priority encoder. (1.5)

PART–B

2. (a) Describe the process of interfacing CMOS and TTL logic families, emphasizing compatibility challenges and solutions. Also realize NAND gate using CMOS. (10)

(b) A transmitter uses a single error-correcting code for the message using even parity.The message received at the receiving end is 1110101. Check and correct the error. (5)

3. (a) Minimize the given four-variable Boolean function using Quine-McCluskey method, incorporating a step-by-step illustration.

$Y(A,B,C,D) = \sum m\ (1,3,5,10,11,12,13,14,15)$ (5)

(b) Illustrate the working principle and implementation of BCD adder using logic diagram. (10)

4. (a) Design a BCD to Excess-3 code converter using truth table, k-maps and logic circuit. (10)

(b) Design a Mod-9 ripple counter using T-flip flop. Also draw its logic diagram. (5)

5. Design a sequential counter using JK-flip flop to generate the following sequence. (15)

$0 \rightarrow 2 \rightarrow 4 \rightarrow 5 \rightarrow 1 \rightarrow 7 \rightarrow 6$

6. (a) Draw and explain the circuit of a Dual slope ADC. (10)

(b) A 12-bit ADC is operating with a 1 -μs clock period. Find the total conversion time for a counting type ADC. (5)

7. Write short notes on :

(a) Error detection and correction codes.

(b) Sampling, quantization and encoding. (15)
