MAULANA ABUL KALAM AZAD UNIVERSITY OF TECHNOLOGY, WEST BENGAL

Paper Code : IT-705D

MICROELECTRONICS AND VLSI DESIGN

Time Allotted : 3 Hours | *Full Marks* : 70

The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable.

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for any *ten* of the following : $10 \times 1 = 10$

   i) Which design rule is scalable in the context of VLSI design ?
   - a) α rule
   - b) β rule
   - c) λ rule
   - d) none of these.

   ii) What is the full form of FPGA ?
   - a) Field Programmable Gate Array
   - b) Full Programmable Gate Array
   - c) Fast Programmable Gate Array
   - d) None of these.

   iii) What is ASIC ?
   - a) Application simple IC
   - b) Authentic sample IC
   - c) Application specific IC
   - d) Authentication specific IC.

   iv) Which of the following processing techniques would be used to create the source and drain regions of a transistor ?
   - a) Oxidation
   - b) Ion implantation
   - c) Sputtering
   - d) Polysilicon deposition.

   v) VHDL is acronym of
   - a) Very High Speed Integrated Circuit HDL
   - b) Vast HDL
   - c) Very simple HDL
   - d) Very important HDL.

   vi) Number of transistors used in LSI is
   - a) 200-2000
   - b) 100-500
   - c) 5-10
   - d) 1.

   vii) In an Enhancement mode MOSFET
   - a) Conducting channel exists at zero gate bias
   - b) Conducting channel exists at negative gate bias
   - c) No conducting channel at zero gate bias
   - d) Conducting channel does not depend on gate bias.

   viii) The Substrate Fermi potential in NMOS is
   - a) Negative
   - b) Positive
   - c) Zero
   - d) Infinite.

   ix) The substrate bias coefficient in PMOS is
   - a) Positive
   - b) Negative
   - c) Zero
   - d) Infinite.

   x) In full scaling, Saturation drain current is scaled down by a factor
   - a) S
   - b) S^2
   - c) S^3
   - d) S^{-1}.

xi) In a PLA
   a) Only AND array is programmable
   b) Only AND array is programmable
   c) Both AND and OR arrays are programmable
   d) Macro-cell is the building block.

xii) VLSI stands for
   a) Very Large Source Integration
   b) Very Large Scale Integration
   c) Very Long Scale Integration
   d) Very Low Scale Integration.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. 3 × 5 = 15

2. Draw the layout of 2 input CMOS NAND gate.
3. What are the differences between ASIC and FPGA ?
4. Describe with proper diagram Gajski-Kuhn chart.
5. Define Moore's Law. What is the basic difference between E-MOS and D-MOS ? 2 + 2 + 1
6. Implement the function F = (A and B) using Static CMOS. 5
7. What are the advantages of Dynamic CMOS over State CMOS ? Define FPGA. 4 + 1

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. 3 × 15 = 45

8. a) Sketch a stick diagram of XOR gate.

   b) Implement the following function using PLA.

$$F_1 = A'BC + AB + AB'C'$$

$$F_2 = AB + A'BC'$$

$$F_3 = A'BC + ABC + AB'C'$$

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   c) Briefly describe the architecture and operation of FPGA. (1 + 3) + 6 + 5

9. a) Explain with proper diagram the different steps involved in the fabrication process of *n*-well CMOS.

   b) Explain the operation of basic CMOS inverter. 10 + 5

10. a) Explain ASIC Design flow.

    b) Classify the design styles used in VLSI Design. Explain any two of the design styles, briefly. 5 + (2 + 4 + 4)

11. a) Derive the expression of threshold voltage of an N-channel MOSFET.

    b) Derive the current-voltage relationships of an Enhancement type *N*-channel MOSFET operating in linear region. 7 + 8

12. Write short notes on any *three* of the following : 3 × 5
    a) Photolithography process
    b) CPLD
    c) Short Channel Effects of MOSFETs.
    d) Constant Voltage Scaling
    e) Capacitances associated with MOSFET
    f) Granularity and Regularity.