



SCHOOL OF INFORMATION TECHNOLOGY AND ENGINEERING

CAT II - B. Tech. - Winter Semester - 2018-19

Course Name: Digital Logic and Microprocessors

Duration: 1.5 hrs

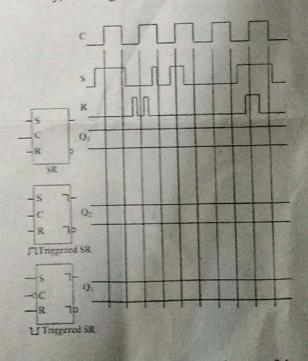
Course Code: ITE1001

Max. Marks : 50

Slot : A2+TA2

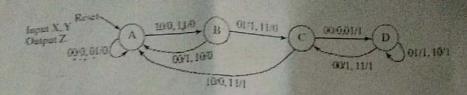
Faculty: Dr. Swarna Priya RM, Dr. Aarthy S L, Dr. Praveen Kumar Reddy

Clock, S and R waveforms, and three flip-flops are shown in Figure below. For
the flip-flops, carefully sketch the output waveform, Qi, obtained in response to
the input waveforms. Assume that the propagation delay of the storage elements
is negligible. Initially, all storage elements store 0. (6 Marks)



- Design a switch-tail counter which uses the complement of the serial output of a right shift register (Binary Shift Right) as its serial input.
 - (a) Draw the modified shift register circuit as per the specified requirement.
 (2 Marks)
 - (b) Starting from an initial state of 000, list the sequence of states after each binary shift until the register returns to 000. (5 Marks)
 - (c) Draw the timing diagram for the same. (5 Marks)

SPARCH YIT QUESTION PAPERS ON TELEGRAM TO JOIN 3. Design an asynchronous sequential circuit using JK Flip Flop for the following state diagram. (12 Marks)



 Identify the machine cycles for the following instructions and also the status and control signals associated with each instruction during the execution by the microprocessor 8085. (10 Marks)

> MVI A, #8FH ADI #72H OUT 01H HLT

- Calculate the execution time for each Machine cycle and the instruction if the clock frequency f=3 MHz. (10 Marks)
 - i) MVI B, #08H
 - ii) LDA 3065H
 - iii) IN 02H
 - iv) INR 1009H
 - v) INR B



**** ALL THE BEST****

So,
$$\frac{t(t+1)}{2}$$
 z $\frac{1}{2}$ $\frac{1$