Sub Code: BECT604B **ROLL NO……..……..**

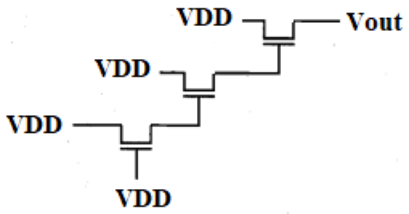
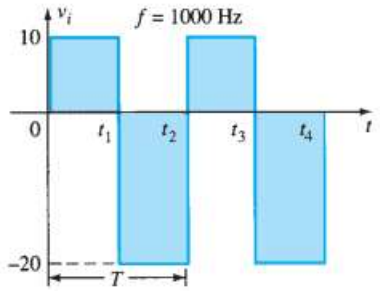
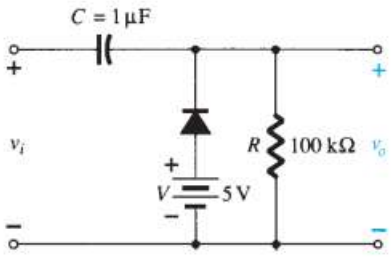
EVEN SEMESTER EXAMINATION, 2023 – 24

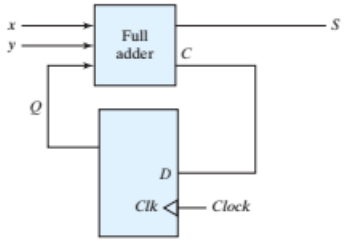
3rd yr B.Tech. – Electronics & Communication Engineering

CMOS Design

Duration: 3:00 hrs **Max Marks: 100**

Note: - Attempt all questions. All Questions carry equal marks. In case of any ambiguity or missing data, the same may be assumed and state the assumption made in the answer.

Q 1.	Answer any four parts of the following. a) Discuss the VLSI design flow. b) Define the terms regularity, modularity, and locality. c) What is CMOS n-well process? d) Explain LOCOS technique and its importance in fabrication process. e) Mention the short-channel effects in ultra-nanoscale regime. f) Discuss the MOSIS layout design rules in detail.	5x4=20
Q 2.	Answer any four parts of the following. a) Calculate the V_{out}, as shown in figure if VDD is 5V and threshold voltage of each device is 1V.  b) Write a SPICE netlist for a CMOS inverter. c) Explain Mealy and Moore machines with examples. d) Sketch the transfer characteristics of a *p*-channel enhancement-type MOSFET if threshold voltage is -5 V and $k = 0.45 \times 10^{-3}$ A/V^2. e) Design 3-input NAND gate using CMOS logic. f) Derive the expression of output impedance for CE configured BJT using hybrid parameter model.	5x4=20
Q 3.	Answer any two parts of the following. a) Define the complete IC fabrication flow in details with schematics. b) Explain the working of Czochralski crystal growth process with diagrams. c) Determine *vo* for the network, as shown in the figure for the input indicated.   	10x2= 20
Q 4.	Answer any two parts of the following. a) Design a 101 sequence detector using Moore's non-overlapping method.	10x2= 20

	b) What are the different CVD methods? Details the APCVD method. c) A sequential circuit has one flip-flop, two inputs x and y, and one output S. It consists of a full-adder circuit connected to a D flip-flop, as shown in figure. Derive the state table and state diagram of the sequential circuit. 	
Q 5.	Answer any two parts of the following. a) Write the IC production steps in detail. b) Derive the formula for junction depth for pre-deposition case of Fick's second law. c) A synchronous Moore FSM has a single input, *x_in*, and a single output *y_out*. The machine is to monitor the input and remain in its initial state until a second sample of *x_in* is detected to be 1. Upon detecting the second assertion of *x_in y_out* is to asserted and remain asserted until a fourth assertion of *x_in* is detected. When the fourth assertion of *x_in* is detected the machine is to return to its initial state and resume monitoring of *x_in*. Draw the state diagram of the machine.	10x2= 20

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