[No. of Printed Pages – 4]

ES201
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Enrol. No. .....

END SEMESTER EXAMINATION : NOV.–DEC., 2018

BASIC ELECTRONICS ENGINEERING

Time : 3 Hrs. *Maximum Marks : 70*

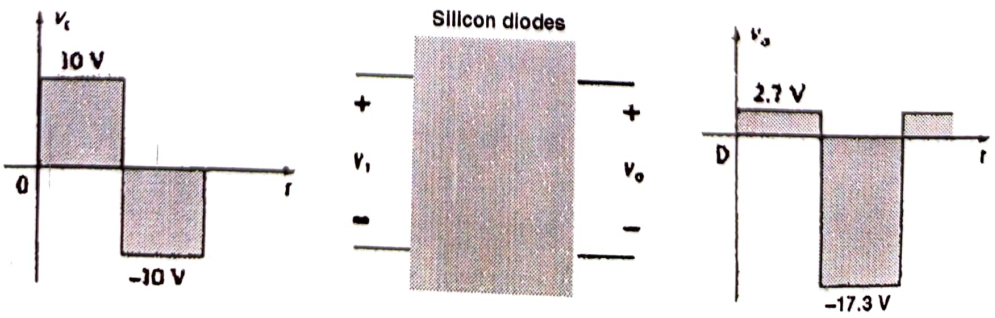
Note: ***Attempt questions from all sections as directed. Use of Scientific calculator is allowed.***

SECTION – A (30 Marks)

Attempt any **five** *questions out of* **six.**
Each question carries **06** *marks.*

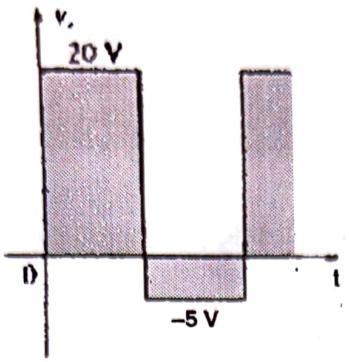
1. Explain base-width modulation (the Early effect) with the aid of plots of potential and minority concentration throughout the base region.

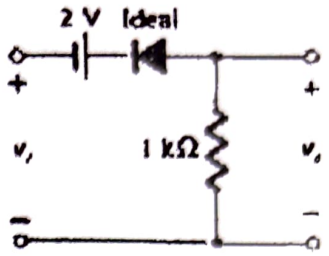
2. (a) Design a clamper that will perform following function : (3)



P.T.O.

(b) Determine V_0 for the following network : (3)





3. Consider an operational amplifier in which the first set of signals is $v_1 = +50\ \mu V$ and $v_2 = -50\ \mu V$ and the second set is $v_1 = 1050\ \mu V$ and $v_2 = 950\ \mu V$. If the common-mode rejection ratio is 100, calculate the percentage difference in output voltage obtained for the two sets of input signals.

4. Give the significance of virtual ground in an op-amp. Also derive the following expression :

$$V_0 = A_d V_d \left(1 + \frac{1}{CMRR}\frac{V_c}{V_d}\right)$$

5. (a) Explain the significance of diffusion capacitance and derive expression for the same. (3)

(b) Reduce the following function to its minimum SOP form :

$Z = A'B'C'D' + A'B'CD' + AB'C'D' + A'BCD + AB'CD' + A'B'CD$ (3)

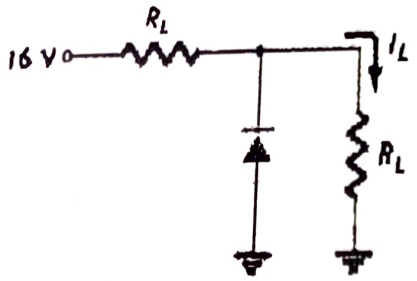
6. (a) The RC coupling amplifier gives constant gain over the mid frequency range. Explain. (3)

(b) Derive an expression for Transformer Utilization Factor (TUF) for the half wave rectifier. (3)

SECTION – B (20 Marks)

Attempt any **two** *questions out of* **three**. *Each question carries* **10** *marks.*

7. (i) Design the network of the given figure to maintain V_L at 12 V for a load variation (I_L) from 0 to 200 mA. Calculate the Rs and V_Z.



(ii) Determine Pzmax for the Zener diode of part (i).

8. (a) Explain the meaning of pinch-off voltage in a JFET. Sketch the circuit of source follower and explain its working. Also determine its output impedance. (5)

(b) The common drain circuit has R1 = 3.5 MΩ, R2 = 1.5 MΩ, Rs = 2 kΩ, R_L = 20 kΩ, g_m = 2.5 mS. Determine input impedance, output impedance and voltage gain. (5)

P.T.O.

9. (a) Simplify the following using K-map and implement the simplified function using NOR gates :

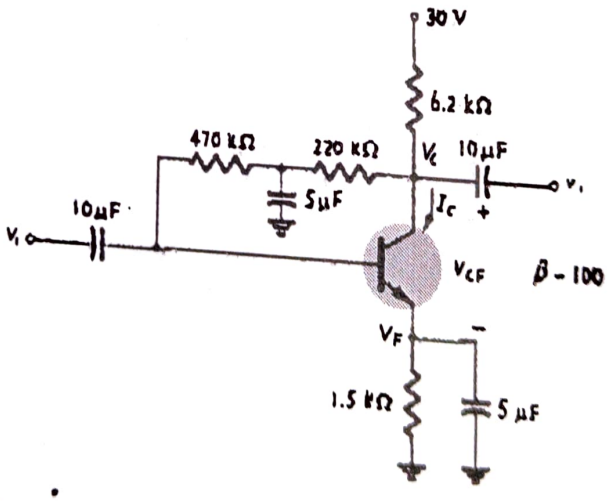
$Y = \Pi M(0,1,5,9,13,14,15) + d(3,4,7,10,11)$. (5)

(b) Show that a full subtractor can be constructed using two half subtractors and an OR gate. Deduce a full adder using EX-OR gate. (5)

SECTION – C (20 Marks)

(Compulsory)

10. (a) For the given voltage feedback network, determine I_C, V_C, V_{CE}, V_E : (10)



(b) Discuss the operation of non-inverting amplifier and also derive the expression for its voltage gain. (5)

(c) Derive the mathematical expression of transconductance for JFET. Also find $V_{GS(off)}$ if the $g_{mo} = 10$ mS and $I_{DSS} = 10$ μA. (5)