Reg. No. : E N G G T R E E . C O M

Question Paper Code : 40989

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2024

Fifth Semester

Electronics and Communication Engineering

EC 3552 – VLSI AND CHIP DESIGN

(Common to: Electronics and Telecommunication Engineering)

(Regulations 2021)

Time : Three hours **Maximum : 100 marks**

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. How NMOS and PMOS act as a switch?
2. What is the body effect of MOS transistor?
3. Draw the stick diagram for two input NOR gate.
4. What is the significance of propagation delay?
5. Differentiate latches and flipflops.
6. What are the basic timing classifications of digital systems?
7. List the interconnect parameters in chip design.
8. Write the logic equation for 4-bit comparators.
9. Sketch the ASIC design flow?
10. Differentiate embedded cores and SOCs.

PART B — (5 × 13 = 65 marks)

11. (a) List and explain the regions of operation of MOS transistor and obtain the drain current for all regions.

Or

(b) Discuss the MOS transistor under dynamic conditions.

12. (a) Realize the 2:1 multiplexer using

(i) Static CMOS logic (5)

(ii) Dynamic CMOS logic (4)

(iii) Pass transistor logic (4)

Or

(b) (i) Illustrate the low power design principles of CMOS circuits. (7)

(ii) Explain the design considerations in static CMOS logic. (6)

13. (a) (i) Elucidate the dynamic latches and registers suitable for sequential circuit design. (7)

(ii) Elaborate the sense amplifier based register for sequential circuit design. (6)

Or

(b) Compare the mono-stable and bistable multivibrator circuit based on MOS transistors.

14. (a) Design a high speed 4-bit adder and compare with the existing adders with respect to speed of operation.

Or

(b) (i) Implement the full adder using PLA. (6)

(ii) Explain the memory architecture and the basic building blocks. (7)

15. (a) (i) Illustrate the microchip design process and identify the issues in test. Validate the verification of the complex chips? (7)

(ii) Model the faults associated in CMOS design. (6)

Or

(b) (i) What is the need for testing? Explain the operation of automatic test pattern generation. (7)

(ii) Write the test bench for VHDL code to test the 2-to-4 decoder logic. (6)

PART C — (1 × 15 = 15 marks)

16. (a) (i) Obtain the elmore delay constant for the four input NAND gate. (8)

(ii) Write the disadvantage(s) of dynamic CMOS logic. Provide three possible solutions to overcome the disadvantages. (7)

Or

(b) (i) Design a master-slave register using transmission gates and draw the logic waveform. Find the setup time and hold time for the register. (8)

(ii) Implement a 2-to-4 decoder using ROM. (7)