Final Assessment Test – November 2019

VIT Vellore Institute of Technology

Course: CSE2001 - Computer Architecture and Organization

Class NBR(s): 0588/0607/0613/0616/0625/0628/0631/ 1214/1216/1218/1220/6645/7472 Slot: G2+TG2

Time: Three Hours Max. Marks: 100

KEEPING MOBILE PHONE/SMART WATCH, EVEN IN 'OFF' POSITION, IS EXAM MALPRACTICE

Answer ALL Questions

(10 X 10 = 100 Marks)

1. The processor A, B C and D has a 2 GHz clock frequency. Find the total execution time for the programme with instruction mix given below. If the CPI of arithmetic instruction was doubled what would be the impact on the execution time of all the processors.

Processors	Instruction mix / Processor			CPI		
	Arithmetic	Load / Store	Branch	Arithmetic	Load / Store	Branch
A	2560	1280	256	1	4	2
B	1280	640	128	1	4	2
C	640	320	64	1	4	2
D	320	160	32	1	4	2

Find the total execution time for this program on A, B, C and D processors. Assume that each processor has a 2 GHz clock frequency. If the CPI of arithmetic instructions is doubled, what would the impact on execution time of this program on A, B, C and D processors?

2. Calculate M multiplied by Q using Booth's Algorithm where M = -11 and Q = 27.

3. Write a program to evaluate the expression X= (A+B)*(C/D) with one address, two address and three address Instructions.

4. a) Give a block diagram for a 8M X 32 memory using 512K X 8 RAM chips. [5]

   b) Multiply the numbers $(0.5)_{10}$ and $(-0.4375)_{10}$ using binary floating point multiplication. [5]

5. The following is a list of 32-bit memory address references, given as word addresses of 8-bit each. 1, 6, 134, 175, 1, 134, 84, 65, 161, 65, 134 and 175. For the above references, identify the binary addresses, the tags and the indexes given a direct-mapped cache with initially 2-word blocks. Assuming the cache being empty initially, list the hit or miss for cache references.

6. Consider a two level memory hierarchy of the form (L1, L2) where L1 is connected directly to the CPU. Determine the average cost per bit and average access time for the data given below.

Level	Capacity	Cost	Access time	Hit ratio
L1	1024	0.1000	10^{-8}	0.9000
L2	2^{16}	0.0100	10^{-6}	-

7. It is necessary to transfer 512 words from a backup store to a memory section starting from address 1000 and the transfer is by means of DMA. i) What are the initial values that the CPU must transfer to the DMA controller? ii) Give step by step account of the actions taken during the input of the first two words.

8. List and explain the levels of RAID. What is the distinction between parallel access and independent access in context of RAID?

9. Assume a pipeline with four stages: fetch instruction (FI), decode instruction and calculate addresses (DA), fetch operand (FO), and execute (EX). Draw a diagram for a sequence of 7 instructions, in which the third instruction is a branch that is taken and in which there are no data dependencies.

10. a) Discuss the differences between tightly coupled multiprocessors and loosely coupled multiprocessors from the viewpoint of hardware organization and programming techniques. [5]

b) What is the use of parity bits in an error correction code? How many check bits are needed if the Hamming error correction code is used to detect single bit errors in a 2048-bit data word? [5]

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