VR10

EE/EI 3005

II/IV B.Tech. DEGREE EXAMINATION, JUNE, 2014

Third Semester

DIGITAL ELECTRONICS

Time: 3hours ***Max. Marks: 70***

Part-A is compulsory

Answer One Question from each unit of Part-B

PART-A

10 x 1 = 10M

a. Convert the decimal $(2262)_{10}$ to Hexa decimal number.

b. Perform subtraction for $(11010)_2$ - $(10000)_2$ by using 2's complement method.

c. State the associative law in related to Boolean functions.

d. What is an essential prime implicant?

e. What are encoders and decoders?

f. What are the advantages of Multiplexers?

g. What is difference between latch and Flip-flop?

h. What is a ring and twisted ring counter?

i. What are the advantages of CMOS over TTL?

j. What is meant by propagation delay?

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PART-B

4 x 15 = 60M

UNIT-I

1. a. Convert the $(2AC5.D)_H$ into decimal and octal form. **6M**

   b. Implement the F (A, B, C) =A⊕B⊕C Boolean Functions with minimum no. of Two input NAND gates. **9M**

(or)

2. a. Simplify the Boolean expression $Y = (A+B)(A'+C)(B+C')$. **5M**

   b. Give the binary, BCD and gray code representation of decimal number 108. **6M**

   c. Determine the value of base x if **4M**

   i) $(193)_X = (623)_8$ ii) $(211)_X = (152)_8$

UNIT-II

3. a. Find all the Prime implicants for the following Boolean Functions and Determine which are essential prime implicants? **6M**

   f(A, B, C, D) = Σ m(0, 2, 3, 5, 7, 8, 10, 11, 14, 15)

   b. Design a 3 bit Gray to Binary code converter using gates. **9M**

(or)

4. a. Simplify the following Boolean functions by using Quine McCluskey Tabular Method.

   f(W, X, Y, Z) = Σ m(1, 2, 3, 5, 13) + (6, 7, 8, 9, 11, 15) **9M**

   b. Design a BCD to Excess-3 code converter using AND, OR, NOT gates. **6M**

UNIT-III

5. a. Design a sequence generator using JK Flip flops for the following sequence1001001. **9M**

   b. How many no. of shift registers are required to build a shift register to store following numbers **6M**

   i) decimal 28 ii) binary 6 bits

   iii) octal 17 iv) hexadecimal A

(or)

6. a. Design Mod 8 Synchronous up and down counter with JK flip-flops. **10M**

   b. Explain about SR flip-flops and T flip-flop with their Truth table, Excitation table and characteristic equation. **5M**

UNIT-IV

7. a. Explain the operation of a HTL and state the advantages over DTL. **8M**

   b. Explain the operation of 3 input CMOS NAND gate circuit. **7M**

(or)

8. a. Explain the working of a Emitter coupled Logic and mention its applications. **7M**

   b. Explain the operation of a IIL and state the advantages over saturated bipolar logic families. **8M**

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