VIT
Vellore Institute of Technology

Final Assessment Test – April 2019

Course: ECE1002 - Semiconductor Devices and Circuits
Class NBR(s): 1226 / 1229 / 1232 / 1234 / 1236 / 1240 / 1248
Slot: C2+TC2
Time: Three Hours
Max. Marks: 100

General Instructions: n_i for Ge = 2.5×10^{13} cm^{-3}, n_i for GaAs = 2×10^{6} cm^{-3}

Answer ALL Questions
(10 X 10 = 100 Marks)

1. Calculate the position of the Fermi level and sketch its band diagram for the following cases: [10]
   a) Ge, n-type, $N_D=10^{17}$ cm^{-3}, T = 300 K.
   b) Si, p-type, $N_A=2\times10^{18}$ cm^{-3}, T = 450 K.
   c) GaAs, n-type, $N_D = 10^{18}$ cm^{-3}, $N_A = 5\times10^{17}$ cm^{-3}, T = 300 K.

2.(a) A Si p-n junction is reverse-biased with $V_a= -10$ V, $N_D= 2\times10^{15}$ cm^{-3} and $N_A = 2\times10^{16}$ cm^{-3}. Determine the percentage change in junction (depletion) capacitance and built-in potential if the doping in the p region is increased by a factor of 2. [10]

OR

2.(b) A Si p-n junction has $N_D = 10^{18}$ cm^{-3} and $N_A = 10^{16}$ cm^{-3}. The junction area is 100µm^2. Calculate the junction (depletion) capacitance in the absence of any applied bias. [10]

3. Sketch the transfer characteristic for the circuit shown in fig.1 with the input range of $-20\text{ V} \le V_1 \le 20$ V. Case (i) Assume the diodes are ideal. (ii) Suppose diode D2 is reversed in the circuit. [10]

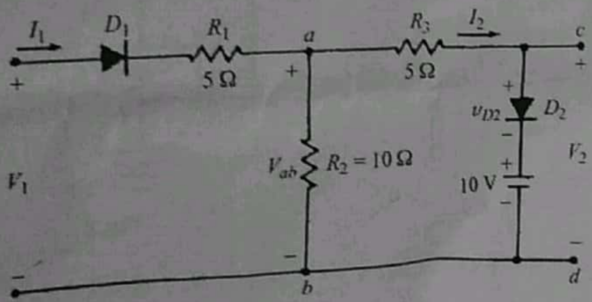

Fig.1

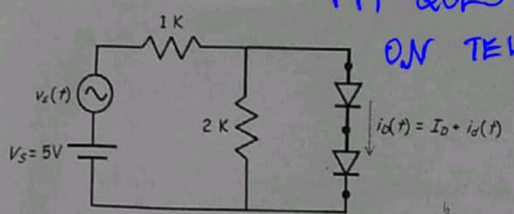

Fig.2

4. For the circuit shown in Fig. 2, If $v_s(t)$= 0.01sinωt, η = 1 and V_γ = 0.6 V what is $i_D(t)$?. [10]

5. Determine the average voltage and current, rms voltage and current and ripple factor for the filtered bridge rectifier with a load as indicated in Fig.3. [10]

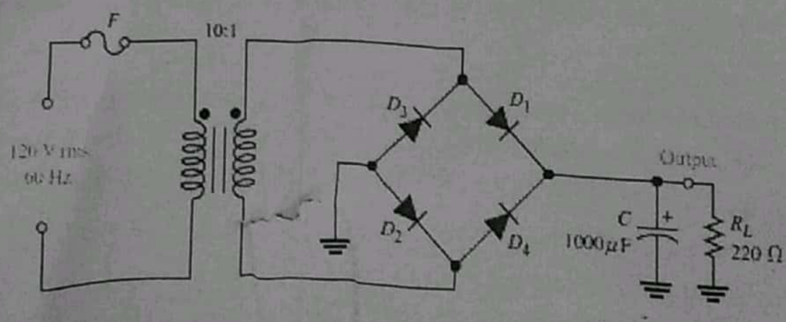

Fig.3

6. Discuss in detail about the different regions of operation of Enhancement MOSFET and the various modes of operation of a BJT along with their I-V Characteristics. [10]

7. a) A Ge transistor with β = 100 has a base-to-collector leakage current I_{CBO} of 5 µA. If the transistor is connected for common-emitter operation, find the collector current for (i) I_B = 0 and (ii) I_B = 40 µA. [5]
   b) The Si transistor in Fig. 4 has α=0.99 and I_{CEO} = 0. Also, V_{EE} = 4V and V_{CC} = 12V. (i) If I_{EQ} = 1.1 mA, find R_E. (ii) If V_{CEQ} = -7V, find R_C. [5]

Possession of Mobile Phone in the exam hall even in switched off condition is a malpractice.

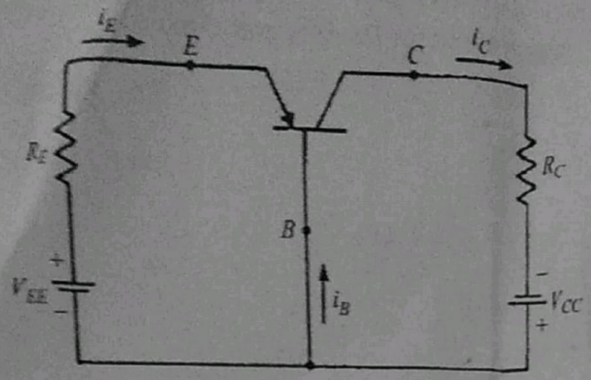

Fig.4

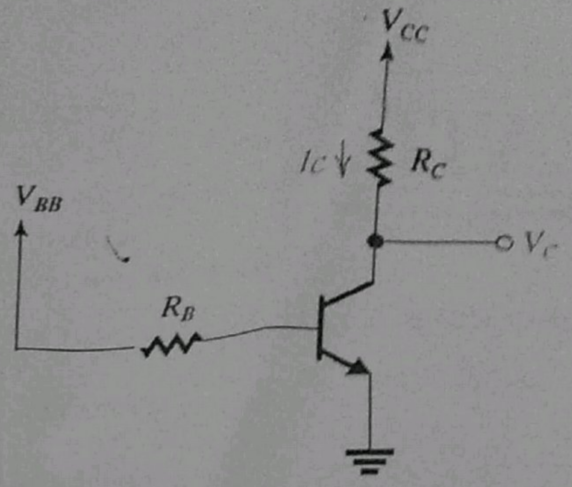

Fig.5

8. Find the value of V_{BB} for the circuit shown in fig.5 with V_{CC} = 5 V, R_C = 1 kΩ, β = 50 and R_B = 20 kΩ that results in the transistor operating (a) in the active mode with V_C = 1 V; (b) at the edge of saturation; (c) deep in saturation with $\beta_{forced} = 10$ **[10]**

9. Find I_{D2} and V_{D2} for the circuit shown in Fig.6. Consider that V_t = 0.6 V, $\mu_n C_{ox}$ = 200 μA/V^2, L = 0.8 μm, W = 8 μm, R_{D1} = 12.5 kΩ, R_{D2} = 10 kΩ, V_{DD} = 3V. Assume that Q1 and Q2 are identical. **[10]**

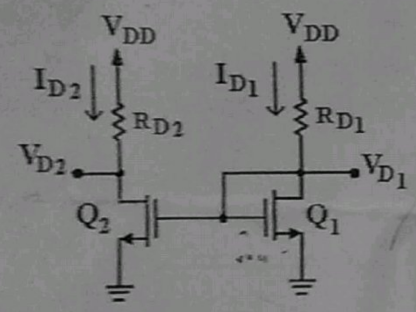

Fig.6

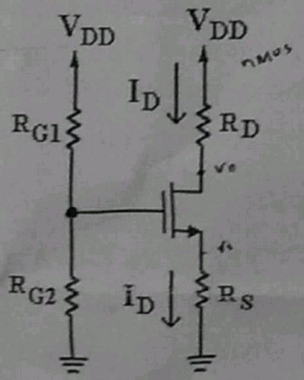

Fig.7

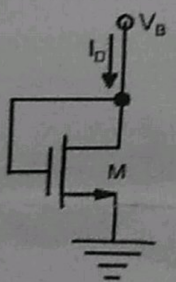

Fig.8

10.(a) For the circuit shown in Fig.7, assume that the NMOS transistor has V_{TH} = 1 V, k'_n (W / L) = 1 mA/V^2, and R_{G1} = R_{G2} = 10 MΩ, R_D = R_S = 6 kΩ, and V_{DD} = 10 V. **[10]**

i) Determine the voltages at all nodes and the currents through all branches.

ii) What is the largest value that R_D can have while the transistor remains in the saturation mode?

OR

10.(b) i) Find the small – signal resistance (i.e. dV_B/dI_D) in kΩ offered by the n-channel MOSFET 'M' shown in Fig. 8, at a bias point of V_B = 2 V is (device data for M: device transconductance parameter $k_N = \mu_n C_{ox}\frac{W}{L} = 40\frac{\mu A}{V^2}$, threshold voltage V_{TN} = 1 V, and neglect body effect and channel length modulation effects). **[5]**

ii) For the two circuits shown in Figure 9(a) and 9(b), Plot I_X as V_X varies from 0 to 3 V. The technology parameters $k'_N = \mu_n C_{ox} = 100\frac{\mu A}{V^2}$, (W/L) = 10, V_t = 0.7 V. **[5]**

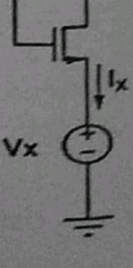

Fig.9 (a)

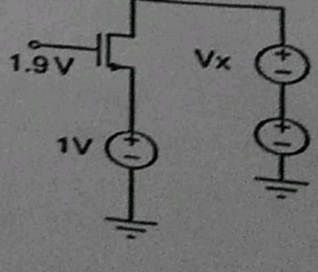

Fig.9 (b)