Name : .....

Roll No. : .....

Invigilator's Signature : .....

2011

COMPUTER ORGANIZATION & ARCHITECTURE

Time Allotted : 3 Hours *Full Marks* : 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for any *ten* of the following :

$10 \times 1 = 10$

i) Maximum number of directly addressable locations in the memory of a processor having 10 bits wide control bus, 20 bits address bus, and 8 bit data bus in

a) 1K b) 2K

c) 1M d) none of these.

ii) The logic circuit in ALU is

a) entirely combinational

b) entirely sequential

c) combinational cum sequential

d) none of these.

iii) When signed numbers are used in binary arithmetic, then which one of the following notations would have unique representation of zero ?

a) 1's complements b) 2's complements

c) sign magnitude d) none of these.

iv) Which of the following addressing modes is used in the instruction PUSH B ?

a) Immediate b) Register

c) Direct d) Register indirect.

v) Virtual memory system allows the employment of

a) more than address space

b) the full address space

c) more than hard disk capacity

d) none of these.

vi) In the absolute addressing mode

a) the address of the operand is inside the instruction

b) the register containing the address of the operand is specified inside the instruction

c) the location of the operand is implicit

d) the operand is inside the instruction.

vii) Given an 8 bit floating point representation with 4 bits for the fraction part and 4 bits for the exponent part, what is the largest number that can be stored ?

a) 30730 b) 30720

c) 20730 d) 20720.

viii) Booth's algorithm for computer arithmetic is used for

a) multiplication of number in sign magnitude form

b) multiplication of number in 2's complement form

c) division of number in sign magnitude form

d) division of number in 2's complement form.

ix) DMA operations need

a) switching logic between I/O and system bus

b) I/O bus

c) special control signals to CPU such as hold and acknowledge

d) no CPU control signals.

x) The conversion of $(FAFAFB)_{16}$ into octal form is

a) 76767676 b) 76575372

c) 76737672 d) none of these.

xi) The branch type instructions in program cause

a) data hazard b) structural hazard

c) control hazard d) none of these.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. $3 \times 5 = 15$

2. What is locality of reference ? What is memory mapping ? Why is it needed ? 2 + 1 + 2

3. Briefly explain the IEEE-754 standard format for floating point representation. How NaN (Not a Number) and Infinity are represented in this standard ? 3 + 2

4. What is pipelining ? Why is it required ? What is the difference between pipeline and parallel processing ? 1 + 2 + 2

5. a) A digital computer has a common bus system for 16 registers of 32 bits each. The bus is constructed with multiplexers.

   i) How many selection inputs are there in each multiplexer ?

   ii) What size of multiplexers is needed ?

   iii) How many multiplexers are there in the bus ?

   b) Why do most computers have a common bus system ?

   3 + 2

6. What is virtual memory ? Why is it called virtual ? Write the advantage of virtual memory. 2 + 1 + 2

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. 3 × 15 = 45

7. a) Explain Booth's algorithm. Apply Booth's algorithm to multiply two numbers (+14) and (–12). Assume that both the multiplier and the multiplicand to be of 5 bit each.

   b) Give the flowchart for division of two binary numbers and explain. 10 + 5

8. a) How does cache memory increase the speed of the processing ? What is hit ratio ?

   b) What is cache mapping ? What is the difference between associative mapping and set-associative mapping ?

   c) A computer has 512 kB cache memory and 2 MB main memory. If the block size is 64 bytes, then find the subfield for

      i) associative mapping

      ii) direct mapping

      iii) set-associative mapping. 2 + 2 + 2 + 3 + 6

9. a) What do you mean by pipeline processing ?

   b) What are instruction pipeline and arithmetic pipeline ?

   c) Differentiate between vectored and non-vectored interrupts.

   d) Explain pipeline hazards.

   e) Compare RISC with CISC. 2 + 2 + 2 + 4 + 5

10. a) What are the advantages of relative addressing mode over direct addressing mode ?

    b) Explain Fynn's classification for multi-processor system.

    c) What are the advantages of carry look ahead adder over ripple carry adder ? Explain.

    d) Explain the different types of addressing modes.

3 + 4 + 3 + 5

11. a) What is instruction cycle ? Draw the Time diagram for memory write operation.

    b) Explain the basic DMA operations for transfer of data between memory and peripherals.

    c) With the help of a neat diagram show the structure of a typical arithmetic pipeline performing $A * B + C$.

1 + 4 + 5 + 5

==========