



Name :

Roll No. :

Invigilator's Signature :

CS/B.TECH (EEE/ICE/PWE) (OLD)/SEM-4/EC-402/2013

2013

DIGITAL ELECTRONICS AND INTEGRATED CIRCUITS

Time Allotted : 3 Hours

Full Marks : 70

The figures in the margin indicate full marks.

*Candidates are required to give their answers in their own words
as far as practicable.*

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for the following : $10 \times 1 = 10$

i) The binary equivalent number of $(25.75)_{10}$ is

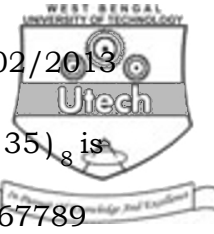
- | | |
|--------------|---------------|
| a) 11001.110 | b) 11001.011 |
| c) 11001.111 | d) 11001.000. |

ii) The hexadecimal equivalent number of $(348.35)_{10}$ is

- | | |
|------------|-------------|
| a) 15C.668 | b) 15C.599 |
| c) 15B.599 | d) 15A.599. |

iii) The decimal equivalent number of $(1101.11)_2$ is

- | | |
|----------|-----------|
| a) 13.25 | b) 13.75 |
| c) 13.5 | d) 13.00. |



- iv) The decimal equivalent number of $(427.35)_8$ is
- a) 279.456732 b) 279.4567789
c) 279.432167 d) 279.453125.
- v) The decimal equivalent number of $(6ABC.2A)_{16}$ is
- a) 27324.125 b) 27325.678
c) 27324.164 d) 27324.654.
- vi) The binary equivalent number of $(155.52)_8$ is
- a) 001101101.101010 b) 001101101.101101
c) 001101101.110000 d) 001101101.110011.
- vii) The binary equivalent number of $(1CEF.2B)_{16}$ is
- a) 1110011101111.00101011
b) 1110011101111.00111011
c) 1110011101111.1101011
d) 1110011101111.1001001.
- viii) The hexadecimal equivalent number of $(7324.456)_8$ is
- a) ED4.87 b) ED4.47
c) ED4.57 d) ED4.97.
- ix) The result of subtraction of the binary bits $11101 - 1101$ is
- a) 00001 b) 10000
c) 10001 d) 10011.
- x) The result of addition of the binary bits $1101 + 11101$ is
- a) 00001 b) 10000
c) 10001 d) 10011.



GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following.

3 × 5 = 15

2. Convert :
 - a) $ABC + AD$ into standard SOP format.
 - b) $(A + B + C)(A + D)$ into standard POS format. $2 \times 2\frac{1}{2}$
3. Design and implement a full-adder circuit using decoder.
4. Describe the operation of successive approximation type ADC. How many clock pulses are required in worst case for each conversion cycle of an 8-bit SAR type ?
5. Construct :
 - a) EX-OR using NAND
 - b) EX-NOR using NOR. Why are NAND and NOR gates called universal gates ?
6. What is 'lock out' in counter ? Explain race around condition in *J-K* flip-flop. $2 + 3$

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following.

3 × 15 = 45

7. What is propagation delay ? What is noise immunity ? Describe the advantages and disadvantages of totem pole output configuration. How can the logic gates of TTL family and CMOS family be interfaced ? $2 + 3 + 5 + 5$
8.
 - a) Explain the operation of weighted register 4-bit D/A converter. Derive the expression of the output voltage.
 - b) Implement a 16 : 1 MUX using only 4 : 1 MUX. Write down the proper truth table.
9.
 - a) What is register ? Name different types of registers. Explain any one in detail.
 - b) Design a BCD to Excess-3 code converter using PROM.

2 + 2 + 5 + 6



10. a) What is the difference between synchronous and asynchronous counters ?

b) Realize a 4-bit Ring counter using JK flip-flops. Develop the state table. Can this circuit be used to realize a frequency divider ?

$$3 + (4 + 3) + 5$$

11. Write short notes on any *three* of the following : 3×5

- a) Quine McCluskey method
- b) Odd parity generator
- c) TTL NAND gates
- d) EEROM
- e) Carry look ahead adder.

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