VR14 Reg. No: | | | | | | | | | | |

VELAGAPUDI RAMAKRISHNA

SIDDHARTHA ENGINEERING COLLEGE

(AUTONOMOUS)

II/IV B.Tech. DEGREE EXAMINATION, NOVEMBER, 2017

Third Semester

ELECTRONICS AND INSTRUMENTATION ENGINEERING

14EI3306 DIGITAL CIRCUITS AND SYSTEMS

Time: 3 hours ***Max. Marks: 70***

Part-A is compulsory

Answer One Question from each Unit of Part - B

Answer to any single question or its part shall be written at one place only

PART-A

10 x 1 = 10M

1. a. Find the number of parity bits required for a 15-bit hamming code.
   b. Minimize the boolean expression AB'C + A'BC + ABC
   c. Solve the following operations using the 2's complement method (23–48).
   d. Evaluate $(153.513)_{10} = ()_8$.
   e. Determine 'b', given $(292)_{10} = (1204)_b$.
   f. Draw full adder using half adder circuits.
   g. What is race around condition?
   h. Infer the applications of shift registers.
   i. Compare TTL with CMOS logic families.
   j. Find the number of PMOS and NMOS devices required for CMOS AND gate.

PART-B

4 x 15 = 60M

UNIT-I

2. Simplify the following expression using Quine–McCluskey minimization technique
$F(A, B, C, D, E) = \sum(0, 9, 15, 24, 29, 30) + d(8, 11, 31)$ **15M**

(or)

3. a. Determine the minimum sum of products expression for
$F = b^I c^I d^I + bcd + ac^I d^I + ab^I bc^I d$. **7M**

b. Design a circuit to convert BCD code to excess-3 code using discrete logic gates. **8M**

UNIT-II

4. a. Draw and explain 4 bit adder-subtractor. **7M**

b. Implement a full adder using 8 x 1 multiplexer. **8M**

(or)

5. a. Design a combinational circuit for 4 bit BCD to gray conversion **6M**

b. Analyse and implement 4 bit carry look ahead adder with generate (g) and propagate(p) bits. **9M**

UNIT-III

6. a. With excitation table elaborately explain the JK flip-flop conversion to T flip-flop. **7M**

b. Draw the circuit diagram of 4 bit ring counter using D flip-flops and explain its operation. **8M**

(or)

7. a. With suitable excitation and state table, design a Mod-10 synchronous counter using JK flip-flops. **9M**

b. Design master slave JK flip-flop. **6M**

UNIT-IV

8. a. Elaborately discuss the characteristics of digital IC's. **7M**

b. Design universal gates with resistor transistor logic and emitter coupled logic. **8M**

(or)

9. a. Draw the transfer characteristics of MOS inverter. **8M**

b. Draw inverter circuit using CMOS logic. **7M**

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