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Paper Code : PCC-CS402 Computer Architecture

UPID : 004442

Time Allotted : 3 Hours *Full Marks :70*

The Figures in the margin indicate full marks.
Candidate are required to give their answers in their own words as far as practicable

Group-A (Very Short Answer Type Question)

1. Answer *any ten* of the following : [1 x 10 = 10]

(I) What is meant by data dependence?

(II) Which page replacement algorithm suffers from Belady's anomaly?

(III) Which architecture is/are suitable for realizing SIMD?

(IV) What is meant by Branch Prediction?

(V) The throughput of a super scalar processor is _____.

(VI) Which unit is responsible for translation of logical address to physical address?

(VII) The _____ plays a very vital role in case of super scalar processors.

(VIII) The set of loosely connected computers are called as _____.

(IX) Write the equation for Amdahl's Law.

(X) Write the statement for memory inclusion property.

(XI) What is meant by instruction level parallelism?

(XII) In tightly coupled systems, the microprocessors share _____.

Group-B (Short Answer Type Question)

Answer *any three* of the following : [5 x 3 = 15]

2. Given a 4 segment pipeline whereby each segment has a delay time as follows: [5]

Segment1: 40 ns Segment2: 25 ns Segment3: 45 ns Segment4: 45 ns

The delay time for the interface register is 5ns. Calculate the:

i) cycle time of the non-pipeline and pipeline,
ii) execution time for 100 tasks,
iii) real speedup,
iv) maximum speed up.

3. In a simple machine with load-store architecture having clock rate of 1.8GHz and the following specifications: [5]

Operations	Frequency	Number of Clock Cycles
ALU	40%	1
Load	20%	2
Store	10%	2
Branch	30%	2

Calculate CPI and MIPS rating for the machine.

4. What is a superscalar processor? State the advantages of vector computer. [5]

5. State the differences between static network and dynamic network. Explain the hypercube interconnection with n=3. [5]

6. Compare superscalar, super-pipelined and superscalar-super-pipelined architecture. [5]

Group-C (Long Answer Type Question)

Answer *any three* of the following : [15 x 3 = 45]

7. a. Compare tightly coupled system and loosely coupled system. [6+9]
b. Explain with suitable diagram: multiprocessor architectures (UMA, NUMA, COMA).

8. a. What is page fault? [2+9+4]
b. Given page reference string: [1,2,3,4,2,1,5,6,2,1,2,3,7,6,3,2,1,2,3,6]. Compare the page fault rates for LRU, FIFO and Optimal page replacement algorithm.
c. Discuss the implementation of virtual memory through segmentation with suitable diagram.

9. a. Discuss SIMD array processor architecture with suitable diagram. [5+2+2+6]
   b. What are vector stride and vectorization?
   c. What is the difference between scalar processor and vector processor?
   d. Explain vector gather and scatter instructions with suitable diagrams.

10. a. What is cache coherency? [2+3+6+4]
    b. Explain the MESI protocol briefly.
    c. Explain the snoopy bus protocol for cache coherency.
    d. Explain how synchronization is ensured in multiprocessor environment?

11. a. Explain VLIW architectures with suitable diagram. [6+5+4]
    b. State the advantages and disadvantages of VLIW architecture.
    c. What are the hurdles in superscalar architecture?

*** END OF PAPER ***