CHENNAI INSTITUTE OF TECHNOLOGY

(An Autonomous Institution, Affiliated to Anna University, Chennai)
CHENNAI - 600 069

B.E. / B.Tech. DEGREE END SEMESTER EXAMINATIONS
NOV / DEC 2024
First Semester
EC4102 – DIGITAL SYSTEM DESIGN
(Common to CSE / ECE / IT / CSBS / CSE-AIML / CSE-CS / EE-VLSI / ECE-AC
(Regulations 2024)

Time: Three Hours | Maximum Marks: 100

Answer ALL Questions

RBT Level : L1- Remembering, L2 – Understanding, L3 – Applying, L4 – Analyzing, L5 – Evaluating, L6 – Creating

PART – A **(10x2=20 Marks)** CO

1. Identify the base x, when $(111101)_2 = (141)x$. CO1

2. Simplify the Boolean expression W = AB + A (B+C) + B (B+C). CO1

3. Draw the Full Adder circuit using two Half Adder circuit. CO

4. What is the limitation of encoder? Mention the circuit that overcome the limitation. CO

5. Give the excitation table for T flip-flop. CO

6. What is the minimum no. of flip-flop needed to design a counter of modulus 60? C

7. Define critical and non-critical race. C

8. What are hazards?

9. Define Fan-out.

10. Compare and contrast EEPROM and EAPROM.

PART - B (5x16=80 Marks)

CO

11. a) Simplify the expression $F(A,B,C,D) = \Sigma m(0,1,2,4,6,9,10,15) + \Sigma d(11,12,14)$ using k-map and implement using (a) NAND gates only (b) NOR gates only. CO1

(OR)

b) Simplify the following function using Tabulation method and draw the corresponding logic circuits using AND, OR and NOT gates. CO1
$F(w, x, y, z) = \sum m(0, 1, 5, 7, 8, 13, 15) + \sum d(2, 9, 10)$

12. a) A combinational circuit compares two 2-bit numbers (A and B) to check if they are equal. The circuit has three outputs EQ, GT and LT. CO2

1) EQ is equal to 1 if the two numbers are equal.

2) GT is equal to 1 if $|A| > |B|$.

3) LT is equal to 1 if $|A| < |B|$.

Derive Boolean equation for the outputs of the combinational logic circuit and draw the logic diagram using only NAND gates.

(OR)

b) A combinational circuit that has four inputs and one output works as below. CO

1) The output is 1 when the decimal value of the inputs is less than 6.

2) The output is 1 when the decimal value of the inputs is an even number.

3) The output is 0 otherwise.

Derive Boolean equation for the output of the combinational logic circuit and draw the logic diagram using only NOR gates.

13. a) Design a synchronous counter using JK flip flop which counts in the sequence – C
000, 010, 011, 0100, 110, 111.

(OR)

b) A sequential machine has one input line where 0's and 1's are being incident. The C
machine has to produce a output of '1' only when exactly two '0's are followed by a '1' or exactly two '1's are followed by a '0'. Using any state assignment and JK flip flop, synthesis the machine.

14. a) Design a asynchronous circuit with 2 inputs T and C. The output attains a value of 1 C
when T = 1 and C moves from 1 to 0. Otherwise the output is 0.

(OR)

b) Design an asynchronous sequential circuit with inputs A and B and an output Y. C
Initially and at any time if both the inputs are 0, the output Y is equal to 1. When A or B becomes 1, Y becomes 0. When the other input also becomes 1, Y becomes 1. The output stays at 1 until circuit goes back to initial state.

15. a) i) Draw the logic diagram for open-collector TTL NAND gate and explain its C
operation.

ii) Implement NAND and NOR logic function using CMOS circuit.

(OR)

b) Draw and write short notes on the following with an example.

1) PLA. 2) PAL.
