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ES201 Enrol. No. 077.....

[ET]

END SEMESTER EXAMINATION : NOV.-DEC., 2016

BASIC ELECTRONICS ENGINEERING

Time : 3 Hrs. *Maximum Mars : 70*

Note: ***Attempt questions from all sections as directed.***

SECTION – A (30 Marks)

Attempt any **five** *questions out of* **six.**
Each question carries **06** *marks.*

1. Define diffusion capacitance of a PN junction diode. Obtain an expression for the same. Explain V-I Characterstics of PN junction diode.

2. (a) Draw the output of given clipper circuit shown in Figure 1, Diode A is (Si), diode B is (Ge). (3)

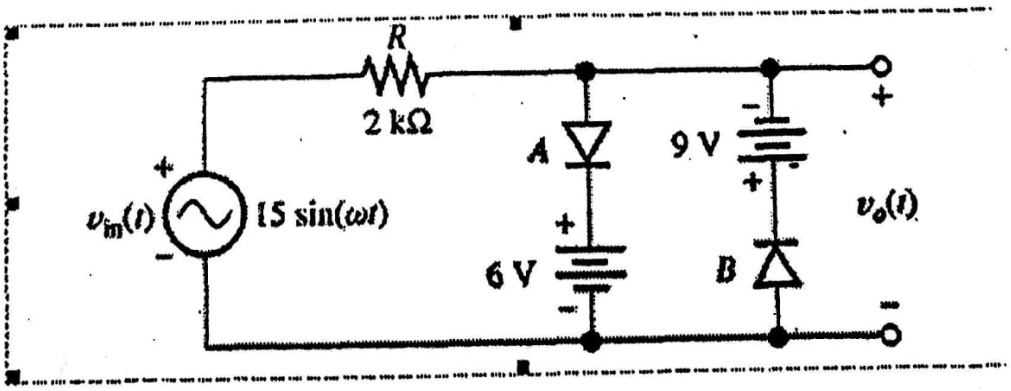


Figure 1

(b) Draw the output of given clamper circuit shown in Figure 2. (3)

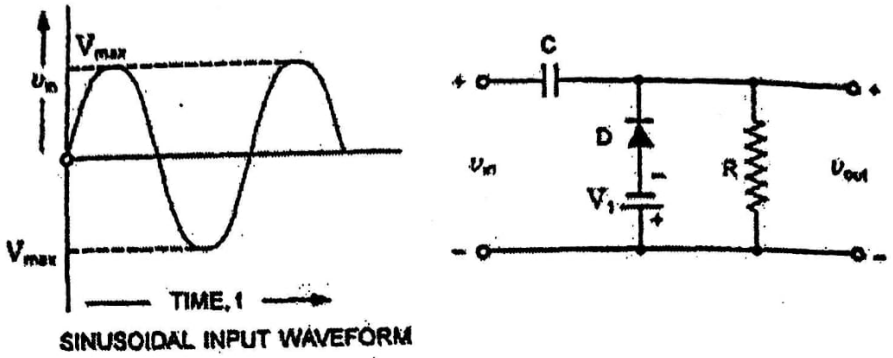


Figure 2

3. State and prove De Morgan's theorem. Draw truth table and implement full adder using only universal gate NAND.

4. Draw the circuit diagram of non-inverting operational amplifier (OP-AMP) and drive the expression for its closed loop voltage gain. Locate the virtual ground point in the circuit and explain its significance.

5. Reduce the following function in SOP form using K–Map.

$$F = \Sigma(5,7,8,10,13,15) + \Sigma d(0,1,2,3)$$

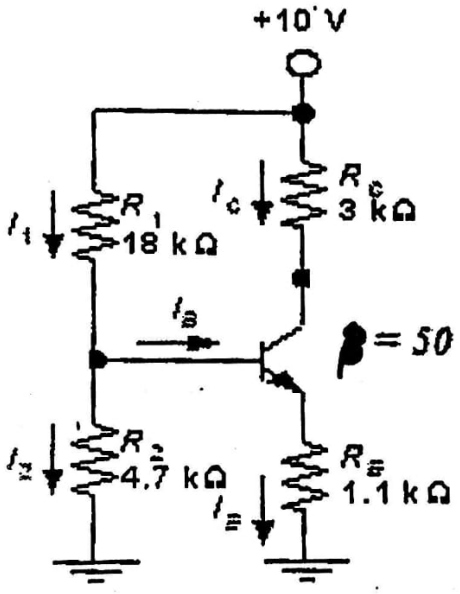
Implement the simplified function using only NAND gate.

6. Explain the working of common base configuration of NPN transistor with the help of circuit diagram. Sketch input and output fiaracteristics and indicate active, cut-off and saturation region.

SECTION – B (20 Marks)

Attempt any **two** *questions out of* **three.**
Each question carries **10** *marks.*

7. Explain why the operating point is fixed in the center of active region of transistor characteristics in a good voltage amplifier. Determine the values of I_{CQ} and V_{CEQ} for the circuit shown in Fig:



8. Why FET is known as unipolar device ? In a common source amplifier drain resistance $R_D = 5K\Omega$, $\mu = 50$ and rd = 35KΩ. Evaluate voltage gain A_V and output resistance Ro.

9. Draw the circuit diagram and explain the working of differential amplifier. An OP-AMP has a slew rate of 1V/μs. The input signal changes by 0.5 V in 10 μs. What can be the closed loop gain of the amplifier ?

P.T.O.

SECTION – C (20 Marks)

(Compulsory)

10. (a) Show how Zener diode can be used as a voltage regulator. In a Zener diode voltage regulator circuit the source series resistance Rs. = 20 ohm zener voltage Vz = 18 volt and lode resistance R_L = 200 ohm. If source voltage Vs can vary from 20 volt to 30 volt find the maximum and minimum current in the diode ? (10)

(b) Explain Depletion type MOSFET structure and operation with the help of circuit diagram. Prove that the transconductance gm of JFET is given by $g_m = 2\sqrt{I_D I_{DSS}}/V_P$ (10)