ABV- Indian Institute of Information Technology & Management, Gwalior
Semester-II (BCCS-1203)

Minor

Course Title: Digital Circuit System

Duration: 2:00 Hours

MM: 30

Note:

1. All parts of a question should be answered consecutively.
2. Question paper has three sections and all the sections are compulsory.

SECTION A **10x1=10**

(1) Design astable/bistable multivibrator using one XOR and two NOT gates.

(2) Using BJT (Transistor), design logic circuit for following Boolean expression.

$$Y=(A+B)\,C+\bar{D}$$

(3) For the logic circuit shown in the figure below, the required input condition (A, B, C) to make output $(X) = 1$.

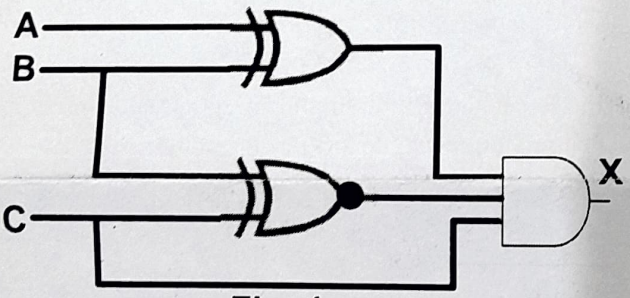


Fig: 1

(4) Implement $Y = A\bar{B}C$ using minimum number of 2-input NAND gates.

(5) Convert $(48)_{10}$ into Excess-3 code.

(6) The figure shows the internal schematic of a TTL AND-OR inverter (AOI) gate. For the input shown in the figure the output Y is.

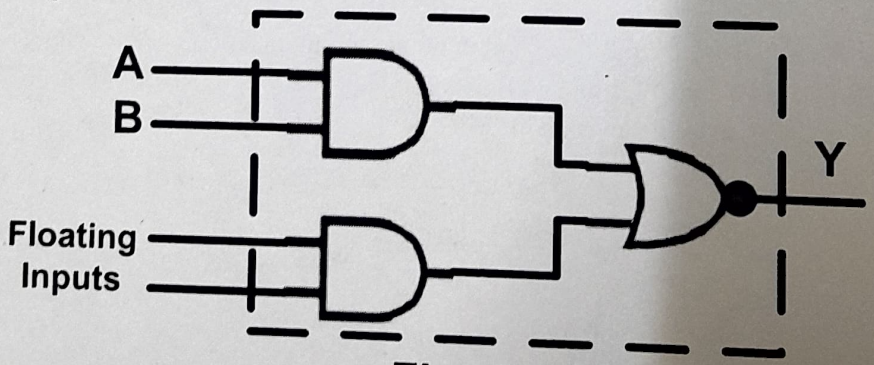


Fig: 2 TTL

(7) Given $X = (1101010)_2$ and $Y = (0101011)_2$, (a) find X-Y and (b) find Y-X using 2's complements.

(8) Minimize the logical Boolean expression $Z = (X.\bar{Y}) + (\bar{X}.Y)$ into reduced form.

(9) In a number system with radix "r", the decimal value of $(110)_r$ is equal to 12. Calculate the decimal values of 110 and r.

(10) Subtract $(3A5)_{16}$ from $(592)_{16}$. using 2's complement

SECTION B

(1) For the given digital circuits draw the timing diagram and calculate the duration of glitch. [5]

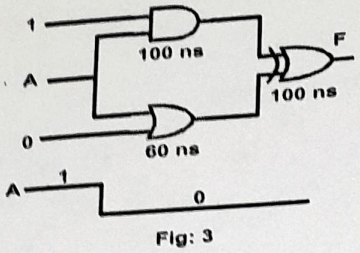


Fig: 3

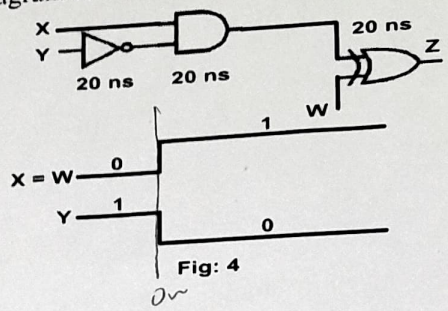


Fig: 4

(2) Map 3-variable K-MAP into 4-variable K-MAP. Also design logic circuit using minimum number of logic gates. [5]

X \ YZ	00	01	11	10
0	0	0	1	$\overline{W}$
1	1	W	0	0

W --- MSB

Z --- LSB

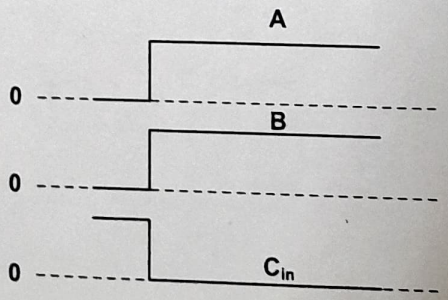
OR

(3) For the given K-map, find Implicant, Prime Implicant, Essential Prime Implicant, Redundant Prime Implicant, and Selective Prime Implicant. Also give the reduced Boolean expression and its logic circuit. [5]

1			1
1			1
1			
1		1	1

SECTION C

(1) Design a full adder from truth table and draw the timing diagram at following given inputs. Also calculate max (Tsum, Tcarry) for given propogation delay of gates (AND = 10 ns, XOR = 30 ns, and OR = 20 ns) and carry input delay is 10 ns. [5]



(2) Design a two-bit (inputs) comparator with output A=B, A>B, and A<B for given variables A&B. Use AND-OR logic to design circuit. [5]

OR

(3) Given $F(w,x,y,z) = \Sigma(0,1,2,3,7,8,10) + \Sigma d(5,6,11,15)$. What is the minimum POS form of F(w,x,y,z)? Further, design a logical circuit using resistor and BJT. [5]