B.Tech. (Computer Science & Engineering) Third Semester (C.B.C.S.)
Computer Architecture & Digital System

P.Pages : 2

Time : Three Hours

PSM/KW/23/2572

Max. Marks : 70

Notes :
1. All questions carry marks as indicated.
2. Solve Question 1 OR Questions No. 2.
3. Solve Question 3 OR Questions No. 4.
4. Solve Question 5 OR Questions No. 6.
5. Solve Question 7 OR Questions No. 8.
6. Solve Question 9 OR Questions No. 10.
7. Due credit will be given to neatness and adequate dimensions.
8. Assume suitable data whenever necessary.
9. Illustrate your answers whenever necessary with the help of neat sketches.

1. a) What is Logic Gate. Explain different logic gates along with its truth table. 7

   b) Implement the following Boolean function with 8:1 multiplexer
      $F(A, B, C, D) = \Pi m(0, 3, 5, 6, 8, 9, 10, 12, 14)$ 7

OR

2. a) Simplify the following logic expression using K-map and realize using NAND gates
      $f(A, B, C, D) = \Pi m(0, 2, 6, 10, 11, 12, 13) + (3, 4, 5, 14, 15)$. 7

   b) State and Explain Demorgan's Law. 7

3. a) Explain basic operational concept. 7

   b) Explain various addressing modes with example which are used in instruction set design. 7

OR

4. a) Solve the following expression using
      i) Zero address   ii) One address
      iii) Two address   iv) Three address
      $Z = (A + B - C) * (C - D + E) / (A * B - C)$ 7

   b) Explain different Bus Organization along with its advantages and disadvantages. 7

5. a) Explain Hardwired Control Unit. 7

   b) Explain single bus architecture of Processing Unit. 7

OR

6. a) Explain Micro-Programmed Control Unit. 7

   b) Define and explain the control sequence of execution of complete instruction. 7

7. a) Solve the following by using Booth's algorithm. 7
      47 x – 3

   b) Design a carry look ahead adder. 7

<div align="center">OR</div>

8. a) Represent- 7
      i) $(-450.725)_{10}$
      ii) –0.000125
      in double precision IEEE format.

   b) Explain hardware for integer division. Divide 17 by 3 using restoring method. 7

9. a) Find the page hit and page fault ratio for the given page address stream using. 7
      i)   Least recently used
      ii) Optimal page replacement policy
           Assume four page buffers.
           Page address stream → [2, 3, 2, 1, 5, 2, 4, 5, 3, 2, 5, 2]

   b) Explain the concept of memory hierarchy and characteristics of memory. 7

<div align="center">OR</div>

10. a) Differentiate between IO mapped I/O & memory mapped I/O devices. 7

    b) Explain the concept of Interrupt with all its types. 7

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