



Continuous Assessment Test - I

Programme Name & Branch:

BTECH COMPUTER SCIENCE AND ENGINEERING

Course Name & Code: MICROPROCESSOR AND INTERFACING TECHNIQUES CSE 2006

COMMON TO ALL BATCHES

Slot: C1

Exam Duration: 1.30 Hr. Maximum Marks: 50

Part A.

Answer all questions

5 x 10 = 50 marks

- ✓ Discuss in detail the pipelined architecture of 8086 microprocessor supported with internal block diagram. Briefly explain the physical memory organization of 1Mbytes of memory and physical address formation 8086.
- Explain the functions of the signals of 8086 mentioned in the following Table 2.1. Also indicate their mode of operation in 8086.

HOLD /HLDA	RQ/GTo, RQ/GT1
JWR .	FOCK
WIO	-52- S1 S0
JØT/R	WEN
ØSo QS1	VALE

Table 2.1

Describe the addressing modes of 8086 mentioned in the following Table 3.1. Briefly explain at least two example instructions for every addressing mode with effective address formation for memory operands.

Register Indirect	Indexed
Register Relative	Based Indexed
Relative based Indexed	

Table 3.1

A. Explain the assembler directives of 8086 mentioned in the Table 4.1. Give examples for every assembler directive mentioned in the Table 4.1.

Assembler Dire	ective	
WB , DW & DT		
€QU (equate)		
ØFFSET		
ASSUME		
LOCAL & GLO	BAL	

Table 4.1

- (5) Write an assembly language program using the instruction set of 8086 to find the factorial of a given number initialized in data segment.
- W) Write an assembly language program using the instruction set of 8086 to generate Fibonacci series with number of terms initialized.