VIT
Vellore Institute of Technology

Final Assessment Test – November 2019

Course: ECE3002 - VLSI System Design
Class NBR(s): 2412
Slot: B2+TB2
Time: Three Hours
Max. Marks: 100

KEEPING MOBILE PHONE/SMART WATCH, EVEN IN 'OFF' POSITION, IS EXAM MALPRACTICE

Answer ALL Questions
(10 X 10 = 100 Marks)

1. Determine the mode of operation (saturation, linear, or cutoff) and drain current *ID* for each of the biasing configurations given below. Verify with SPICE. Use the following transistor data: NMOS: $k'n$ = 115μA/V², $VT0$ = 0.43 V, λ = 0.06 V⁻¹, PMOS: $k'p$ = 30μA/V², $VT0$ = −0.4 V, λ = -0.1 V⁻¹. Assume (W/L) = 1 and neglect body effect.
   a) NMOS: VGS = 2.5 V, VDS = 2.5 V. PMOS: VGS = −0.5 V, VDS = −1.25 V.
   b) NMOS: VGS = 3.3 V, VDS = 2.2 V. PMOS: VGS = −2.5 V, VDS = −1.8 V.

2. a) Explain the following short channel effects
   (i) Channel length modulation.
   (ii) Body effect. **[5]**

   b) Types of power consumption, dependence on V, f, and C. Write the equation for dynamic power consumption and the equation for static power consumption. Explain the circuit characteristics (e.g., V_t, temperature, or gate size) that each depends on. **[5]**

3. a) What is the output function of the circuit shown in Fig.1 **[5]**

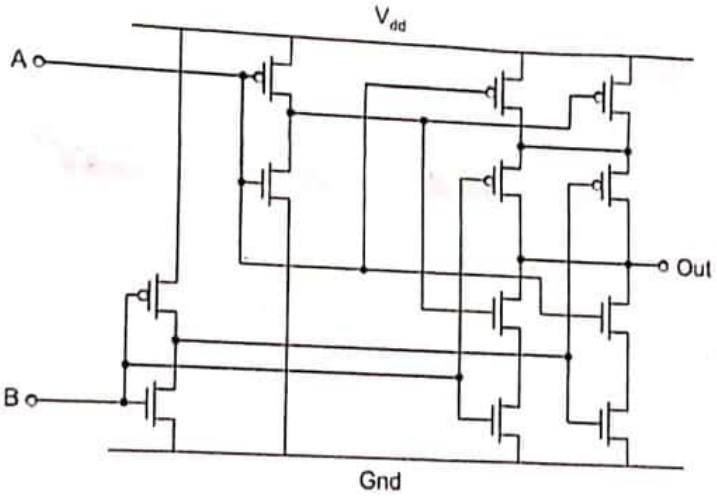


Fig.1

   b) Implement 1-bit comparator using PMOS PTL. **[5]**

4. Implement $f(a,b,c,d) = ab'cd' + a'c' + dab$ using TG and NMOS pass transistors.

5. a) Sketch a 2-input NOR gate with transistor width chosen to achieve effective rise and fall resistance equal to a unit inverter. Compute the worst case rising and falling propagation delay of the NOR gate driving "h" identical NOR gates using the Elmore delay model. If C= 2fF/μm and R=2.5KΩ/μm in a 90nm process. What is the delay of a fanout of 3 NOR gates (2-input)?

[OR]

   b) Implement the following function as a single CMOS logic gate. Indicate the widths of all gates in terms of k, the minimal gate width. Size the transistors to achieve the same worst case resistance as a balanced minimal width inverter (i.e., an inverter with a k-wide NMOSFET and a 3k-wide PMOSFET). Estimate the rise and fall propagation delay of CMOS logic gate.

$$f(a,b,c,d) = \bar{a}\,(b\bar{c} + d)$$

6. Size the circuit given in Fig.2 for minimum delay. Show delay on each path.

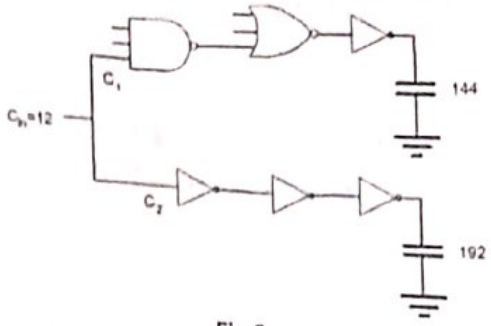


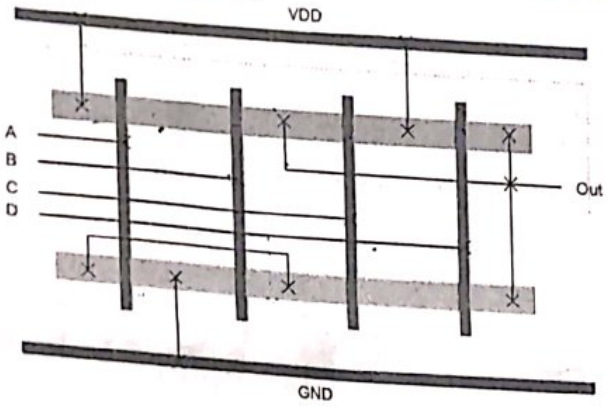
Fig.2

7. a) Sketch a layout diagram for a CMOS gate computing the following expression and estimate the optimized area using lambda based rules.

$$Z = \overline{A + B + (C \cdot D)}$$

[OR]

b) Sketch the schematic for the layout shown in Fig.3. Determine the Boolean expression for the gate. Also estimate the optimized area using lambda rules.



$256\lambda^2$ / $(A+B).CD$

Fig.3

8. Consider the dynamic gate shown in the Fig.4. Based on the input signals draw the output signal. Implement the output function using DCVSL.

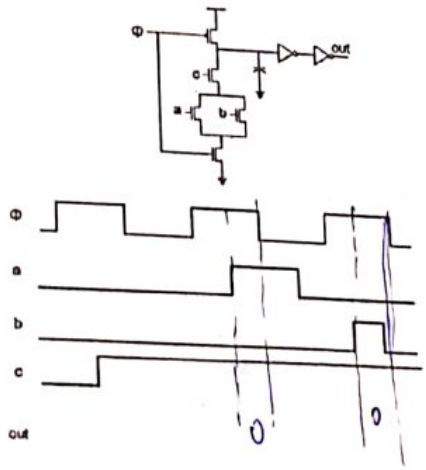


Fig.4

9. Design a negative edge triggered Master-Slave D-FF based on switching keys with asynchronous SET and RESET inputs. Explain its operation with timing diagram.

10. Design the 8 bit right barrel shifter using 2x1 Multiplexers.

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