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Paper Code : OE-EE501C/OE-EEE501C Computer Organization

UPID : 005517

Time Allotted : 3 Hours *Full Marks :70*

The Figures in the margin indicate full marks.
Candidate are required to give their answers in their own words as far as practicable

Group-A (Very Short Answer Type Question)

1. Answer *any ten* of the following : [1 x 10 = 10]

(I) What is Computer Organization?

(II) What is Content Addressable Memory (CAM)?

(III) Represent decimal number -0.75 in IEEE single precision floating point format.

(IV) What is the difference between LOAD and STORE instruction?

(V) What are different functional units of a computer?

(VI) In IEEE754 32-bit representations, how many bits are used to store the mantissa?

(VII) What are the three states in a tri-state buffer?

(VIII) What is maskable interrupt?

(IX) What is the difference between MAR and MDR?

(X) What is the largest possible value for n bit 2's complement binary number?

(XI) How many address lines are required to access a 512 X 8 bit of memory?

(XII) What is Polled I/O technique?

Group-B (Short Answer Type Question)

Answer *any three* of the following : [5 x 3 = 15]

2. Compute division of 13 by 5 using Non- restoring division algorithm. [5]

3. An instruction" LOAD AC" is stored at location 200 with its address field at location 201. The address field has the value 500. Evaluate the effective address and Content of AC after execution of this statement if the addressing mode of the instruction is i) direct ii) immediate iii) relative [5]

4. Consider the following memory references: [5]
1,2,1,3,7,4,5,6,3,1
There are three blocks in cache memory. How many misses occur for the following page replacement policies?
(i) LRU (ii) FIFO

5. A digital computer has a common bus system for 16 registers of 32 bit each. The bus is constructed with multiplexers. [5]
i) How many selection inputs are there in each multiplexer?
ii) How many multiplexers are there in the bus?

6. Explain difference between hardwired control unit and microprogrammed control unit. [5]

Group-C (Long Answer Type Question)

Answer *any three* of the following : [15 x 3 = 45]

7. (a) In a computer, there are 30 processor registers, 6 addressing modes and 32K X 32 main memory. Each instruction (having size of 32 bits) supports one register operand and one memory address operand. State the instruction format, after finding out the size of each field. [5]

(b) Consider the instruction "Load A,R1", which means value is read from memory location A into the CPU register R1. Describe the sequence of steps needed for the CPU to fetch and execute the above instruction. You may assume any suitable CPU architecture. [5]

(c) Evaluate the arithmetic statement X=(A+B)-(C+D) using (i) zero address instructions and (ii) two address instructions format [5]

8. (a) In a hierarchical memory system, cache access time is 100ns and main memory access time is 1000ns. Hit ratio of cache is 0.9 for read access and 85% of the memory requests are for read. [5]

Calculate the average access time of the memory system for both read and write requests. Consider Write Through policy.

(b) From the entry in a segment table, it is understood that segment #0 has base address 215 and length of 500 words, segment #1 has base address 2000 and length of 160 words, segment #2 has base address 1200 and length of 40 words. Find out the physical addresses corresponding to the following logical addresses? [4]
(i) 0, 430 (ii) 1, 234 (iii) 2, 13 (iv) 1, 100

(c) How are "Tag" bits used in cache memory systems? Explain with reference to the three cache mapping techniques. [6]

9. (a) Discuss the Memory Hierarchy in computer system with respect to Speed, Size and Cost? [8]

(b) Explain about main memory and its types. [7]

10. (a) Explain Booth's algorithm. [4]

(b) Apply Booth's algorithm to multiply the signed numbers +13 and -6. [8]

(c) Add +5 and -9 using 2's compliment method. [3]

11. (a) State one advantage and one disadvantage of memory-mapped IO, compared to IO-mapped IO. [3]

(b) Describe step-by-step what happens when the CPU is interrupted while it was executing the i th instruction of a program. [3]

(c) Describe briefly, the sequence of events involved in DMA Transfer. [6]

(d) Consider a 4 segments pipeline with 20 ns clock period. Find out speedup for 100 tasks. [3]

*** END OF PAPER ***