Final Assessment Test (FAT) - APRIL/MAY 2023

Programme	**B.Tech**	Semester	**Winter Semester 2022-23**
Course Title	**COMPUTER ARCHITECTURE AND ORGANIZATION**	Course Code	**BCSE205L**
Faculty Name	**Prof. Bhanu Chander Balusa**	Slot	**D1+TD1**
		Class Nbr	**CH2022235000645**
Time	**3 Hours**	Max. Marks	**100**

Part A (10 X 10 Marks)
Answer All questions

01. i) Express the following statement in 3 address instruction format. Assume that the program is available from address location $(500)_{16}$ onwards and the data is stored from memory location $(2000)_{16}$ onwards and each address is 40 bits in length. (4 marks) [10]

X=(A-B)/(C*3)

ii) Demonstrate John Von Neumann IAS architecture using the above expression with suitable diagram and give detailed explanation on the content of all the required registers. (6 marks)

02. Illustrate how the Booth's algorithm is implemented in the processor for multiplying the following signed numbers. (10 marks) [10]

Multiplicand : $(011001)_2$

Multiplier : $(111100)_2$

03. i) Represent $-(125.25)_{10}$ in IEEE double precision format. (5 marks) [10]

ii) Perform floating point addition for the given numbers $(0.25)_{10}$ and $(0.45)_{10}$. Represent the final answer in single precision format (5 marks)

04. i) Write an assembly language program to evaluate the statement X = (2/3) x (3Y−6). [1

a) Using a stack organized computer with zero address instruction format (3 Marks)

b) Using two address instruction format (3 Marks)

ii) Given the following memory address in the word and its corresponding accumulator value in a one address machine: Word 20 contains 40, Word 30 contains 45 and Word 40 contains 50. What values do the following instructions load into the accumulator after execution? (4 marks)

Load DIRECT 20

Load INDIRECT 20

Load DIRECT 30

Load IMMEDIATE 40

05. i) Consider a main memory of size 32 bytes and a direct mapped cache with block size of 2 bytes, illustrate how the memory addresses 10101, 11001, 11011, 11110, 01110, 10000, 11001, 11011, 10010, 10011 map to the cache lines 0(000) to 3(011). Determine the hit and miss ratio. (5 marks)

ii) Apply appropriate replacement strategy that evicts the block that is not referenced for long time, assuming that fully associative mapping is used for the above addresses. Discuss how this can reduce the miss ratio. (5 marks)

06. i) Identify the I/O accessing mechanism used for communication between high speed devices and memory. Discuss this mechanism in detail with appropriate diagram. (5 marks)

(c) There are 3 devices A, B and C requesting for bus control with IDs: 0101, 1000, and 0110 respectively. Identify the device that can become bus master using distributed arbitration technique. (5 marks)

08. Consider a bit stream 10101101 transmitted using the standard error detection method that uses a generator polynomial expressed as $x^4 + 1$ [10]

i) Apply the appropriate error detection method and deduce the actual bit string transmitted. (5 Marks)

ii) Suppose the fourth bit from the left is inverted during the transmission, help the receiver in detecting this error. (5 Marks)

09. i) A web service application is handling millions of user requests and sensitive data. Identify the appropriate hybrid RAID levels that are used to increase the performance and reliability of data storage and discuss in detail with a diagram. (5 Marks) [10]

ii) If a drive fails, you still have access to all the data, even while the failed drive is being replaced and the storage controller rebuilds the data on the new drive. Which RAID level is more secure? Justify your answer. Discuss with appropriate diagram. (5 Marks)

09 i) A company uses a 5-stage pipelining for instruction execution in their processor named "Arch". These stages of pipelining takes a time duration of 90ns, 115ns, 110ns, 70ns and 130ns respectively to execute a task. Registers with a delay of 5ns are used before each stage to avoid cycle mismatch. Find the total time taken to process 750 instructions on this pipeline assuming a constant clock rate. (5 marks) [10]

ii) According to Flynn's taxonomy, multiple instruction single data category of parallel processing is practically feasible. Comment on the trueness of this statement with valid justification using a specific scenario. (5 marks)

10. i) Consider the following sequence of instructions executed in a processor using pipeline architecture [10]

[1] ADD R2, R1, R7

[2] AND R2, R12, (R19)

Identify the specific type of data hazard for the given instructions with proper justification. Discuss the other data hazards which are not observed in the given sequence of instructions with necessary examples. (6 marks)

ii) Specify the steps available to eliminate the above hazards. (4 marks)