MAULANA ABUL KALAM AZAD UNIVERSITY OF TECHNOLOGY, WEST BENGAL

IT-705D

MICROELECTRONICS AND VLSI DESIGN

Time Allotted: 3 Hours | Full Marks: 70

The questions are of equal value.
The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable.
All symbols are of usual significance.

GROUP A
(Multiple Choice Type Questions)

1. Answer any *ten* questions. 10×1 = 10

(i) Synthesis translate from

(A) physical description behavioral description
(B) structural to physical description
(C) behavioral description to structural description
(D) structural description to behavioral description

(ii) FPGA is a

(A) Full custom ASIC (B) Semi custom ASIC
(C) Programmable ASIC (D) Structured ASIC

(iii) Which technology is not use in FPGA

(A) Static Technology (B) Dynamic Ram
(C) Anti-fuse Technology (D) EEROM Technology

(iv) CLBs stand for

(A) gate array design style
(B) slandered cell based design
(C) field programmable gate array layout
(D) full custom design

(v) The example of physical defect is

(A) oxide de-effects (B) resistive shorts and opens
(C) slower transition (D) none of these

(vi) LUT is used in

(A) CPLD (B) ASIC
(C) FPGA (D) SPDL

(vii) What is the full form of VSDL

(A) Very High Speed Digital Logic
(B) Verilog Hardware Description Language
(C) Very High Digital Language
(D) None of these

(viii) In PLA

(A) only AND array is programmable
(B) only OR array is programmable
(C) both AND and OR array are programmable
(D) microcell is the binding block

(ix) Which of the following is not the part of the FPGA

(A) RTL (B) I/O
(C) PI (D) CLB

(x) In which type of ASIC, the cell size is variable?

(A) full custom (B) standard cell
(C) gate array (D) FPGA

(xi) Min-cut algorithm is a

(A) placement algorithm (B) routing algorithm
(C) testing algorithm (D) floor planning algorithm

GROUP B
(Short Answer Type Questions)

Answer any *three* questions. 3×5 = 15

2. What is ASIC? What is the advantage of ASIC? Describe ASIC Design flow? 2+1+2

3. What is Y chart? Describe the steps of digital VLSI design? 2+3

4. What is FPGA? Describe the basic architecture of FPGA? 2+3

5. Draw a 2 input NAND gate using lay out technique? Derive the current voltage equation of the n-channel MOSFET? 3+2

6. Write a VSDL code in behavioral mode for full adder. 5

GROUP C
(Long Answer Type Questions)

Answer any *three* questions. 3×15 = 45

7. (a) What is the advantage of VLSI technology? What are the challenges of VLSI technology? 3+2
(b) Describe the FPGA Design flow? Explain the feature of ASIC? 3+2
(c) Explain the front end and back end process in a VLSI design process? What is noise margin? 4+1

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8. (a) How logic capability of PLA is measured? 3
(b) What is the different between PAL and PLA? 2
(c) Implements the following function using PLA: 5
(i) f = A'B + AB'
(ii) f = A + (B + C').D
(d) Explain the architecture of PLD? 5

9. (a) Describe p-well fabrication mode with proper diagram? 8
(b) What is stick diagram? 1
(c) Describe CMOS inverter with stick diagram? 3
(d) Explain short channel effect of MOS structure? 3

10.(a) What are the different styles of describing the architecture of VSDL? Explain with example. 9
(b) Write down VSDL code for 4 to 1 MUX and obtain the code for 16 to 1 MUX using this 4 to 1 module? 6

11. Write short notes on any *three* of the following: 3×5
(a) n-well fabrication
(b) Body Effect
(c) NOR gate using CMOS
(d) Look Up Table (LUT) for FPGA
(e) Types of VLSI Chips.

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