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Paper Code : IT-502

COMPUTER ARCHITECTURE

Time Allotted: 3 Hours

Full Marks: 70

The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable.

Group – A

(Multiple Choice Type Questions)

1. Choose the correct alternative of the following: 1×10=10

(i) The number of cycles required to complete n takes in a K stage pipeline is
  (a) K cycles
  (b) K+(n+1) cycles
  (c) K+n cycles
  (d) None of the above

(ii) A computer with cache access time 100ns, main memory access time 1000ns and a hit ratio of 0·9 produces the average access time
  (a) 250ns
  (b) 200ns
  (c) 190ns
  (d) None of the above

(iii) A 4-ary 3-cube hypercube architecture has
  (a) 3 dimensions with 4 nodes along each dimension.
  (b) 4 dimensions with 3 nodes along each dimension.
  (c) Both (a) and (b)
  (d) None of the above

Turn Over

(iv) What is the speed up for a four stage pipeline when the number of instructions n = 64?
(a) 4·5
(b) 6·5
(c) 7·1
(d) None of the above

(v) Dynamic pipeline allows
(a) multiple functions to evaluate.
(b) only streamline connection.
(c) fixed function to evaluate.
(d) None of the above

(vi) Consider a main memory of size 32K X 12 and cache memory of size 512 X 12 and block size of 1 word. The addressing relationship using direct mapping would be
(a) Tag field 6 bits, index field 9 bits
(b) Tag field 9 bits, index field 6 bits
(c) Tag field 7 bits, index field 8 bits
(d) None of the above

(vii) Branch penalties occur in which type of hazard?
(a) Instruction hazard
(b) Data hazard
(c) Structural hazard
(d) None of the above

(viii) In which cases data hazard occurs?
(a) RAW
(b) RAR
(c) Both (a) and (b)
(d) None of the above

(ix) Latency implies
(a) Time delay between two procedure calls.
(b) Time period of one clock cycle.
(c) Evaluation time.
(d) None of the above

(x) In case of Direct Mapped Cache we need _____ gates for the generation of the match bit where n is the number of the tag fields.
(a) 15n
(b) 13n
(c) $(13 \times n) + n$
(d) $(13 \times n) + 1$

Group – B
(Short Answer Type Questions)

Answer *any three* of the following. 5×3=15

2. Compare Superscalar, Superpipeline and Superscalar Superpipeline Processor.
3. Explain the main factors influencing the performance of interconnection networks.
4. Explain S access and C access memory organization.
5. What is RAW Hazard? Explain two solution techniques of Raw with example. 1+4=5
6. Describe Dataflow Architecture. Compare Dataflow Computer with Control Flow Computer.

Group – C
(Long Answer Type Questions)

Answer *any three* of the following. 15×3=45

7. (a) Define and compare linear pipelining and non-linear pipelining.

   (b) Consider the following reservation table for a four stage pipeline:

	1	2	3	4	5	6
S1	X					X
S2		X		X		
S3			X			
S4				X	X	

   (i) What are the Forbidden Latencies and the Initial Collision Vector?

   (ii) Draw the State Transition diagram for scheduling the pipeline.

   (iii) Determine the Gready Cycle among the Simple Cycle.

   (iv) Determine the minimum average latency, and upper and lower bound on MAL.

   (c) Determine speed up of Pipeline Processor compared to Non Pipeline Processor. What are efficiency and throughput of pipeline processor? 4+(2+3+1+2)+(1+2)=15

8. (a) What is Cycle Per Instruction (CPI) and Million Instruction Per Second (MIPS)? Derive equation for CPI and MIPS.

(b) Consider the execution of an object code with 1,00,000 instructions on a 40 MHz processor. The program consist of four major types of instructions. The instruction mix and number of cycle needed for each instruction type are given below:

Instruction type	Number of cycles needed for each instruction	Instruction mix
Arithmetic and logic	1	60%
Load/store with cache hit	2	18%
Branch	4	12%
Memory reference with cache miss	8	10%

(i) Calculate the average CPI.

(ii) Calculate the corresponding MIPS based on the CPI.

(c) According to Flynn classification define different type of computer architecture. 4+(2+2)+7=15

9. (a) You are asked to perform to capacity planning for a two level memory system. The first level M1 is a cache with capacity 64KBytes. Second level M2 is a main memory with a 4MByte capacity. Let c1 and c2 be the cost per byte and t1 and t2 the access time for M1 and M2 respectively. Assume c1=20c2 and t2=10t1. The cache hit ratio is 0·7.

(i) What is the average access time in terms of t1=20ns?

(ii) Express the average Byte cost of the entire memory hierarchy if 2=$0·2/Kbyte.

(b) Explain different type of locality associated with program/data access in memory hierarchy.

(d) Define different technique for reducing miss penalty. (3+3)+4+5=15

10. (a) What is connection network?

(b) Compare node degree and diameter for linear array, ring, barrel shifter, tree and mesh connection.

(c) Define and compare Omega network and Baseline network and Baseline network with suitable diagrams. 2+5+4+4=15

11. Write short notes on *any three* of the following: 5×3=15

(i) Systolic architecture

(ii) VLIW architecture

(iii) Reduction machine

(iv) Compiler technology to improve performance

(v) Vector processor
