Reg. No. : E N G G T R E E . C O M

Question Paper Code : 41029

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2024.

Third Semester

Electrical and Electronics Engineering

EE 3302 — DIGITAL LOGIC CIRCUITS

(Regulations 2021)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Define Propagation Delay.

2. Show $(377)_{10}$ in Octal and Hexa-Decimal equivalent.

3. Simplify the Expression $Z = AB' + AB(A'C')'$.

4. What is K-map?

5. What is flip-flop?

6. Differentiate Mealy and Moore models.

7. What is Static Hazard and Dynamic Hazard?

8. State the difference between Static 0 and Static 1 Hazard.

9. Expand the following acronyms.

   (a) VHDL

   (b) VHLSI.

10. What is sequential circuit?

PART B — (5 × 13 = 65 marks)

11. (a) (i) Explain the numbering system in detail. (7)

(ii) Encode the Binary Word 1011 into Seven Bit Even Parity Hamming Code. (6)

Or

(b) (i) Explain hamming code with an example. State its advantage over parity codes. (7)

(ii) Design a TTL logic circuit for a 3 input NAND gate. (6)

12. (a) (i) Draw the logic diagram of a 4 bit carry look ahead adder and explain how this adder is advantageous over the ripple carry adder. (7)

(ii) Explain with the suitable example how a multiplexer is used to implement the Boolean function. (6)

Or

(b) (i) With Block Diagram, Explain the Full Subtractor in detail with logic diagrams. (7)

(ii) Design a Full Adder using two half adders and an OR gate. (6)

13. (a) (i) Explain the operation of Master-Slave JK flipflop in detail. (7)

(ii) Design a 5-bit ring counter and explain with its logic diagrams. (6)

Or

(b) Illustrate with Appropriate Truth Tables and Equations the 4-bit BCD ripple counters.

14. (a) Explain the various types of hazards in sequential circuit design and the methods to eliminate them. Give suitable examples.

Or

(b) (i) Find a circuit that has no static hazards and implement Boolean function $F(A, B, C, D) = \sum(0, 2, 6, 7, 8, 10, 12)$. (7)

(ii) Explain the different types of programmable logic devices with neat sketch and compare them. (6)

15. (a) Design a 3- bit Magnitude Comparator and Write the VHDL coding to realize it using Structural Modelling.

Or

(b) (i) Explain in detail the various programming constructs used in VHDL for designing a logic circuit. (7)

(ii) Discuss the various packages. Write a VHDL code for the implementation of Decoder/De-Multiplexer. (6)

PART C — (1 × 15 = 15 marks)

16. (a) Design a CMOS inverter and explain its operation. Comment on its characteristics such as Fan-in, Fan-out power dissipation, propagation delay and noise margin. Compare its advantages over other logic families.

Or

(b) Explain in detail with neat illustrations, Design a Full Adder using 4×1 multiplexer; also write its truth table and logical diagram.