

VR20



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VELAGAPUDI RAMAKRISHNA

**SIDDHARTHA ENGINEERING COLLEGE**

(AUTONOMOUS)

II/IV B.Tech. DEGREE EXAMINATION, March, 2022

Third Semester

**ELECTRONICS AND INSTRUMENTATION ENGINEERING**

**20EI3303 DIGITAL CIRCUITS & SYSTEMS**

*Time: 3 hours*

*Max. Marks: 70*

*Part-A is compulsory*

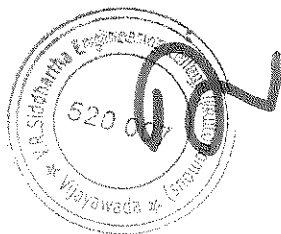
*Answer One Question from each Unit of Part - B*

*Answer to any single question or its part shall be written at one place only*

**PART-A**

**10 x 1 = 10M**

1.
  - a. What are Universal Gates?
  - b. Write the expressions for De Morgan's Laws.
  - c. What is the 10's complement of 74546?
  - d. Sketch the symbol of Exclusive OR gate with its truth table.
  - e. Name some combinational circuits.
  - f. Define flip flop.
  - g. Design a half adder.
  - h. Write the applications of multiplexer.
  - i. Difference between synchronous and asynchronous counters.
  - j. List out some programmable memories.



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**PART-B**

**4 x 15 = 60M**

**UNIT-I**

2. a. Convert the following numbers. **7M**  
i)  $(26153.7406)_8$  to binary.  
ii)  $(2155.3)_8$  to binary and then to Hexa Decimal.  
iii)  $(FACE.2)_{16}$  to decimal.
- b. Assume that the even parity hamming code is  $(0100111)_2$  is transmitted and that  $(0100011)_2$  is received. The receiver does not know what is transmitted. Determine the bit location where error has occurred in the code received. **8M**

(or)

3. a. Explain the properties of Exclusive- OR function in detail. **5M**  
b. Minimize the following using Karnaugh map. **10M**  
 $F(P,Q,R,S,T) = \sum m(1,2,3,6,13,14,15,18,19,23,24,25,26,31)$

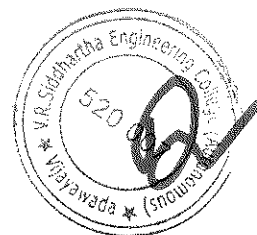
**UNIT-II**

4. a. Design a BCD to gray code converter. **8M**  
b. Construct a 4 to 16 line decoder using 2 to 4 line decoder. **7M**

(or)

5. a. Design a BCD to seven segment decoder which is need for society. **8M**  
b. Apply the following Boolean function using 4:1 MUX **7M**  
 $F(A,B,C,D) = \sum m(0,1,2,4,6,9,12,14).$

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**UNIT-III**

6. a. Analyze the operation of JK flip flop with truth table with excitation table. **7M**  
b. Discuss how can we avoid race around condition in JK flip flop. **8M**

(or)

7. a. Discuss the applications of shift registers. **7M**  
b. Convert SR Flip-Flop to D Flip-Flop. **8M**

**UNIT-IV**

8. a. Write a program for logic gates using behavioural model of VHDL. **10M**  
b. Realize the following functions using a 8X3 PROM. **5M**  
 $F_1 = \sum m(0,4,7), F_2 = \sum m(1,3,6), F_3 = \sum m(1,2,4,6)$

(or)

9. a. Write a detailed note on MOS and CMOS logic families. **7M**  
b. Explain in detail the different types of RAMS. **8M**

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