VIT
Vellore Institute of Technology

Final Assessment Test – November 2019

Course: ECE3002 - VLSI System Design

Class NBR(s): 2411

Slot: B1+TB1

Time: Three Hours

Max. Marks: 100

KEEPING MOBILE PHONE/SMART WATCH, EVEN IN 'OFF' POSITION, IS EXAM MALPRACTICE

Answer ALL Questions

(100 Marks)

1. Determine for each of the measurements the operation region of the transistor. [10]

Measurement number	VGS (V)	VDS (V)	VSB (V)	ID (uA)	Operation Region?
1	-2.5	-2.5	0	-84.375	
2	1	1	0	0.0	
3	-0.7	-0.8	0	-1.04	
4	-2.0	-2.5	0	-56.25	

2. a) Explain the following short channel effects, [5]

(i) Velocity Saturation

(ii) Sub-threshold leakage current

b) Consider the CMOS inverter with the following device parameters: [5]

nMOS : $V_{tn} = 0.4$ V $K_n = 60\ \mu A/V^2$

pMOS : $V_{tp} = -0.6$ V $K_p = 25\ \mu A/V^2$

Also let the power supply voltage be $V_{DD} = 3.0$ V and the channel length of both transistors be $L_n = L_p = 0.8\ \mu m$.

Determine the (W_n/W_p) ratio such that the inverter switching threshold voltage $V_M = 1.5$ V

3. a) What is the output function of the circuit shown in Fig.1 [5]

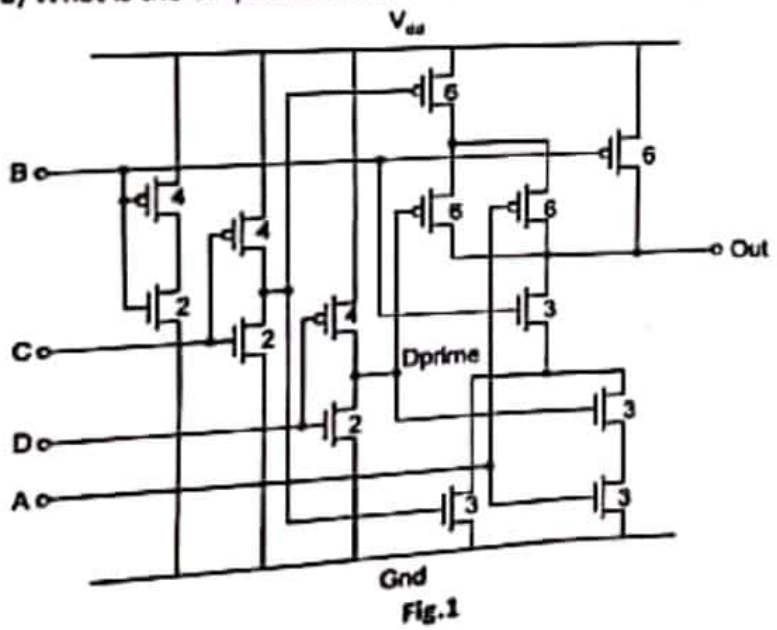

Fig.1

b) Consider the circuit of Fig.2, [5]

I) Assume that the initial voltage on $V_{out} = 0$. A step from 0 to V_{DD} is applied at the input. Determine the final voltage at V_{out}.

II) Subsequently, a negative step (from V_{DD} to 0 V) is applied at the input. Determine again the final voltage at V_{out}.

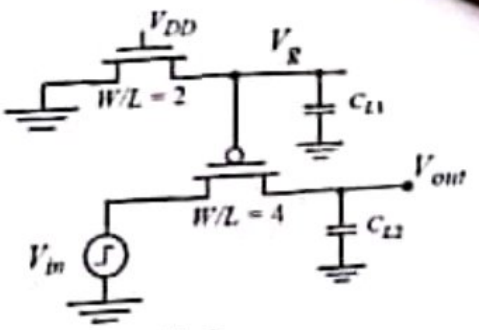

Fig.2

4. Show the circuit diagram for $f(a,b,c) = ab + \bar{a}\bar{b}\bar{c}$ implemented with Transmission gate and PMOS PTL. [10]

5.(a) Determine the worst case t_{phl} and t_{plh} transitions in the complex gate given in Fig.3 below. Assume $W_n = 2\mu m$. [10]

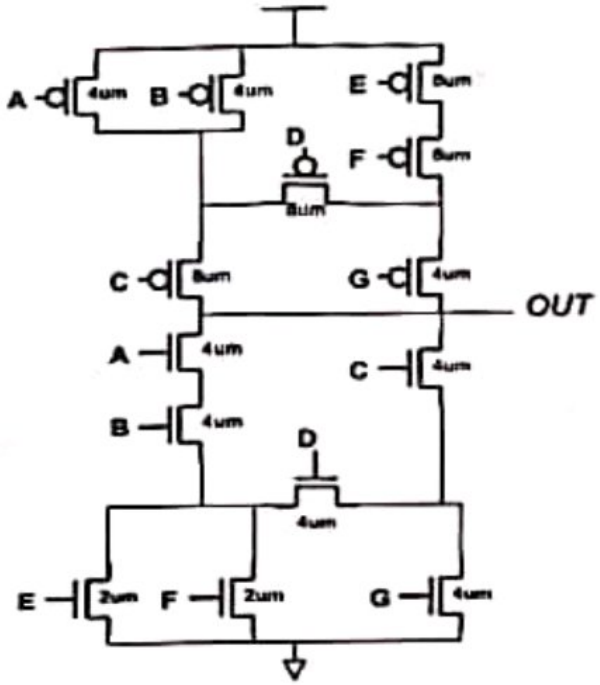

Fig.3

OR

5.(b) Size the transistors in an implementation of $f(a,b,c,d) = ab'cd' + a'c' + dab$ to achieve the same worst-case pull-up and pull-down resistances as a minimum-width balanced inverter. Explain the impact of capacitance on delay, and why considering only resistances is insufficient for perfectly balancing t_{plh} and t_{phl}. [10]

6. Use the concept of logical effort to size the gates in the circuit shown in Fig.4 to minimize the delay for path A to B. [10]

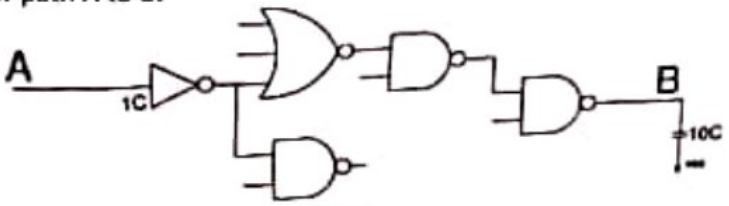

Fig.4

7.(a) Sketch the schematic for the layout shown in Fig.5. Determine the Boolean expression for the gate. [10]
Also estimate the optimized area using lambda rules.

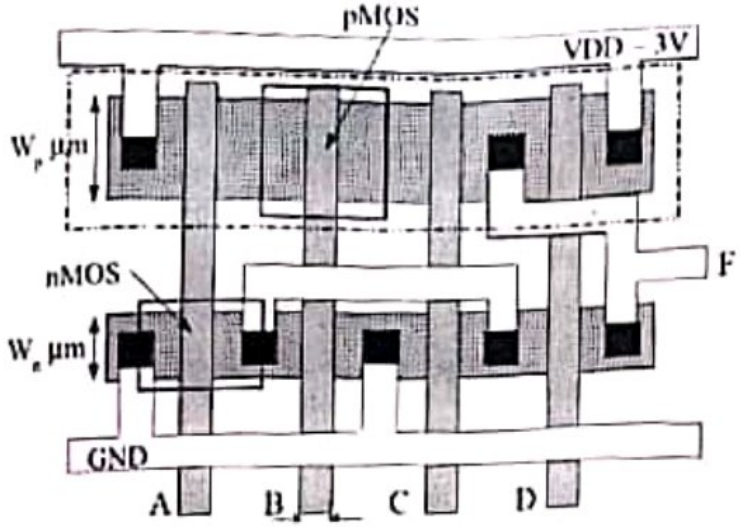

Fig.5

OR

7.(b) Design a single CMOS logic gate to perform the following function. Sketch a stick diagram for the designed CMOS gate. [10]

$Y = (\overline{A} \cdot B) + \overline{B \cdot C} + C$

8. a) List two advantages of ratioed logic, and two disadvantages of ratioed logic. [10]
b) Implement $f(a, b, c, d) = ab'cd' + a'c' + dab$ using DCVSL. State the main advantages of DCVSL.

9. The circuit shown in Fig.6 is a static or dynamic sequential circuit? Justify your answer. Is this a positive or negative latch? For which clock phase is the output equal to the input? Justify your answer. [10]

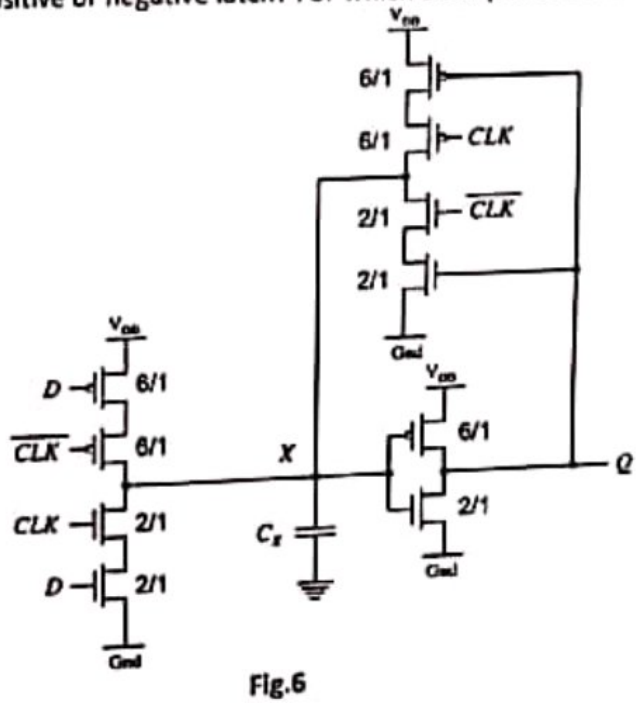

Fig.6

10. Design a carry look ahead adder and compare its speed with Ripple carry adder. [10]