VIT

Vellore Institute of Technology

CAT-1

Course: ECE3002-VLSI System Design

Programme: B.Tech (ECE)

Time: 1.5 hours

Max.Marks:50

Slot: B1+TB1

Sem: Fall 2019-20

Answer ALL Questions

1) Assume, nMOS : $V_{in} = 0.6$ V $K_n = 60\ \mu A/V^2$. Also let the power supply voltage be $V_{DD} = 3.0$ V and the width and channel length of the transistors be $W_n = L_n = 0.8\ \mu m$. Find the region of operation for each transistor in Fig.1. Find the drain current in each of the cases. (10)

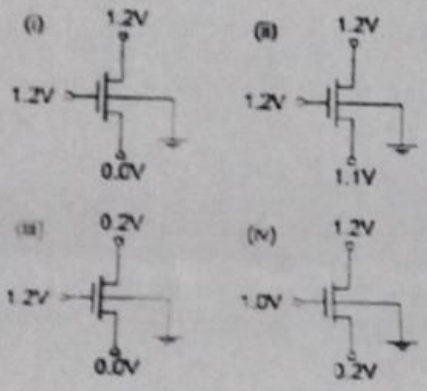

Fig.1

2) a) Consider an nMOS transistor with the following parameters: t_{ox} = 8nm, L= 0.4μm, W=0.6 μm, $L_D = L_S = 0.25\ \mu m$, $C_{jo} = 2 \times 10^{-3}$ F/m^2, and $C_{jswo} = 2.75 \times 10^{-10}$ F/m, $\varepsilon_{ox} = 3.97\varepsilon_0$, $\varepsilon_0 = 8.85 \times 10^{-14}$ F/cm, Mj = 0.4 and Mjsw = 0.25. Determine C_{DB} and C_{SB} capacitances at $V_G = 5$V. ($V_D = V_{DD} = 5$V, $V_B = 0$ and $V_S = 0$). (5)

b) Explain the following short channel effects (5)

(i) Channel length modulation.

(ii) Body effect.

3) Implement the following function F using CMOS logic and nMOS PTL. (10)

$F(A,B,C,D) = \sum(0,2,3,4,5,8,9,11,14,15)$

4) a) What is the output function of the circuit shown in Fig.2? (5)