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## Before Starting Physical Design

The RTL to GDS (Register Transfer Level to Graphic Data System) process involves multiple stages, including RTL design, synthesis, equivalence checking, Design for Test (DFT), and finally, physical design. The physical design phase transforms the netlist into a Graphic Data System (GDS) layout. To initiate the physical design, a structural netlist with precise timing constraints, generated post-DFT, is utilized. Below are the details associated with the netlist utilized for the physical design phase.

```
create_clock -name clk -period 4.22 [get_ports clk]
set_clock_transition -rise 0.5 [get_clocks clk]
set_clock_transition -fall 0.5 [get_clocks clk]
set_clock_uncertainty 0.1 [get_clocks clk]
set_input_delay -clock [get_clocks clk] 1.5 [all_inputs]
set_output_delay -clock [get_clocks clk] 0.05 [all_outputs]
set_load 1 [all_outputs]
```

## Constraint File

### Timing Information:

The "report\_timing" command in Tempus software furnishes details about different paths within the design, including the delay across each entire path. This command identifies the starting node and ending node for each path.

Static Timing Analysis operates by constructing a timing graph for the circuit and calculates the arrival time (AT) through forward traversal originating from the timing start point. It then determines the required time (RT) through backward traversal starting from the timing end point. Subsequently, it calculates the slack as the difference between RT and AT.

STA employs Graph Based Analysis (GBA) as a conservative approach, ensuring safety by considering the worst-case scenario. GBA identifies a single pessimistic path with the minimum slack value.

On the other hand, Path Based Analysis (PBA) is specific to individual paths but is computationally intensive. In PBA, the user specifies the maximum number of paths for the tool to analyze arrival times and check for slack. Therefore, PBA tends to be more accurate than GBA. PBA provides a list of 'n' pessimistic paths, ordered from the minimum slack path (path 1) to the maximum slack path.

When GBA indicates a setup or hold violation on a critical path, confirming it in a real circuit is done using PBA. If PBA doesn't show any violation, we can be confident that there's no actual violation. However, if PBA confirms the violation, then it needs to be addressed.

## AREA

```
=====
Generated by:      Encounter(R) RTL Compiler v14.10-s022_1
Generated on:      Nov 14 2024  02:10:46 am
Module:           ticket_machine_fsm
Technology library: slow
Operating conditions: slow (balanced_tree)
Wireload mode:     enclosed
Area mode:         timing library
=====

      Instance    Cells  Cell Area  Net Area  Total Area  Wireload
-----  
ticket_machine_fsm    391       2717        0       2717  <none> (D)

(D) = wireload is default in technology library
```

## POWER

```
=====
Generated by:      Encounter(R) RTL Compiler v14.10-s022_1
Generated on:      Nov 14 2024  02:18:57 am
Module:           ticket_machine_fsm
Technology library: slow
Operating conditions: slow (balanced_tree)
Wireload mode:     enclosed
Area mode:         timing library
=====

      Instance    Cells  Leakage   Dynamic   Total
                  Power(nW)  Power(nW)  Power(nW)
-----  
ticket_machine_fsm    391  12532.071  428432.497  440964.567
```

## GBA SETUP SLACK

```
#####
# Generated by: Cadence Tempus 20.10-p003_1
# OS: Linux x86_64(Host ID edatools-server2.iiitd.edu.in)
# Generated on: Thu Nov 14 02:03:34 2024
# Design: ticket_machine_fsm
# Command: report_timing -late > $report_dir/timing_report_min_time_dft_setup.rpt
#####
Path 1: MET Recovery Check with Pin fare_reg[6]/RN
Endpoint: fare_reg[6]/RN (^) checked with leading edge of 'clk'
Beginpoint: reset (v) triggered by leading edge of 'clk'
Path Groups: {async_default}
Other End Arrival Time 0.000
- Recovery 0.806
+ Phase Shift 4.220
- Uncertainty 0.100
= Required Time 3.314
- Arrival Time 3.059
= Slack Time 0.255
    Clock Rise Edge 0.000
    + Input Delay 1.500
    = Beginpoint Arrival Time 1.500
-----
Instance Arc Cell Delay Arrival Required
Time Time
-----
- reset v - - 1.500 1.755
g10192 A v -> Y ^ INVXL 1.559 3.059 3.314
fare_reg[6] RN ^ SDFFRHQX1 0.000 3.059 3.314
-----
```

The critical setup path identified by GBA starts from the begin point **reset** and ends at **fare\_reg[6]/RN**.

In this **GBA analysis**, the Required Time (RT) is calculated as the End Arrival Time (default latency of clock, which is 0 but can be modified with constraints) - Setup + Phase Shift (defined clock time period in the constraint file) - Uncertainty. In this case, it is  $0 - 0.806 + 4.220 - 0.100 = 3.314$ .

Arrival time is determined through Forward Traversal of the Timing Graph and is found to be 3.059. Hence, the Slack is computed as (Required Time - Arrival Time), resulting in a value of 0.255( no violation).

## PBA SETUP SLACK

```
#####
# Generated by: Cadence Tempus 20.10-p003_1
# OS: Linux x86_64(Host ID edatools-server2.iitd.edu.in)
# Generated on: Thu Nov 14 02:03:34 2024
# Design: ticket_machine fsm
# Command: report timing -retime path slew_propagation -max_paths 50 -nworst 50 -late -path_type full_clock > $report_dir/pba_min_time_dft_setup.rpt
#####
Path 1: MET Recovery Check with Pin state_reg[6]/CK
Endpoint: state_reg[6]/RN (^) checked with leading edge of 'clk'
Beginpoint: reset (v) triggered by leading edge of 'clk'
Path Groups: {async default}
Retime Analysis { Data Path-Slew }
Other End Arrival Time 0.000
- Recovery 0.806
+ Phase Shift 4.220
- Uncertainty 0.100
= Required Time 3.314
- Arrival Time 3.059
= Slack Time 0.255
= Slack Time(original) 0.255
    Clock Rise Edge 0.000
    + Input Delay 1.500
    = Beginpoint Arrival Time 1.500
Timing Path:
-----  
Instance Arc Cell Retime Arrival Required  
Delay Time Time  
-----  
- reset v - 0.000 1.500 1.755  
g10192 - INVXL 0.000 1.500 1.755  
g10192 A v -> Y ^ INVXL 1.559 3.059 3.314  
state_reg[6] - SDFFRHQX1 0.000 3.059 3.314
```

The most critical setup path identified by PBA begins at the startpoint **reset** and ends at **state\_reg[6]/RN**.

**In this PBA analysis**, the Required Time (RT) is calculated as the End Arrival Time (default clock latency, which is 0 but can be altered using constraints) - Setup + Phase Shift (defined clock period in the constraint file) - uncertainty. The computation yields  $0 - 0.806 + 4.220 - 0.100 = 3.314$ .

Arrival time is determined through Forward Traversal of the Timing Graph and is found to be 3.059. Therefore, the Slack is calculated as (Required Time- Arrival Time), resulting in a value of 0.255. In this case PBA and GBA gives same setup slack.

## GBA HOLD SLACK

```
#####
# Generated by: Cadence Tempus 20.10-p003_1
# OS: Linux x86_64(Host ID edatools-server2.iiitd.edu.in)
# Generated on: Thu Nov 14 02:03:34 2024
# Design: ticket_machine_fsm
# Command: report_timing -early > $report_dir/timing_report_min_time_dft_hold.rpt
#####

Path 1: MET Hold Check with Pin remaining_reg[1]/CK
Endpoint: remaining_reg[1]/SI (v) checked with leading edge of 'clk'
Beginpoint: remaining_reg[0]/Q (v) triggered by leading edge of 'clk'
Path Groups: {clk}
Other End Arrival Time      0.000
+ Hold                      0.044
+ Phase Shift                0.000
+ Uncertainty                0.100
= Required Time              0.144
Arrival Time                 0.355
Slack Time                  0.211
Clock Rise Edge              0.000
+ Clock Network Latency (Ideal) 0.000
= Beginpoint Arrival Time   0.000
-----
Instance          Arc        Cell     Delay    Arrival  Required
                    Time       Time
-----
remaining_reg[0] CK ^      -        -      0.000   -0.211
remaining_reg[0] CK ^ -> Q v SDFFRHQX1 0.355  0.355   0.144
remaining_reg[1] SI v      SDFFRHQX1 0.000  0.355   0.144
-----
```

The Worst Hold Path of GBA is mentioned above with begin point of remaining\_reg[0]/Q and endpoint of remaining\_reg[1]/SI. In the above GBA the Required Time = End Arrival Time(latency of clock which is 0 by default but can be changed using constraint) + hold + Phase Shift(clock time period defined in constraint file)+Uncertainty = 0 + 0.044+0.1 = 0.144 ns Arrival time is computed using Forward Traversal of Timing Graph.

Arrival time = 0.355

Slack = Arrival Time - Required Time = 0.211

## PBA HOLD SLACK

```
#####
# Generated by: Cadence Tempus 20.10-p003.1
# OS: Linux x86_64 (Host ID edatools-server2.iitd.edu.in)
# Generated on: Thu Nov 14 02:03:34 2024
# Design: ticket_machine fsm
# Command: report timing -retime path slew propagation -max_paths 50 -nworst 50 -early -path_type full_clock > $report_dir/pba_min_time_dft_hold.rpt
#####
Path 1: MET Hold Check with Pin remaining_reg[1]/CK
Endpoint: remaining_reg[1]/SI (v) checked with leading edge of 'clk'
Beginpoint: remaining_reg[0]/Q (v) triggered by leading edge of 'clk'
Path Groups: {clk}
Retime Analysis { Data Path-Slew }
Other End Arrival Time 0.000
+ Hold 0.044
+ Phase Shift 0.000
+ Uncertainty 0.100
= Required Time 0.144
Arrival Time 0.355
Slack Time 0.211
= Slack Time(original) 0.211
    Clock Rise Edge 0.000
    = Beginpoint Arrival Time 0.000
Timing Path:
-----
Instance Arc Cell Retime Arrival Required
          Delay Time Time
-----
- clk ^ - 0.000 -0.211
remaining_reg[0] - SDFFRHQX1 0.000 0.000 -0.211
remaining_reg[0] CK ^ -> Q v SDFFRHQX1 0.355 0.355 0.144
remaining_reg[1] - SDFFRHQX1 0.000 0.355 0.144
-----
```

The Worst Hold Path of PBA is mentioned above with begin point of remaining\_reg[0]/Q and endpoint of remaining\_reg[1]/SI.

In the above PBA the Required Time = End Arrival Time(latency of clock which is 0 by default but can be changed using constraint) + hold + Phase Shift(clock time period defined in constraint file)+Uncertainty = 0 + 0.044+0.1 = 0.144ns

Arrival time is computed using Forward Traversal of Timing Graph.

Arrival time = 0 Slack = Arrival Time - Required Time = 0.211ns. The GBA and PBA hold slack are equal.

## EFFECT OF SLEW:

Slew is the rate of transition of signal which is provided to model slow rising and falling signals for particular nodes to prevent the timing violation. So, delay increases when slew decreases.

Now we are going to change clock slew from 0.5 ns to 2 ns

### GBA SETUP SLACK

```
#####
# Generated by: Cadence Tempus 20.10-p003_1
# OS: Linux x86_64(Host ID edatools-server2.iitiid.edu.in)
# Generated on: Thu Nov 14 09:58:17 2024
# Design: ticket_machine_fsm
# Command: report timing -late > $report_dir/timing_report_min_time_dft_setup.rpt
#####
Path 1: VIOLATED Recovery Check with Pin fare_reg[6]/CK
Endpoint: fare_reg[6]/RN (^) checked with leading edge of 'clk'
Beginpoint: reset (v) triggered by leading edge of 'clk'
Path Groups: {async_default}
Other End Arrival Time      0.000
- Recovery                  1.871
+ Phase Shift                4.220
- Uncertainty                 0.100
= Required Time              2.249
- Arrival Time               3.059
= Slack Time                -0.809
  Clock Rise Edge           0.000
  + Input Delay              1.500
  = Beginpoint Arrival Time  1.500
  -----
  Instance       Arc      Cell      Delay    Arrival   Required
                           Time      Time
  -----                  -----
  -             reset v     -        -       1.500    0.691
  g10192       A v -> Y ^ INVXL   1.559   3.059    2.249
  fare_reg[6]   RN ^          SDFFRHQX1 0.000   3.059    2.249
  -----
```

We can observe above when Input clock Slew is 0.5 ns setup slack is 0.255ns and when we increase input clock slew of to 2ns the setup slack decreases to -0.809ns.

### PBA SETUP SLACK

```
#####
# Generated by: Cadence Tempus 20.10-p003_1
# OS: Linux x86_64(Host ID edatools-server2.iitiid.edu.in)
# Generated on: Thu Nov 14 09:58:17 2024
# Design: ticket_machine_fsm
# Command: report timing -retime path slew_propagation -max_paths 50 -nworst 50 -late -path_type full_clock > $report_dir/pba_min_time_dft_setup.rpt
#####
Path 1: VIOLATED Recovery Check with Pin state_reg[6]/CK
Endpoint: state_reg[6]/RN (^) checked with leading edge of 'clk'
Beginpoint: reset (v) triggered by leading edge of 'clk'
Path Groups: {async_default}
Retime Analysis { Data Path-Slew }
Other End Arrival Time      0.000
- Recovery                  1.871
+ Phase Shift                4.220
- Uncertainty                 0.100
= Required Time              2.249
- Arrival Time               3.059
= Slack Time                -0.809
= Slack Time(original)      -0.809
  Clock Rise Edge           0.000
  + Input Delay              1.500
  = Beginpoint Arrival Time  1.500
  -----
  Instance       Arc      Cell      Retime   Arrival   Required
                           Delay    Time      Time
  -----                  -----
  -             reset v     -        1.500    0.691
  g10192       -           INVXL   0.000   1.500    0.691
  g10192       A v -> Y ^ INVXL   1.559   3.059    2.249
  state_reg[6]  -          SDFFRHQX1 0.000   3.059    2.249
  -----
```

We can observe above when Input clock Slew is 0.5 ns setup slack is 0.255ns and when we increase input clock slew of to 2ns the setup slack decreases to -0.809ns

## GBA HOLD SLACK

```
#####
# Generated by: Cadence Tempus 20.10-p003_1
# OS: Linux x86_64(Host ID edatools-server2.iitd.edu.in)
# Generated on: Thu Nov 14 09:58:17 2024
# Design: ticket_machine_fsm
# Command: report_timing -early > $report_dir/timing_report_min_time_dft_hold.rpt
#####

Path 1: MET Hold Check with Pin remaining_reg[1]/SI
Endpoint: remaining_reg[1]/SI (v) checked with leading edge of 'clk'
Beginpoint: remaining_reg[0]/Q (v) triggered by leading edge of 'clk'
Path Groups: {clk}
Other End Arrival Time      0.000
+ Hold                      0.150
+ Phase Shift                0.000
+ Uncertainty                0.100
= Required Time              0.250
Arrival Time                 0.482
Slack Time                  0.233
  Clock Rise Edge            0.000
  + Clock Network Latency (Ideal) 0.000
  = Beginpoint Arrival Time    0.000
-----
  Instance        Arc       Cell     Delay   Arrival  Required
                           Time     Time
-----  

  remaining_reg[0] CK ^      -        -      0.000   -0.233
  remaining_reg[0] CK ^ -> Q v SDFFRHQX1 0.482   0.482   0.250
  remaining_reg[1] SI v      SDFFRHQX1 0.000   0.482   0.250
-----
```

We can observe above when Input clock Slew is 0.5 ns hold slack is 0.211ns and when we increase input clock slew of to 2ns the setup slack increases to 0.233ns

## PBA HOLD SLACK

```
#####
# Generated by: Cadence Tempus 20.10-p003_1
# OS: Linux x86_64(Host ID edatools-server2.iitd.edu.in)
# Generated on: Thu Nov 14 09:58:17 2024
# Design: ticket_machine_fsm
# Command: report_timing -retime path slew_propagation -max_paths 50 -nworst 50 -early -path_type full_clock > $report_dir/pba_min_time_dft_hold.rpt
#####

Path 1: MET Hold Check with Pin remaining_reg[1]/CK
Endpoint: remaining_reg[1]/SI (v) checked with leading edge of 'clk'
Beginpoint: remaining_reg[0]/Q (v) triggered by leading edge of 'clk'
Path Groups: {clk}
Retime Analysis { Data Path-Slew }
Other End Arrival Time      0.000
+ Hold                      0.149
+ Phase Shift                0.000
+ Uncertainty                0.100
= Required Time              0.249
Arrival Time                 0.482
Slack Time                  0.233
= Slack Time(original)      0.233
  Clock Rise Edge            0.000
  = Beginpoint Arrival Time  0.000
Timing Path:
-----
  Instance        Arc       Cell     Retime  Arrival  Required
                           Delay   Time     Time
-----  

  -          clk ^      -        0.000   -0.233
  remaining_reg[0] -      SDFFRHQX1 0.000   0.000   -0.233
  remaining_reg[0] CK ^ -> Q v SDFFRHQX1 0.482   0.482   0.249
  remaining_reg[1] -      SDFFRHQX1 0.000   0.482   0.249
-----
```

We can observe above when Input clock Slew is 0.5ns hold slack is 0.211ns and when we increase input clock slew of to 2ns the hold slack increases to 0.233ns

## EFFECT OF LOAD

Delay of a path is a function of output load. For correct static timing analysis, we use set\_load to model the load that will be driven by the output port. Whenever load increases the delay will increase.

**Now we change load from 1 to 5 library unit**

### GBA SETUP SLACK

```
#####
# Generated by: Cadence Tempus 20.10-p003_1
# OS: Linux x86_64(Host ID edatools-server2.iiitd.edu.in)
# Generated on: Thu Nov 14 10:39:11 2024
# Design: ticket_machine_fsm
# Command: report_timing -late > $report_dir/timing_report_min_time_dft_setup.rpt
#####
Path 1: VIOLATED Setup Check with Pin return_amt_reg[6]/CK
Endpoint: return_amt_reg[6]/D (^) checked with leading edge of 'clk'
Beginpoint: total_amount_reg[6]/Q (^) triggered by leading edge of 'clk'
Path Groups: {clk}
Other End Arrival Time      0.000
- Setup                      0.547
+ Phase Shift                4.220
- Uncertainty                 0.100
= Required Time               3.573
- Arrival Time                37.125
= Slack Time                  -33.552
Clock Rise Edge              0.000
+ Clock Network Latency (Ideal) 0.000
= Beginpoint Arrival Time    0.000
-----
Instance          Arc       Cell     Delay   Arrival  Required
                   Time      Time
-----
total_amount_reg[6] CK ^     -        -      0.000  -33.552
total_amount_reg[6] CK ^ -> Q ^ SDFFRHQX1 30.226 30.226 -3.326
g10172           B ^ -> Y v NAND2BX1 3.963 34.188 0.637
g10144           A v -> Y ^ NAND2XL 1.554 35.743 2.191
g9891            A0 ^ -> Y v AOI32X1 0.322 36.065 2.513
g9861            B0 v -> Y ^ OA12BB1XL 1.061 37.125 3.573
return_amt_reg[6] D ^        SDFFRHQX8 0.000 37.125 3.573
```

After increasing the load from 1 library unit to 5 library unit we observe there is decrease in setup slack from 0.255ns to -33.552ns. Setup slack violation occurs on increasing the load.

## PBA SETUP SLACK

```
#####
# Generated by: Cadence Tempus 20.10-p003_1
# OS: Linux x86_64(Host ID edatools-server2.iiitd.edu.in)
# Generated on: Thu Nov 14 10:39:11 2024
# Design: ticket_machine_fsm
# Command: report timing -retime path slew_propagation -max_paths 50 -nworst 50 -late -path_type full_clock > $report_dir/pba_min_time_dft_setup.rpt
#####
Path 1: VIOLATED Setup Check with Pin return_amt_reg[6]/Q
Endpoint: return_amt_reg[6]/Q ('') checked with leading edge of 'clk'
Beginpoint: total_amount_reg[6]/Q ('') triggered by leading edge of 'clk'
Path Groups: {clk}
Retime Analysis { Data Path-Slew }
Other End Arrival Time 0.000
- Setup 0.247
+ Phase Shift 4.220
- Uncertainty 0.100
= Required Time 3.873
- Arrival Time 36.220
= Slack Time -32.346
= Slack Time(original) -33.552
Clock Rise Edge 0.000
= Beginpoint Arrival Time 0.000
Timing Path:
-----
Instance Arc Cell Retime Delay Arrival Required
----- Time Time Time
- clk ^ - 0.000 -32.346
total_amount_reg[6] - SDFFRHQX1 0.000 -32.346
total_amount_reg[6] CK ^ -> Q ^ SDFFRHQX1 30.226 30.226 -2.121
g10172 - NAND2BX1 0.000 30.226 -2.121
g10172 B ^ -> Y v NAND2BX1 3.963 34.188 1.842
g10144 - NAND2XL 0.000 34.188 1.842
g10144 A v -> Y ^ NAND2XL 1.555 35.744 3.397
g9891 - A0132X1 0.000 35.744 3.397
g9891 A0 ^ -> Y v A0132X1 0.322 36.066 3.720
g9861 - OA12BB1XL 0.000 36.066 3.720
g9861 B0 v -> Y ^ OA12BB1XL 0.154 36.220 3.873
return_amt_reg[6] - SDFFRHQX8 0.000 36.220 3.873
-----
Clock Rise Edge 0.000
= Beginpoint Arrival Time 0.000
Other End Path:
-----
Instance Arc Cell Retime Delay Arrival Required
----- Time Time Time
- clk ^ - 0.000 32.346
return_amt_reg[6] - SDFFRHQX8 0.000 0.000 32.346
-----
```

After increasing the load from 1 library unit to 5 library unit we observe there is decrease in setup slack from 0.255ns to -33.552ns.

## GBA HOLD SLACK

```
#####
# Generated by: Cadence Tempus 20.10-p003_1
# OS: Linux x86_64(Host ID edatools-server2.iiitd.edu.in)
# Generated on: Thu Nov 14 10:39:11 2024
# Design: ticket_machine_fsm
# Command: report timing -early > $report_dir/timing_report_min_time_dft_hold.rpt
#####
Path 1: MET Hold Check with Pin total_amount_reg[1]/CK
Endpoint: total_amount_reg[1]/SI (v) checked with leading edge of 'clk'
Beginpoint: total_amount_reg[0]/Q (v) triggered by leading edge of 'clk'
Path Groups: {clk}
Other End Arrival Time 0.000
+ Hold 0.063
+ Phase Shift 0.000
+ Uncertainty 0.100
= Required Time 0.163
Arrival Time 0.389
Slack Time 0.225
Clock Rise Edge 0.000
+ Clock Network Latency (Ideal) 0.000
= Beginpoint Arrival Time 0.000
-----
Instance Arc Cell Delay Arrival Required
----- Time Time Time
total_amount_reg[0] CK ^ - - 0.000 -0.225
total_amount_reg[0] CK ^ -> Q v SDFFRHQX1 0.389 0.389 0.163
total_amount_reg[1] SI v SDFFRHQX1 0.000 0.389 0.163
-----
```

The hold slack increases from 0.221ns to 0.225 as we increase the load from 1 library unit(pf) to 5 library unit(pf).

## PBA HOLD SLACK

```
#####
# Generated by: Cadence Tempus 20.10-p003_1
# OS: Linux x86_64(Host ID edatools-server2.iitd.edu.in)
# Generated on: Thu Nov 14 10:39:11 2024
# Design: ticket machine fsm
# Command: report timing -retime path slew propagation -max_paths 50 -nworst 50 -early -path_type full_clock > $report_dir/pba_min_time_dft_hold.rpt
#####
Path 1: MET Hold Check with Pin total_amount_reg[1]/CK
Endpoint: total_amount_reg[1]/SI (V) checked with leading edge of 'clk'
Beginpoint: total_amount_reg[0]/Q (V) triggered by leading edge of 'clk'
Path Groups: {clk}
Retime Analysis { Data Path-Slew }
Other End Arrival Time 0.000
+ Hold 0.063
+ Phase Shift 0.000
+ Uncertainty 0.100
= Required Time 0.163
Arrival Time 0.389
Slack Time 0.225
= Slack Time(original) 0.225
Clock Rise Edge 0.000
= Beginpoint Arrival Time 0.000
Timing Path:
-----
Instance Arc Cell Retime Arrival Required
----- Delay Time Time
-----
- clk ^ - 0.000 -0.225
total_amount_reg[0] - SDFFRH0X1 0.000 0.000 -0.225
total_amount_reg[0] CK ^ -> Q v SDFFRH0X1 0.389 0.389 0.163
total_amount_reg[1] - SDFFRH0X1 0.000 0.389 0.163
```

The hold slack increases from 0.221ns to 0.225 as we increase the load from 1 library unit(pf) to 5 library unit(pf).

## EFFECT OF POSITIVE / NEGATIVE UNATENESS:

### Positive Unateness:

A positive unate timing arc occurs when the output signal rises (or does not change) with a rising transition on the input and falls (or does not change) with a falling transition on the input. Example of positive Unate are buffer, AND gate, OR gate.

### Negative Unateness:

A negative unate timing arc occurs when the output signal falls (or shows no change) with a rising transition on the input and rises (or shows no change) with a falling transition on the input. Example of negative Unate are inverter, NAND gate, NOR gate.

- The unateness of a logic function plays a crucial role in VLSI design as it influences the timing slack by defining the circuit's timing constraints. When a logic function is unate, it can be represented as a linear delay component. This linear model simplifies the characterization of its timing behavior, making it easier to calculate the timing slack and optimize the performance of the circuit.
- Conversely, when a logic function is non-unate, it cannot be depicted as a linear delay component. Instead, its timing behavior necessitates a more intricate non-linear model for characterization. This complexity can pose challenges in calculating the timing slack and optimizing the circuit's performance, possibly resulting in timing violations.
- Knowing the unateness of an element reduces the number of potential rise/fall combinations, allowing the tool to predict the output transition accurately based on the input transition type. This efficiency not only saves time for the tool but also reduces the overall calculation time required.

Instance	Arc	Cell	Retime Delay	Arrival Time	Required Time
-	clk ^	-	0.000	0.000	-32.346
total_amount_reg[6]	-	SDFFRHQX1	0.000	0.000	-32.346
total_amount_reg[6]	CK ^ -> Q ^	SDFFRHQX1	30.226	30.226	-2.121
g10172	-	NAND2BX1	0.000	30.226	-2.121
g10172	B ^ -> Y v	NAND2BX1	3.963	34.188	1.842
g10144	-	NAND2XL	0.000	34.188	1.842
g10144	A v -> Y ^	NAND2XL	1.555	35.744	3.397
g9891	-	AOI32X1	0.000	35.744	3.397
g9891	A0 ^ -> Y v	AOI32X1	0.322	36.066	3.720
g9861	-	OAI2BB1XL	0.000	36.066	3.720
g9861	B0 v -> Y ^	OAI2BB1XL	0.154	36.220	3.873
return_amt_reg[6]	-	SDFFRHQX8	0.000	36.220	3.873

## TIMING SLACK (SETUP)

- Throughout the physical design process, timing slacks undergo changes. During placement, tools aim to minimize total wire length by positioning each standard cell based on its connectivity with input-output pins. This optimization effort can adversely affect critical path timing, leading to a reduction in slack.
- Following pre-optimization steps in Clock Tree Synthesis (CTS), clock networks are integrated to accommodate actual clock delays, resulting in variable slack. Generally, slack decreases as arrival time increases. Subsequent to optimization post-CTS, buffers are inserted to introduce additional delay in the paths, thereby further decreasing slack.
- During detailed routing, the actual interconnections of the layout are established, leading to interconnect delays that further diminish the slack.

## TIMING SLACK (HOLD):

- Following Clock Tree Synthesis (CTS), clock tree networks are constructed, leveraging precise clock delay information. Any hold violations are addressed by inserting clock buffers into the violated paths, thereby increasing delay and subsequently improving arrival time during post-CTS optimization. This results in an overall enhancement of slack.
- After routing, hold slack further reduces.

## NUMBER OF CELLS AND AREA OF STANDARD CELLS

- In both pre-placement and post-placement stages, the quantity of cells remains constant. During placement, standard cells within the netlist are positioned, ensuring that the area occupied by the standard cell remains unchanged.
- Following CTS pre-optimization, supplementary clock inverter cells are included, resulting in a rise in the total cell count and consequently expanding the area occupied by standard cells.
- After CTS post-optimization, additional clock buffers are inserted, leading to a further increase in the total cell count and consequently expanding the area occupied by standard cells.
- After routing, no standard cells are added so the number of cells and area remain the same.

### POWER CONSUMED:

- Power consumption rises following placement, primarily attributed to increased device switching frequency. Elevated rates of device switching contribute to heightened dynamic power dissipation. Furthermore, power consumption is influenced by device leakages and voltage drop across input-output pins.
- After CTS extra inverters and clock buffers are added which consume power and hence overall power consumption increases.

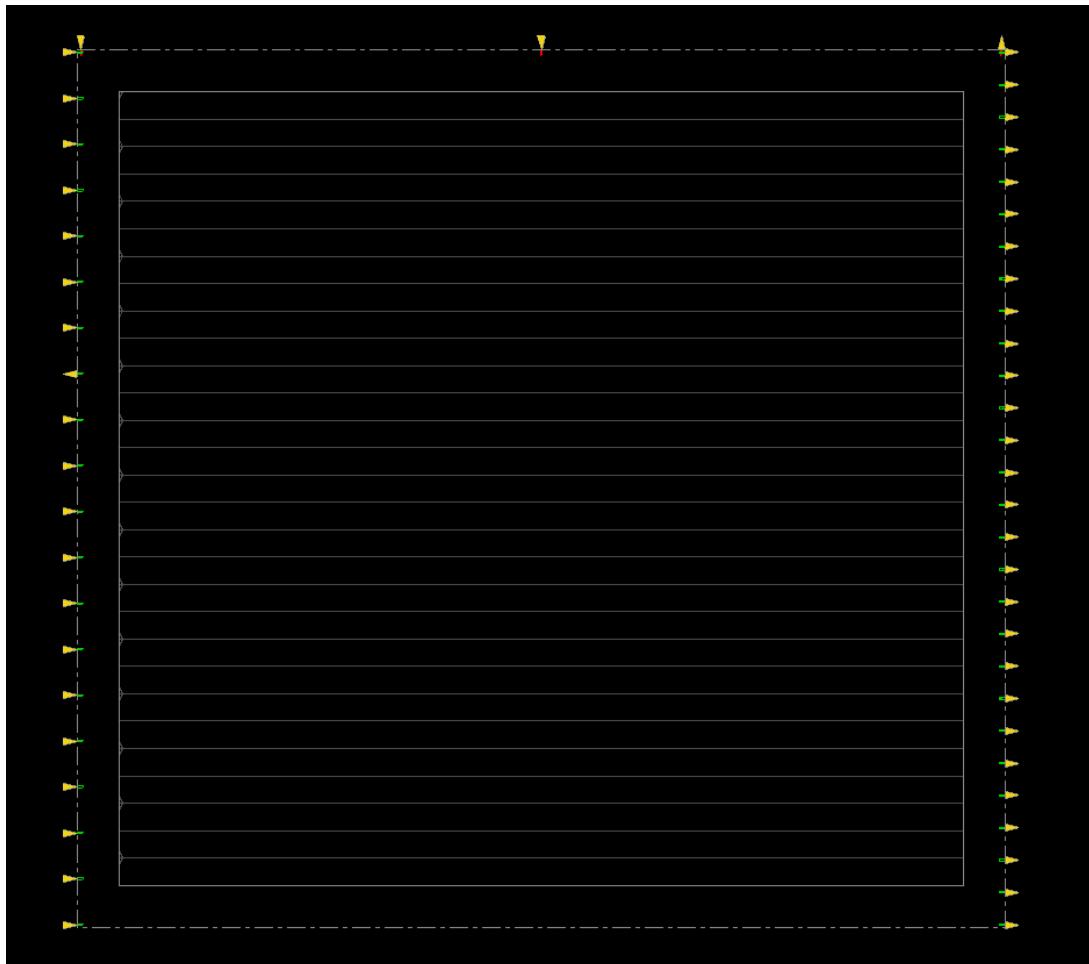
### ROUTABILITY ON CHANGE OF FLOORPLAN:

- In a scenario with 0.5 core utilization, 50 percent of the area is allocated for routing, resulting in favorable routability compared to the case with 0.8 core utilization, where only 20 percent of the area is reserved for routing.
- Reduced routing area leads to increased congestion within the design, consequently raising concerns about signal integrity due to crosstalk. This issue arises from the diminished spacing between wires, which significantly amplifies coupling capacitance.
- In our design, the cell count is low. Therefore, for 0.8 utilization, cells are positioned closely together. This proximity reduces the need for extensive routing resources to connect the cells,

resulting in lower interconnect delays. Consequently, the timing slack in 0.8 utilization cells exceeds that of 0.5 core utilization

## FLOOR PLANNING :

Utilization 0.5 (larger die area):



## BEFORE PLACEMENT

### GBA SETUP SLACK

```
#####
# Generated by: Cadence Innovus 20.10-p004_1
# OS: Linux x86_64(Host ID edatools-server2.iitd.edu.in)
# Generated on: Thu Nov 14 12:48:14 2024
# Design: ticket_machine fsm
# Command: report_timing -max_path 100 -late > report_dir/before_placement/timing_setup_report_GBA.rpt
#####
Path 1: VIOLATED Setup Check with Pin return_amt_reg[6]/CK
Endpoint: return_amt_reg[6]/D (^) checked with leading edge of 'clk'
Beginpoint: total_amount_reg[6]/Q (^) triggered by leading edge of 'clk'
Path Groups: {clk}
Analysis View: view1
Other End Arrival Time      0.000
- Setup                      0.298
+ Phase Shift                4.220
- Uncertainty                 0.100
= Required Time              3.822
- Arrival Time               8.279
= Slack Time                -4.457
    Clock Rise Edge          0.000
    + Clock Network Latency (Ideal) 0.000
    = Beginpoint Arrival Time 0.000
+-----+
| Instance | Arc | Cell | Delay | Arrival | Required |
|          |     |      |        | Time   | Time       |
+-----+
| total_amount_reg[6] | CK ^ |       |       | 0.000 | -4.457 |
| total_amount_reg[6] | CK ^ -> Q ^ | SDFFRHQX1 | 6.338 | 6.338 | 1.881 |
| g10172           | B ^ -> Y v | NAND2BX1 | 0.876 | 7.214 | 2.757 |
| g9911            | B0 v -> Y ^ | OAI2BB1X1 | 0.251 | 7.466 | 3.009 |
| g9903            | AN ^ -> Y ^ | NOR2BX1 | 0.340 | 7.806 | 3.349 |
| g9891            | A2 ^ -> Y v | AOI32X1 | 0.180 | 7.986 | 3.529 |
| g9861            | B0 v -> Y ^ | OAI2BB1XL | 0.293 | 8.279 | 3.822 |
| return_amt_reg[6] | D ^ | SDFFRHQX8 | 0.000 | 8.279 | 3.822 |
+-----+
```

The critical setup path identified by GBA starts from the begin point **total\_amount\_reg[6]/Q** and ends at **return\_amt\_reg[6]/D**.

In this **GBA analysis**, the Required Time (RT) is calculated as the End Arrival Time (default latency of clock, which is 0 but can be modified with constraints) - Setup + Phase Shift (defined clock time period in the constraint file) - Uncertainty. In this case, it is  $0 - 0.298 + 4.220 - 0.100 = 3.822$ .

Arrival time is determined through Forward Traversal of the Timing Graph and is found to be 8.279. Hence, the Slack is computed as (Required Time - Arrival Time), resulting in a value of -4.457(violation).

## PBA SETUP SLACK

```
#####
# Generated by: Cadence Innovus 20.10-p004_1
# OS: Linux x86_64(Host ID edatools-server2.iitd.edu.in)
# Generated on: Thu Nov 14 12:48:15 2024
# Design: ticket_machine_fsm
# Command: report_timing -retime path slew_propagation -max_path 100 -late -format retime_slew > report_dir/before_placement/timing_setup_report_PBA.rpt
#####
Path 1: VIOLATED Setup Check with Pin return_amt_reg[6]/CK
Endpoint: return_amt_reg[6]/D (^) checked with leading edge of 'clk'
Beginpoint: total_amount_reg[6]/Q (^) triggered by leading edge of 'clk'
Path Groups: {clk}
Analysis View: view1
Retime Analysis { Data Path-Slew }
Other End Arrival Time 0.000
- Setup 0.219
+ Phase Shift 4.220
- Uncertainty 0.100
= Required Time 3.901
- Arrival Time 8.084
= Slack Time -4.182
= Slack Time(original) -4.457
    Clock Rise Edge 0.000
    + Clock Network Latency (Ideal) 0.000
    = Beginpoint Arrival Time 0.000
+-----+
| Retime |
| Slew |
+-----+
| 0.100 |
| 0.037 |
| 0.037 |
| 1.811 |
| 1.811 |
| 0.417 |
| 0.417 |
| 0.311 |
| 0.311 |
| 0.183 |
| 0.183 |
| 0.095 |
| 0.095 |
+-----+
```

The critical setup path identified by GBA starts from the begin point **total\_amount\_reg[6]/Q** and ends at **return\_amt\_reg[6]/D**.

In this **GBA analysis**, the Required Time (RT) is calculated as the End Arrival Time (default latency of clock, which is 0 but can be modified with constraints) - Setup + Phase Shift (defined clock time period in the constraint file) - Uncertainty. In this case, it is  $0 - 0.219 + 4.220 - 0.100 = 3.901$ .

Arrival time is determined through Forward Traversal of the Timing Graph and is found to be 8.084. Hence, the Slack is computed as (Required Time - Arrival Time), resulting in a value of -4.457(violation).

## GBA HOLD SLACK

```
#####
# Generated by: Cadence Innovus 20.10-p004_1
# OS: Linux x86_64(Host ID edatools-server2.iitd.edu.in)
# Generated on: Thu Nov 14 12:48:14 2024
# Design: ticket_machine_fsm
# Command: report_timing -max_path 100 -early > report_dir/before_placement/timing_hold_report_GBA.rpt
#####
Path 1: MET Hold Check with Pin total_amount reg[1]/CK
Endpoint: total_amount_reg[1]/SI (v) checked with leading edge of 'clk'
Beginpoint: total_amount_reg[0]/Q (v) triggered by leading edge of 'clk'
Path Groups: {clk}
Analysis View: view1
Other End Arrival Time 0.000
+ Hold 0.063
+ Phase Shift 0.000
+ Uncertainty 0.100
= Required Time 0.163
Arrival Time 0.389
Slack Time 0.225
    Clock Rise Edge 0.000
    + Clock Network Latency (Ideal) 0.000
    = Beginpoint Arrival Time 0.000
+-----+
| Instance | Arc | Cell | Delay | Arrival | Required |
|          |     |      |       | Time   | Time    |
|-----+-----+-----+-----+-----+-----+
| total_amount_reg[0] | CK ^ |        |       | 0.000 | -0.225 |
| total_amount_reg[0] | CK ^ -> Q v | SDFFRHQX1 | 0.389 | 0.389 | 0.163 |
| total_amount_reg[1] | SI v | SDFFRHQX1 | 0.000 | 0.389 | 0.163 |
+-----+
```

The Worst Hold Path of GBA is mentioned above with begin point of **total\_amount\_reg[0]/Q** and endpoint of **total\_amount\_reg[1]/SI**.

In the above GBA the Required Time = End Arrival Time(latency of clock which is 0 by default but can be changed using constraint) + hold + Phase Shift(clock time period defined in constraint file)+Uncertainty =  $0 + 0.063 + 0.1 = 0.163$  ns Arrival time is computed using Forward Traversal of Timing Graph.

Arrival time = 0.389

Slack = Arrival Time - Required Time = 0.225

### PBA HOLD SLACK

```
#####
# Generated by: Cadence Innovus 20.10-p004.1
# OS: Linux x86_64(Host ID: edatools-server2.iiti.edu.in)
# Generated on: Thu Nov 14 12:48:15 2024
# Design: ticket_machine_fsm
# Command: report timing -retiming_path_slew propagation -max_path 100 -early -format retime_slew > report_dir/before_placement/timing_hold_report_PBA.rpt
#####
Path 1: MET Hold Check with Pin total_amount_reg[1]/CK
Endpoint: total_amount_reg[1]/SI (V) checked with leading edge of 'clk'
Beginpoint: total_amount_reg[0]/Q (V) triggered by leading edge of 'clk'
Path Groups: {clk}
Analysis View: View1
Retiming Analysis { Data Path-Slew }
Other End Arrival Time 0.000
+ Hold 0.063
+ Phase Shift 0.000
+ Uncertainty 0.100
= Required Time 0.163
Arrival Time 0.389
Slack Time 0.225
= Slack Time(original) 0.225
    Clock Rise Edge 0.000
    + Clock Network Latency (Ideal) 0.000
    = Beginpoint Arrival Time 0.000
    +-----+
    | Retime |
    | Slew |
    |-----|
    | 0.100 |
    | 0.093 |
    | 0.093 |
    +-----+
```

The Worst Hold Path of GBA is mentioned above with begin point of total\_amount\_reg[0]/Q and endpoint of total\_amount\_reg[1]/SI.

In the above PBA the Required Time = End Arrival Time(latency of clock which is 0 by default but can be changed using constraint) + hold + Phase Shift(clock time period defined in constraint file)+Uncertainty =  $0 + 0.063 + 0.1 = 0.163$  ns Arrival time is computed using Forward Traversal of Timing Graph.

Arrival time = 0.389

Slack = Arrival Time - Required Time = 0.225

**Hence both GBA and PBA analysis give same hold slack timing.**

### AREA

Hinst Name	Module Name	Inst Count	Total Area	Buffer	Inverter	Combinational	Flop	Latch	Clock Gate	Macro
Physical	ticket_machine_fsm	391	3043.495	0.000	84.016	1731.038	1228.449	0.000	0.000	0.000

#### Area Report:

Area of Buffers: 0.000 um<sup>2</sup>

Area of Inverters: 84.016 um<sup>2</sup>

Area of flip flops: 1228.449 um<sup>2</sup>

Area of Combinational cells: 1731.038 um<sup>2</sup>

Total Area: 3043.495 um<sup>2</sup>

## POWER

### Power Report:

**Internal power:** It is the power consumed within the confines of a cell, arises from the charging or discharging of internal capacitances during switching. The cumulative internal power dissipation is measured at 0.5313mW which is 27.503 % of total consumed power.

**Switching power:** It refers to the energy consumed by a driving cell when it charges and discharges the load capacitance connected to its output. In this case, the overall switching power amounts to 1.3837mW which is 71.6229 % of total power.

**Leakage power:** This leakage current is the current that flows from VDD to GND when there is no switching. The total leakage power is 0.0168mW which is 0.8753 % of total power.

**Total power:** Total power is the sum of the all above powers which is 1.9319mW.

```
*-----*
Innovus 20.1B-p094.1 (64bit) 05/07/2020 20:02 (Linux 2.6.32-431.11.2.el6.x86_64)
*-----*
Date & Time: 2024-Nov-14 12:48:15 (2024-Nov-14 07:18:15 GMT)

-----
Design: ticket_machine_fsm
Liberty Libraries used:
viewl ..../lib/99/slew.lib

Power Domain used:
Rail: VDD Voltage: 0.9

Power View : viewl
User-Defined Activity : N.A.
Activity File: N.A.
Hierarchical Global Activity: N.A.
Global Activity: N.A.
Sequential Element Activity: N.A.
Primary Input Activity: 0.200000
Default Iog Ratio: N.A.
Global Comb ClockGate Ratio: N.A.
Power Units = 1mW
Time Units = 1e-09 secs
Temperature = 125
report_power -outfile 50_before_placement_reports/power.rpt -rail_analysis format VS
*-----*
```

Cell	Internal Power	Switching Power	Total Power	Leakage Power	Cell Name
fare_reg[5]	0.0100	0.0743	0.0887	0.0003009	SDFFRHQX8
fare_reg[6]	0.0169	0.0726	0.0896	0.0003009	SDFFRHQX8
print_ticket_req	0.01489	0.06441	0.0796	0.0003009	SDFFRHQX8
remaining_reg[0]	0.01403	0.05894	0.0737	0.0003009	SDFFRHQX8
fare_reg[4]	0.01384	0.05829	0.0724	0.0003009	SDFFRHQX8
remaining_reg[1]	0.01351	0.05000	0.06804	0.0003009	SDFFRHQX8

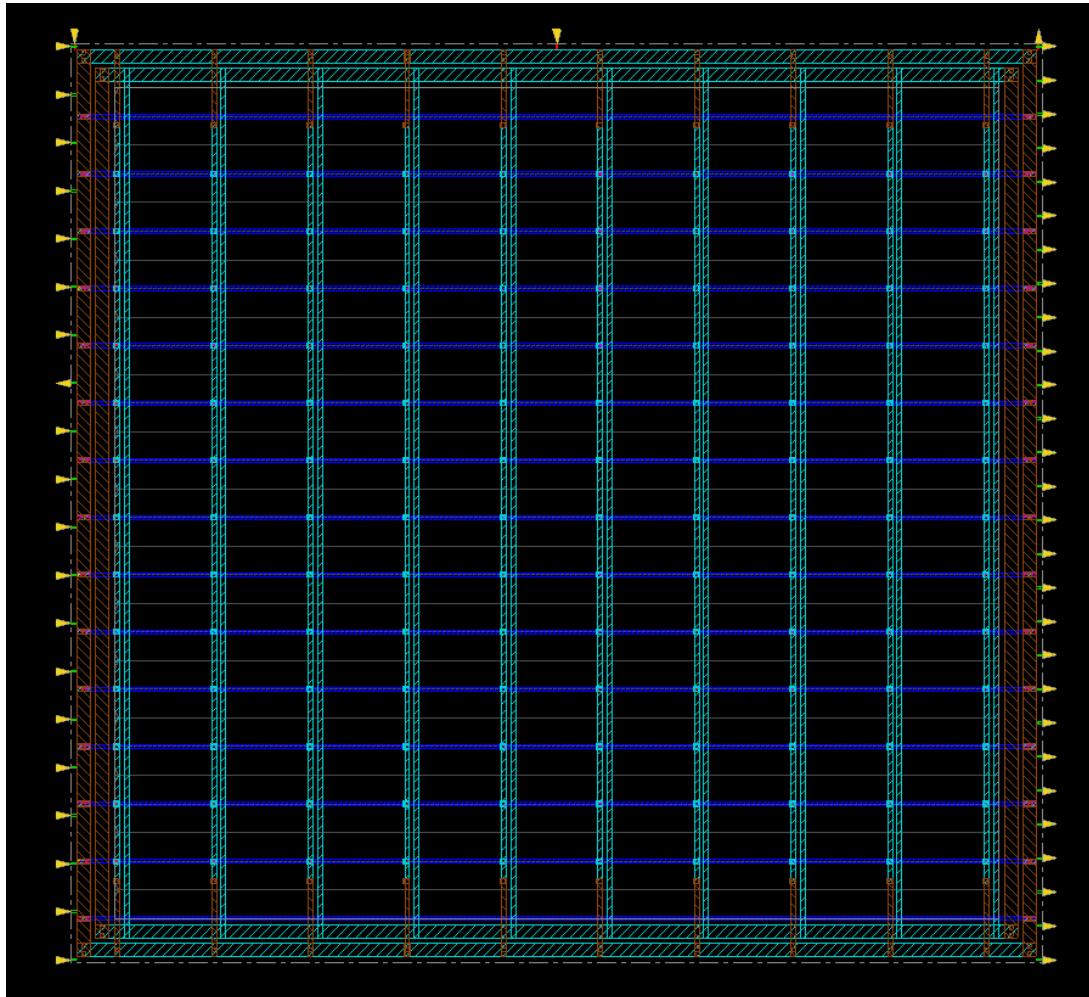
### Total Power

Total Internal Power:	0.53135948	27.5036%
Total Switching Power:	1.38372751	71.6229%
Total Leakage Power:	0.01687614	0.8735%
Total Power:	1.93196313	

Ended Static Power Report Generation: (cpu=0:00:00, real=0:00:00,  
mem(process/total/peak)=941.00MB/2334.19MB/941.00MB)

g10007	0.000101	0.766e-05	0.0001774	8.757e-06	INVXL
g9882	0.0001343	3.028e-05	0.0001767	1.22e-05	AOI21XL
g10113	0.0001242	3.989e-05	0.0001764	1.236e-05	NOR2XL
g10114	0.0001242	3.989e-05	0.0001764	1.236e-05	NOR2XL
g9903	6.771e-05	7.974e-05	0.0001675	2.004e-05	NOR2BX1
g10117	9.149e-05	6.617e-05	0.000167	9.289e-06	NAND2XL
g10188	7.36e-05	8.4e-05	0.0001669	9.289e-06	NAND2XL
g9900	0.0001161	3.417e-05	0.0001633	1.299e-05	OAI21X1
g10003	5.963e-05	9.031e-05	0.000163	1.301e-05	CLKINVX1
g10163	7.42e-05	6.33e-05	0.0001468	9.289e-06	NAND2XL
g10079	8.758e-05	3.688e-05	0.0001457	2.127e-05	OAI2BB1X1
g9860	8.137e-05	4.379e-05	0.0001444	1.92e-05	OAI2BB1XL
g10118	4.692e-05	2.291e-05	0.0001367	6.69e-05	OR4XL
g9885	0.0001016	1.884e-05	0.0001328	1.236e-05	NOR2XL
g9914	8.869e-05	2.979e-05	0.0001315	1.299e-05	OAI21X1
g9916	0.0001001	1.845e-05	0.0001309	1.236e-05	NOR2XL
g10037	4.935e-05	5.212e-05	0.0001214	1.995e-05	AOI211X1
g10125	3.975e-05	7.086e-05	0.0001199	9.289e-06	NAND2XL
g10123	7.165e-05	3.934e-05	0.0001198	8.757e-06	INVXL
g10072	6.277e-05	4.584e-05	0.0001179	9.289e-06	NAND2XL
g9852	5.833e-05	2.177e-05	0.0001143	3.419e-05	NAND3BX1
g9902	3.458e-05	6.285e-05	0.0001098	1.236e-05	NOR2XL
g10219	6.778e-05	2.583e-05	0.0001024	8.757e-06	INVXL
g9856	7.112e-05	2.248e-05	0.0001023	8.728e-06	OAI21XL
g9930	6.774e-05	2.185e-05	0.000102	1.236e-05	NOR2XL
g9927	6.852e-05	1.996e-05	0.0001015	1.299e-05	OAI21X1
g9891	7.513e-05	6.606e-06	0.0001002	1.851e-05	AOI32X1
g10132	6.564e-05	2.364e-05	9.857e-05	9.289e-06	NAND2XL
g10119	3.666e-05	3.177e-05	9.623e-05	2.78e-05	NAND4BXL
g10074	6.093e-05	2.154e-05	9.176e-05	9.289e-06	NAND2XL
g9905	5.794e-05	1.129e-05	8.158e-05	1.236e-05	NOR2XL
g10042	4.374e-05	7.852e-06	7.163e-05	2.004e-05	NOR2BX1
g9886	3.219e-05	2.867e-05	7.016e-05	9.289e-06	NAND2XL
g10080	1.64e-05	2.521e-05	6.942e-05	2.78e-05	NAND4BXL
g9850	3.876e-05	1.648e-05	6.453e-05	9.289e-06	NAND2XL
g9995	3.319e-05	5.435e-06	5.677e-05	1.815e-05	AOI21X1
g9823	3.223e-05	1.362e-05	5.514e-05	9.289e-06	NAND2XL
g9917	2.531e-05	1.868e-05	5.329e-05	9.289e-06	NAND2XL
g10036	2.313e-05	1.493e-05	5.107e-05	1.301e-05	CLKINVX1
g10008	2.48e-05	8.588e-06	4.637e-05	1.299e-05	OAI21X1
g10071	2.025e-05	1.388e-05	4.342e-05	9.289e-06	NAND2XL
g9904	1.928e-05	1.349e-05	4.206e-05	9.289e-06	NAND2XL
g9943	8.654e-06	5.544e-06	3.34e-05	1.92e-05	OAI2BB1XL
g9931	1.103e-05	7.562e-06	2.788e-05	9.289e-06	NAND2XL
g10078	1.07e-05	3.01e-06	2.364e-05	9.93e-06	NAND3XL
g9829	8.32e-06	5.248e-06	2.286e-05	9.289e-06	NAND2XL
<hr/>					
Total ( 391 of 391 )	0.5314	1.384	1.932	0.01688	
Total Capacitance	3.237e-11 F				
Power Density	*** No Die Area ***				

## LAYOUT



## AFTER PLACEMENT

### GBA SETUP SLACK

```
#####
# Generated by: Cadence Innovus 20.10-p004_1
# OS: Linux x86_64(Host ID edatools-server2.iitd.edu.in)
# Generated on: Thu Nov 14 13:41:44 2024
# Design: ticket_machine_fsm
# Command: report timing -max_path 100 -late > report_dir/after_placement/timing_setup_report_GBA.rpt
#####
Path 1: VIOLATED Setup Check with Pin return_amt_reg[6]/CK
Endpoint: return_amt_reg[6]/D (^) checked with leading edge of 'clk'
Beginpoint: total_amount_reg[6]/Q (^) triggered by leading edge of 'clk'
Path Groups: {clk}
Analysis View: view1
Other End Arrival Time 0.000
- Setup 0.312
+ Phase Shift 4.220
- Uncertainty 0.100
= Required Time 3.808
- Arrival Time 9.259
= Slack Time -5.452
    Clock Rise Edge 0.000
    + Clock Network Latency (Ideal) 0.000
    = Beginpoint Arrival Time 0.000
+-----+
| Instance | Arc | Cell | Delay | Arrival | Required |
|          |     |      |        | Time   | Time     |
+-----+-----+-----+-----+-----+-----+
| total_amount_reg[6] | CK ^ |       |       | 0.000 | -5.452 |
| total_amount_reg[6] | CK ^ -> Q ^ | SDFFRHQX1 | 6.386 | 6.386 | 0.935 |
| g10194 | A ^ -> Y v | CLKINVX1 | 1.060 | 7.447 | 1.995 |
| g10167 | B v -> Y ^ | NAND2XL | 0.407 | 7.854 | 2.402 |
| g9911 | A0N ^ -> Y ^ | OAI2BB1X1 | 0.245 | 8.099 | 2.648 |
| g9903 | AN ^ -> Y ^ | NOR2BX1 | 0.496 | 8.595 | 3.143 |
| g9891 | A2 ^ -> Y v | AOI32X1 | 0.287 | 8.881 | 3.430 |
| g9861 | B0 v -> Y ^ | OAI2BB1XL | 0.378 | 9.259 | 3.808 |
| return_amt_reg[6] | D ^ | SDFFRHQX8 | 0.000 | 9.259 | 3.808 |
+-----+
```

The critical setup path identified by GBA starts from the begin point **total\_amount\_reg[6]/Q** and ends at **return\_amt\_reg[6]/D**.

In this **GBA analysis**, the Required Time (RT) is calculated as the End Arrival Time (default latency of clock, which is 0 but can be modified with constraints) - Setup + Phase Shift (defined clock time period in the constraint file) - Uncertainty. In this case, it is  $0 - 0.312 + 4.220 - 0.100 = 3.808$ .

Arrival time is determined through Forward Traversal of the Timing Graph and is found to be 9.259. Hence, the Slack is computed as (Required Time - Arrival Time), resulting in a value of -5.452(violation).

## PBA SETUP SLACK

```
#####
# Generated by: Cadence Innovus 20.10-p004_1
# OS: Linux x86_64(Host ID edatools-server2.iitd.edu.in)
# Generated on: Thu Nov 14 13:41:44 2024
# Design: ticket_machine_fsm
# Command: report_timing -retime path slew propagation -max_path 100 -late -format retime_slew > report_dir/after_placement/timing_setup_report_PBA.rpt
#####
Path 1: VIOLATED Setup Check with Pin return_amt_reg[6]/D
Endpoint: return_amt_reg[6]/D (^) checked with leading edge of 'clk'
Beginpoint: total_amount_reg[6]/Q (^) triggered by leading edge of 'clk'
Path Groups: {clk}
Analysis View: view1
Retime Analysis { Data Path-Slew }
Other End Arrival Time 0.000
- Setup 0.241
+ Phase Shift 4.220
- Uncertainty 0.100
= Required Time 3.879
- Arrival Time 8.988
= Slack Time -5.108
= Slack Time(original) -5.452
    Clock Rise Edge 0.000
    + Clock Network Latency (Ideal) 0.000
    = Beginpoint Arrival Time 0.000
    +-----+
    | Retime |
    | Slew |
    |-----|
    | 0.100 |
    | 8.216 |
    | 8.216 |
    | 2.129 |
    | 2.129 |
    | 0.591 |
    | 0.591 |
    | 0.188 |
    | 0.188 |
    | 0.529 |
    | 0.529 |
    | 0.302 |
    | 0.302 |
    | 0.149 |
    | 0.149 |
    +-----+
```

The critical setup path identified by GBA starts from the begin point **total\_amount\_reg[6]/Q** and ends at **return\_amt\_reg[6]/D**.

In this **PBA analysis**, the Required Time (RT) is calculated as the End Arrival Time (default latency of clock, which is 0 but can be modified with constraints) - Setup + Phase Shift (defined clock time period in the constraint file) - Uncertainty. In this case, it is  $0 - 0.241 + 4.220 - 0.100 = 3.879$ .

Arrival time is determined through Forward Traversal of the Timing Graph and is found to be 8.988. Hence, the Slack is computed as (Required Time - Arrival Time), resulting in a value of -5.108(violation).

On comparison we analyzed that slack of PBA is more than GBA.

## GBA HOLD SLACK

```
#####
# Generated by: Cadence Innovus 20.10-p004_1
# OS: Linux x86_64(Host ID edatools-server2.iiti.edu.in)
# Generated on: Thu Nov 14 13:41:44 2024
# Design: ticket_machine_fsm
# Command: report_timing -max_path 100 -early > report_dir/after_placement/timing_hold_report_GBA.rpt
#####
Path 1: MET Hold Check with Pin total_amount_reg[5]/CK
Endpoint: total_amount_reg[5]/SI (v) checked with leading edge of 'clk'
Beginpoint: total_amount_reg[0]/Q (v) triggered by leading edge of 'clk'
Path Groups: {clk}
Analysis View: view1
Other End Arrival Time      0.000
+ Hold                      0.040
+ Phase Shift                0.000
+ Uncertainty                0.100
= Required Time              0.140
Arrival Time                 0.431
Slack Time                  0.291
  Clock Rise Edge           0.000
  + Clock Network Latency (Ideal) 0.000
  = Beginpoint Arrival Time    0.000
+-----+
|   Instance     |   Arc     |   Cell     |   Delay   |   Arrival  |   Required  |
|             |           |           |           |           |           |
+-----+
| total_amount_reg[0] | CK ^ |           |           | 0.000 | -0.291 |
| total_amount_reg[0] | CK ^ -> Q v | SDFFRHQX1 | 0.431 | 0.431 | 0.140 |
| total_amount_reg[5] | SI v | SDFFRHQX1 | 0.000 | 0.431 | 0.140 |
+-----+
```

The Worst Hold Path of GBA is mentioned above with begin point of total\_amount\_reg[0]/Q and endpoint of total\_amount\_reg[5]/SI.

In the above GBA the Required Time = End Arrival Time(latency of clock which is 0 by default but can be changed using constraint) + hold + Phase Shift(clock time period defined in constraint file)+ Uncertainty = 0 + 0.040+0.1 = 0.140 ns Arrival time is computed using Forward Traversal of Timing Graph.

Arrival time = 0.431

Slack = Arrival Time - Required Time = 0.291

## PBA HOLD SLACK

```
#####
# Generated by: Cadence Innovus 20.10-p004_1
# OS: Linux x86_64(Host ID edatools-server2.iiti.edu.in)
# Generated on: Thu Nov 14 13:41:44 2024
# Design: ticket_machine_fsm
# Command: report_timing -retiming_path_slew_propagation -max_path 100 -early -format retiming_slew > report_dir/after_placement/timing_hold_report_PBA.rpt
#####
Path 1: MET Hold Check with Pin total_amount_reg[5]/CK
Endpoint: total_amount_reg[5]/SI (v) checked with leading edge of 'clk'
Beginpoint: total_amount_reg[0]/Q (v) triggered by leading edge of 'clk'
Path Groups: {clk}
Analysis View: view1
Retiming Analysis { Data Path-Slew }
Other End Arrival Time      0.000
+ Hold                      0.040
+ Phase Shift                0.000
+ Uncertainty                0.100
= Required Time              0.140
Arrival Time                 0.432
Slack Time                  0.291
= Slack Time(original)      0.291
  Clock Rise Edge           0.000
  + Clock Network Latency (Ideal) 0.000
  = Beginpoint Arrival Time    0.000
+-----+
| Retime |
| Slew   |
|-----|
| 0.100 |
| 0.149 |
| 0.149 |
+-----+
```

The Worst Hold Path of GBA is mentioned above with begin point of total\_amount\_reg[0]/Q and endpoint of total\_amount\_reg[5]/SI.

In the above GBA the Required Time = End Arrival Time(latency of clock which is 0 by default but can be changed using constraint) + hold + Phase Shift(clock time period defined in constraint file)+ Uncertainty = 0 + 0.040+0.1 = 0.140 ns Arrival time is computed using Forward Traversal of Timing Graph.

Arrival time = 0.431

Slack = Arrival Time - Required Time = 0.291

## AREA

Hinst Name	Module Name	Inst Count	Total Area	Buffer	Inverter	Combinational	Flop	Latch	Clock Gate	Macro
Physical 0.000	ticket_machine_fsm	391	3043.495	0.000	84.016	1731.030	1228.449	0.000	0.000	0.000

### Area Report:

Area of Buffers: 0.000 um<sup>2</sup>

Area of Inverters: 84.016 um<sup>2</sup>

Area of flip flops: 1228.449 um<sup>2</sup>

Area of Combinational cells: 1731.038 um<sup>2</sup>

Total Area: 3043.495 um<sup>2</sup>

## POWER

### Power Report:

**Internal power:** It is the power consumed within the confines of a cell, arises from the charging or discharging of internal capacitances during switching. The cumulative internal power dissipation is measured at 0.5688mW which is 26.6084 % of total consumed power.

**Switching power:** It refers to the energy consumed by a driving cell when it charges and discharges the load capacitance connected to its output. In this case, the overall switching power amounts to 1.5521mW which is 72.6022 % of total power.

**Leakage power:** This leakage current is the current that flows from VDD to GND when there is no switching. The total leakage power is 0.01687mW which is 0.7894 % of total power.

**Total power:** Total power is the sum of the all above powers which is 2.1378mW.

```

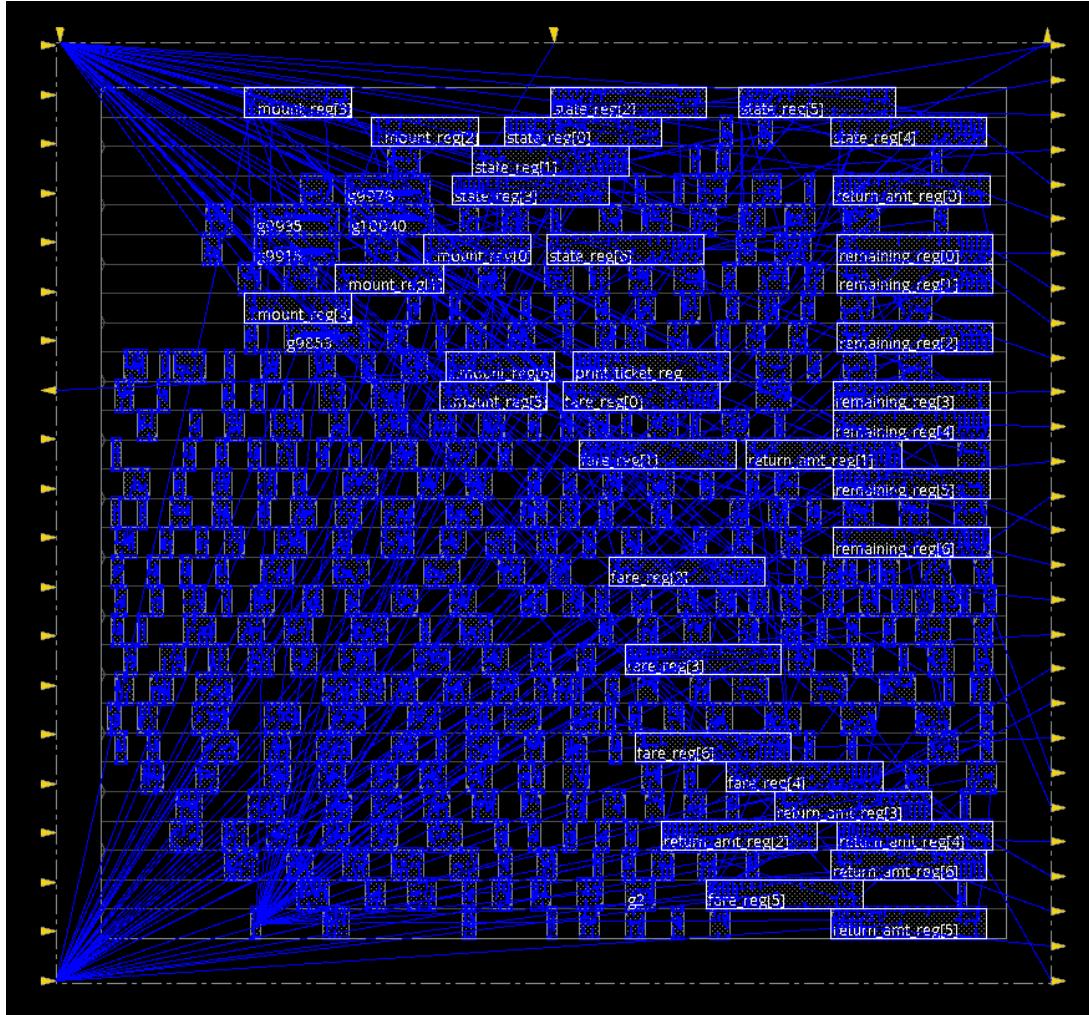
*-----*
*      Innovus 20.10-p004_1 (64bit) 05/07/2020 20:02 (Linux 2.6.32-431.11.2.el6.x86_64)
*
*
*      Date & Time:    2024-Nov-14 13:41:45 (2024-Nov-14 08:11:45 GMT)
*
*-----*
*
*      Design: ticket_machine_fsm
*
*      Liberty Libraries used:
*          view1: ../../lib/90/slow.lib
*
*      Power Domain used:
*          Rail:      VDD      Voltage:      0.9
*
*      Power View : view1
*
*      User-Defined Activity : N.A.
*
*      Activity File: N.A.
*
*      Hierarchical Global Activity: N.A.
*
*      Global Activity: N.A.
*
*      Sequential Element Activity: N.A.
*
*      Primary Input Activity: 0.200000
*
*      Default icg ratio: N.A.
*
*      Global Comb ClockGate Ratio: N.A.
*
*      Power Units = 1mW
*
*      Time Units = 1e-09 secs
*
*      Temperature = 125
*
*      report_power -outfile 50_after_placement_reports/power.rpt -rail_analysis_format VS
*-----*

Cell           Internal   Switching   Total     Leakage   Cell
                  Power       Power      Power     Power     Name
-----*
fare_reg[5]        0.01734    0.07543    0.09307  0.0003009 SDFFRHQX8
return_amt_reg[2]  0.01638    0.07448    0.09116  0.0003009 SDFFRHQX8
return_amt_reg[1]  0.01621    0.07327    0.08978  0.0003009 SDFFRHQX8
return_amt_reg[5]  0.0153     0.06757    0.08317  0.0003009 SDFFRHQX8
remaining_reg[6]   0.01585    0.06481    0.08096  0.0003009 SDFFRHQX8
return_amt_reg[6]  0.01481    0.06371    0.07887  0.0003009 SDFFRHQX8
-----*
Total Power
-----*
Total Internal Power:      0.56886144      26.6084%
Total Switching Power:     1.55216238      72.6022%
Total Leakage Power:       0.01687614      0.7894%
Total Power:               2.13789996
-----*
Ended Static Power Report Generation: (cpu=0:00:00, real=0:00:00,
mem(process/total/peak)=977.00MB/2364.65MB/977.00MB)

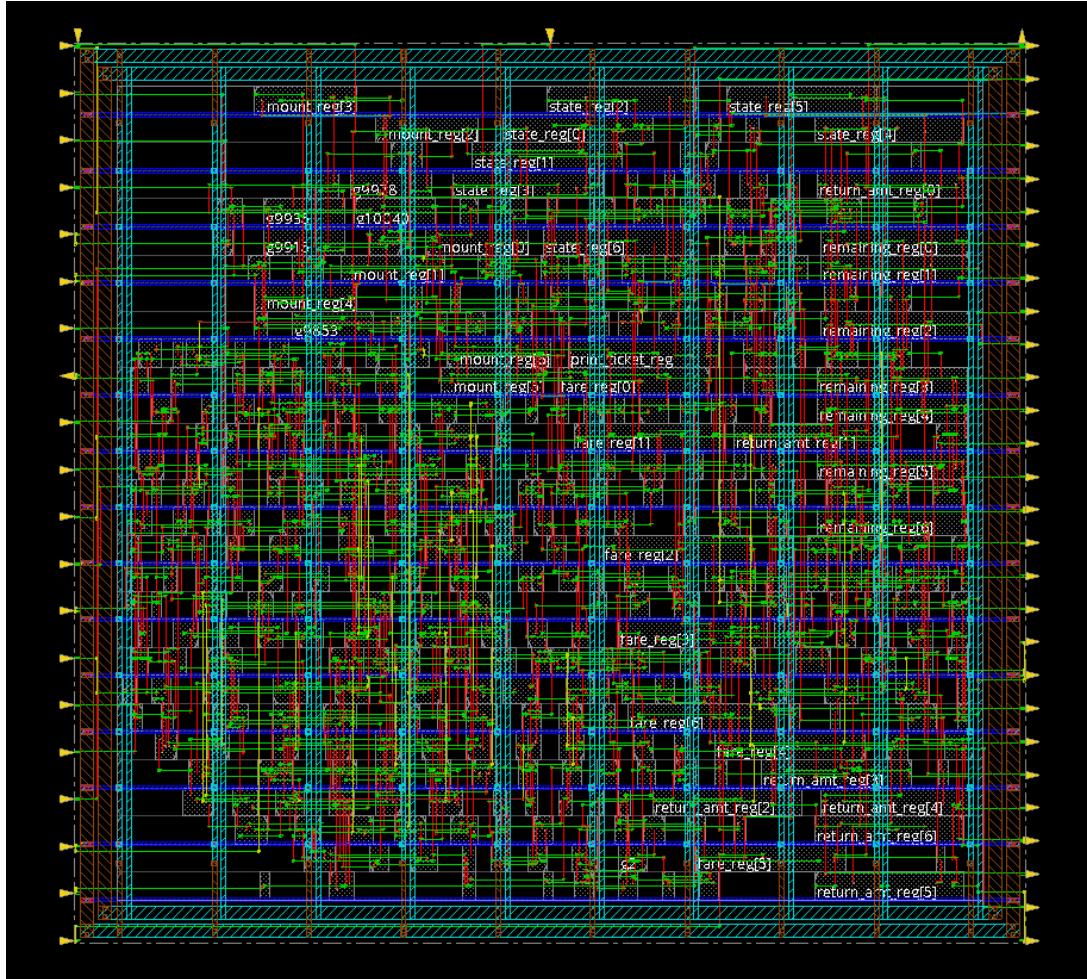
```

g10090	0.0001599	5.094e-05	0.0002491	3.833e-05	OAZZXL
g9902	5.895e-05	0.0001768	0.0002481	1.236e-05	NOR2XL
g10080	6.591e-05	0.0001354	0.0002291	2.78e-05	NAND4BXL
g10043	0.0001312	8.247e-05	0.000223	9.336e-06	OAI211XL
g10004	6.638e-05	0.0001387	0.0002174	1.236e-05	NOR2XL
g10188	7.381e-05	0.0001274	0.0002105	9.289e-06	NAND2XL
g10067	0.0001106	8.861e-05	0.000208	8.757e-06	INVXL
g10003	5.89e-05	0.0001307	0.0002026	1.301e-05	CLKINVX1
g10117	9.264e-05	9.999e-05	0.0002019	9.289e-06	NAND2XL
g10053	0.0001078	8.312e-05	0.0001996	8.757e-06	INVXL
g10114	0.0001301	5.287e-05	0.0001954	1.236e-05	NOR2XL
g9901	0.0001252	5.575e-05	0.0001932	1.22e-05	A0I21XL
g10113	0.0001304	5.013e-05	0.0001928	1.236e-05	NOR2XL
g10118	4.714e-05	7.64e-05	0.0001904	6.69e-05	OR4XL
g9913	0.0001207	5.425e-05	0.0001871	1.22e-05	A0I21XL
g10215	0.000111	6.265e-05	0.0001867	1.301e-05	CLKINVX1
g10163	7.44e-05	9.644e-05	0.0001801	9.289e-06	NAND2XL
g10125	4.103e-05	0.0001227	0.000173	9.289e-06	NAND2XL
g9882	0.0001226	3.574e-05	0.0001706	1.22e-05	A0I21XL
g10079	9.089e-05	4.839e-05	0.0001606	2.127e-05	OAI2BB1X1
g10119	5.34e-05	7.871e-05	0.0001599	2.78e-05	NAND4BXL
g9900	0.0001094	3.656e-05	0.000159	1.299e-05	OAI21X1
g10072	7.956e-05	6.963e-05	0.0001585	9.289e-06	NAND2XL
g10123	9.604e-05	4.613e-05	0.0001509	8.757e-06	INVXL
g9891	9.759e-05	3.173e-05	0.0001478	1.851e-05	A0I32X1
g9885	9.658e-05	2.373e-05	0.0001327	1.236e-05	NOR2XL
g9916	9.51e-05	2.375e-05	0.0001312	1.236e-05	NOR2XL
g9914	8.01e-05	3.12e-05	0.0001243	1.299e-05	OAI21X1
g10037	3.582e-05	5.731e-05	0.0001131	1.995e-05	A0I211X1
g10132	7.23e-05	2.972e-05	0.0001113	9.289e-06	NAND2XL
g9927	6.474e-05	2.163e-05	9.936e-05	1.299e-05	OAI21X1
g9856	6.463e-05	2.593e-05	9.929e-05	8.728e-06	OAI21XL
g9930	6.102e-05	2.427e-05	9.765e-05	1.236e-05	NOR2XL
g9860	4.562e-05	3.179e-05	9.662e-05	1.92e-05	OAI2BB1XL
g9852	3.283e-05	1.439e-05	8.141e-05	3.419e-05	NAND3BX1
g9905	5.223e-05	1.421e-05	7.881e-05	1.236e-05	NOR2XL
g9886	2.994e-05	3.658e-05	7.581e-05	9.289e-06	NAND2XL
g10078	4.365e-05	1.676e-05	7.035e-05	9.93e-06	NAND3XL
g9850	3.517e-05	1.785e-05	6.23e-05	9.289e-06	NAND2XL
g9823	3.221e-05	1.568e-05	5.718e-05	9.289e-06	NAND2XL
g9917	2.367e-05	2.106e-05	5.402e-05	9.289e-06	NAND2XL
g10036	1.996e-05	1.375e-05	4.672e-05	1.301e-05	CLKINVX1
g9904	1.899e-05	1.502e-05	4.33e-05	9.289e-06	NAND2XL
g10071	1.697e-05	1.299e-05	3.925e-05	9.289e-06	NAND2XL
g9931	1.108e-05	7.859e-06	2.822e-05	9.289e-06	NAND2XL
g9829	6.407e-06	4.994e-06	2.069e-05	9.289e-06	NAND2XL
<hr/>					
Total ( 391 of 391 )	0.5689	1.552	2.138	0.01688	
Total Capacitance	3.365e-11 F				
Power Density	*** No Die Area ***				

## FLY LINES



## LAYOUT



## AFTER CTS NON-OPTIMIZED

### GBA SETUP SLACK

```
#####
# Generated by: Cadence Innovus 20.10-p004_1
# OS: Linux x86_64(Host ID edatools-server2.iitd.edu.in)
# Generated on: Thu Nov 14 14:57:33 2024
# Design: ticket_machine_fsm
# Command: report_timing -max_path 100 -late > report_dir/before_optimisation/timing_setup_report_GBA.rpt
#####

Path 1: MET Setup Check with Pin fare_reg[4]/CK
Endpoint: fare_reg[4]/D ('') checked with leading edge of 'clk'
Beginpoint: dest_station[3] (v) triggered by leading edge of 'clk'
Path Groups: {clk}
Analysis View: view1
Other End Arrival Time -0.001
- Setup 0.276
+ Phase Shift 4.220
- Uncertainty 0.100
= Required Time 3.843
- Arrival Time 3.840
= Slack Time 0.003
    Clock Rise Edge 0.000
    + Input Delay 1.500
    = Beginpoint Arrival Time 1.500
+-----+
| Instance | Arc | Cell | Delay | Arrival | Required |
|          |     |      |        | Time   | Time     |
+-----+-----+-----+-----+-----+-----+
|          | dest_station[3] v |      |      | 1.500 | 1.503 |
| g10181 | B v -> Y ^ | NAND2XL | 0.224 | 1.724 | 1.726 |
| g10064 | C0 ^ -> Y v | OAI222XL | 0.256 | 1.980 | 1.982 |
| g10028 | B0 v -> Y ^ | AOI2BB1X1 | 0.132 | 2.112 | 2.115 |
| g10013 | C0 ^ -> Y v | OAI221X1 | 0.149 | 2.261 | 2.263 |
| g9990 | D v -> Y v | OR4X1 | 0.281 | 2.542 | 2.544 |
| g9941 | B v -> Y ^ | NOR2XL | 0.315 | 2.856 | 2.859 |
| g9922 | A1 ^ -> Y v | OAI21X1 | 0.193 | 3.049 | 3.052 |
| g9909 | A1 v -> Y ^ | OAI21X1 | 0.242 | 3.291 | 3.294 |
| g9897 | A1 ^ -> Y v | AOI21X2 | 0.164 | 3.455 | 3.458 |
| g9885 | B v -> Y ^ | NOR2XL | 0.126 | 3.582 | 3.584 |
| g9882 | B0 ^ -> Y v | AOI21XL | 0.064 | 3.645 | 3.648 |
| g9825 | A1 v -> Y ^ | OAI21XL | 0.194 | 3.840 | 3.843 |
| fare_reg[4] | D ^ | SDFFRHQX8 | 0.000 | 3.840 | 3.843 |
+-----+
```

The critical setup path identified by GBA starts from the begin point **dest\_station[3]** and ends at **fare\_reg[4]/D**.

In this **GBA analysis**, the Required Time (RT) is calculated as the End Arrival Time (default latency of clock, which is 0 but can be modified with constraints) - Setup + Phase Shift (defined clock time period in the constraint file) - Uncertainty. In this case, it is  $-0.001 - 0.276 + 4.220 - 0.100 = 3.843$ .

Arrival time is determined through Forward Traversal of the Timing Graph and is found to be 3.840. Hence, the Slack is computed as (Required Time - Arrival Time), resulting in a value of 0.003(no violation).

## PBA SETUP SLACK

```
#####
# Generated by: Cadence Innevus 20.10-p004_1
# OS: Linux x86_64(Host ID edatools-server2.iitd.edu.in)
# Generated on: Thu Nov 14 14:57:33 2024
# Design: ticket_machine fsm
# Command: report_timing -retime path slew_propagation -max_path 100 -late -format retime_slew > report_dir/before_optimisation/timing_setup_report_PBA.rpt
#####
Path 1: MET Setup Check with Pin fare reg[4]/CK
Endpoint: fare reg[4]/D ('-) checked with leading edge of 'clk'
Beginpoint: dest_station[3] (v) triggered by leading edge of 'clk'
Path Groups: {clk}
Analysis View: view1
Retime Analysis { Data Path-Slew }
Other End Arrival Time -0.001
- Setup 0.273
+ Phase Shift 4.220
- Uncertainty 0.100
= Required Time 3.846
- Arrival Time 3.801
= Slack Time 0.046
= Slack Time(original) 0.003
    Clock Rise Edge 0.000
    + Input Delay 1.500
    = Beginpoint Arrival Time 1.500
    +-----+
    | Retime |
    | Slew |
    +-----+
    | 0.003 |
    | 0.003 |
    | 0.302 |
    | 0.302 |
    | 0.279 |
    | 0.279 |
    | 0.122 |
    | 0.122 |
    | 0.160 |
    | 0.160 |
    | 0.108 |
    | 0.108 |
    | 0.398 |
    | 0.398 |
    | 0.196 |
    | 0.196 |
    | 0.259 |
    | 0.259 |
    | 0.170 |
    | 0.170 |
    | 0.117 |
    | 0.117 |
    | 0.067 |
    | 0.007 |

```

The critical setup path identified by GBA starts from the begin point **dest\_station[3]** and ends at **fare\_reg[4]/D**.

In this **PBA analysis**, the Required Time (RT) is calculated as the End Arrival Time (default latency of clock, which is 0 but can be modified with constraints) - Setup + Phase Shift (defined clock time period in the constraint file) - Uncertainty. In this case, it is  $-0.001 - 0.273 + 4.220 - 0.100 = 3.846$ .

Arrival time is determined through Forward Traversal of the Timing Graph and is found to be 3.801. Hence, the Slack is computed as (Required Time - Arrival Time), resulting in a value of 0.046(no violation).

The Setup Slack Time in PBA increases by 0.043 in comparison with GBA .

## GBA HOLD SLACK

```
#####
# Generated by: Cadence Innovus 20.10-p004_1
# OS: Linux x86_64(Host ID edatools-server2.iitd.edu.in)
# Generated on: Thu Nov 14 14:57:33 2024
# Design: ticket_machine_fsm
# Command: report timing -max_path 100 -early > report_dir/before_optimisation/timing_hold_report_GBA.rpt
#####
Path 1: MET Hold Check with Pin remaining_reg[2]/CK
Endpoint: remaining_reg[2]/SI (v) checked with leading edge of 'clk'
Beginpoint: remaining_reg[3]/Q (v) triggered by leading edge of 'clk'
Path Groups: {clk}
Analysis View: view1
Other End Arrival Time      0.000
+ Hold                      0.049
+ Phase Shift                0.000
+ Uncertainty                0.100
= Required Time              0.149
  Arrival Time               0.372
Slack Time                  0.223
  Clock Rise Edge            0.000
  + Clock Network Latency (Prop) 0.000
  = Beginpoint Arrival Time   0.000
+-----+
| Instance | Arc | Cell | Delay | Arrival | Required |
|         |     |     |       | Time    | Time     |
+-----+-----+-----+-----+-----+-----+
| remaining_reg[3] | CK ^ |        | 0.000 | 0.372 | -0.223 |
| remaining_reg[3] | CK ^ -> Q v | SDFFRHQX1 | 0.372 | 0.372 | 0.149 |
| remaining_reg[2] | SI v | SDFFRHQX1 | 0.000 | 0.372 | 0.149 |
+-----+
```

The Worst Hold Path of GBA is mentioned above with begin point of remaining\_reg[3]/Q and endpoint of remaining\_reg [2]/SI.

In the above GBA the Required Time = End Arrival Time(latency of clock which is 0 by default but can be changed using constraint) + hold + Phase Shift(clock time period defined in constraint file)+ Uncertainty = 0 + 0.049+0.1 = 0.149 ns Arrival time is computed using Forward Traversal of Timing Graph.

Arrival time = 0.372

Slack = Arrival Time - Required Time = 0.223

## PBA HOLD SLACK

```
#####
# Generated by: Cadence Innovus 20.10-p004_1
# OS: Linux x86_64 (Host ID edatools-server2.iitd.edu.in)
# Generated on: Thu Nov 14 14:57:33 2024
# Design: ticket_machine fsm
# Command: report_timing -retime path slew propagation -max_path 100 -early -format retime_slew > report_dir/before_optimisation/timing_hold_report_PBA.rpt
#####
Path 1: ME Hold Check with Pin remaining_reg[2]/SI
Endpoint: remaining_reg[2]/SI (v) checked with leading edge of 'clk'
Beginpoint: remaining_reg[3]/Q (v) triggered by leading edge of 'clk'
Path Groups: {clk}
Analysis View: view1
Retime Analysis { Data Path-Slew }
Other End Arrival Time 0.000
+ Hold 0.049
+ Phase Shift 0.000
+ Uncertainty 0.100
= Required Time 0.149
Arrival Time 0.372
Slack Time 0.223
= Slack Time(original) 0.223
Clock Rise Edge 0.000
+ Clock Network Latency (Prop) 0.000
= Beginpoint Arrival Time 0.000
+-----+
| Retime |
| Slew |
|-----|
| 0.007 |
| 0.091 |
| 0.091 |
+-----+
```

The Worst Hold Path of GBA is mentioned above with begin point of remaining\_reg[3]/Q and endpoint of remaining\_reg [2]/SI.

In the above GBA the Required Time = End Arrival Time(latency of clock which is 0 by default but can be changed using constraint) + hold + Phase Shift(clock time period defined in constraint file)+ Uncertainty = 0 + 0.049+0.1 = 0.149 ns Arrival time is computed using Forward Traversal of Timing Graph.

Arrival time = 0.372

Slack = Arrival Time - Required Time = 0.223

## POWER

### Power Report:

**Internal power:** It is the power consumed within the confines of a cell, arises from the charging or discharging of internal capacitances during switching. The cumulative internal power dissipation is measured at 0.3517mW which is 34.0704% of total consumed power.

**Switching power:** It refers to the energy consumed by a driving cell when it charges and discharges the load capacitance connected to its output. In this case, the overall switching power amounts to 0.6614mW which is 64.0718% of total power.

**Leakage power:** This leakage current is the current that flows from VDD to GND when there is no switching. The total leakage power is 0.01918mW which is 1.8578 % of total power.

**Total power:** Total power is the sum of the all above powers which is 1.0324mW.

```

*-----*
*      Innovus 20.10-p004_1 (64bit) 05/07/2020 20:02 (Linux 2.6.32-431.11.2.el6.x86_64)
*
*      Date & Time:    2024-Nov-14 14:57:34 (2024-Nov-14 09:27:34 GMT)
*
*-----*
*      Design: ticket_machine_fsm
*
*      Liberty Libraries used:
*          view1: ../lib/90/slow.lib
*
*      Power Domain used:
*          Rail:      VDD      Voltage:      0.9
*
*      Power View : view1
*
*      User-Defined Activity : N.A.
*
*      Activity File: N.A.
*
*      Hierarchical Global Activity: N.A.
*
*      Global Activity: N.A.
*
*      Sequential Element Activity: 0.200000
*
*      Primary Input Activity: 0.200000
*
*      Default icg ratio: N.A.
*
*      Global Comb ClockGate Ratio: N.A.
*
*      Power Units = 1mW
*
*      Time Units = 1e-09 secs
*
*      Temperature = 125
*
*      report_power -outfile 50_before_optimisation_reports/power.rpt -rail_analysis_format VS
*

```

Cell	Internal Power	Switching Power	Total Power	Leakage Power	Cell Name
FE_OFC0_DFT_sdo_1	0.001992	0.01972	0.02193	0.0002199	CLKBUFX12
FE_OFC4_state_5	0.001991	0.01959	0.0218	0.0002199	CLKBUFX12
FE_OFC7_fare_6	0.001989	0.01956	0.02177	0.0002199	CLKBUFX12
FE_OFC13_return_amt_0	0.001992	0.01954	0.02176	0.0002199	CLKBUFX12
FE_OFC19_state_6	0.001993	0.01951	0.02172	0.0002199	CLKBUFX12
FF_OFC20_state_4	0.001992	0.0195	0.02171	0.0002199	CLKBUFX12

#### Total Power

```

-----
Total Internal Power:      0.35174899      34.0704%
Total Switching Power:     0.66149028      64.0718%
Total Leakage Power:       0.01918026      1.8578%
Total Power:                1.03241953
-----
```

```

-----  

Ended Static Power Report Generation: (cpu=0:00:00, real=0:00:00,  

mem(process/total/peak)=1097.40MB/2593.87MB/1132.86MB)
```

	2.009e-03	5.070e-03	0.040e-03	2.002e-03	NAND2XL
g10121	2.443e-05	2.14e-05	7.184e-05	2.601e-05	AND4X1
g10033	1.813e-05	2.262e-05	6.855e-05	2.78e-05	NAND4BXL
g10080	1.214e-05	2.639e-05	6.633e-05	2.78e-05	NAND4BXL
g9889	3.007e-05	2.241e-05	6.55e-05	1.301e-05	CLKINVX1
g10042	3.076e-05	1.206e-05	6.286e-05	2.004e-05	NOR2BX1
g9995	3.358e-05	1.077e-05	6.25e-05	1.815e-05	AOI21X1
g10119	1.296e-05	1.924e-05	6e-05	2.78e-05	NAND4BXL
g9993	1.873e-05	2.713e-05	5.887e-05	1.301e-05	CLKINVX1
g9902	1.069e-05	3.425e-05	5.73e-05	1.236e-05	NOR2XL
g10022	1.496e-05	2.842e-05	5.64e-05	1.301e-05	CLKINVX1
g9926	2.897e-05	7.972e-06	5.509e-05	1.815e-05	AOI21X1
g10073	2.278e-05	1.718e-05	5.231e-05	1.236e-05	NOR2XL
g10037	1.215e-05	1.947e-05	5.156e-05	1.995e-05	AOI211X1
FE_OF_C43_n_363	9.323e-06	2.87e-05	5.104e-05	1.301e-05	INVX1
g10008	2.606e-05	1.122e-05	5.027e-05	1.299e-05	OAI21X1
g9891	2.017e-05	1.122e-05	4.99e-05	1.851e-05	AOI32X1
g10041	2.209e-05	5.323e-06	4.746e-05	2.004e-05	NOR2BX1
g9943	1.202e-05	1.458e-05	4.58e-05	1.92e-05	OAI2BB1XL
g9852	6.738e-06	2.979e-06	4.391e-05	3.419e-05	NAND3BX1
g10004	8.5e-06	1.765e-05	3.851e-05	1.236e-05	NOR2XL
g10003	7.516e-06	1.598e-05	3.651e-05	1.301e-05	CLKINVX1
g9901	1.6e-05	7.2e-06	3.54e-05	1.22e-05	AOI21XL
g9860	9.283e-06	6.494e-06	3.498e-05	1.92e-05	OAI2BB1XL
g9913	1.539e-05	6.832e-06	3.442e-05	1.22e-05	AOI21XL
g10005	9.684e-06	3.3e-06	3.391e-05	2.093e-05	NOR4X1
g9882	1.552e-05	4.641e-06	3.236e-05	1.22e-05	AOI21XL
g9900	1.286e-05	4.687e-06	3.053e-05	1.299e-05	OAI21X1
g9914	1.011e-05	4.098e-06	2.719e-05	1.299e-05	OAI21X1
g9885	1.088e-05	3.028e-06	2.626e-05	1.236e-05	NOR2XL
g9916	1.067e-05	3.044e-06	2.607e-05	1.236e-05	NOR2XL
g9886	5.755e-06	4.738e-06	2.452e-05	1.403e-05	NAND2X1
g10078	1.004e-05	4.083e-06	2.406e-05	9.93e-06	NAND3XL
g10036	5.681e-06	4.625e-06	2.332e-05	1.301e-05	CLKINVX1
g9927	7.541e-06	2.752e-06	2.328e-05	1.299e-05	OAI21X1
g9930	7.708e-06	3.098e-06	2.316e-05	1.236e-05	NOR2XL
g9905	6.583e-06	1.734e-06	2.068e-05	1.236e-05	NOR2XL
g9856	8.092e-06	3.341e-06	2.016e-05	8.728e-06	OAI21XL
g10071	4.794e-06	4.235e-06	1.832e-05	9.289e-06	NAND2XL
g10072	4.501e-06	4.042e-06	1.783e-05	9.289e-06	NAND2XL
g9850	4.357e-06	2.275e-06	1.592e-05	9.289e-06	NAND2XL
g9823	4.043e-06	1.915e-06	1.525e-05	9.289e-06	NAND2XL
g9917	2.836e-06	2.688e-06	1.481e-05	9.289e-06	NAND2XL
g9904	2.362e-06	1.904e-06	1.356e-05	9.289e-06	NAND2XL
g9829	1.872e-06	1.544e-06	1.27e-05	9.289e-06	NAND2XL
g9931	1.348e-06	9.912e-07	1.163e-05	9.289e-06	NAND2XL

---

Total ( 435 of 435 )	0.3517	0.6615	1.032	0.01918
Total Capacitance	3.416e-11 F			
Power Density	*** No Die Area ***			

## AREA

Hinst Name	Module Name	Inst Count	Total Area	Buffer	Inverter	Combinational	Flop	Latch	Cloc
Physical									
ticket_machine_fsm 0.000		435	3263.753	295.191	259.617	1773.417	935.528	0.000	

### Area Report

Area of Buffers: 295.191 um<sup>2</sup>

Area of Inverters: 259.617 um<sup>2</sup>

Area of flip flops: 935.528 um<sup>2</sup>

Area of Combinational cells: 1773.417 um<sup>2</sup>

Total Area: 3263.753 um<sup>2</sup>

## AFTER CTS OPTIMIZED

### GBA SETUP SLACK

# Generated by: Cadence Innovus 20.10-p004_1						
# OS: Linux x86_64(Host ID edatools-server2.iitiid.edu.in)						
# Generated on: Thu Nov 14 14:26:54 2024						
# Design: ticket_machine_fsm						
# Command: report_timing -max_path 100 -late > report_dir/after_optimisation/timing_setup_report_GBA.rpt						
#-----#						
Path 1: MET Setup Check with Pin fare_reg[5]/CK						
Endpoint: fare_reg[5]/D (^) checked with leading edge of 'clk'						
Beginpoint: dest_station[2] (^) triggered by leading edge of 'clk'						
Path Groups: {clk}						
Analysis View: view1						
Other End Arrival Time -0.001						
- Setup 0.250						
+ Phase Shift 4.220						
- Uncertainty 0.100						
= Required Time 3.869						
- Arrival Time 3.858						
= Slack Time 0.011						
Clock Rise Edge 0.000						
+ Input Delay 1.500						
= Beginpoint Arrival Time 1.500						
+-----+						
Instance	Arc	Cell	Delay	Arrival Time	Required Time	
g10239	dest_station[2] ^ A ^ -> Y v	CLKINVX1	0.064	1.500	1.511	
g10189	B v -> Y ^	NOR2X1	0.140	1.564	1.575	
g10137	B ^ -> Y v	NAND2XL	0.552	1.704	1.715	
g10095	A1 v -> Y ^	OAI22X1	0.242	2.256	2.268	
g9990	C ^ -> Y v	OR4X1	0.167	2.499	2.510	
g9940	A ^ -> Y v	NAND2X1	0.121	2.665	2.677	
g9923	A0 v -> Y ^	OAI21X1	0.121	2.787	2.798	
g9910	A1 ^ -> Y v	OAI21X2	0.236	3.023	3.034	
g9896	A1 v -> Y ^	OAI21X2	0.141	3.164	3.175	
g9858	A1 ^ -> Y v	OAI21X2	0.166	3.330	3.342	
g9834	B v -> Y ^	MXI2X1	0.108	3.438	3.450	
g9823	B ^ -> Y v	NAND2XL	0.102	3.540	3.552	
g9818	A1N v -> Y v	OAI2BB1X1	0.085	3.625	3.637	
g9816	B0 v -> Y ^	OAI2BB1X1	0.162	3.787	3.799	
fare_reg[5]	D ^	SDFFRHQX8	0.000	3.858	3.869	
+-----+						

The critical setup path identified by GBA starts from the begin point **dest\_station[2]** and ends at **fare\_reg[5]/D**.

In this **GBA analysis**, the Required Time (RT) is calculated as the End Arrival Time (default latency of clock, which is 0 but can be modified with constraints) - Setup + Phase Shift (defined clock time period in the constraint file) - Uncertainty. In this case, it is  $-0.001 - 0.250 + 4.220 - 0.100 = 3.869$ .

Arrival time is determined through Forward Traversal of the Timing Graph and is found to be 3.858. Hence, the Slack is computed as (Required Time - Arrival Time), resulting in a value of 0.011( no violation).

## PBA SETUP SLACK

```
#####
# Generated by: Cadence Innovus 20.10-p004.1
# OS: Linux x86_64(Host ID edatools-server2.iitiid.edu.in)
# Generated on: Thu Nov 14 14:26:54 2024
# Design: ticket_machine fsm
# Command: report_timing -retime path slew_propagation -max_path 100 -late -format retime_slew > report_dir/after_optimisation/timing_setup_report_PBA.rpt
#####
Path 1: MET Setup Check with Pin fare_reg[5]/CK
Endpoint: fare_reg[5]/D (^) checked with leading edge of 'clk'
Beginpoint: dest_station[2] (^) triggered by leading edge of 'clk'
Path Groups: {clk}
Analysis View: view1
Retime Analysis { Data Path-Slew }
Other End Arrival Time -0.001
- Setup 0.242
+ Phase Shift 4.220
- Uncertainty 0.100
= Required Time 3.876
- Arrival Time 3.807
= Slack Time 0.070
= Slack Time(original) 0.011
    Clock Rise Edge 0.000
    + Input Delay 1.500
    = Beginpoint Arrival Time 1.500
    +-----+
    | Retime |
    | Slew |
    |-----|
    | 0.003 |
    | 0.003 |
    | 0.080 |
    | 0.080 |
    | 0.159 |
    | 0.159 |
    | 0.748 |
    | 0.748 |
    | 0.269 |
    | 0.269 |
    | 0.872 |
    | 0.872 |
    | 0.136 |
    | 0.136 |
    | 0.241 |
    | 0.241 |
    | 0.145 |
    | 0.145 |
    | 0.167 |
    | 0.167 |
    | 0.105 |
    | 0.105 |
    | 0.087 |
    | @ R#7 |

```

The critical setup path identified by GBA starts from the begin point **dest\_station[2]** and ends at **fare\_reg[5]/D**.

In this **PBA analysis**, the Required Time (RT) is calculated as the End Arrival Time (default latency of clock, which is 0 but can be modified with constraints) - Setup + Phase Shift (defined clock time period in the constraint file) - Uncertainty. In this case, it is  $-0.001 - 0.242 + 4.220 - 0.100 = 3.876$ .

Arrival time is determined through Forward Traversal of the Timing Graph and is found to be 3.807. Hence, the Slack is computed as (Required Time - Arrival Time), resulting in a value of 0.011( no violation).

## GBA HOLD SLACK

```
#####
# Generated by: Cadence Innovus 20.10-p004_1
# OS: Linux x86_64(Host ID edatools-server2.iitd.edu.in)
# Generated on: Thu Nov 14 14:26:54 2024
# Design: ticket_machine_fsm
# Command: report_timing -max_path 100 -early > report_dir/after_optimisation/timing_hold_report_GBA.rpt
#####
Path 1: MET Hold Check with Pin remaining_reg[2]/CK
Endpoint: remaining_reg[2]/SI (v) checked with leading edge of 'clk'
Beginpoint: remaining_reg[3]/Q (v) triggered by leading edge of 'clk'
Path Groups: {clk}
Analysis View: view1
Other End Arrival Time 0.000
+ Hold 0.049
+ Phase Shift 0.000
+ Uncertainty 0.100
= Required Time 0.149
Arrival Time 0.372
Slack Time 0.223
Clock Rise Edge 0.000
+ Clock Network Latency (Prop) 0.000
= Beginpoint Arrival Time 0.000
+-----+
| Instance | Arc | Cell | Delay | Arrival | Required |
|          |     |      |       | Time   | Time    |
+-----+
| remaining_reg[3] | CK ^ |          | 0.000 | 0.372 | -0.223 |
| remaining_reg[3] | CK ^ -> Q v | SDFFRHQX1 | 0.372 | 0.372 | 0.149 |
| remaining_reg[2] | SI v | SDFFRHQX1 | 0.000 | 0.372 | 0.149 |
+-----+
```

The Worst Hold Path of GBA is mentioned above with begin point of remaining\_reg[3]/Q and endpoint of remaining\_reg [2]/SI.

In the above GBA the Required Time = End Arrival Time(latency of clock which is 0 by default but can be changed using constraint) + hold + Phase Shift(clock time period defined in constraint file)+ Uncertainty = 0 + 0.049+0.1 = 0.149 ns Arrival time is computed using Forward Traversal of Timing Graph.

Arrival time = 0.372

Slack = Arrival Time - Required Time = 0.223

## PBA HOLD SLACK

```
#####
# Generated by: Cadence Innovus 20.10-p004_1
# OS: Linux x86_64(Host ID edatools-server2.iitd.edu.in)
# Generated on: Thu Nov 14 14:26:54 2024
# Design: ticket_machine_fsm
# Command: report_timing -retime path slew_propagation -max_path 100 -early -format retime_slew > report_dir/after_optimisation/timing_hold_report_PBA.rpt
#####
Path 1: MET Hold Check with Pin remaining_reg[2]/CK
Endpoint: remaining_reg[2]/SI (v) checked with leading edge of 'clk'
Beginpoint: remaining_reg[3]/Q (v) triggered by leading edge of 'clk'
Path Groups: {clk}
Analysis View: view1
Retime Analysis { Data Path-Slew }
Other End Arrival Time 0.000
+ Hold 0.049
+ Phase Shift 0.000
+ Uncertainty 0.100
= Required Time 0.149
Arrival Time 0.372
Slack Time 0.223
= Slack Time(original) 0.223
Clock Rise Edge 0.000
+ Clock Network Latency (Prop) 0.000
= Beginpoint Arrival Time 0.000
+-----+
| Retime |
| Slew   |
|-----|
| 0.007  |
| 0.091  |
| 0.091  |
|-----+
```

The Worst Hold Path of GBA is mentioned above with begin point of remaining\_reg[3]/Q and endpoint of remaining\_reg [2]/SI.

In the above GBA the Required Time = End Arrival Time(latency of clock which is 0 by default but can be changed using constraint) + hold + Phase Shift(clock time period defined in constraint file)+ Uncertainty = 0 + 0.049+0.1 = 0.149 ns Arrival time is computed using Forward Traversal of Timing Graph.

Arrival time = 0.372

Slack = Arrival Time - Required Time = 0.223

## POWER

### Power Report

**Internal power:** It is the power consumed within the confines of a cell, arises from the charging or discharging of internal capacitances during switching. The cumulative internal power dissipation is measured at 0.3510mW which is 34.0406% of total consumed power.

**Switching power:** It refers to the energy consumed by a driving cell when it charges and discharges the load capacitance connected to its output. In this case, the overall switching power amounts to 0.6611mW which is 64.1015% of total power.

**Leakage power:** This leakage current is the current that flows from VDD to GND when there is no switching. The total leakage power is 0.01916mW which is 1.8579 % of total power.

**Total power:** Total power is the sum of the all above powers which is 1.0313mW.

```

*-----*
*      Innovus 20.10-p004_1 (64bit) 05/07/2020 20:02 (Linux 2.6.32-431.11.2.el6.x86_64)
*
*
*      Date & Time:    2024-Nov-14 14:26:55 (2024-Nov-14 08:56:55 GMT)
*
*-----*
*
*      Design: ticket_machine_fsm
*
*      Liberty Libraries used:
*          view1: ./lib/90/slow.lib
*
*      Power Domain used:
*          Rail:      VDD      Voltage:      0.9
*
*      Power View : view1
*
*      User-Defined Activity : N.A.
*
*      Activity File: N.A.
*
*      Hierarchical Global Activity: N.A.
*
*      Global Activity: N.A.
*
*      Sequential Element Activity: 0.200000
*
*      Primary Input Activity: 0.200000
*
*      Default icg ratio: N.A.
*
*      Global Comb ClockGate Ratio: N.A.
*
*      Power Units = 1mW
*
*      Time Units = 1e-09 secs
*
*      Temperature = 125
*
*      report_power -outfile 50_after_optimisation_reports/power.rpt -rail_analysis_format VS
*
*-----*

```

Cell	Internal Power	Switching Power	Total Power	Leakage Power	Cell Name
FE_OFC0_DFT_sdo_1	0.001992	0.01972	0.02193	0.0002199	CLKBUFX12
FE_OFC4_state_5	0.001991	0.01959	0.0218	0.0002199	CLKBUFX12
FE_OFC7_fare_6	0.001989	0.01956	0.02177	0.0002199	CLKBUFX12
FE_OFC13_return_amt_0	0.001992	0.01954	0.02176	0.0002199	CLKBUFX12
FE_OFC19_state_6	0.001993	0.01951	0.02172	0.0002199	CLKBUFX12
FE_OFC20_state_4	0.001992	0.0195	0.02171	0.0002199	CLKBUFX12

**Total Power**

---

Total Internal Power:	0.35109094	34.0406%
Total Switching Power:	0.66113667	64.1015%
Total Leakage Power:	0.01916239	1.8579%
Total Power:	1.03138999	

---

Ended Static Power Report Generation: (cpu=0:00:00, real=0:00:00,  
mem(process/total/peak)=1273.14MB/2813.46MB/1273.14MB)

g10002	2.009e-05	3.075e-05	8.540e-05	2.802e-05	NAND2X2
g10121	2.443e-05	2.14e-05	7.183e-05	2.601e-05	AND4X1
g10033	1.813e-05	2.261e-05	6.854e-05	2.78e-05	NAND4BXL
g10080	1.214e-05	2.638e-05	6.632e-05	2.78e-05	NAND4BXL
g9889	3.008e-05	2.241e-05	6.55e-05	1.301e-05	CLKINVX1
g10042	3.075e-05	1.206e-05	6.285e-05	2.004e-05	NOR2BX1
g9995	3.358e-05	1.078e-05	6.25e-05	1.815e-05	A0I21X1
g10119	1.296e-05	1.923e-05	6e-05	2.78e-05	NAND4BXL
g9993	1.873e-05	2.713e-05	5.887e-05	1.301e-05	CLKINVX1
g9902	1.069e-05	3.423e-05	5.728e-05	1.236e-05	NOR2XL
g10022	1.496e-05	2.842e-05	5.64e-05	1.301e-05	CLKINVX1
g9926	2.896e-05	7.973e-06	5.508e-05	1.815e-05	A0I21X1
g10073	2.278e-05	1.718e-05	5.231e-05	1.236e-05	NOR2XL
g10037	1.215e-05	1.944e-05	5.153e-05	1.995e-05	A0I211X1
FE_OFc43_n_363	9.323e-06	2.87e-05	5.104e-05	1.301e-05	INVX1
g10008	2.606e-05	1.121e-05	5.026e-05	1.299e-05	OAI21X1
g9891	2.017e-05	1.123e-05	4.991e-05	1.851e-05	A0I32X1
g10041	2.209e-05	5.323e-06	4.746e-05	2.004e-05	NOR2BX1
g9943	1.202e-05	1.458e-05	4.58e-05	1.92e-05	OAI2BB1XL
g9852	6.738e-06	2.979e-06	4.391e-05	3.419e-05	NAND3BX1
g10004	8.5e-06	1.765e-05	3.851e-05	1.236e-05	NOR2XL
g10003	7.516e-06	1.598e-05	3.651e-05	1.301e-05	CLKINVX1
g9901	1.6e-05	7.202e-06	3.54e-05	1.22e-05	A0I21XL
g9860	9.283e-06	6.494e-06	3.498e-05	1.92e-05	OAI2BB1XL
g9913	1.54e-05	6.834e-06	3.443e-05	1.22e-05	A0I21XL
g10005	9.684e-06	3.3e-06	3.391e-05	2.093e-05	NOR4X1
g9882	1.552e-05	4.642e-06	3.236e-05	1.22e-05	A0I21XL
g9900	1.286e-05	4.688e-06	3.053e-05	1.299e-05	OAI21X1
g9914	1.012e-05	4.099e-06	2.72e-05	1.299e-05	OAI21X1
g9885	1.088e-05	3.029e-06	2.626e-05	1.236e-05	NOR2XL
g9916	1.067e-05	3.043e-06	2.607e-05	1.236e-05	NOR2XL
g9886	5.755e-06	4.739e-06	2.452e-05	1.403e-05	NAND2X1
g10078	1.004e-05	4.082e-06	2.405e-05	9.93e-06	NAND3XL
g10036	5.678e-06	4.626e-06	2.332e-05	1.301e-05	CLKINVX1
g9927	7.535e-06	2.752e-06	2.327e-05	1.299e-05	OAI21X1
g9930	7.7e-06	3.097e-06	2.315e-05	1.236e-05	NOR2XL
g9905	6.584e-06	1.734e-06	2.068e-05	1.236e-05	NOR2XL
g9856	8.092e-06	3.341e-06	2.016e-05	8.728e-06	OAI21XL
g10071	4.794e-06	4.234e-06	1.832e-05	9.289e-06	NAND2XL
g10072	4.501e-06	4.041e-06	1.783e-05	9.289e-06	NAND2XL
g9850	4.357e-06	2.276e-06	1.592e-05	9.289e-06	NAND2XL
g9823	4.043e-06	1.915e-06	1.525e-05	9.289e-06	NAND2XL
g9917	2.834e-06	2.688e-06	1.481e-05	9.289e-06	NAND2XL
g9904	2.363e-06	1.904e-06	1.356e-05	9.289e-06	NAND2XL
g9829	1.871e-06	1.544e-06	1.27e-05	9.289e-06	NAND2XL
g9931	1.34e-06	9.912e-07	1.162e-05	9.289e-06	NAND2XL

---

Total ( 435 of 435 )	0.3511	0.6611	1.031	0.01916
Total Capacitance	3.415e-11 F			
Power Density	*** No Die Area ***			

## AREA

Hinst Name	Module Name	Inst Count	Total Area	Buffer	Inverter	Combinational	Flop	Latc
Physical ticket_machine_fsm 0.000		435	3259.968	295.191	259.617	1769.632	935.528	0.00

## Area Report

Area of Buffers: 295.191  $\mu\text{m}^2$

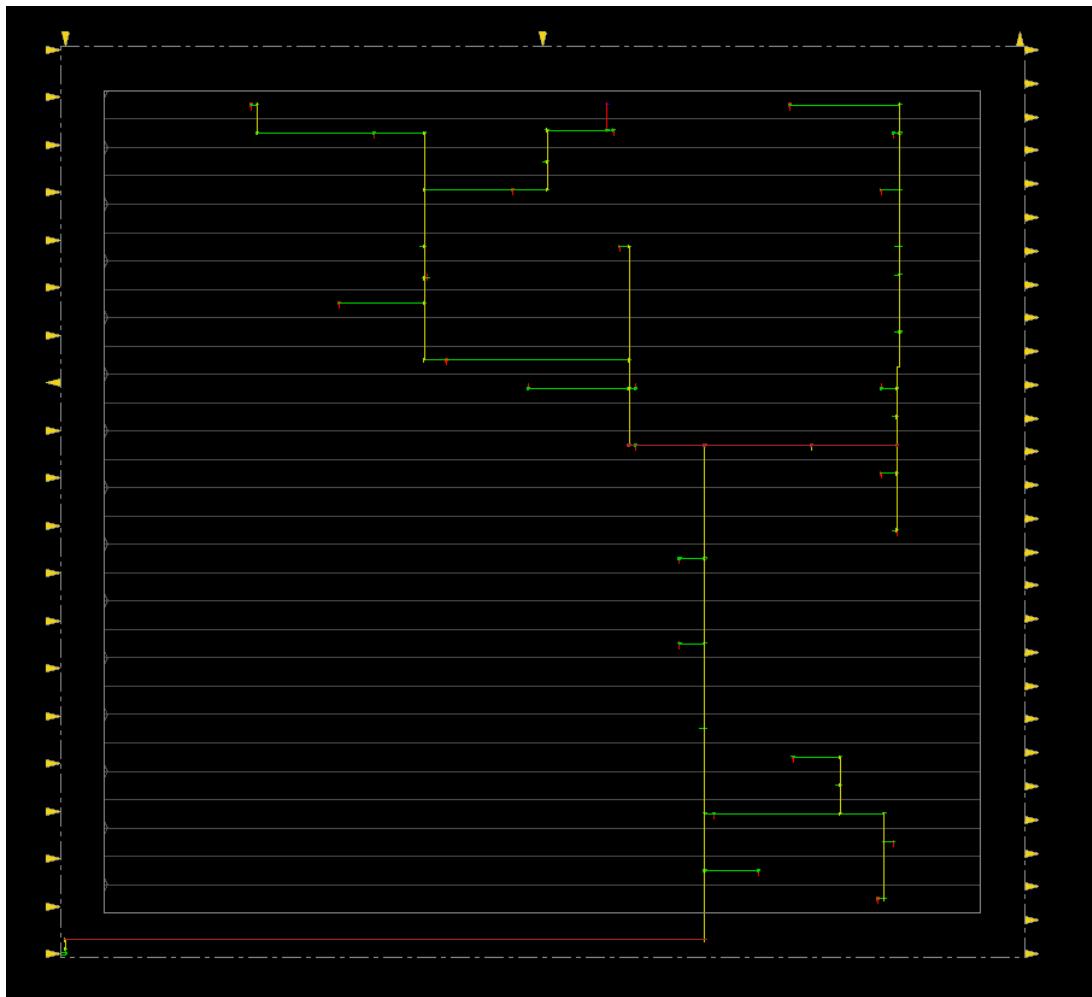
Area of Inverters: 259.617  $\mu\text{m}^2$

Area of flip flops: 935.528  $\mu\text{m}^2$

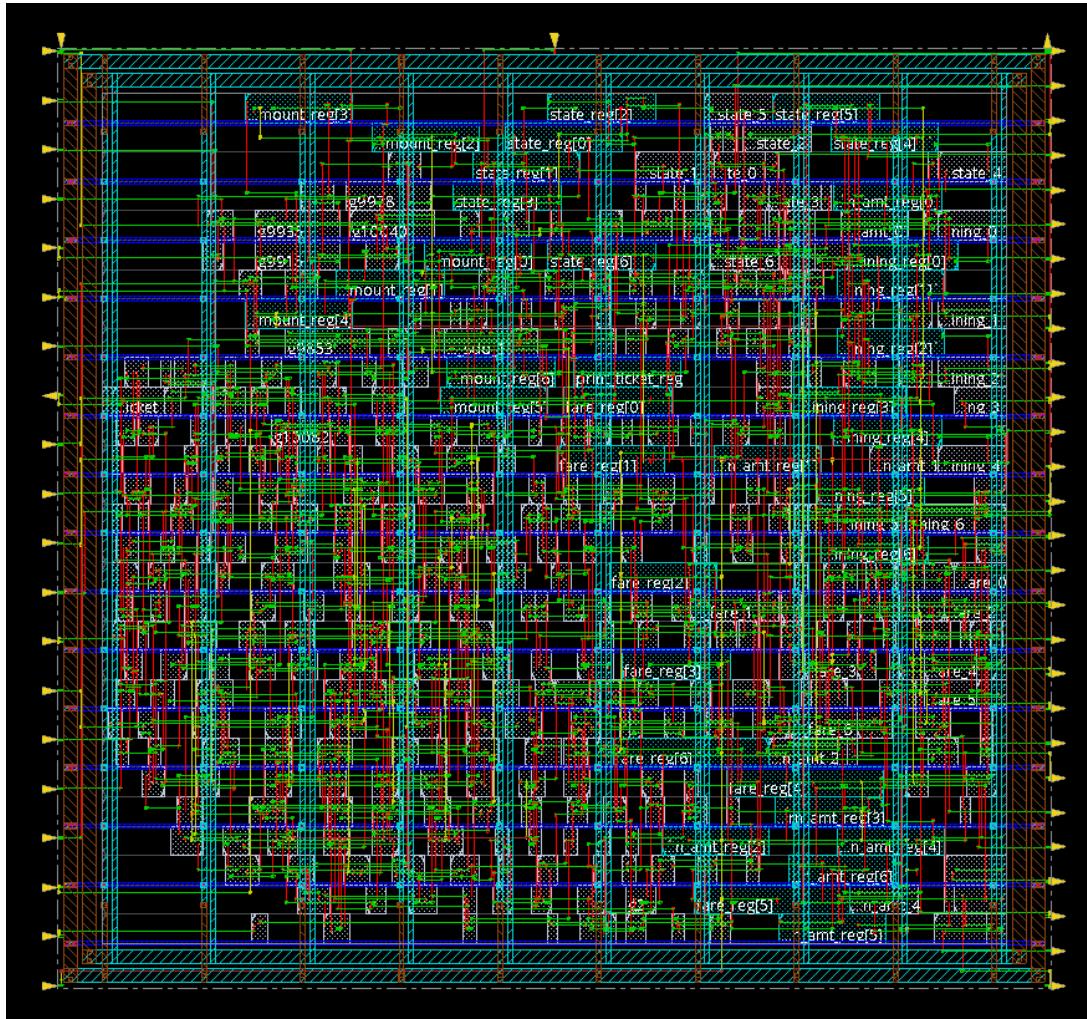
Area of Combinational cells: 1769.632  $\mu\text{m}^2$

Total Area: 3259.968  $\mu\text{m}^2$

## CLOCK ROUTING



## LAYOUT



## AFTER ROUTING

### GBA SETUP SLACK

```
#####
# Generated by: Cadence Innovus 20.10-p004_1
# OS: Linux x86_64(Host ID edatools-server2.iitd.edu.in)
# Generated on: Thu Nov 14 16:19:53 2024
# Design: ticket_machine_fsm
# Command: report_timing -max_path 100 -late > report_dir/after_routing/timing_setup_report_GBA.rpt
#####
Path 1: MET Setup Check with Pin fare_reg[5]/CK
Endpoint: fare_reg[5]/D ('^') checked with leading edge of 'clk'
Beginpoint: dest_station[2] (^) triggered by leading edge of 'clk'
Path Groups: {clk}
Analysis View: view1
Other End Arrival Time -0.001
- Setup 0.248
+ Phase Shift 4.220
- Uncertainty 0.100
= Required Time 3.871
- Arrival Time 3.859
= Slack Time 0.012
    Clock Rise Edge 0.000
    + Input Delay 1.500
    = Beginpoint Arrival Time 1.500
+-----+
| Instance | Arc | Cell | Delay | Arrival | Required |
|          |     |      |        | Time   | Time    |
+-----+-----+-----+-----+-----+-----+
|          | dest_station[2] ^ |       |       |       |       |
| g10239 | A ^ -> Y v | CLKINVX1 | 0.065 | 1.565 | 1.512 |
| g10189 | B v -> Y ^ | NOR2X1  | 0.138 | 1.703 | 1.715 |
| g10137 | B ^ -> Y v | NAND2XL | 0.553 | 2.256 | 2.268 |
| g10095 | A1 v -> Y ^ | OAI22X1 | 0.241 | 2.497 | 2.509 |
| g9990 | C ^ -> Y ^ | OR4X1   | 0.165 | 2.662 | 2.674 |
| g9940 | A ^ -> Y v | NAND2X1 | 0.128 | 2.790 | 2.802 |
| g9923 | A0 v -> Y ^ | AOI21X1 | 0.233 | 3.023 | 3.034 |
| g9910 | A1 ^ -> Y v | AOI21X2 | 0.142 | 3.165 | 3.177 |
| g9896 | A1 v -> Y ^ | OAI21X2 | 0.166 | 3.330 | 3.342 |
| g9858 | A1 ^ -> Y v | AOI21X2 | 0.108 | 3.438 | 3.450 |
| g9834 | B v -> Y ^ | MXI2X1  | 0.101 | 3.539 | 3.551 |
| g9823 | B ^ -> Y v | NAND2XL | 0.087 | 3.626 | 3.638 |
| g9818 | A1N v -> Y v | OAI2BB1X1 | 0.164 | 3.789 | 3.801 |
| g9816 | B0 v -> Y ^ | OAI21X1 | 0.070 | 3.859 | 3.871 |
| fare_reg[5] | D ^ | SDFFRHQX8 | 0.000 | 3.859 | 3.871 |
+-----+
```

The critical setup path identified by GBA starts from the begin point **dest\_station[2]** and ends at **fare\_reg[5]/D**.

In this **GBA analysis**, the Required Time (RT) is calculated as the End Arrival Time (default latency of clock, which is 0 but can be modified with constraints) - Setup + Phase Shift (defined clock time period in the constraint file) - Uncertainty. In this case, it is  $-0.001 - 0.248 + 4.220 - 0.100 = 3.871$ .

Arrival time is determined through Forward Traversal of the Timing Graph and is found to be 3.859. Hence, the Slack is computed as (Required Time - Arrival Time), resulting in a value of 0.012 (no violation).

## PBA SETUP SLACK

```
#####
# Generated by: Cadence Innovus 20.10-p004
# OS: Linux x86_64(Host ID edatools-server2.iitd.edu.in)
# Generated on: Thu Nov 14 16:19:53 2024
# Design: ticket_machine fsm
# Command: report timing -retime path slew_propagation -max_path 100 -late -format retime_slew > report_dir/after_routing/timing_setup_report_PBA.rpt
#####
Path 1: MET Setup Check with Pin fare_reg[5]/CK
Endpoint: fare_reg[5]/D (^) checked with leading edge of 'clk'
Beginpoint: dest_station[2] (^) triggered by leading edge of 'clk'
Path Groups: {clk}
Analysis View: view1
Retime Analysis { Data Path-Slew }
Other End Arrival Time -0.001
- Setup 0.243
+ Phase Shift 4.220
- Uncertainty 0.100
= Required Time 3.876
- Arrival Time 3.808
= Slack Time 0.068
= Slack Time(original) 0.012
  Clock Rise Edge 0.000
  + Input Delay 1.500
  = Beginpoint Arrival Time 1.500
  +-----+
    | Retime |
    | Slew |
    |-----|
    | 0.003 |
    | 0.003 |
    | 0.003 |
    | 0.003 |
    | 0.154 |
    | 0.154 |
    | 0.751 |
    | 0.751 |
    | 0.268 |
    | 0.268 |
    | 0.071 |
    | 0.071 |
    | 0.145 |
    | 0.145 |
    | 0.234 |
    | 0.234 |
    | 0.145 |
    | 0.145 |
    | 0.165 |
    | 0.165 |
    | 0.164 |
    | 0.164 |
    | 0.085 |
    | 0.085 |

```

The critical setup path identified by GBA starts from the begin point **dest\_station[2]** and ends at **fare\_reg[5]/D**.

In this **GBA analysis**, the Required Time (RT) is calculated as the End Arrival Time (default latency of clock, which is 0 but can be modified with constraints) - Setup + Phase Shift (defined clock time period in the constraint file) - Uncertainty. In this case, it is  $-0.001 - 0.243 + 4.220 - 0.100 = 3.876$ .

Arrival time is determined through Forward Traversal of the Timing Graph and is found to be 3.808. Hence, the Slack is computed as (Required Time - Arrival Time), resulting in a value of 0.012( no violation).

## GBA HOLD SLACK

```
#####
# Generated by: Cadence Innovus 20.10-p004_1
# OS: Linux x86_64(Host ID edatools-server2.iitd.edu.in)
# Generated on: Thu Nov 14 16:19:53 2024
# Design: ticket_machine_fsm
# Command: report_timing -max_path 100 -early > report_dir/after_routing/timing_hold_report_GBA.rpt
#####
Path 1: MET Hold Check with Pin remaining_reg[2]/CK
Endpoint: remaining_reg[2]/SI (v) checked with leading edge of 'clk'
Beginpoint: remaining_reg[3]/Q (v) triggered by leading edge of 'clk'
Path Groups: {clk}
Analysis View: view1
Other End Arrival Time 0.001
+ Hold 0.048
+ Phase Shift 0.000
+ Uncertainty 0.100
= Required Time 0.149
Arrival Time 0.373
Slack Time 0.224
    Clock Rise Edge 0.000
    + Clock Network Latency (Prop) 0.001
    = Beginpoint Arrival Time 0.001
+-----+
| Instance | Arc | Cell | Delay | Arrival | Required |
|          |     |      |        | Time   | Time     |
+-----+
| remaining_reg[3] | CK ^ |          |        | 0.001 | -0.224 |
| remaining_reg[3] | CK ^ -> Q v | SDFFRHQX1 | 0.373 | 0.373 | 0.149 |
| remaining_reg[2] | SI v | SDFFRHQX1 | 0.000 | 0.373 | 0.149 |
+-----+
```

The Worst Hold Path of GBA is mentioned above with begin point of remaining\_reg[3]/Q and endpoint of remaining\_reg [2]/SI.

In the above GBA the Required Time = End Arrival Time(latency of clock which is 0 by default but can be changed using constraint) + hold + Phase Shift(clock time period defined in constraint file)+ Uncertainty = 0 + 0.048+0.1 = 0.148 ns Arrival time is computed using Forward Traversal of Timing Graph.

Arrival time = 0.373

Slack = Arrival Time - Required Time = 0.224

## PBA HOLD SLACK

```
#####
# Generated by: Cadence Innovus 20.10-p004_1
# OS: Linux x86_64(Host ID edatools-server2.iitd.edu.in)
# Generated on: Thu Nov 14 16:19:54 2024
# Design: ticket_machine_fsm
# Command: report_timing -retime_path_slew_propagation -max_path 100 -early -format retime_slew > report_dir/after_routing/timing_hold_report_PBA.rpt
#####
Path 1: MET Hold Check with Pin remaining_reg[2]/CK
Endpoint: remaining_reg[2]/SI (v) checked with leading edge of 'clk'
Beginpoint: remaining_reg[3]/Q (v) triggered by leading edge of 'clk'
Path Groups: {clk}
Analysis View: view1
Retime Analysis { Data Path-Slew }
Other End Arrival Time 0.001
+ Hold 0.049
+ Phase Shift 0.000
+ Uncertainty 0.100
= Required Time 0.149
Arrival Time 0.373
Slack Time 0.224
= Slack Time(original) 0.224
    Clock Rise Edge 0.000
    + Clock Network Latency (Prop) 0.001
    = Beginpoint Arrival Time 0.001
+-----+
| Retime | Slew |
|-----|
| 0.007 | 0.092 |
| 0.092 | 0.092 |
+-----+
```

The Worst Hold Path of GBA is mentioned above with begin point of remaining\_reg[3]/Q and endpoint of remaining\_reg [2]/SI.

In the above GBA the Required Time = End Arrival Time(latency of clock which is 0 by default but can be changed using constraint) + hold + Phase Shift(clock time period defined in constraint file)+ Uncertainty = 0 + 0.049+0.1 = 0.149 ns Arrival time is computed using Forward Traversal of Timing Graph.

Arrival time = 0.373

Slack = Arrival Time - Required Time = 0.224

## AREA

Hinst Name	Module Name	Inst Count	Total Area	Buffer	Inverter	Combinational	Flop
Physical	ticket_machine_fsm	435	3259.968	295.191	259.617	1769.632	935.528

### Area Report:

Area of Buffers: 295.191  $\mu\text{m}^2$

Area of Inverters: 259.617  $\mu\text{m}^2$

Area of Flip flops: 935.528  $\mu\text{m}^2$

Area of Combinational cells: 1769.632  $\mu\text{m}^2$

Total Area: 3259.968  $\mu\text{m}^2$

## POWER

### Power Report

**Internal power:** It is the power consumed within the confines of a cell, arises from the charging or discharging of internal capacitances during switching. The cumulative internal power dissipation is measured at 0.3511mW which is 34.0547% of total consumed power.

**Switching power:** It refers to the energy consumed by a driving cell when it charges and discharges the load capacitance connected to its output. In this case, the overall switching power amounts to 0.6607mW which is 64.0867% of total power.

**Leakage power:** This leakage current is the current that flows from VDD to GND when there is no switching. The total leakage power is 0.01916mW which is 1.8586 % of total power.

**Total power:** Total power is the sum of the all above powers which is 1.0310mW.

```

Total Power
-----
Total Internal Power:      0.35111485      34.0547%
Total Switching Power:    0.66075394      64.0867%
Total Leakage Power:      0.01916239      1.8586%
Total Power:              1.03103118

Ended Static Power Report Generation: (cpu=0:00:00, real=0:00:00,
mem(process/total/peak)=1119.99MB/2615.21MB/1158.04MB)

-----
*           Innovus 20.10-p004_1 (64bit) 05/07/2020 20:02 (Linux 2.6.32-431.11.2.el6.x86_64)
*
*
*       Date & Time:    2024-Nov-14 16:19:54 (2024-Nov-14 10:49:54 GMT)
*
*-----*
*       Design: ticket_machine_fsm
*
*       Liberty Libraries used:
*           view1: ../lib/90/slow.lib
*
*       Power Domain used:
*           Rail:      VDD      Voltage:      0.9
*
*       Power View : view1
*
*       User-Defined Activity : N.A.
*
*       Activity File: N.A.
*
*       Hierarchical Global Activity: N.A.
*
*       Global Activity: N.A.
*
*       Sequential Element Activity: 0.200000
*
*       Primary Input Activity: 0.200000
*
*       Default icg ratio: N.A.
*
*       Global Comb ClockGate Ratio: N.A.
*
*       Power Units = 1mW
*
*       Time Units = 1e-09 secs
*
*       Temperature = 125
*
*       report_power -outfile 50_after_routing_reports/power.rpt -rail_analysis_format VS
*-----*

Cell          Internal      Switching      Total      Leakage      Cell
                  Power        Power        Power        Power        Name
-----
FE_OFC0_DFT_sdo_1      0.001992      0.01973      0.02195      0.0002199  CLKBUFX12
FE_OFC4_state_5        0.001991      0.01959      0.0218      0.0002199  CLKBUFX12
FE_OFC7_fare_6         0.001989      0.01956      0.02177      0.0002199  CLKBUFX12
FE_OFC13_return_amt_0   0.001992      0.01953      0.02174      0.0002199  CLKBUFX12
FE_OFC18_return_amt_1   0.001993      0.0195      0.02171      0.0002199  CLKBUFX12
FF_OFR12_return_amt_2   0.001995      0.0195      0.02171      0.0002199  CLKBUFX12

```

Total Power

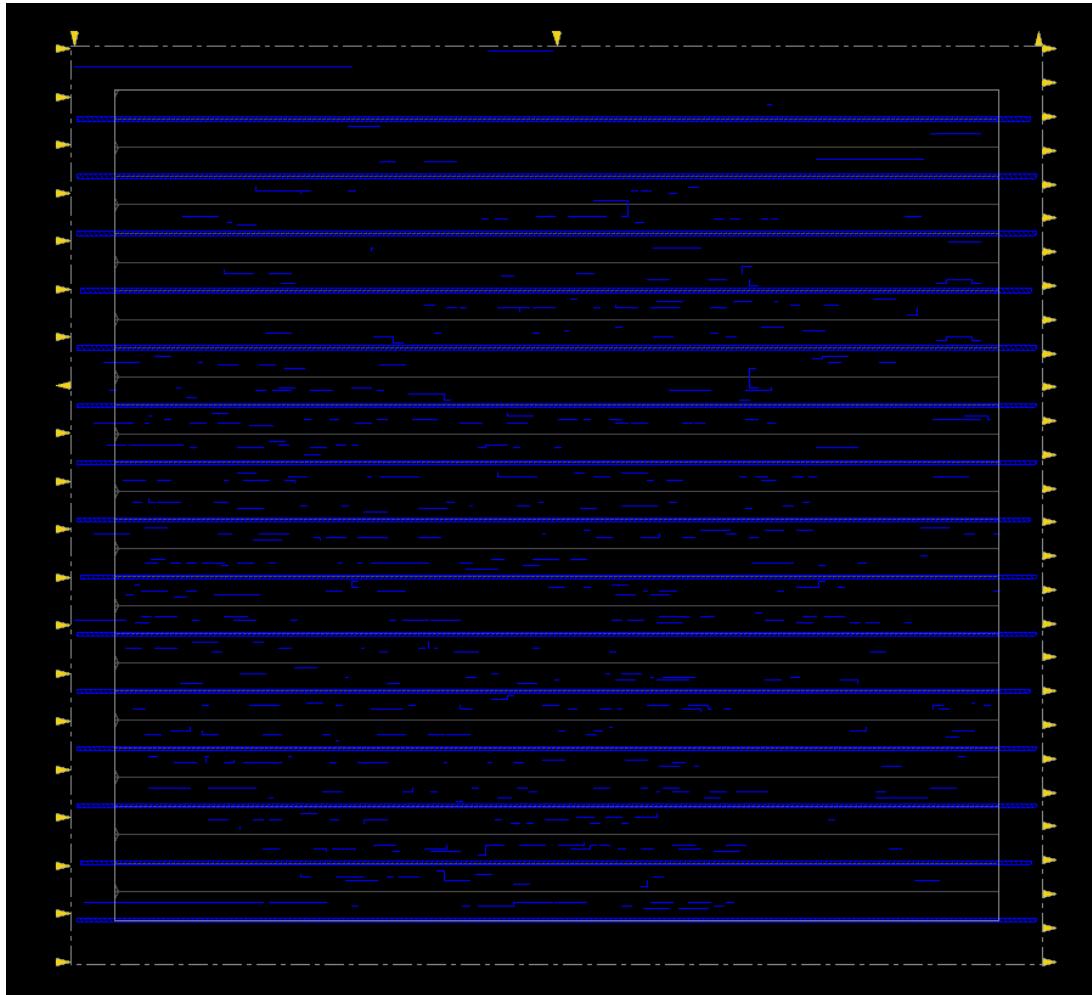
Total Internal Power:	0.35111485	34.0547%
Total Switching Power:	0.66075394	64.0867%
Total Leakage Power:	0.01916239	1.8586%
Total Power:	1.03103118	

Ended Static Power Report Generation: (cpu=0:00:00, real=0:00:00,  
mem(process/total/peak)=1119.99MB/2615.21MB/1158.04MB)

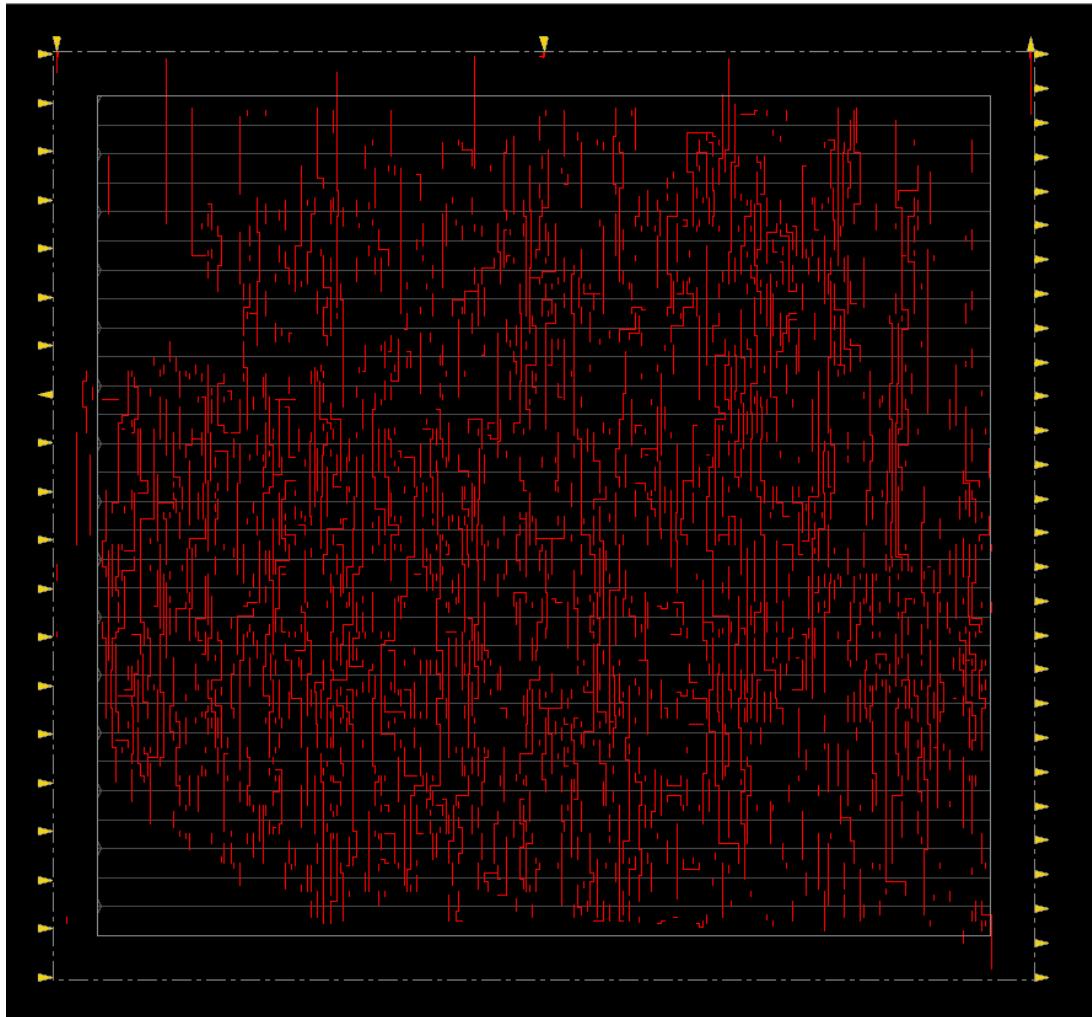
g10000Z	2.073e-05	3.517e-05	8.392e-05	2.802e-05	NAND2X2
g10121	2.441e-05	2.134e-05	7.176e-05	2.601e-05	AND4X1
g10033	1.813e-05	2.314e-05	6.907e-05	2.78e-05	NAND4BXL
g10080	1.212e-05	2.702e-05	6.694e-05	2.78e-05	NAND4BXL
g9889	3.006e-05	2.277e-05	6.585e-05	1.301e-05	CLKINVX1
g10042	3.089e-05	1.211e-05	6.304e-05	2.004e-05	NOR2BX1
g9995	3.36e-05	1.059e-05	6.233e-05	1.815e-05	AOI21X1
g9993	1.9e-05	2.778e-05	5.98e-05	1.301e-05	CLKINVX1
g10119	1.296e-05	1.898e-05	5.974e-05	2.78e-05	NAND4BXL
g9902	1.069e-05	3.482e-05	5.786e-05	1.236e-05	NOR2XL
g10022	1.489e-05	2.941e-05	5.731e-05	1.301e-05	CLKINVX1
g9926	2.897e-05	7.904e-06	5.502e-05	1.815e-05	AOI21X1
g10073	2.279e-05	1.665e-05	5.179e-05	1.236e-05	NOR2XL
g10037	1.215e-05	1.94e-05	5.149e-05	1.995e-05	AOI211X1
FE_OF_C43_n_363	9.302e-06	2.818e-05	5.05e-05	1.301e-05	INVX1
g10008	2.618e-05	1.129e-05	5.046e-05	1.299e-05	OAI21X1
g9891	2.018e-05	1.105e-05	4.974e-05	1.851e-05	AOI32X1
g10041	2.206e-05	5.299e-06	4.74e-05	2.004e-05	NOR2BX1
g9943	1.202e-05	1.487e-05	4.61e-05	1.92e-05	OAI2BB1XL
g9852	6.732e-06	2.763e-06	4.369e-05	3.419e-05	NAND3BX1
g10004	8.505e-06	1.718e-05	3.804e-05	1.236e-05	NOR2XL
g10003	7.484e-06	1.542e-05	3.592e-05	1.301e-05	CLKINVX1
g9901	1.599e-05	6.86e-06	3.505e-05	1.22e-05	AOI21XL
g9860	9.276e-06	6.395e-06	3.487e-05	1.92e-05	OAI2BB1XL
g9913	1.538e-05	6.643e-06	3.423e-05	1.22e-05	AOI21XL
g10005	9.684e-06	3.325e-06	3.393e-05	2.093e-05	NOR4X1
g9882	1.55e-05	4.606e-06	3.23e-05	1.22e-05	AOI21XL
g9900	1.286e-05	4.487e-06	3.033e-05	1.299e-05	OAI21X1
g9914	1.011e-05	4.075e-06	2.717e-05	1.299e-05	OAI21X1
g9885	1.087e-05	2.953e-06	2.618e-05	1.236e-05	NOR2XL
g9916	1.066e-05	3.046e-06	2.606e-05	1.236e-05	NOR2XL
g9886	5.745e-06	4.624e-06	2.439e-05	1.403e-05	NAND2X1
g10078	1.001e-05	4.448e-06	2.438e-05	9.93e-06	NAND3XL
g9930	7.68e-06	3.38e-06	2.342e-05	1.236e-05	NOR2XL
g9927	7.528e-06	2.728e-06	2.324e-05	1.299e-05	OAI21X1
g10036	5.69e-06	4.474e-06	2.318e-05	1.301e-05	CLKINVX1
g9905	6.576e-06	1.684e-06	2.062e-05	1.236e-05	NOR2XL
g9856	8.084e-06	3.483e-06	2.03e-05	8.728e-06	OAI21XL
g10071	4.797e-06	4.177e-06	1.826e-05	9.289e-06	NAND2XL
g10072	4.502e-06	3.992e-06	1.778e-05	9.289e-06	NAND2XL
g9850	4.357e-06	2.269e-06	1.592e-05	9.289e-06	NAND2XL
g9823	4.001e-06	2.018e-06	1.531e-05	9.289e-06	NAND2XL
g9917	2.83e-06	2.691e-06	1.481e-05	9.289e-06	NAND2XL
g9904	2.346e-06	1.954e-06	1.359e-05	9.289e-06	NAND2XL
g9829	1.867e-06	1.58e-06	1.274e-05	9.289e-06	NAND2XL
g9931	1.332e-06	9.95e-07	1.162e-05	9.289e-06	NAND2XL

Total ( 435 of 435 )	0.3511	0.6608	1.031	0.01916
Total Capacitance	3.414e-11 F			
Power Density	*** No Die Area ***			

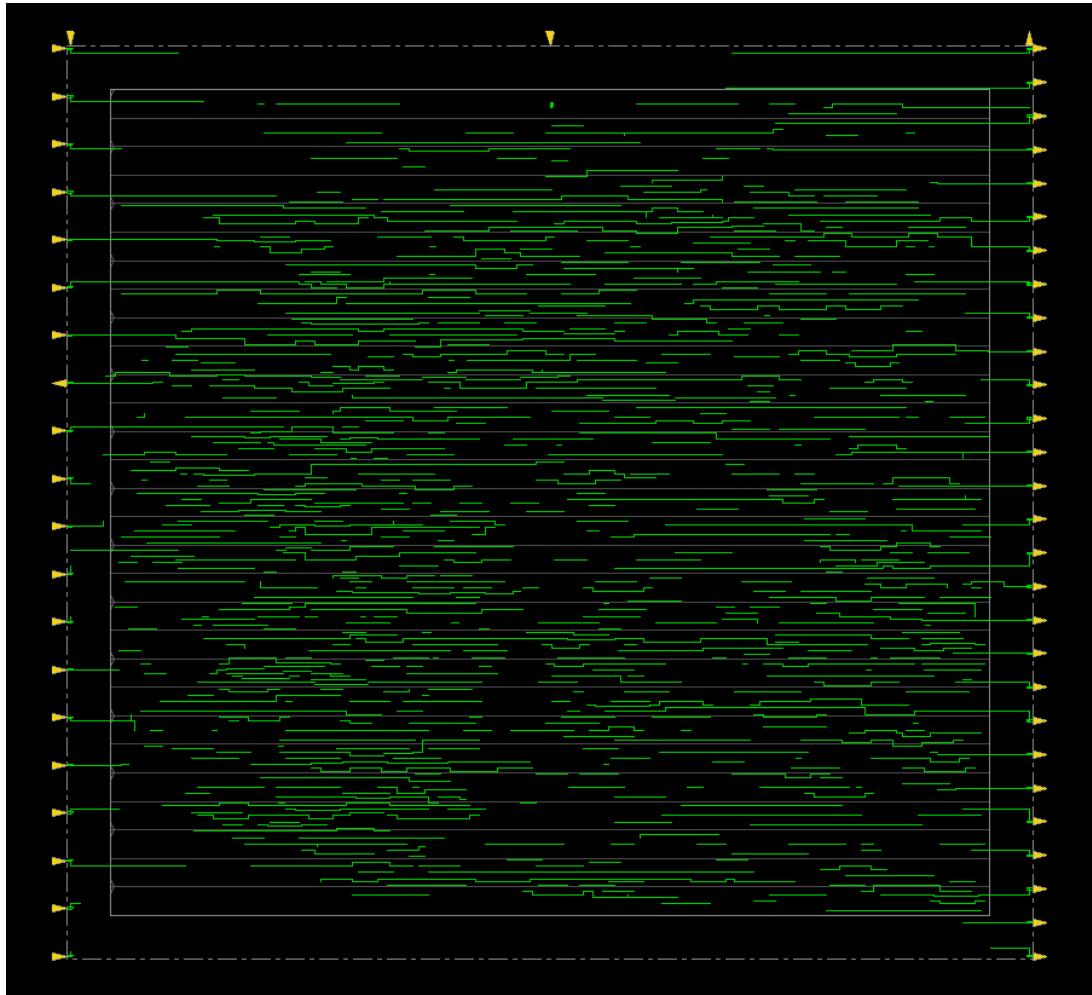
## METAL-1



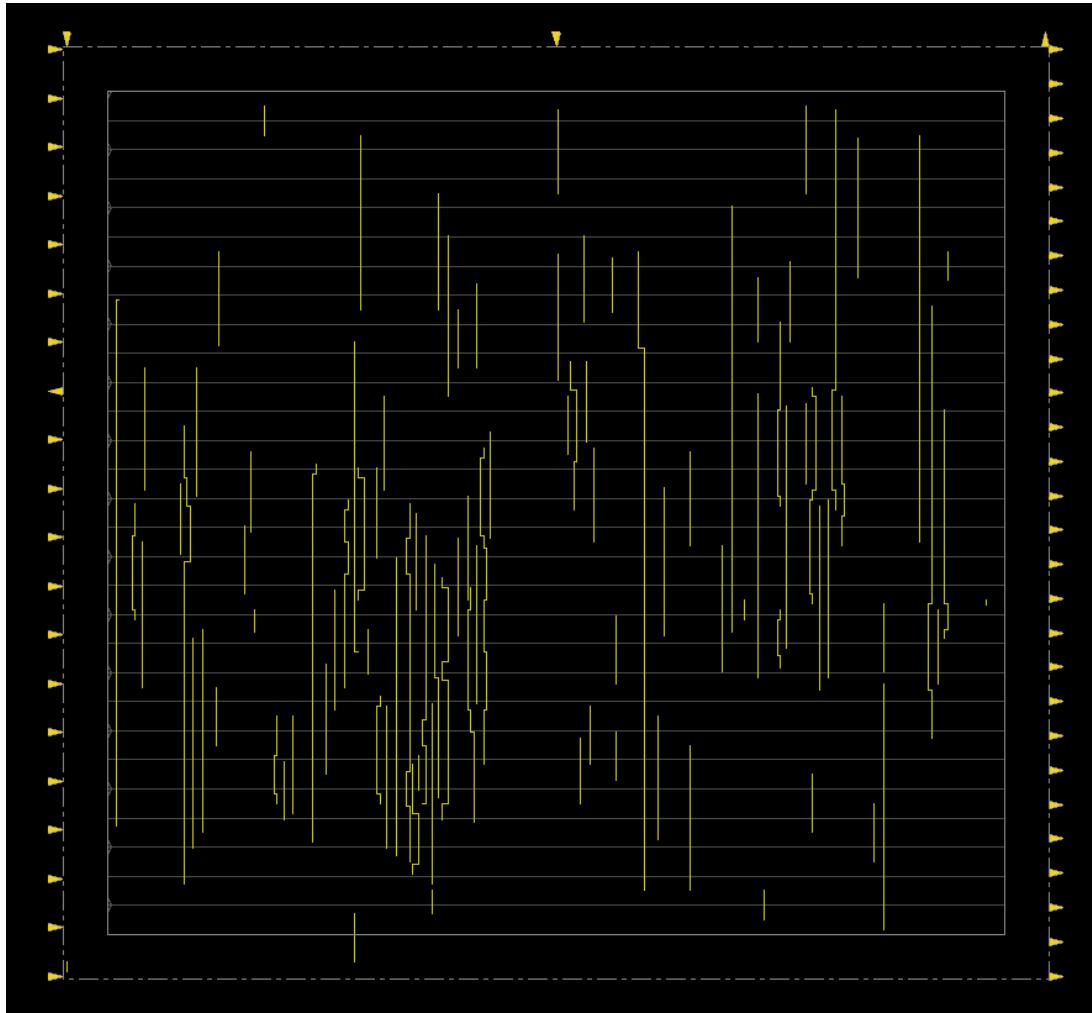
## METAL-2



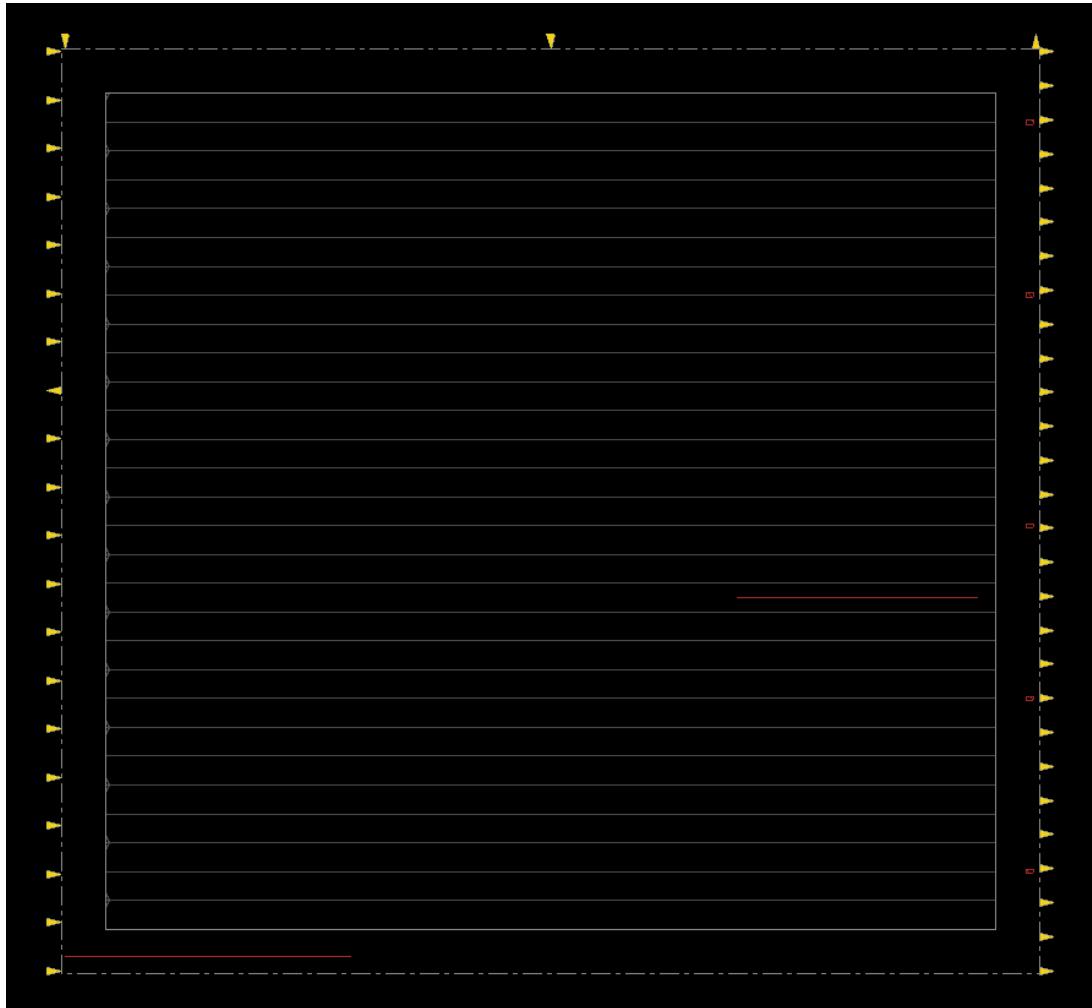
## METAL-3



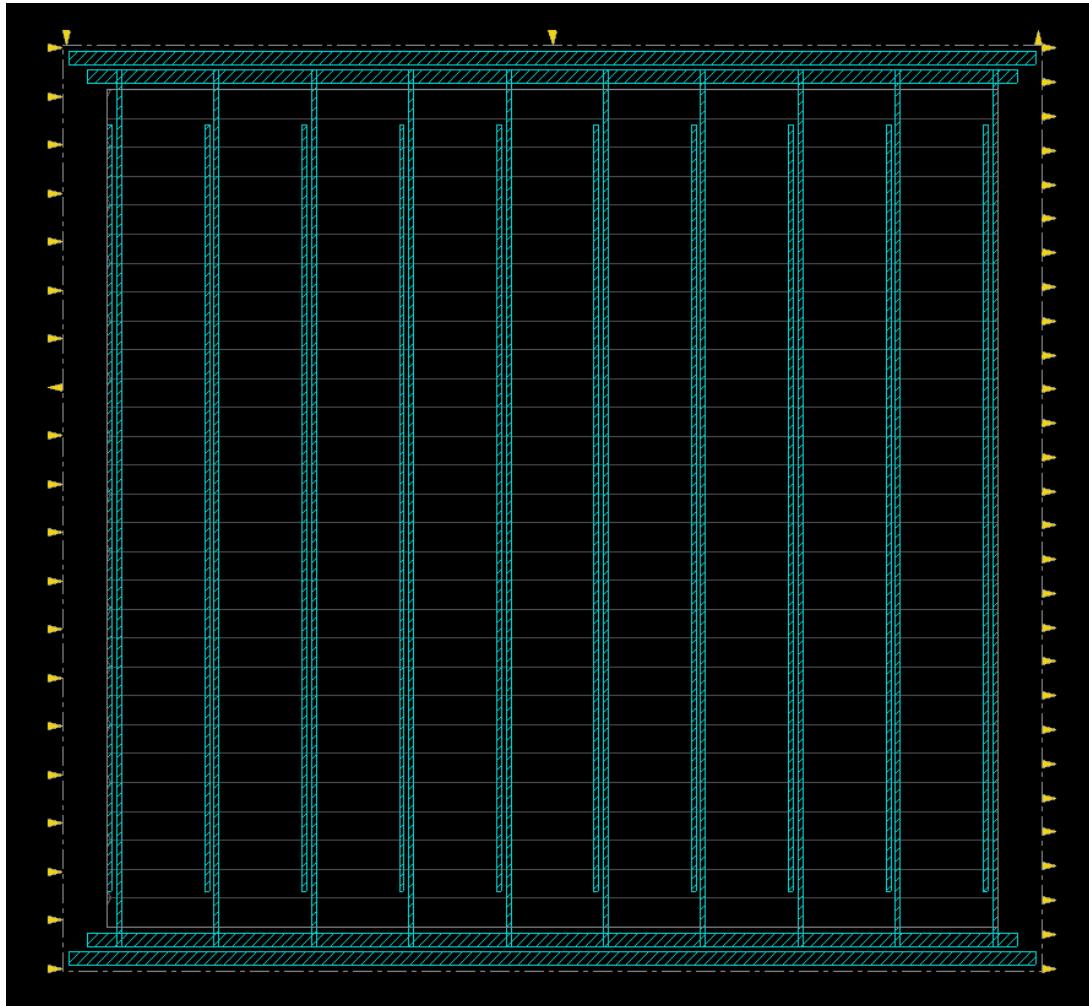
## METAL-4



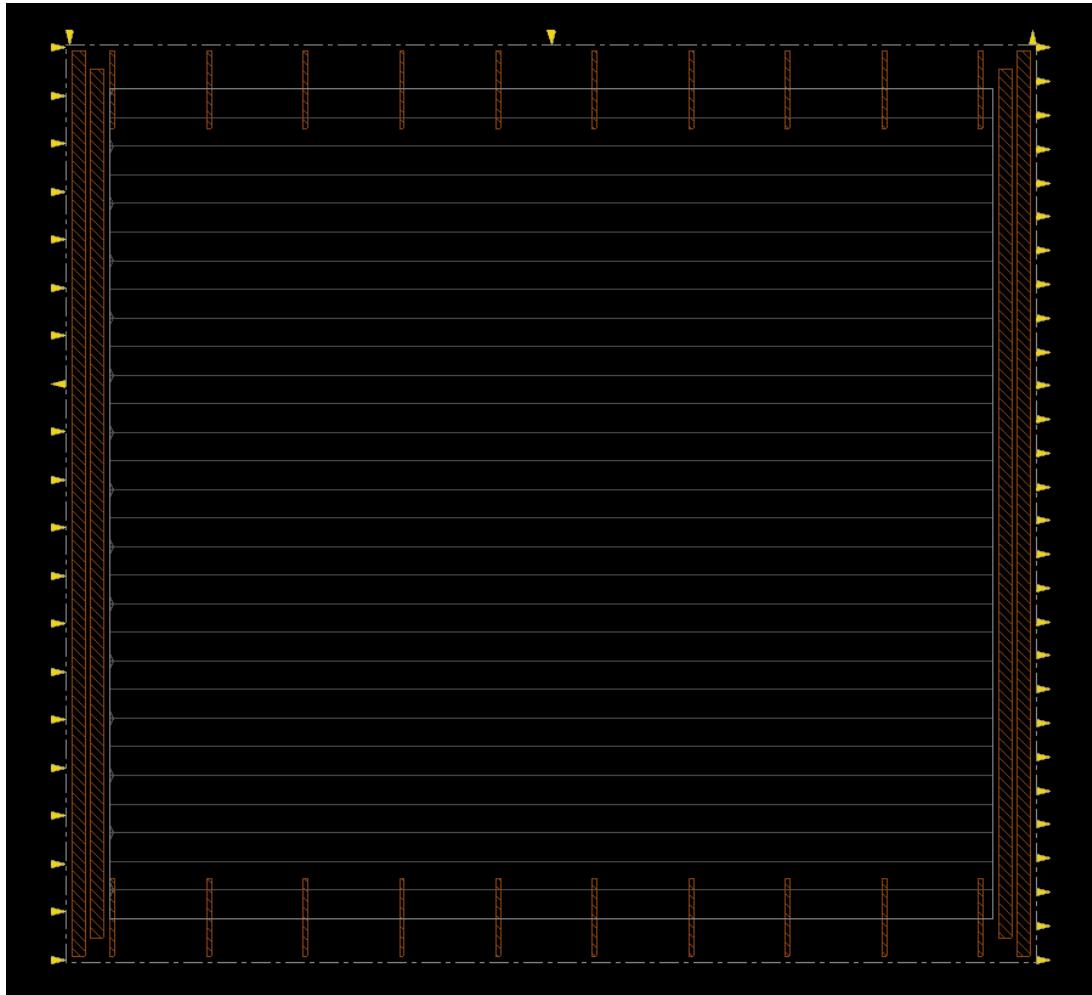
## METAL-5



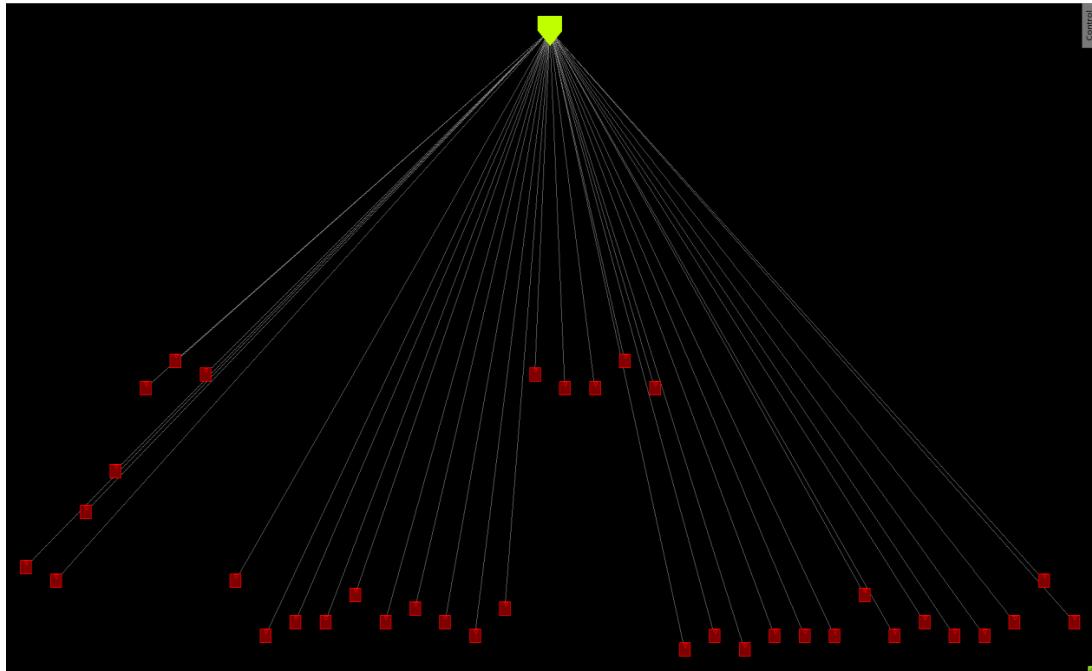
## METAL-8



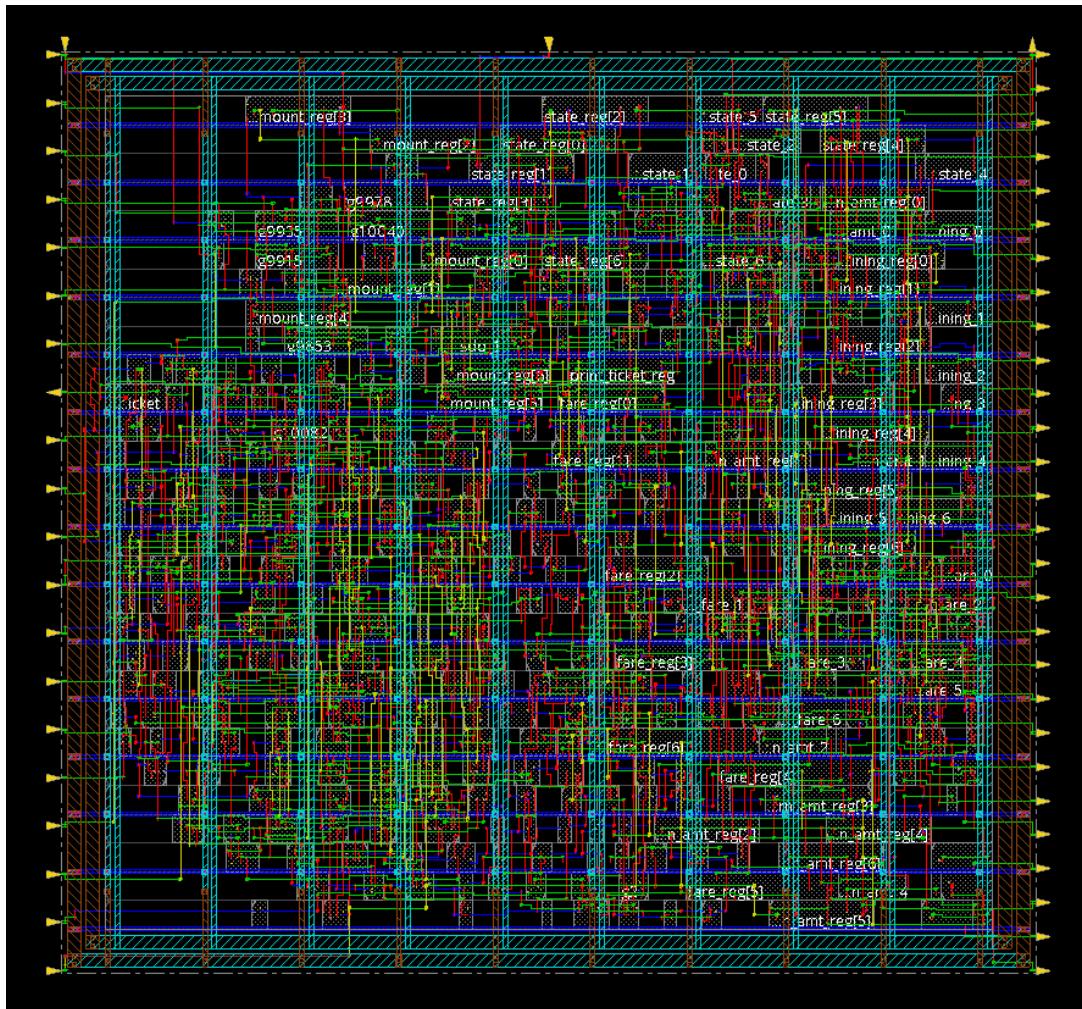
## METAL-9



CTS



## FINAL ROUTING

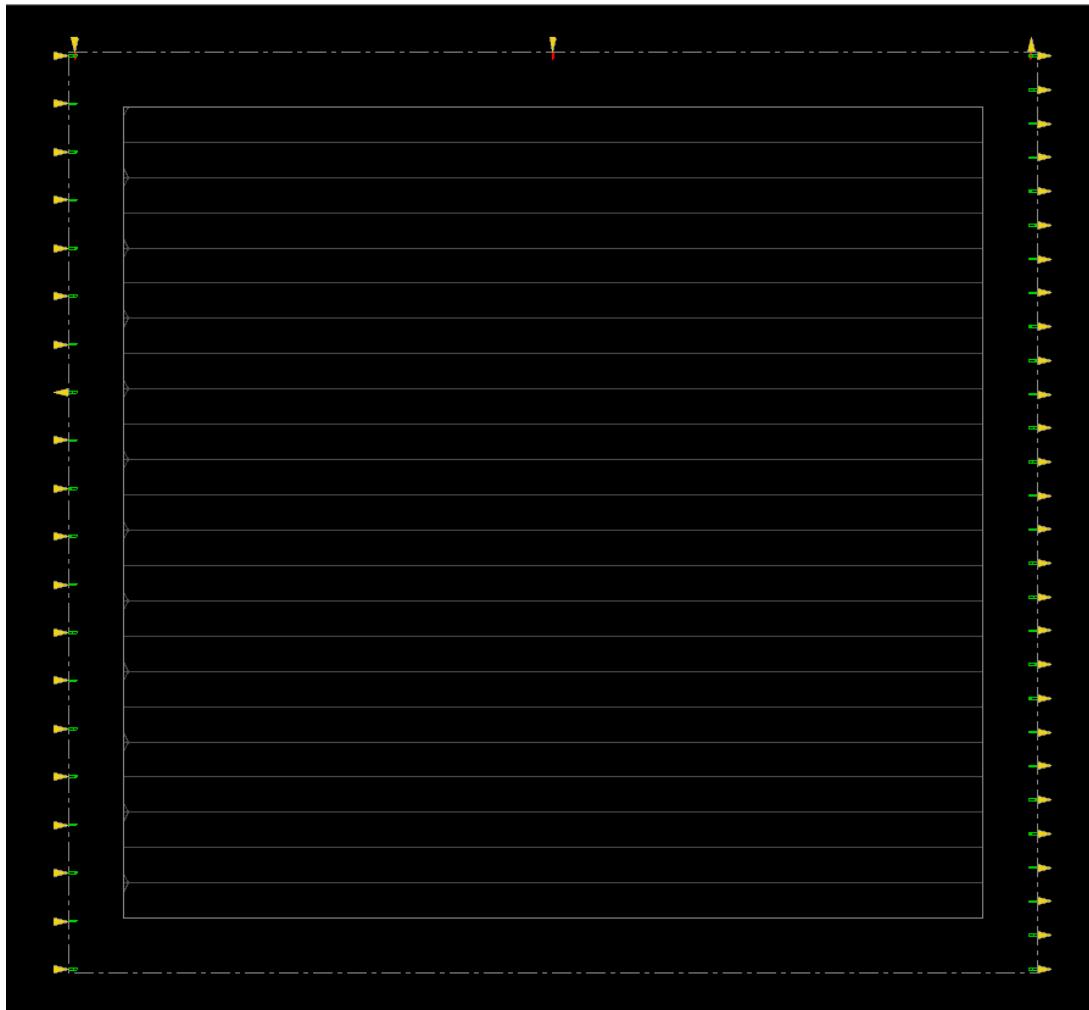


## DRC VIOLATION

```
*** Starting Verify DRC (MEM: 1399.7) ***  
  
VERIFY DRC ..... Starting Verification  
VERIFY DRC ..... Initializing  
VERIFY DRC ..... Deleting Existing Violations  
VERIFY DRC ..... Creating Sub-Areas  
VERIFY DRC ..... Using new threading  
VERIFY DRC ..... Sub-Area: {0.000 0.000 88.740 83.810} 1 of 1  
VERIFY DRC ..... Sub-Area : 1 complete 0 Viols.  
  
Verification Complete : 0 Viols.  
  
*** End Verify DRC (CPU: 0:00:00.1 ELAPSED TIME: 0.00 MEM: 0.0M) ***
```

## FLOOR PLANNING :

Utilization 0.8 (Smaller die area):



## BEFORE PLACEMENT

### GBA SETUP SLACK

```
#####
# Generated by: Cadence Innovus 20.10-p004_1
# OS: Linux x86_64(Host ID edatools-server2.iitd.edu.in)
# Generated on: Fri Nov 15 12:06:30 2024
# Design: ticket_machine fsm
# Command: report_timing -max_path 100 -late > report_dir/before_placement_80/timing_setup_report_GBA.rpt
#####
Path 1: VIOLATED Setup Check with Pin return_amt_reg[6]/D
Endpoint: return_amt_reg[6]/D (^) checked with leading edge of 'clk'
Beginpoint: total_amount_reg[6]/Q (^) triggered by leading edge of 'clk'
Path Groups: {clk}
Analysis View: view1
Other End Arrival Time      0.000
- Setup                      0.242
+ Phase Shift                4.220
- Uncertainty                 0.100
= Required Time              3.878
- Arrival Time               8.359
= Slack Time                 -4.481
    Clock Rise Edge          0.000
    + Clock Network Latency (Ideal) 0.000
    = Beginpoint Arrival Time   0.000
+-----+
| Instance | Arc | Cell | Delay | Arrival | Required |
|-----+-----+-----+-----+-----+-----+
| total_amount_reg[6] | CK ^ |          |       | 0.000 | -4.481 |
| total_amount_reg[6] | CK ^ -> Q ^ | SDFFRHQX1 | 6.418 | 6.418 | 1.937 |
| g10172           | B ^ -> Y v | NAND2BX1  | 0.877 | 7.294 | 2.813 |
| g9911            | B0 v -> Y ^ | OAI2BB1X1 | 0.251 | 7.546 | 3.065 |
| g9903            | AN ^ -> Y ^ | NOR2BX1   | 0.340 | 7.886 | 3.405 |
| g9891            | A2 ^ -> Y v | AOI32X1   | 0.180 | 8.066 | 3.585 |
| g9861            | B0 v -> Y ^ | OAI2BB1XL | 0.293 | 8.359 | 3.878 |
| return_amt_reg[6] | D ^ | SDFFRHQX8 | 0.000 | 8.359 | 3.878 |
+-----+
```

The critical setup path identified by GBA starts from the begin point **total\_amount\_reg[6]/Q** and ends at **return\_amt\_reg[6]/D**.

In this **GBA analysis**, the Required Time (RT) is calculated as the End Arrival Time (default latency of clock, which is 0 but can be modified with constraints) - Setup + Phase Shift (defined clock time period in the constraint file) - Uncertainty. In this case, it is  $0 - 0.242 + 4.220 - 0.100 = 3.878$ .

Arrival time is determined through Forward Traversal of the Timing Graph and is found to be 8.359. Hence, the Slack is computed as (Required Time - Arrival Time), resulting in a value of -4.481(violation).

## PBA SETUP SLACK

```
#####
# Generated by: Cadence Innovus 20.10-p004.1
# OS: Linux x86_64(Host ID edatools-server2.iitd.edu.in)
# Generated on: Fri Nov 15 12:06:31 2024
# Design: ticket_machine_fsm
# Command: report_timing -retime path slew_propagation -max_path 100 -late -format retime_slew > report_dir/before_placement_80/timing_setup_report_PBA.rpt
#####
Path 1: VIOLATED Setup Check with Pin return_amt_reg[6]/D
Endpoint: return_amt_reg[6]/D (^) checked with leading edge of 'clk'
Beginpoint: total_amount_reg[6]/Q (^) triggered by leading edge of 'clk'
Path Groups: {clk}
Analysis View: view1
Retime Analysis { Data Path-Slew }
Other End Arrival Time 0.000
- Setup 0.165
+ Phase Shift 4.220
- Uncertainty 0.100
= Required Time 3.955
- Arrival Time 8.164
= Slack Time -4.209
= Slack Time(original) -4.481
    Clock Rise Edge 0.000
    + Clock Network Latency (Ideal) 0.000
    = Beginpoint Arrival Time 0.000
    +
    | Retime |
    | Slew |
    |-----|
    0.500 |
    8.038 |
    8.038 |
    1.812 |
    1.812 |
    0.417 |
    0.417 |
    0.311 |
    0.311 |
    0.183 |
    0.183 |
    0.095 |
    0.095 |
    +-----+
```

The critical setup path identified by GBA starts from the begin point **total\_amount\_reg[6]/Q** and ends at **return\_amt\_reg[6]/D**.

In this **PBA analysis**, the Required Time (RT) is calculated as the End Arrival Time (default latency of clock, which is 0 but can be modified with constraints) - Setup + Phase Shift (defined clock time period in the constraint file) - Uncertainty. In this case, it is  $0 - 0.165 + 4.220 - 0.100 = 3.955$ .

Arrival time is determined through Forward Traversal of the Timing Graph and is found to be 8.164. Hence, the Slack is computed as (Required Time - Arrival Time), resulting in a value of -4.209(violation).

Hence setup lack of PBA increased in comparison to GBA .

## GBA HOLD SLACK

```
#####
# Generated by: Cadence Innovus 20.10-p004_1
# OS: Linux x86_64(Host ID edatools-server2.iitiid.edu.in)
# Generated on: Fri Nov 15 12:06:31 2024
# Design: ticket_machine_fsm
# Command: report_timing -max_path 100 -early > report_dir/before_placement_80/timing_hold_report_GBA.rpt
#####
Path 1: MET Hold Check with Pin total_amount_reg[1]/CK
Endpoint: total_amount_reg[1]/SI (v) checked with leading edge of 'clk'
Beginpoint: total_amount_reg[0]/Q (v) triggered by leading edge of 'clk'
Path Groups: {clk}
Analysis View: view1
Other End Arrival Time 0.000
+ Hold 0.117
+ Phase Shift 0.000
+ Uncertainty 0.100
= Required Time 0.217
Arrival Time 0.469
Slack Time 0.252
Clock Rise Edge 0.000
+ Clock Network Latency (Ideal) 0.000
= Beginpoint Arrival Time 0.000
+-----+
| Instance | Arc | Cell | Delay | Arrival | Required |
|-----+-----+-----+-----+-----+-----+
| total_amount_reg[0] | CK ^ | | | 0.000 | -0.252 |
| total_amount_reg[0] | CK ^ -> Q v | SDFFRHQX1 | 0.469 | 0.469 | 0.217 |
| total_amount_reg[1] | SI v | SDFFRHQX1 | 0.000 | 0.469 | 0.217 |
+-----+
```

The Worst Hold Path of GBA is mentioned above with begin point of **total\_amount\_reg[0]/Q** and endpoint of **total\_amount\_reg[1]/SI**. In the above GBA the Required Time = End Arrival Time(latency of clock which is 0 by default but can be changed using constraint) + hold + Phase Shift(clock time period defined in constraint file)+Uncertainty =  $0 + 0.117 + 0.1 = 0.217$  ns Arrival time is computed using Forward Traversal of Timing Graph.

Arrival time = 0.469

Slack = Arrival Time - Required Time = 0.252

## PBA HOLD SLACK

```
#####
# Generated by: Cadence Innovus 20.10-p004_1
# OS: Linux x86_64(Host ID edatools-server2.iitiid.edu.in)
# Generated on: Fri Nov 15 12:06:31 2024
# Design: ticket_machine_fsm
# Command: report_timing -retime path slew_propagation -max_path 100 -early -format retime_slew > report_dir/before_placement_80/timing_hold_report_PBA.rpt
#####
Path 1: MET Hold Check with Pin total_amount_reg[1]/CK
Endpoint: total_amount_reg[1]/SI (v) checked with leading edge of 'clk'
Beginpoint: total_amount_reg[0]/Q (v) triggered by leading edge of 'clk'
Path Groups: {clk}
Analysis View: view1
Retime Analysis { Data Path-Slew }
Other End Arrival Time 0.000
+ Hold 0.117
+ Phase Shift 0.000
+ Uncertainty 0.100
= Required Time 0.217
Arrival Time 0.469
Slack Time 0.252
= Slack Time(original) 0.252
Clock Rise Edge 0.000
+ Clock Network Latency (Ideal) 0.000
= Beginpoint Arrival Time 0.000
+-----+
| Retime |
| Slew |
|-----|
| 0.500 |
| 0.094 |
| 0.094 |
+-----+
```

The Worst Hold Path of GBA is mentioned above with begin point of **total\_amount\_reg[0]/Q** and endpoint of **total\_amount\_reg[1]/SI**. In the above GBA the Required Time = End Arrival Time(latency of clock which is 0 by default but can be changed using constraint) + hold + Phase Shift(clock time period defined in constraint file)+Uncertainty =  $0 + 0.117 + 0.1 = 0.217$  ns Arrival time is computed using Forward Traversal of Timing Graph.

Arrival time = 0.469

Slack = Arrival Time - Required Time = 0.252

**Hold slack is same for both the analysis.**

## AREA

Hinst Name	Module Name	Inst Count	Total Area	Buffer	Inverter	Combinational	Flop	Latch	Clock Gate	Macro
Physical										
ticket_machine_fsn 0.000		391	3043.495	0.000	84.016	1731.030	1228.449	0.000	0.000	0.000

Area Report:

Area of Buffers: 0.000 um^2

Area of Inverters: 84.016 um^2

Area of flip flops: 1228.449 um^2

Area of Combinational cells: 1731.038 um^2

Total Area: 3043.495 um^2

## POWER

### Power Report:

**Internal power:** It is the power consumed within the confines of a cell, arises from the charging or discharging of internal capacitances during switching. The cumulative internal power dissipation is measured at 0.5492mW which is 28.1672 % of total consumed power.

**Switching power:** It refers to the energy consumed by a driving cell when it charges and discharges the load capacitance connected to its output. In this case, the overall switching power amounts to 1.3837mW which is 70.9673 % of total power.

**Leakage power:** This leakage current is the current that flows from VDD to GND when there is no switching. The total leakage power is 0.0168mW which is 0.8655 % of total power.

**Total power:** Total power is the sum of the all above powers which is 1.9498mW.

```

*-----*
*   Innovus 20.10-p004_1 (64bit) 05/07/2020 20:02 (Linux 2.6.32-431.11.2.el6.x86_64)
*
*
*   Date & Time:    2024-Nov-15 12:06:31 (2024-Nov-15 06:36:31 GMT)
*
*-----*
*
*   Design: ticket_machine_fsm
*
*   Liberty Libraries used:
*       view1: ../../lib/90/slow.lib
*
*   Power Domain used:
*       Rail:      VDD      Voltage:      0.9
*
*   Power View : view1
*
*   User-Defined Activity : N.A.
*
*   Activity File: N.A.
*
*   Hierarchical Global Activity: N.A.
*
*   Global Activity: N.A.
*
*   Sequential Element Activity: N.A.
*
*   Primary Input Activity: 0.200000
*
*   Default icg ratio: N.A.
*
*   Global Comb ClockGate Ratio: N.A.
*
*   Power Units = 1mW
*
*   Time Units = 1e-09 secs
*
*   Temperature = 125
*
*   report_power -outfile 80_before_placement_reports/power.rpt -rail_analysis_format VS
*-----*

```

Cell	Internal Power	Switching Power	Total Power	Leakage Power	Cell Name
fare_reg[5]	0.01683	0.07431	0.09144	0.0003009	SDFFRHQX8
fare_reg[6]	0.01665	0.07263	0.08958	0.0003009	SDFFRHQX8
print_ticket_reg	0.01543	0.06441	0.08014	0.0003009	SDFFRHQX8
remaining_reg[0]	0.01455	0.05894	0.0738	0.0003009	SDFFRHQX8
fare_reg[4]	0.01436	0.05829	0.07296	0.0003009	SDFFRHQX8
remaining_reg[1]	0.01407	0.05599	0.07036	0.0003009	SDFFRHQX8

Total Power

Total Internal Power:	0.54920678	28.1672%
Total Switching Power:	1.38372751	70.9673%
Total Leakage Power:	0.01687614	0.8655%
Total Power:	1.94981043	

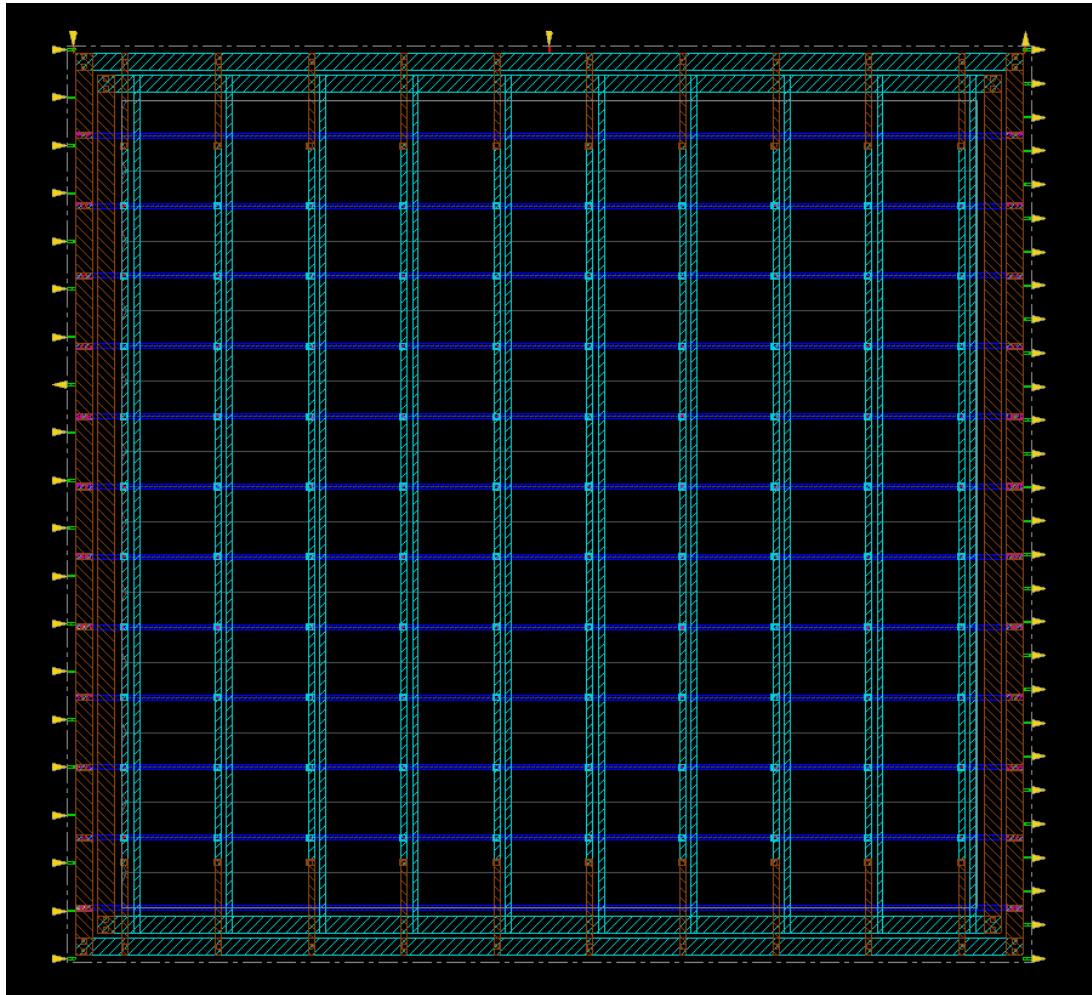
Ended Static Power Report Generation: (cpu=0:00:00, real=0:00:00,  
mem(process/total/peak)=941.61MB/2351.16MB/941.61MB)

					INVXL
g10000					
g9882	0.0001343	3.028e-05	0.0001767	1.22e-05	AOI21XL
g10113	0.0001242	3.989e-05	0.0001764	1.236e-05	NOR2XL
g10114	0.0001242	3.989e-05	0.0001764	1.236e-05	NOR2XL
g9903	6.771e-05	7.974e-05	0.0001675	2.004e-05	NOR2BX1
g10117	9.149e-05	6.617e-05	0.000167	9.289e-06	NAND2XL
g10188	7.36e-05	8.4e-05	0.0001669	9.289e-06	NAND2XL
g9900	0.0001161	3.417e-05	0.0001633	1.299e-05	OAI21X1
g10003	5.963e-05	9.031e-05	0.000163	1.301e-05	CLKINVX1
g10163	7.42e-05	6.33e-05	0.0001468	9.289e-06	NAND2XL
g10079	8.758e-05	3.688e-05	0.0001457	2.127e-05	OAI2BB1X1
g9860	8.137e-05	4.379e-05	0.0001444	1.92e-05	OAI2BB1XL
g10118	4.691e-05	2.291e-05	0.0001367	6.69e-05	OR4XL
g9885	0.0001016	1.884e-05	0.0001328	1.236e-05	NOR2XL
g9914	8.869e-05	2.979e-05	0.0001315	1.299e-05	OAI21X1
g9916	0.0001001	1.845e-05	0.0001309	1.236e-05	NOR2XL
g10037	4.935e-05	5.212e-05	0.0001214	1.995e-05	AOI211X1
g10125	3.975e-05	7.086e-05	0.0001199	9.289e-06	NAND2XL
g10123	7.165e-05	3.934e-05	0.0001198	8.757e-06	INVXL
g10072	6.277e-05	4.584e-05	0.0001179	9.289e-06	NAND2XL
g9852	5.833e-05	2.177e-05	0.0001143	3.419e-05	NAND3BX1
g9902	3.458e-05	6.285e-05	0.0001098	1.236e-05	NOR2XL
g9856	7.112e-05	2.248e-05	0.0001023	8.728e-06	OAI21XL
g10219	6.773e-05	2.583e-05	0.0001023	8.757e-06	INVXL
g9930	6.774e-05	2.185e-05	0.000102	1.236e-05	NOR2XL
g9927	6.852e-05	1.996e-05	0.0001015	1.299e-05	OAI21X1
g9891	7.513e-05	6.606e-06	0.0001002	1.851e-05	AOI32X1
g10132	6.564e-05	2.364e-05	9.857e-05	9.289e-06	NAND2XL
g10119	3.666e-05	3.177e-05	9.623e-05	2.78e-05	NAND4BXL
g10074	6.091e-05	2.154e-05	9.174e-05	9.289e-06	NAND2XL
g9905	5.794e-05	1.129e-05	8.158e-05	1.236e-05	NOR2XL
g10042	4.374e-05	7.852e-06	7.163e-05	2.004e-05	NOR2BX1
g9886	3.219e-05	2.867e-05	7.016e-05	9.289e-06	NAND2XL
g10080	1.64e-05	2.521e-05	6.941e-05	2.78e-05	NAND4BXL
g9850	3.876e-05	1.648e-05	6.453e-05	9.289e-06	NAND2XL
g9995	3.319e-05	5.435e-06	5.677e-05	1.815e-05	AOI21X1
g9823	3.223e-05	1.362e-05	5.514e-05	9.289e-06	NAND2XL
g9917	2.531e-05	1.868e-05	5.329e-05	9.289e-06	NAND2XL
g10036	2.313e-05	1.493e-05	5.107e-05	1.301e-05	CLKINVX1
g10008	2.48e-05	8.588e-06	4.637e-05	1.299e-05	OAI21X1
g10071	2.024e-05	1.388e-05	4.341e-05	9.289e-06	NAND2XL
g9904	1.928e-05	1.349e-05	4.206e-05	9.289e-06	NAND2XL
g9943	8.655e-06	5.544e-06	3.34e-05	1.92e-05	OAI2BB1XL
g9931	1.103e-05	7.562e-06	2.788e-05	9.289e-06	NAND2XL
g10078	1.069e-05	3.01e-06	2.363e-05	9.93e-06	NAND3XL
g9829	8.32e-06	5.248e-06	2.286e-05	9.289e-06	NAND2XL

---

Total ( 391 of 391 )	0.5492	1.384	1.95	0.01688
Total Capacitance	3.237e-11 F			
Power Densitv	*** No Die Area ***			

## LAYOUT



## AFTER PLACEMENT

### GBA SETUP SLACK

```
#####
# Generated by: Cadence Innovus 20.10-p004_1
# OS: Linux x86_64(Host ID edatools-server2.iiti.edu.in)
# Generated on: Fri Nov 15 12:15:56 2024
# Design: ticket_machine fsm
# Command: report_timing -max_path 100 -late > report_dir/after_placement_80/timing_setup_report_GBA.rpt
#####
Path 1: VIOLATED Setup Check with Pin return_amt_reg[6]/CK
Endpoint: return_amt_reg[6]/D (^) checked with leading edge of 'clk'
Beginpoint: total_amount_reg[6]/Q (^) triggered by leading edge of 'clk'
Path Groups: {clk}
Analysis View: view1
Other End Arrival Time      0.000
- Setup                      0.253
+ Phase Shift                4.220
- Uncertainty                 0.100
= Required Time              3.867
- Arrival Time               9.134
= Slack Time                 -5.267
  Clock Rise Edge           0.000
  + Clock Network Latency (Ideal) 0.000
  = Beginpoint Arrival Time   0.000
+-----+
| Instance | Arc | Cell | Delay | Arrival | Required |
|          |     |      |        | Time    | Time     |
+-----+
| total_amount_reg[6] | CK ^ |       |       | 0.000 | -5.267 |
| total_amount_reg[6] | CK ^ -> Q ^ | SDFFRHQX1 | 6.467 | 6.467 | 1.200 |
| g10194 | A ^ -> Y v | CLKINVX1 | 0.915 | 7.382 | 2.115 |
| g10167 | B v -> Y ^ | NAND2XL | 0.453 | 7.835 | 2.569 |
| g9911 | A0N ^ -> Y ^ | OAI2BB1X1 | 0.226 | 8.061 | 2.795 |
| g9903 | AN ^ -> Y ^ | NOR2BX1 | 0.462 | 8.523 | 3.257 |
| g9891 | A2 ^ -> Y v | AOI32X1 | 0.253 | 8.777 | 3.510 |
| g9861 | B0 v -> Y ^ | OAI2BB1XL | 0.357 | 9.134 | 3.867 |
| return_amt_reg[6] | D ^ | SDFFRHQX8 | 0.000 | 9.134 | 3.867 |
+-----+
```

The critical setup path identified by GBA starts from the begin point **total\_amount\_reg[6]/Q** and ends at **return\_amt\_reg[6]/D**.

In this **GBA analysis**, the Required Time (RT) is calculated as the End Arrival Time (default latency of clock, which is 0 but can be modified with constraints) - Setup + Phase Shift (defined clock time period in the constraint file) - Uncertainty. In this case, it is  $0 - 0.253 + 4.220 - 0.100 = 3.867$ .

Arrival time is determined through Forward Traversal of the Timing Graph and is found to be 9.134. Hence, the Slack is computed as (Required Time - Arrival Time), resulting in a value of -5.267(violation).

## PBA SETUP SLACK

```
#####
# Generated by: Cadence Innovus 20.10-p004.1
# OS: Linux x86_64(Host ID edatools-server2.iitd.edu.in)
# Generated on: Fri Nov 15 12:15:56 2024
# Design: ticket_machine_fsm
# Command: report_timing -retime path_slew_propagation -max_path 100 -late -format retime_slew > report_dir/after_placement_80/timing_setup_report_PBA.rpt
#####
Path 1: VIOLATED Setup Check with Pin return_amt_reg[6]/D
Endpoint: return_amt_reg[6]/D (^) checked with leading edge of 'clk'
Beginpoint: total_amount_reg[6]/Q (^) triggered by leading edge of 'clk'
Path Groups: {clk}
Analysis View: view1
Retime Analysis { Data Path-Slew }
Other End Arrival Time 0.000
- Setup 0.181
+ Phase Shift 4.220
- Uncertainty 0.100
= Required Time 3.939
- Arrival Time 8.867
= Slack Time -4.927
= Slack Time(original) -5.267
    Clock Rise Edge 0.000
    + Clock Network Latency (Ideal) 0.000
    = Beginpoint Arrival Time 0.000
    +-----
    | Retime |
    Slew
    +-----
    0.500
    0.182
    0.182
    2.003
    2.003
    0.596
    0.596
    0.091
    0.091
    0.485
    0.485
    0.264
    0.264
    0.133
    0.133
    +-----+
```

The critical setup path identified by GBA starts from the begin point **total\_amount\_reg[6]/Q** and ends at **return\_amt\_reg[6]/D**.

In this **PBA analysis**, the Required Time (RT) is calculated as the End Arrival Time (default latency of clock, which is 0 but can be modified with constraints) - Setup + Phase Shift (defined clock time period in the constraint file) - Uncertainty. In this case, it is  $0 - 0.181 + 4.220 - 0.100 = 3.939$ .

Arrival time is determined through Forward Traversal of the Timing Graph and is found to be 8.867. Hence, the Slack is computed as (Required Time - Arrival Time), resulting in a value of -4.927(violation).

**Setup slack in PBA analysis increases in comparison with GBA analysis.**

## GBA HOLD SLACK

```
#####
# Generated by: Cadence Innovus 20.10-p004_1
# OS: Linux x86_64(Host ID edatools-server2.iiitd.edu.in)
# Generated on: Fri Nov 15 12:15:56 2024
# Design: ticket_machine_fsm
# Command: report_timing -max_path 100 -early > report_dir/after_placement_80/timing_hold_report_GBA.rpt
#####
Path 1: MET Hold Check with Pin total_amount_reg[6]/CK
Endpoint: total_amount_reg[6]/SI (v) checked with leading edge of 'clk'
Beginpoint: total_amount_reg[0]/Q (v) triggered by leading edge of 'clk'
Path Groups: {clk}
Analysis View: view1
Other End Arrival Time      0.000
+ Hold                      0.098
+ Phase Shift                0.000
+ Uncertainty                0.100
= Required Time              0.198
  Arrival Time               0.505
  Slack Time                 0.307
    Clock Rise Edge           0.000
    + Clock Network Latency (Ideal) 0.000
    = Beginpoint Arrival Time   0.000
+-----+
| Instance | Arc | Cell | Delay | Arrival | Required |
|          |     |      |        | Time    | Time      |
+-----+
| total_amount_reg[0] | CK ^ |       |        | 0.000 | -0.307 |
| total_amount_reg[0] | CK ^ -> Q v | SDFFRHQX1 | 0.505 | 0.505 | 0.198 |
| total_amount_reg[6] | SI v | SDFFRHQX1 | 0.000 | 0.505 | 0.198 |
+-----+
```

The Worst Hold Path of GBA is mentioned above with begin point of **total\_amount\_reg[0]/Q** and endpoint of **total\_amount\_reg[6]/SI**. In the above GBA the Required Time = End Arrival Time(latency of clock which is 0 by default but can be changed using constraint) + hold + Phase Shift(clock time period defined in constraint file)+Uncertainty = 0 + 0.098+0.1 = 0.198 ns Arrival time is computed using Forward Traversal of Timing Graph.

Arrival time = 0.505

Slack = Arrival Time - Required Time = 0.307

## PBA HOLD SLACK

```
#####
# Generated by: Cadence Innovus 20.10-p004.1
# OS: Linux x86_64 (Host ID edatools-server2.iitd.edu.in)
# Generated on: Fri Nov 15 12:15:57 2024
# Design: ticket_machine fsm
# Command: report_timing -retime path slew_propagation -max_path 100 -early -format retime_slew > report_dir/after_placement_80/timing_hold_report_PBA.rpt
#####
Path 1: MET Hold Check with Pin total_amount_reg[6]/CK
Endpoint: total_amount_reg[6]/SI (v) checked with leading edge of 'clk'
Beginpoint: total_amount_reg[0]/Q (v) triggered by leading edge of 'clk'
Path Groups: {clk}
Analysis View: view1
Retime Analysis { Data Path-Slew }
Other End Arrival Time 0.000
+ Hold 0.098
+ Phase Shift 0.000
+ Uncertainty 0.100
= Required Time 0.198
Arrival Time 0.505
Slack Time 0.307
= Slack Time(original) 0.307
    Clock Rise Edge 0.000
    + Clock Network Latency (Ideal) 0.000
    = Beginpoint Arrival Time 0.000
    +-----+
    | Retime |
    | Slew   |
    +-----+
    | 0.500 |
    | 0.140 |
    | 0.140 |
    +-----+
```

The Worst Hold Path of GBA is mentioned above with begin point of **total\_amount\_reg[0]/Q** and endpoint of **total\_amount\_reg[6]/SI**. In the above GBA the Required Time = End Arrival Time(latency of clock which is 0 by default but can be changed using constraint) + hold + Phase Shift(clock time period defined in constraint file)+Uncertainty = 0 + 0.098+0.1 = 0.198 ns Arrival time is computed using Forward Traversal of Timing Graph.

Arrival time = 0.505

Slack = Arrival Time - Required Time = 0.307

**Hold slack is same for both the analysis.**

## AREA

Host Name	Module Name	Inst Count	Total Area	Buffer	Inverter	Combinational	Flop	Latch	Clock Gate	Macro
Physical 0.000	ticket_machine_fsm	391	3043.495	0.000	84.016	1731.038	1228.449	0.000	0.000	0.000

### Area Report:

Area of Buffers: 0.000 um<sup>2</sup>

Area of Inverters: 84.016 um<sup>2</sup>

Area of flip flops: 1228.449 um<sup>2</sup>

Area of Combinational cells: 1731.038 um<sup>2</sup>

Total Area: 3043.495 um<sup>2</sup>

## POWER

### Power Report:

**Internal power:** It is the power consumed within the confines of a cell, arises from the charging or discharging of internal capacitances during switching. The cumulative internal power dissipation is measured at 0.5717mW which is 27.4673 % of total consumed power.

**Switching power:** It refers to the energy consumed by a driving cell when it charges and discharges the load capacitance connected to its output. In this case, the overall switching power amounts to 1.4928mW which is 71.7220 % of total power.

**Leakage power:** This leakage current is the current that flows from VDD to GND when there is no switching. The total leakage power is 0.0168mW which is 0.8108 % of total power.

**Total power:** Total power is the sum of the all above powers which is 2.0815mW.

```

*-----*
*   Innovus 20.10-p004_1 (64bit) 05/07/2020 20:02 (Linux 2.6.32-431.11.2.el6.x86_64)
*
*   Date & Time:    2024-Nov-15 12:15:57 (2024-Nov-15 06:45:57 GMT)
*
*-----*
*
*   Design: ticket_machine_fsm
*
*   Liberty Libraries used:
*       view1: ../lib/90/slow.lib
*
*   Power Domain used:
*       Rail:      VDD      Voltage:      0.9
*
*   Power View : view1
*
*   User-Defined Activity : N.A.
*
*   Activity File: N.A.
*
*   Hierarchical Global Activity: N.A.
*
*   Global Activity: N.A.
*
*   Sequential Element Activity: N.A.
*
*   Primary Input Activity: 0.200000
*
*   Default icg ratio: N.A.
*
*   Global Comb ClockGate Ratio: N.A.
*
*   Power Units = 1mW
*
*   Time Units = 1e-09 secs
*
*   Temperature = 125
*
*   report_power -outfile 80_after_placement_reports/power.rpt -rail_analysis_format VS
*-----*

```

Cell	Internal Power	Switching Power	Total Power	Leakage Power	Cell Name
fare_reg[5]	0.01656	0.07289	0.08975	0.0003009	SDFFRHQX8
fare_reg[6]	0.01631	0.07087	0.08748	0.0003009	SDFFRHQX8
return_amt_reg[5]	0.0154	0.06423	0.07994	0.0003009	SDFFRHQX8
return_amt_reg[4]	0.0148	0.06071	0.07582	0.0003009	SDFFRHQX8
return_amt_reg[6]	0.01524	0.05725	0.07279	0.0003009	SDFFRHQX8
fare_ren[4]	0.01413	0.05678	0.07121	0.0003009	SDFFRHQX8

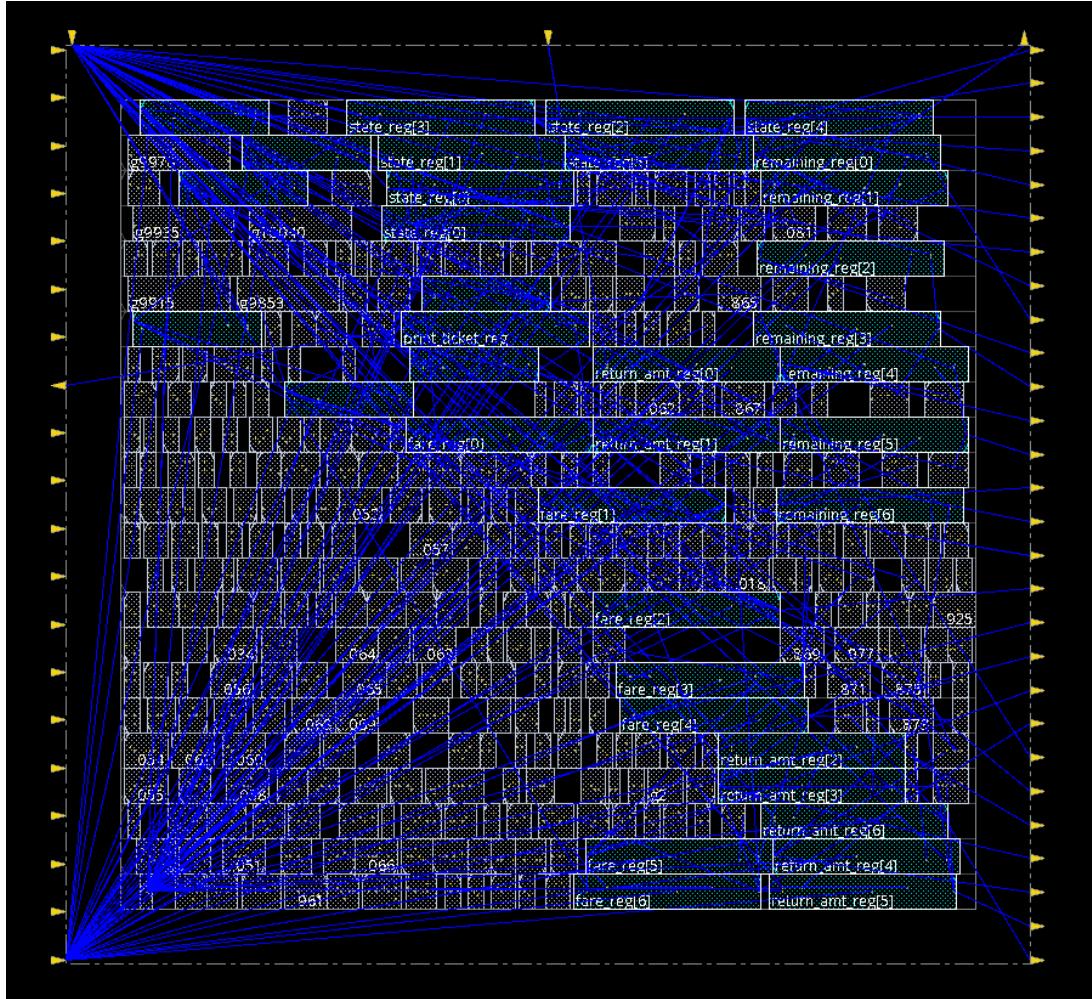
**Total Power**

Total Internal Power:	0.57173149	27.4673%
Total Switching Power:	1.49289395	71.7220%
Total Leakage Power:	0.01687614	0.8108%
Total Power:	2.08150159	

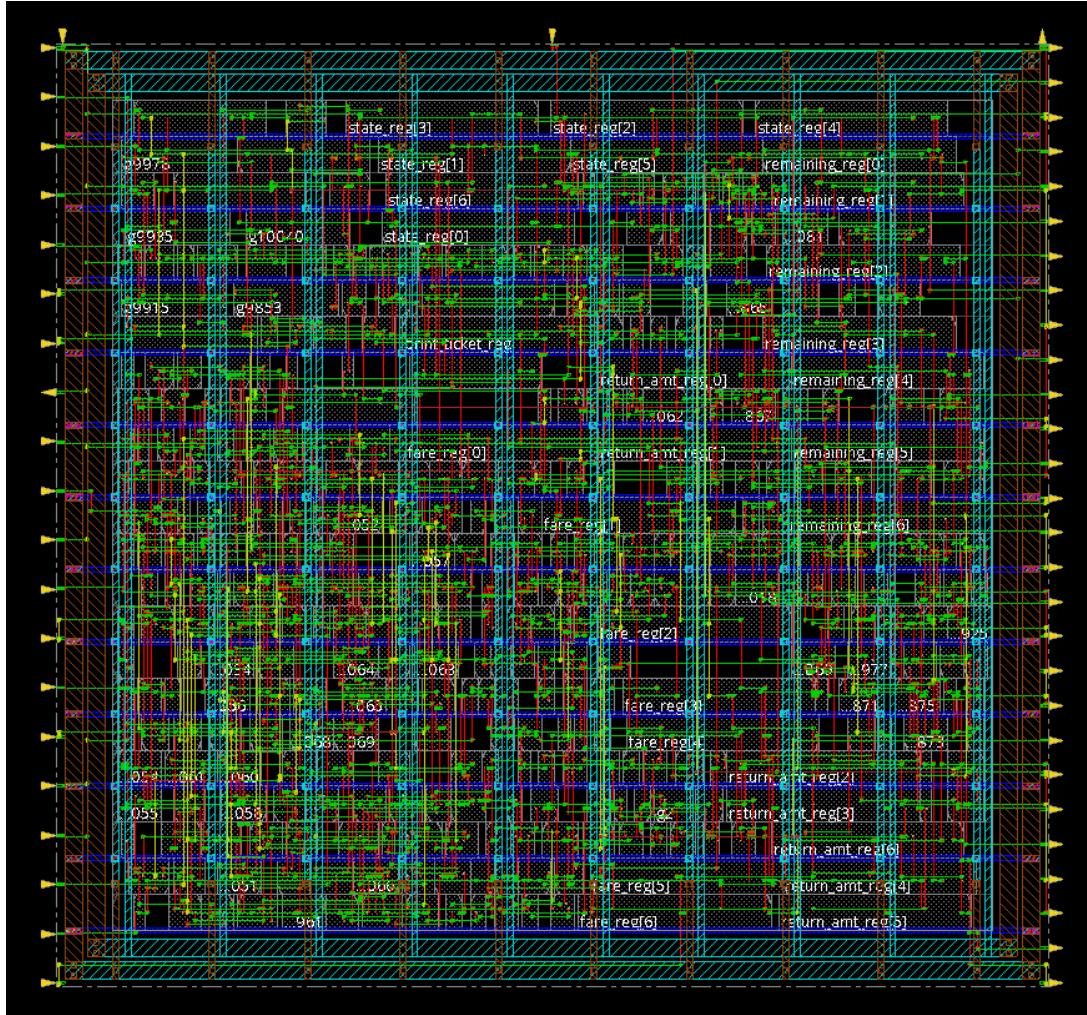
Ended Static Power Report Generation: (cpu=0:00:00, real=0:00:00,  
mem(process/total/peak)=996.27MB/2395.79MB/996.27MB)

g10005	0.0001523	4.702e-05	0.0002203	2.093e-05	NOR4X1
g10067	0.0001116	8.158e-05	0.0002019	8.757e-06	INVXL
g10114	0.0001294	5.652e-05	0.0001983	1.236e-05	NOR2XL
g10053	0.0001072	8.122e-05	0.0001972	8.757e-06	INVXL
g10113	0.0001299	4.965e-05	0.0001919	1.236e-05	NOR2XL
g10188	7.374e-05	0.0001083	0.0001913	9.289e-06	NAND2XL
g10117	9.376e-05	8.486e-05	0.0001879	9.289e-06	NAND2XL
g10215	0.0001111	6.186e-05	0.0001859	1.301e-05	CLKINVX1
g9902	4.512e-05	0.0001268	0.0001843	1.236e-05	NOR2XL
g10037	6.854e-05	9.479e-05	0.0001833	1.995e-05	AOI211X1
g10125	4.071e-05	0.0001156	0.0001656	9.289e-06	NAND2XL
g10163	7.43e-05	8.008e-05	0.0001637	9.289e-06	NAND2XL
g10079	9.005e-05	4.991e-05	0.0001612	2.127e-05	OAI2BB1X1
g10004	5.253e-05	9.411e-05	0.000159	1.236e-05	NOR2XL
g9913	9.414e-05	4.652e-05	0.0001529	1.22e-05	AOI21XL
g9901	9.786e-05	3.827e-05	0.0001483	1.22e-05	AOI21XL
g10003	4.529e-05	8.778e-05	0.0001461	1.301e-05	CLKINVX1
g10123	9.226e-05	4.317e-05	0.0001442	8.757e-06	INVXL
g10072	6.685e-05	6.608e-05	0.0001422	9.289e-06	NAND2XL
g9891	0.000103	1.99e-05	0.0001414	1.851e-05	OAI32X1
g9882	9.518e-05	2.615e-05	0.0001335	1.22e-05	AOI21XL
g10119	3.974e-05	6.358e-05	0.0001311	2.78e-05	NAND4BXL
g10042	8.521e-05	2.47e-05	0.0001299	2.004e-05	NOR2BX1
g10080	3.315e-05	6.749e-05	0.0001284	2.78e-05	NAND4BXL
g9900	8.349e-05	2.575e-05	0.0001222	1.299e-05	OAI21X1
g9860	5.742e-05	4.053e-05	0.0001172	1.92e-05	OAI2BB1XL
g10132	7.067e-05	2.92e-05	0.0001092	9.289e-06	NAND2XL
g9885	7.33e-05	2.076e-05	0.0001064	1.236e-05	NOR2XL
g9916	7.271e-05	1.89e-05	0.000104	1.236e-05	NOR2XL
g9914	6.195e-05	2.858e-05	0.0001035	1.299e-05	OAI21X1
g9852	4.03e-05	1.631e-05	9.081e-05	3.419e-05	NAND3BX1
g9856	4.968e-05	2.115e-05	7.956e-05	8.728e-06	OAI21XL
g9930	4.74e-05	1.865e-05	7.841e-05	1.236e-05	NOR2XL
g9927	4.921e-05	1.562e-05	7.781e-05	1.299e-05	OAI21X1
g10078	4.443e-05	2.322e-05	7.758e-05	9.93e-06	NAND3XL
g10036	3.567e-05	2.526e-05	7.395e-05	1.301e-05	CLKINVX1
g9943	2.949e-05	2.23e-05	7.099e-05	1.92e-05	OAI2BB1XL
g9905	4.041e-05	9.8e-06	6.257e-05	1.236e-05	NOR2XL
g10071	3.042e-05	2.036e-05	6.007e-05	9.289e-06	NAND2XL
g9886	2.283e-05	2.616e-05	5.828e-05	9.289e-06	NAND2XL
g9850	2.697e-05	1.624e-05	5.25e-05	9.289e-06	NAND2XL
g9823	2.401e-05	1.321e-05	4.651e-05	9.289e-06	NAND2XL
g9917	1.806e-05	1.536e-05	4.271e-05	9.289e-06	NAND2XL
g9904	1.427e-05	1.069e-05	3.425e-05	9.289e-06	NAND2XL
g9829	1.268e-05	9.588e-06	3.156e-05	9.289e-06	NAND2XL
g9931	8.152e-06	6.488e-06	2.393e-05	9.289e-06	NAND2XL
<hr/>					
Total ( 391 of 391 )		0.5717	1.493	2.082	0.01688
Total Capacitance		3.346e-11 F			
Power Density		*** No Die Area ***			

## FLY LINES



## LAYOUT



## AFTER CTS NON-OPTIMIZED

### GBA SETUP SLACK

# Generated by: Cadence Innovus 20.10-p004_1						
# OS: Linux x86_64 (Host ID edatools-server2.iitd.edu.in)						
# Generated on: Fri Nov 15 12:34:01 2024						
# Design: ticket_machine fsm						
# Command: report timing -max_path 100 -late > report_dir/before_optimisation_80/timing_setup_report_GBA.rpt						
Path 1: MET Setup Check with Pin fare_reg[5]/CK						
Endpoint: fare_reg[5]/D (^) checked with leading edge of 'clk'						
Beginpoint: dest_station[2] (^) triggered by leading edge of 'clk'						
Path Groups: {clk}						
Analysis View: view1						
Other End Arrival Time -0.000						
- Setup 0.268						
+ Phase Shift 4.220						
- Uncertainty 0.100						
= Required Time 3.851						
- Arrival Time 3.849						
= Slack Time 0.003						
Clock Rise Edge 0.000						
+ Input Delay 1.500						
= Beginpoint Arrival Time 1.500						
+						
Instance	Arc	Cell	Delay	Arrival Time	Required Time	
				Time	Time	
g10239	A ^ -> Y v	CLKINVX1	0.059	1.559	1.561	
g10189	B v -> Y ^	NOR2X1	0.120	1.679	1.682	
g10137	B ^ -> Y v	NAND2XL	0.537	2.216	2.219	
g10091	A1 v -> Y ^	OAI22X1	0.222	2.438	2.441	
g9987	C ^ -> Y ^	OR4XL	0.158	2.597	2.600	
g9938	A ^ -> Y v	NAND2XL	0.248	2.845	2.847	
g9922	A0 v -> Y ^	OAI21X1	0.239	3.084	3.087	
g9909	A1 ^ -> Y v	OAI21X1	0.190	3.273	3.276	
g9897	A1 v -> Y ^	OAI21X2	0.174	3.447	3.450	
g9857	A1 ^ -> Y v	OAI21X1	0.199	3.557	3.559	
g9849	B v -> Y ^	NOR2XL	0.097	3.654	3.657	
g9833	B0 ^ -> Y v	OAI21XL	0.076	3.730	3.733	
g9816	A1 v -> Y ^	OAI21X1	0.119	3.849	3.851	
fare_reg[5]	D ^	SDFFRHQX8	0.000	3.849	3.851	

The critical setup path identified by GBA starts from the begin point **dest\_station[2]** and ends at **fare\_reg[5]/D**.

In this **GBA analysis**, the Required Time (RT) is calculated as the End Arrival Time (default latency of clock, which is 0 but can be modified with constraints) - Setup + Phase Shift (defined clock time period in the constraint file) - Uncertainty. In this case, it is  $0 - 0.268 + 4.220 - 0.100 = 3.851$ .

Arrival time is determined through Forward Traversal of the Timing Graph and is found to be 3.849. Hence, the Slack is computed as (Required Time - Arrival Time), resulting in a value of 0.003 ( no violation).

## PBA SETUP SLACK

```
#####
# Generated by: Cadence Innovus 20.10-p004_1
# OS: Linux x86_64(Host ID edatools-server2.liitd.edu.in)
# Generated on: Fri Nov 15 12:34:01 2024
# Design: ticket_machine_fsm
# Command: report_timing -retime path slew_propagation -max_path 100 -late -format retime_slew > report_dir/before_optimisation_80/timing_setup_report_PBA.rpt
#####
Path 1: MET Setup Check with pin fare_reg[5]/CK
Endpoint: fare_reg[5]/D (*) checked with leading edge of 'clk'
Beginpoint: dest_station[2] (*) triggered by leading edge of 'clk'
Path Groups: {clk}
Analysis View: view1
Retime Analysis { Data Path-Slew }
Other End Arrival Time -0.000
- Setup 0.236
+ Phase Shift 4.220
- Uncertainty 0.100
= Required Time 3.884
- Arrival Time 3.806
= Slack Time 0.078
= Slack Time(original) 0.003
Clock Rise Edge 0.000
+ Input Delay 1.500
= Beginpoint Arrival Time 1.500
+-----+
| Retime |
| Slew |
+-----+
| 0.003 |
| 0.003 |
| 0.073 |
| 0.073 |
| 0.134 |
| 0.134 |
| 0.735 |
| 0.735 |
| 0.231 |
| 0.231 |
| 0.089 |
| 0.089 |
| 0.324 |
| 0.324 |
| 0.226 |
| 0.226 |
| 0.194 |
| 0.194 |
| 0.148 |
| 0.148 |
| 0.094 |
| 0.094 |
| 0.092 |
| 0.092 |
```

The critical setup path identified by GBA starts from the begin point **dest\_station[2]** and ends at **fare\_reg[5]/D**.

In this **GBA analysis**, the Required Time (RT) is calculated as the End Arrival Time (default latency of clock, which is 0 but can be modified with constraints) - Setup + Phase Shift (defined clock time period in the constraint file) - Uncertainty. In this case, it is  $0 - 0.236 + 4.220 - 0.100 = 3.884$ .

Arrival time is determined through Forward Traversal of the Timing Graph and is found to be 3.806. Hence, the Slack is computed as (Required Time - Arrival Time), resulting in a value of 0.078 (no violation).

**Setup slack in PBA increases in comparison with Setup slack in GBA .**

## GBA HOLD SLACK

```
#####
# Generated by: Cadence Innovus 20.10-p004.1
# OS: Linux x86_64 (Host ID edatools-server2.iiitd.edu.in)
# Generated on: Fri Nov 15 12:34:01 2024
# Design: ticket_machine fsm
# Command: report timing -max_path 100 -early > report_dir/before_optimisation_80/timing_hold_report_GBA.rpt
#####
Path 1: MET Hold Check with Pin state_reg[5]/CK
Endpoint: state_reg[5]/SI (v) checked with leading edge of 'clk'
Beginpoint: state_reg[2]/Q (v) triggered by leading edge of 'clk'
Path Groups: {clk}
Analysis View: view1
Other End Arrival Time 0.000
+ Hold 0.047
+ Phase Shift 0.000
+ Uncertainty 0.100
= Required Time 0.147
Arrival Time 0.374
Slack Time 0.227
Clock Rise Edge 0.000
+ Clock Network Latency (Prop) 0.000
= Beginpoint Arrival Time 0.000
+-----+
| Instance | Arc | Cell | Delay | Arrival | Required |
|          |     |      |       | Time   |     |
+-----+
| state_reg[2] | CK ^ |          | 0.000 | -0.227 | |
| state_reg[2] | CK ^ -> Q v | SDFFRHQX1 | 0.374 | 0.374 | 0.147 |
| state_reg[5] | SI v | SDFFRHQX1 | 0.000 | 0.374 | 0.147 |
+-----+
```

The Worst Hold Path of GBA is mentioned above with begin point of **state\_reg[2]/Q** and endpoint of **state\_reg[5]/SI**. In the above GBA the Required Time = End Arrival Time(latency of clock which is 0 by default but can be changed using constraint) + hold + Phase Shift(clock time period defined in constraint file)+Uncertainty = 0 + 0.047+0.1 = 0.147 ns Arrival time is computed using Forward Traversal of Timing Graph.

Arrival time = 0.374

Slack = Arrival Time - Required Time = 0.227

## PBA HOLD SLACK

```
#####
# Generated by: Cadence Innovus 20.10-p094_1
# OS: Linux x86_64 (Host ID edatools-server2.iitiid.edu.in)
# Generated on: Fri Nov 15 12:34:01 2024
# Design: ticket_machine fsm
# Command: report_timing -retiming_path slew propagation -max_path 100 -early -format retiming_slew > report_dir/before_optimisation_80/timing_hold_report_PBA.rpt
#####
Path 1: MET Hold Check with Pin state reg[5]/CK
Endpoint: state_reg[5]/SI (v) checked with leading edge of 'clk'
Beginpoint: state_reg[2]/Q (v) triggered by leading edge of 'clk'
Path Groups: {clk}
Analysis View: view1
Retiming Analysis { Data Path-Slew }
Other End Arrival Time 0.000
+ Hold 0.047
+ Phase Shift 0.000
+ Uncertainty 0.100
= Required Time 0.147
Arrival Time 0.374
Slack Time 0.227
= Slack Time(original) 0.227
  Clock Rise Edge 0.000
  + Clock Network Latency (Prop) 0.000
  = Beginpoint Arrival Time 0.000
  +-----+
  | Retiming |
  | Slew |
  |-----|
  | 0.004 |
  | 0.094 |
  | 0.094 |
  +-----+
```

The Worst Hold Path of GBA is mentioned above with begin point of **state\_reg[2]/Q** and endpoint of **state\_reg[5]/SI**. In the above GBA the Required Time = End Arrival Time(latency of clock which is 0 by default but can be changed using constraint) + hold + Phase Shift(clock time period defined in constraint file)+Uncertainty =  $0 + 0.047 + 0.1 = 0.147$  ns Arrival time is computed using Forward Traversal of Timing Graph.

Arrival time = 0.374

Slack = Arrival Time - Required Time = 0.227

**Hold slack is same for both the analysis.**

## AREA

Inst Name	Module Name	Inst Count	Total Area	Buffer	Inverter	Combinational	Flop	Latch	Clock Gate	Macro
Physical 0.000	ticket_machine_fsm	439	3291.758	158.949	369.367	1757.522	1005.928	0.000	0.000	0.000

### Area Report:

Area of Buffers: 158.949 um<sup>2</sup>

Area of Inverters: 369.367 um<sup>2</sup>

Area of flip flops: 1005.920um<sup>2</sup>

Area of Combinational cells: 1757.522 um<sup>2</sup>

Total Area: 3291.758 um<sup>2</sup>

## POWER

### Power Report:

**Internal power:** It is the power consumed within the confines of a cell, arises from the charging or discharging of internal capacitances during switching. The cumulative internal power dissipation is measured at 0.3608mW which is 34.6179 % of total consumed power.

**Switching power:** It refers to the energy consumed by a driving cell when it charges and discharges the load capacitance connected to its output. In this case, the overall switching power amounts to 0.6621mW which is 63.5242 % of total power.

**Leakage power:** This leakage current is the current that flows from VDD to GND when there is no switching. The total leakage power is 0.01936mW which is 1.8579 % of total power.

**Total power:** Total power is the sum of the all above powers which is 1.0423mW.

#### Total Power

Total Internal Power:	0.36083044	34.6179%
Total Switching Power:	0.66212686	63.5242%
Total Leakage Power:	0.01936497	1.8579%
Total Power:	1.04232226	

Ended Static Power Report Generation: (cpu=0:00:00, real=0:00:00,  
mem(process/total/peak)=1106.46MB/2607.09MB/1160.39MB)

```

*-----*
*      Innovus 20.10-p004_1 (64bit) 05/07/2020 20:02 (Linux 2.6.32-431.11.2.el6.x86_64)
*
*
*      Date & Time:    2024-Nov-15 12:34:02 (2024-Nov-15 07:04:02 GMT)
*
*-----*
*
*      Design: ticket_machine_fsm
*
*      Liberty Libraries used:
*          view1: ../../lib/90/slow.lib
*
*      Power Domain used:
*          Rail:      VDD      Voltage:      0.9
*
*      Power View : view1
*
*      User-Defined Activity : N.A.
*
*      Activity File: N.A.
*
*      Hierarchical Global Activity: N.A.
*
*      Global Activity: N.A.
*
*      Sequential Element Activity: 0.200000
*
*      Primary Input Activity: 0.200000
*
*      Default icg ratio: N.A.
*
*      Global Comb ClockGate Ratio: N.A.
*
*      Power Units = 1mW
*
*      Time Units = 1e-09 secs
*
*      Temperature = 125
*
*      report_power -outfile 80_before_optimisation_reports/power.rpt -rail_analysis_format VS
*

```

Cell	Internal Power	Switching Power	Total Power	Leakage Power	Cell Name
FE_OFC2_fare_6	0.001989	0.01964	0.02185	0.0002199	CLKBUFX12
FE_OFC8_fare_0	0.001993	0.01957	0.02178	0.0002199	CLKBUFX12
FE_OFC11_state_4	0.001989	0.01956	0.02177	0.0002199	CLKBUFX12
FE_OFC12_return_amt_1	0.001994	0.01954	0.02176	0.0002199	CLKBUFX12
FE_OFC17_state_1	0.001993	0.01952	0.02173	0.0002199	CLKBUFX12
FE_OFC18_fare_2	0.001993	0.01952	0.02173	0.0002199	CLKBUFX12

#### Total Power

Total Internal Power:	0.36083044	34.6179%
Total Switching Power:	0.66212686	63.5242%
Total Leakage Power:	0.01936497	1.8579%
Total Power:	1.04232226	

Ended Static Power Report Generation: (cpu=0:00:00, real=0:00:00,  
mem(process/total/peak)=1106.46MB/2607.09MB/1160.39MB)

g10171	2.498e-05	2.014e-05	7.113e-05	2.001e-05	AND4X1
g10033	1.819e-05	2.314e-05	6.913e-05	2.78e-05	NAND4BXL
g10080	1.101e-05	2.684e-05	6.565e-05	2.78e-05	NAND4BXL
g10119	1.254e-05	2.278e-05	6.312e-05	2.78e-05	NAND4BXL
g9995	3.357e-05	9.255e-06	6.097e-05	1.815e-05	AOI21X1
g9889	3.058e-05	1.709e-05	6.069e-05	1.301e-05	CLKINVX1
g10042	3.114e-05	9.46e-06	6.064e-05	2.004e-05	NOR2BX1
g9993	1.78e-05	2.627e-05	5.708e-05	1.301e-05	CLKINVX1
g9902	1.075e-05	3.206e-05	5.517e-05	1.236e-05	NOR2XL
g9926	2.942e-05	6.826e-06	5.439e-05	1.815e-05	AOI21X1
g10022	1.467e-05	2.577e-05	5.346e-05	1.301e-05	CLKINVX1
g10001	1.17e-05	2.752e-05	5.224e-05	1.301e-05	CLKINVX1
g10002	6.357e-06	3.434e-05	4.998e-05	9.289e-06	NAND2XL
g10008	2.625e-05	1.054e-05	4.978e-05	1.299e-05	OAI21X1
g10073	2.261e-05	1.469e-05	4.966e-05	1.236e-05	NOR2XL
g9891	2.323e-05	7.395e-06	4.913e-05	1.851e-05	AOI32X1
g10037	1.215e-05	1.651e-05	4.861e-05	1.995e-05	AOI211X1
g10041	2.192e-05	5.806e-06	4.777e-05	2.004e-05	NOR2BX1
g9852	6.762e-06	3.161e-06	4.411e-05	3.419e-05	NAND3BX1
g9943	1.198e-05	1.158e-05	4.276e-05	1.92e-05	OAI2BB1XL
g10004	8.4e-06	1.67e-05	3.746e-05	1.236e-05	NOR2XL
g9860	9.441e-06	7.759e-06	3.64e-05	1.92e-05	OAI2BB1XL
g9901	1.609e-05	8.01e-06	3.63e-05	1.22e-05	AOI21XL
g10003	7.363e-06	1.563e-05	3.601e-05	1.301e-05	CLKINVX1
g9913	1.536e-05	7.672e-06	3.523e-05	1.22e-05	AOI21XL
g10005	9.679e-06	3.12e-06	3.372e-05	2.093e-05	NOR4X1
g9882	1.547e-05	5.007e-06	3.268e-05	1.22e-05	AOI21XL
g9900	1.358e-05	4.498e-06	3.107e-05	1.299e-05	OAI21X1
g9914	1.011e-05	4.87e-06	2.797e-05	1.299e-05	OAI21X1
g9916	1.172e-05	3.621e-06	2.77e-05	1.236e-05	NOR2XL
g9885	1.188e-05	3.177e-06	2.742e-05	1.236e-05	NOR2XL
g10078	9.105e-06	7.077e-06	2.611e-05	9.93e-06	NAND3XL
g9886	5.971e-06	4.33e-06	2.433e-05	1.403e-05	NAND2X1
g9927	8.074e-06	2.374e-06	2.343e-05	1.299e-05	OAI21X1
g9930	7.709e-06	3.033e-06	2.31e-05	1.236e-05	NOR2XL
g10036	5.33e-06	4.478e-06	2.282e-05	1.301e-05	CLKINVX1
g9905	6.569e-06	1.629e-06	2.056e-05	1.236e-05	NOR2XL
g9856	8.073e-06	2.898e-06	1.97e-05	8.728e-06	OAI21XL
g10072	4.476e-06	5.036e-06	1.88e-05	9.289e-06	NAND2XL
g10071	4.675e-06	3.597e-06	1.756e-05	9.289e-06	NAND2XL
g9850	4.367e-06	3.039e-06	1.67e-05	9.289e-06	NAND2XL
g9823	3.93e-06	2.218e-06	1.544e-05	9.289e-06	NAND2XL
g9917	2.932e-06	2.869e-06	1.509e-05	9.289e-06	NAND2XL
g9904	2.312e-06	2.065e-06	1.367e-05	9.289e-06	NAND2XL
g9829	1.797e-06	1.5e-06	1.259e-05	9.289e-06	NAND2XL
g9931	1.344e-06	1.028e-06	1.166e-05	9.289e-06	NAND2XL

---

Total ( 439 of 439 )	0.3608	0.6621	1.042	0.01936
Total Capacitance	3.423e-11 F			
Power Density	*** No Die Area ***			

## AFTER CTS OPTIMIZED

### GBA SETUP SLACK

```
#####
# Generated by: Cadence Innovus 20.10-p004_1
# OS: Linux x86_64 (Host ID edatools-server2.iiitd.edu.in)
# Generated on: Fri Nov 15 12:58:45 2024
# Design: ticket_machine_fsm
# Command: report_timing -max_path 100 -late > report_dir/after_optimisation_80/timing_setup_report_GBA.rpt
#####
Path 1: VIOLATED Setup Check with Pin fare_reg[6]/CK
Endpoint: fare_reg[6]/D (^) checked with leading edge of 'clk'
Beginpoint: dest_station[1] (^) triggered by leading edge of 'clk'
Path Groups: {clk}
Analysis View: view1
Other End Arrival Time      -0.000
- Setup                      0.259
+ Phase Shift                4.220
- Uncertainty                 0.100
= Required Time              3.861
- Arrival Time               3.889
= Slack Time                -0.028
Clock Rise Edge             0.000
+ Input Delay                1.500
= Beginpoint Arrival Time   1.500
+-----+
| Instance | Arc          | Cell       | Delay | Arrival | Required |
|          |              |            |        | Time    | Time     |
+-----+
|          | dest_station[1] ^ | CLKINVX1  | 0.094 | 1.594 | 1.472 |
| g10197  | A ^ -> Y v    | NAND3X1  | 0.183 | 1.777 | 1.749 |
| g10150  | C v -> Y ^    | OAI222X1 | 0.208 | 1.985 | 1.957 |
| g10052  | B1 ^ -> Y v    | OAI2BB1X1 | 0.118 | 2.103 | 2.075 |
| g10024  | B0 v -> Y ^    | OAI221X1  | 0.145 | 2.248 | 2.220 |
| g10015  | C0 ^ -> Y v    | OR4XL    | 0.262 | 2.510 | 2.483 |
| g9987   | D v -> Y v    | NOR2XL   | 0.292 | 2.802 | 2.774 |
| g9939   | A v -> Y ^    | OAI21X1  | 0.238 | 3.041 | 3.013 |
| g9923   | A1 ^ -> Y v    | OAI21X2  | 0.154 | 3.194 | 3.167 |
| g9910   | A1 v -> Y ^    | OAI21X2  | 0.112 | 3.306 | 3.279 |
| g9896   | A1 ^ -> Y v    | OAI21X1  | 0.169 | 3.475 | 3.448 |
| g9858   | A1 v -> Y ^    | OAI21X1  | 0.098 | 3.573 | 3.546 |
| g9831   | A1 ^ -> Y v    | NOR2XL   | 0.103 | 3.676 | 3.648 |
| g9824   | B v -> Y ^    | OAI21X1  | 0.069 | 3.745 | 3.718 |
| g9822   | B0 ^ -> Y v    | OAI21X1  | 0.144 | 3.889 | 3.861 |
| fare_reg[6] | D ^ | SDFFRHQX8 | 0.000 | 3.889 | 3.861 |
+-----+
```

The critical setup path identified by GBA starts from the begin point **dest\_station[1]** and ends at **fare\_reg[6]/D**.

In this **GBA analysis**, the Required Time (RT) is calculated as the End Arrival Time (default latency of clock, which is 0 but can be modified with constraints) - Setup + Phase Shift (defined clock time period in the constraint file) - Uncertainty. In this case, it is  $0 - 0.259 + 4.220 - 0.100 = 3.861$ .

Arrival time is determined through Forward Traversal of the Timing Graph and is found to be 3.889. Hence, the Slack is computed as (Required Time - Arrival Time), resulting in a value of -0.028 (violation).

## PBA SETUP SLACK

```
# Generated by: Cadence Innovus 20.10-p004_1
# OS: Linux x86_64 (Host ID edatools-server2.iitiid.edu.in)
# Generated on: Fri Nov 15 12:58:46 2024
# Design: ticket_machine fsm
# Command: report_timing -retime path_slew_propagation -max_path 100 -late -format retime_slew > report_dir/after_optimisation_80/timing_setup_report_PBA.rpt
#####
Path 1: MET Setup Check with Pin fare_reg[6]/CK
Endpoint: fare_reg[6]/D ("") checked with leading edge of 'clk'
Beginpoint: dest_station[1] ("") triggered by leading edge of 'clk'
Path Groups: {clk}
Analysis View: view1
Retime Analysis { Data Path-Slew }
Other Env Arrival Time -0.000
- Setup 0.252
+ Phase Shift 4.220
- Uncertainty 0.100
= Required Time 3.867
- Arrival Time 3.813
= Slack Time 0.055
= Slack Time(original) -0.028
Clock Rise Edge 0.000
+ Input Delay 1.500
= Beginpoint Arrival Time 1.500
+-----+
| Retime |
| Slew |
+-----+
0.003
0.003
0.125
0.125
0.197
0.197
0.197
0.197
0.197
0.197
0.098
0.098
0.158
0.158
0.194
0.194
0.360
0.360
0.138
0.245
0.130
0.130
0.100
0.100
0.149
0.149
```

The critical setup path identified by GBA starts from the begin point **dest\_station[1]** and ends at **fare\_reg[6]/D**.

In this **GBA analysis**, the Required Time (RT) is calculated as the End Arrival Time (default latency of clock, which is 0 but can be modified with constraints) - Setup + Phase Shift (defined clock time period in the constraint file) - Uncertainty. In this case, it is  $0 - 0.252 + 4.220 - 0.100 = 3.867$ .

Arrival time is determined through Forward Traversal of the Timing Graph and is found to be 3.813. Hence, the Slack is computed as (Required Time - Arrival Time), resulting in a value of 0.055 (no violation).

**Setup slack in PBA increases in comparison with Setup slack in GBA and violation is cured.**

## GBA HOLD SLACK

```
#####
# Generated by: Cadence Innovus 20.10-p004_1
# OS: Linux x86_64(Host ID edatools-server2.iitd.edu.in)
# Generated on: Fri Nov 15 12:58:45 2024
# Design: ticket_machine_fsm
# Command: report timing -max_path 100 -early > report_dir/after_optimisation_80/timing_hold_report_GBA.rpt
#####
Path 1: MET Hold Check with Pin remaining_reg[4]/CK
Endpoint: remaining_reg[4]/SI (v) checked with leading edge of 'clk'
Beginpoint: remaining_reg[5]/Q (v) triggered by leading edge of 'clk'
Path Groups: {clk}
Analysis View: view1
Other End Arrival Time 0.000
+ Hold 0.047
+ Phase Shift 0.000
+ Uncertainty 0.100
= Required Time 0.148
Arrival Time 0.361
Slack Time 0.213
Clock Rise Edge 0.000
+ Clock Network Latency (Prop) 0.000
= Beginpoint Arrival Time 0.000
+-----+
| Instance | Arc | Cell | Delay | Arrival | Required |
|-----+-----+-----+-----+-----+-----+
| remaining_reg[5] | CK ^ |          | 0.000 | -0.213 | |
| remaining_reg[5] | CK ^ -> Q v | SDFFRHQX1 | 0.361 | 0.361 | 0.148 |
| remaining_reg[4] | SI v | SDFFRHQX1 | 0.000 | 0.361 | 0.148 |
+-----+
```

The Worst Hold Path of GBA is mentioned above with begin point of **remaining\_reg[5]/Q** and endpoint of **remaining\_reg[4]/SI**. In the above GBA the Required Time = End Arrival Time(latency of clock which is 0 by default but can be changed using constraint) + hold + Phase Shift(clock time period defined in constraint file)+Uncertainty = 0 + 0.048+0.1 = 0.148 ns Arrival time is computed using Forward Traversal of Timing Graph.

Arrival time = 0.361

Slack = Arrival Time - Required Time = 0.213

## PBA HOLD SLACK

```
#####
# Generated by: Cadence Innovus 20.10-p004 1
# OS: Linux x86_64 (Host ID edatools-server2.iitd.edu.in)
# Generated on: Fri Nov 15 12:58:46 2024
# Design: ticket_machine fsm
# Command: report timing -retime path slew_propagation -max_path 100 -early -format retime_slew > report_dir/after_optimisation 80/timing_hold_report_PBA.rpt
#####
Path 1: MET Hold Check with Pin remaining_reg[4]/CK
Endpoint: remaining_reg[4]/SI (v) checked with leading edge of 'clk'
Beginpoint: remaining_reg[5]/Q (v) triggered by leading edge of 'clk'
Path Groups: {clk}
Analysis View: view1
Retime Analysis { Data Path-Slew }
Other End Arrival Time 0.000
+ Hold 0.047
+ Phase Shift 0.000
+ Uncertainty 0.100
= Required Time 0.148
Arrival Time 0.361
Slack Time 0.213
= Slack Time(original) 0.213
    | Clock Rise Edge 0.000
    + Clock Network Latency (Prop) 0.000
    = Beginpoint Arrival Time 0.000
    +-----
    | Retime |
    | Slew |
    +-----+
    | 0.004 |
    | 0.078 |
    | 0.078 |
    +-----+
```

The Worst Hold Path of GBA is mentioned above with begin point of **remaining\_reg[5]/Q** and endpoint of **remaining\_reg[4]/SI**. In the above GBA the Required Time = End Arrival Time(latency of clock which is 0 by default but can be changed using constraint) + hold + Phase Shift(clock time period defined in constraint file)+Uncertainty =  $0 + 0.048 + 0.1 = 0.148$  ns Arrival time is computed using Forward Traversal of Timing Graph.

Arrival time = 0.361

Slack = Arrival Time - Required Time = 0.213

**Hold Slack is same for both the analysis.**

## Comparison of different metal layers on the timing of the path

### Increasing the bottom metal layer (M1 to M4) :

- 1. Setup slack may decrease:** Increasing the bottom metal layer may increase the delay in the signal path, which can decrease the available time for the data signal to stabilize before the clock signal arrives. This can cause a decrease in the setup slack.
- 2. Hold slack may increase:** Increasing the bottom metal layer may decrease the delay in the signal path, which can result in an increase in the time that the data signal can be held stable after the clock signal arrives. This can cause an increase in the hold slack.

### Increasing the Top metal layer (M3 to M7):

- 1. Setup slack may increase:** Increasing the top layer can reduce the parasitic capacitance and resistance of the signal path, which can result in a reduction of delay and an increase in the available time for the data signal to stabilize before the clock signal arrives. This can cause an increase in the setup slack.
- 2. Hold slack may decrease:** Increasing the top layer can reduce the time that the data signal can be held stable after the clock signal arrives due to the reduced parasitic capacitance and resistance of the signal path. This can cause a decrease in the hold slack.

## AREA

Inst Name	Module Name	Inst Count	Total Area	Buffer	Inverter	Combinational	Flop	Latch	Clock Gate	Macro
Physical 0.000	ticket_machine_fsm	439	3234.234	158.949	368.610	1757.522	949.153	0.000	0.000	0.000

### Area Report:

Area of Buffers: 158.949  $\mu\text{m}^2$

Area of Inverters: 368.610  $\mu\text{m}^2$

Area of flip flops: 949.153  $\mu\text{m}^2$

Area of Combinational cells: 1757.522  $\mu\text{m}^2$

Total Area: 3234.234  $\mu\text{m}^2$

## POWER

### Power Report:

**Internal power:** It is the power consumed within the confines of a cell, arises from the charging or discharging of internal capacitances during switching. The cumulative internal power dissipation is measured at 0.3470mW which is 33.8526 % of total consumed power.

**Switching power:** It refers to the energy consumed by a driving cell when it charges and discharges the load capacitance connected to its output. In this case, the overall switching power amounts to 0.6595mW which is 64.3320 % of total power.

**Leakage power:** This leakage current is the current that flows from VDD to GND when there is no switching. The total leakage power is 0.01861mW which is 1.8154 % of total power.

**Total power:** Total power is the sum of the all above powers which is 1.0251mW.

```

*-----*
*   Innovus 20.10-p004_1 (64bit) 05/07/2020 20:02 (Linux 2.6.32-431.11.2.el6.x86_64)
*
*   Date & Time:    2024-Nov-15 12:58:46 (2024-Nov-15 07:28:46 GMT)
*
*-----*
*
*   Design: ticket_machine_fsm
*
*   Liberty Libraries used:
*       view1: ../../lib/90/slow.lib
*
*   Power Domain used:
*       Rail:      VDD      Voltage:      0.9
*
*   Power View : view1
*
*   User-Defined Activity : N.A.
*
*   Activity File: N.A.
*
*   Hierarchical Global Activity: N.A.
*
*   Global Activity: N.A.
*
*   Sequential Element Activity: 0.200000
*
*   Primary Input Activity: 0.200000
*
*   Default icg ratio: N.A.
*
*   Global Comb ClockGate Ratio: N.A.
*
*   Power Units = 1mW
*
*   Time Units = 1e-09 secs
*
*   Temperature = 125
*
*   report_power -outfile 80_after_optimisation_reports/power.rpt -rail_analysis_format VS
*-----*

```

Cell	Internal Power	Switching Power	Total Power	Leakage Power	Cell Name
FE_OFC2_fare_6	0.001989	0.0196	0.02181	0.0002199	CLKBUFX12
FE_OFC11_state_4	0.001989	0.01957	0.02178	0.0002199	CLKBUFX12
FE_OFC8_fare_0	0.001992	0.01955	0.02176	0.0002199	CLKBUFX12
FE_OFC12_return_amt_1	0.001992	0.01953	0.02174	0.0002199	CLKBUFX12
FE_OFC17_state_1	0.001991	0.01953	0.02174	0.0002199	CLKBUFX12
FE_OFC18_fare_?	0.001991	0.01953	0.0217	0.0002199	CLKBUFX12

**Total Power**

Total Internal Power:	0.34704497	33.8526%
Total Switching Power:	0.65950922	64.3320%
Total Leakage Power:	0.01861048	1.8154%
Total Power:	1.02516467	

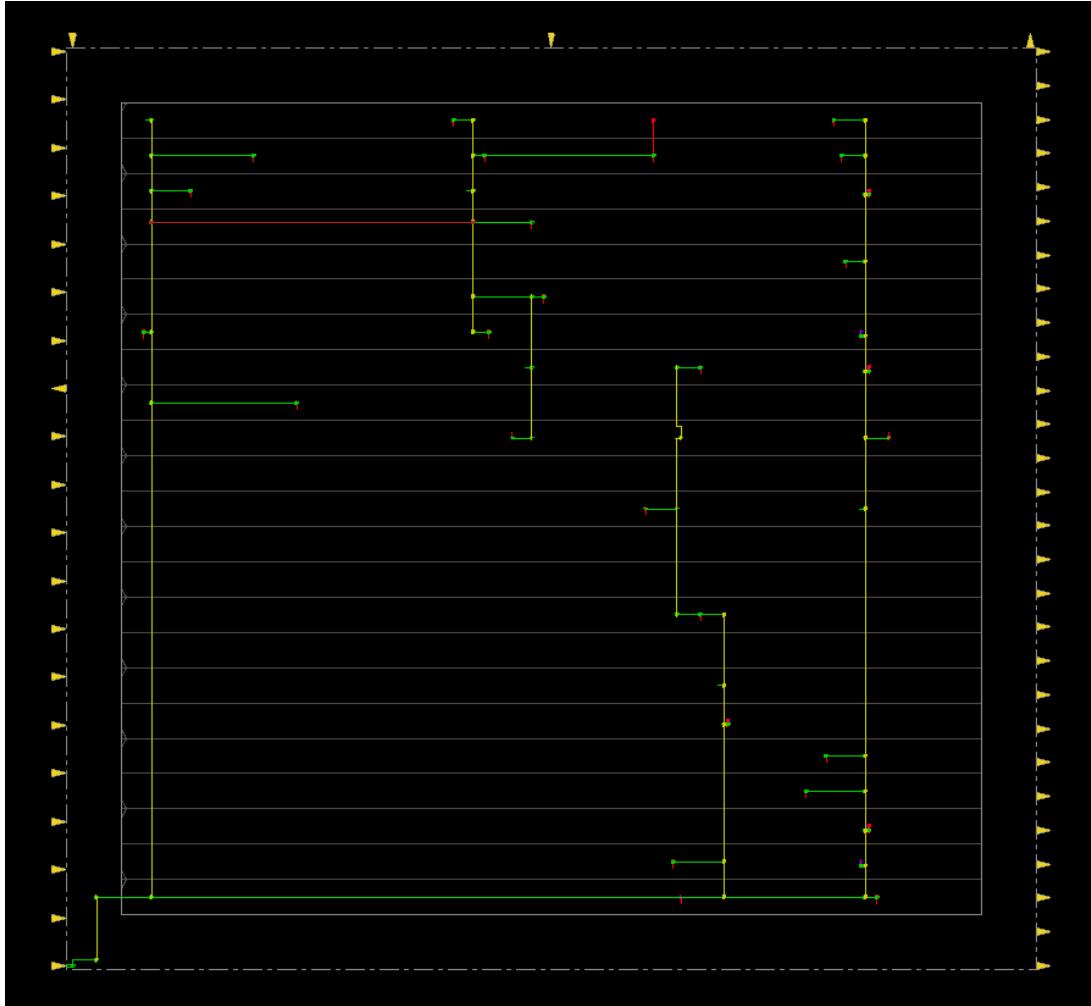
-----  
Ended Static Power Report Generation: (cpu=0:00:00, real=0:00:00,  
mem(process/total/peak)=1289.34MB/2837.14MB/1289.34MB)

g10121	2.497e-05	2.048e-05	7.145e-05	2.001e-05	NAND4XL
g10033	1.807e-05	2.181e-05	6.768e-05	2.78e-05	NAND4BXL
g9995	3.353e-05	1.156e-05	6.325e-05	1.815e-05	A0I21X1
g10080	1.102e-05	2.413e-05	6.295e-05	2.78e-05	NAND4BXL
g9889	2.981e-05	1.869e-05	6.151e-05	1.301e-05	CLKINVX1
g10119	1.249e-05	2.003e-05	6.032e-05	2.78e-05	NAND4BXL
g10042	3.052e-05	9.262e-06	5.982e-05	2.004e-05	NOR2BX1
g9993	1.78e-05	2.627e-05	5.708e-05	1.301e-05	CLKINVX1
g9926	2.939e-05	7.556e-06	5.51e-05	1.815e-05	A0I21X1
g9902	1.071e-05	3.045e-05	5.351e-05	1.236e-05	NOR2XL
g10001	1.165e-05	2.835e-05	5.302e-05	1.301e-05	CLKINVX1
g10073	2.252e-05	1.592e-05	5.08e-05	1.236e-05	NOR2XL
g10022	1.485e-05	2.291e-05	5.077e-05	1.301e-05	CLKINVX1
g10002	6.352e-06	3.434e-05	4.998e-05	9.289e-06	NAND2XL
g10008	2.595e-05	1.021e-05	4.914e-05	1.299e-05	OAI21X1
g9891	2.31e-05	7.074e-06	4.868e-05	1.851e-05	OAI32X1
g10037	1.215e-05	1.648e-05	4.858e-05	1.995e-05	A0I211X1
g10041	2.2e-05	5.806e-06	4.785e-05	2.004e-05	NOR2BX1
g9852	6.74e-06	2.937e-06	4.387e-05	3.419e-05	NAND3BX1
g9943	1.197e-05	1.125e-05	4.242e-05	1.92e-05	OAI2BB1XL
g9901	1.61e-05	8.024e-06	3.632e-05	1.22e-05	A0I21XL
g10004	8.439e-06	1.46e-05	3.54e-05	1.236e-05	NOR2XL
g9860	9.435e-06	6.728e-06	3.537e-05	1.92e-05	OAI2BB1XL
g10003	7.119e-06	1.496e-05	3.509e-05	1.301e-05	CLKINVX1
g9913	1.527e-05	6.675e-06	3.414e-05	1.22e-05	A0I21XL
g10005	9.679e-06	3.166e-06	3.377e-05	2.093e-05	NOR4X1
g9882	1.542e-05	4.562e-06	3.218e-05	1.22e-05	A0I21XL
g9900	1.358e-05	4.458e-06	3.102e-05	1.299e-05	OAI21X1
g9885	1.183e-05	3.765e-06	2.795e-05	1.236e-05	NOR2XL
g9914	1.008e-05	4.013e-06	2.708e-05	1.299e-05	OAI21X1
g9916	1.182e-05	2.678e-06	2.685e-05	1.236e-05	NOR2XL
g9886	5.965e-06	4.675e-06	2.467e-05	1.403e-05	NAND2X1
g9927	8.062e-06	2.825e-06	2.387e-05	1.299e-05	OAI21X1
g10078	9.121e-06	4.796e-06	2.385e-05	9.93e-06	NAND3XL
g9930	7.692e-06	2.787e-06	2.284e-05	1.236e-05	NOR2XL
g10036	5.326e-06	4.48e-06	2.282e-05	1.301e-05	CLKINVX1
g9856	8.065e-06	3.635e-06	2.043e-05	8.728e-06	OAI21XL
g9905	6.549e-06	1.474e-06	2.038e-05	1.236e-05	NOR2XL
g10072	4.494e-06	4.791e-06	1.857e-05	9.289e-06	NAND2XL
g10071	4.594e-06	3.6e-06	1.748e-05	9.289e-06	NAND2XL
g9850	4.351e-06	2.283e-06	1.592e-05	9.289e-06	NAND2XL
g9823	3.78e-06	2.681e-06	1.575e-05	9.289e-06	NAND2XL
g9917	2.94e-06	2.54e-06	1.477e-05	9.289e-06	NAND2XL
g9904	2.27e-06	1.711e-06	1.327e-05	9.289e-06	NAND2XL
g9829	1.797e-06	1.502e-06	1.259e-05	9.289e-06	NAND2XL
g9931	1.313e-06	1.106e-06	1.171e-05	9.289e-06	NAND2XL

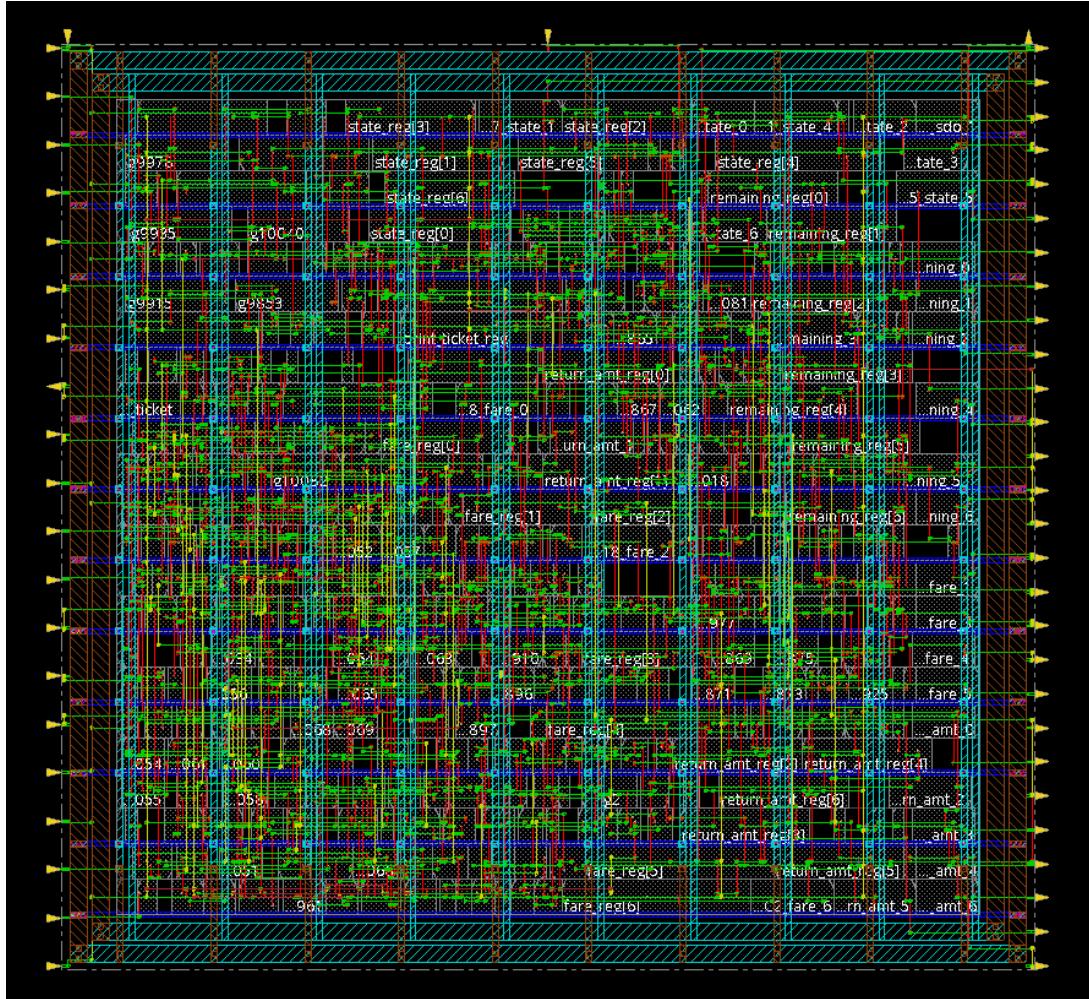
---

Total ( 439 of 439 )	0.347	0.6595	1.025	0.01861
Total Capacitance	3.41e-11 F			
Power Density	*** No Die Area ***			

## CLOCK ROUTING



## LAYOUT



## AFTER ROUTING

### GBA SETUP SLACK

```
#####
# Generated by: Cadence Innovus 20.10-p004_1
# OS: Linux x86_64(Host ID edatools-server2.iitd.edu.in)
# Generated on: Fri Nov 15 13:20:08 2024
# Design: ticket_machine_fsm
# Command: report_timing -max_path 100 -late > report_dir/after_routing_80/timing_setup_report_GBA.rpt
#####

Path 1: VIOLATED Setup Check with Pin fare_reg[6]/CK
Endpoint: fare_reg[6]/D (^) checked with leading edge of 'clk'
Beginpoint: dest_station[1] (^) triggered by leading edge of 'clk'
Path Groups: {clk}
Analysis View: view1
Other End Arrival Time -0.000
- Setup 0.259
+ Phase Shift 4.220
- Uncertainty 0.100
= Required Time 3.861
- Arrival Time 3.887
= Slack Time -0.026
    Clock Rise Edge 0.000
    + Input Delay 1.500
    = Beginpoint Arrival Time 1.500
+-----+
| Instance | Arc | Cell | Delay | Arrival | Required |
|          |     |      |        | Time   | Time     |
+-----+-----+-----+-----+-----+-----+
|          | dest_station[1] ^ |       |       | 1.500 | 1.474 |
| g10197 | A ^ -> Y v | CLKINVX1 | 0.094 | 1.594 | 1.567 |
| g10150 | C v -> Y ^ | NAND3X1 | 0.190 | 1.784 | 1.758 |
| g10052 | B1 ^ -> Y v | OAI222X1 | 0.206 | 1.990 | 1.963 |
| g10024 | B0 v -> Y ^ | AOI2BB1X1 | 0.117 | 2.106 | 2.080 |
| g10015 | C0 ^ -> Y v | OAI221X1 | 0.145 | 2.251 | 2.225 |
| g9987 | D v -> Y v | OR4XL | 0.265 | 2.516 | 2.490 |
| g9939 | A v -> Y ^ | NOR2XL | 0.287 | 2.803 | 2.777 |
| g9923 | A1 ^ -> Y v | AOI21X1 | 0.234 | 3.037 | 3.011 |
| g9910 | A1 v -> Y ^ | AOI21X2 | 0.151 | 3.188 | 3.162 |
| g9896 | A1 ^ -> Y v | AOI21X2 | 0.111 | 3.299 | 3.273 |
| g9858 | A1 v -> Y ^ | AOI21X1 | 0.171 | 3.470 | 3.444 |
| g9831 | A1 ^ -> Y v | OAI21X1 | 0.101 | 3.571 | 3.545 |
| g9824 | B v -> Y ^ | NOR2XL | 0.103 | 3.674 | 3.648 |
| g9822 | B0 ^ -> Y v | AOI21XL | 0.069 | 3.743 | 3.717 |
| g9817 | A1 v -> Y ^ | OAI211X1 | 0.144 | 3.887 | 3.861 |
| fare_reg[6] | D ^ | SDFFRHQX8 | 0.000 | 3.887 | 3.861 |
+-----+
```

The critical setup path identified by GBA starts from the begin point **dest\_station[1]** and ends at **fare\_reg[6]/D**.

In this **GBA analysis**, the Required Time (RT) is calculated as the End Arrival Time (default latency of clock, which is 0 but can be modified with constraints) - Setup + Phase Shift (defined clock time period in the constraint file) - Uncertainty. In this case, it is  $0 - 0.259 + 4.220 - 0.100 = 3.861$ .

Arrival time is determined through Forward Traversal of the Timing Graph and is found to be 3.887. Hence, the Slack is computed as (Required Time - Arrival Time), resulting in a value of -0.026 (violation).

## PBA SETUP SLACK

```
#####
# Generated by: Cadence Innovus 20.10-p004_1
# OS: Linux x86_64(Host ID edatools-server2.iitd.edu.in)
# Generated on: Fri Nov 15 13:20:08 2024
# Design: ticket_machine fsm
# Command: report_timing -retime path slew propagation -max_path 100 -late -format retime_slew > report_dir/after_routing_80/timing_setup_report_PBA.rpt
#####
Path 1: MET Setup Check with Pin fare_reg[6]/CK
Endpoint: fare_reg[6]/D (^) checked with leading edge of 'clk'
Beginpoint: dest_station[1] (^) triggered by leading edge of 'clk'
Path Groups: {clk}
Analysis View: view1
Retime Analysis { Data Path-Slew }
Other End Arrival Time -0.000
- Setup 0.253
+ Phase Shift 4.220
- Uncertainty 0.100
= Required Time 3.867
- Arrival Time 3.810
= Slack Time 0.057
= Slack Time(original) -0.026
    Clock Rise Edge 0.000
    + Input Delay 1.500
    = Beginpoint Arrival Time 1.500
+-----+
| Retime |
| Slew |
+-----+
| 0.003 |
| 0.003 |
| 0.126 |
| 0.126 |
| 0.207 |
| 0.207 |
| 0.192 |
| 0.192 |
| 0.097 |
| 0.097 |
| 0.159 |
| 0.159 |
| 0.105 |
| 0.353 |
| 0.353 |
| 0.243 |
| 0.243 |
| 0.127 |
| 0.127 |
| 0.099 |
| 0.099 |
| 0.151 |
| 0.151 |
```

The critical setup path identified by GBA starts from the begin point **dest\_station[1]** and ends at **fare\_reg[6]/D**.

In this **PBA analysis**, the Required Time (RT) is calculated as the End Arrival Time (default latency of clock, which is 0 but can be modified with constraints) - Setup + Phase Shift (defined clock time period in the constraint file) - Uncertainty. In this case, it is  $0 - 0.253 + 4.220 - 0.100 = 3.867$ .

Arrival time is determined through Forward Traversal of the Timing Graph and is found to be 3.810. Hence, the Slack is computed as (Required Time - Arrival Time), resulting in a value of 0.057 (no violation).

**Setup slack in PBA increases in comparison with Setup slack in GBA and violation is cured.**

## GBA HOLD SLACK

```
#####
# Generated by: Cadence Innovus 20.10-p004_1
# OS: Linux x86_64(Host ID edatools-server2.iitd.edu.in)
# Generated on: Fri Nov 15 13:20:08 2024
# Design: ticket machine fsm
# Command: report_timing -max_path 100 -early > report_dir/after_routing_80/timing_hold_report_GBA.rpt
#####
Path 1: MET Hold Check with Pin remaining_reg[0]/CK
Endpoint: remaining_reg[0]/SI (v) checked with leading edge of 'clk'
Beginpoint: remaining_reg[1]/Q (v) triggered by leading edge of 'clk'
Path Groups: {clk}
Analysis View: view1
Other End Arrival Time 0.000
+ Hold 0.047
+ Phase Shift 0.000
+ Uncertainty 0.100
= Required Time 0.147
Arrival Time 0.360
Slack Time 0.213
Clock Rise Edge 0.000
+ Clock Network Latency (Prop) 0.000
= Beginpoint Arrival Time 0.000
+-----+
| Instance | Arc | Cell | Delay | Arrival | Required |
|          |     |      |       | Time   | Time    |
+-----+
| remaining_reg[1] | CK ^ |          | 0.000 | -0.213 | |
| remaining_reg[1] | CK ^ -> Q v | SDFFRHQX1 | 0.360 | 0.147 |
| remaining_reg[0] | SI v |          | 0.000 | 0.360 | 0.147 |
+-----+
```

The Worst Hold Path of GBA is mentioned above with begin point of **remaining\_reg[1]/Q** and endpoint of **remaining\_reg[0]/SI**. In the above GBA the Required Time = End Arrival Time(latency of clock which is 0 by default but can be changed using constraint) + hold + Phase Shift(clock time period defined in constraint file)+Uncertainty = 0 + 0.047+0.1 = 0.147 ns Arrival time is computed using Forward Traversal of Timing Graph.

Arrival time = 0.360

Slack = Arrival Time - Required Time = 0.213

## PBA HOLD SLACK

```
#####
# Generated by: Cadence Innovus 20.10-p004_1
# OS: Linux x86_64(Host ID edatools-server2.iitd.edu.in)
# Generated on: Fri Nov 15 13:20:08 2024
# Design: ticket_machine_fsm
# Command: report_timing -retime path_slew propagation -max_path 100 -early -format retime_slew > report_dir/after_routing_00/timing_hold_report_PBA.rpt
#####
Path 1: MET Hold Check with Pin remaining_reg[0]/CK
Endpoint: remaining_reg[0]/SI (v) checked with leading edge of 'clk'
Beginpoint: remaining_reg[1]/Q (v) triggered by leading edge of 'clk'
Path Groups: {clk}
Analysis View: view1
Retime Analysis { Data Path-Slew }
Other End Arrival Time 0.000
+ Hold 0.047
+ Phase Shift 0.000
+ Uncertainty 0.100
= Required Time 0.147
Arrival Time 0.360
Slack Time 0.213
= Slack Time(original) 0.213
  Clock Rise Edge 0.000
  + Clock Network Latency (Prop) 0.000
  = Beginpoint Arrival Time 0.000
  +-----+
  | Retime |
  | Slew |
  |-----|
  | 0.004 |
  | 0.077 |
  | 0.077 |
  +-----+
```

The Worst Hold Path of GBA is mentioned above with begin point of **remaining\_reg[1]/Q** and endpoint of **remaining\_reg[0]/SI**. In the above GBA the Required Time = End Arrival Time(latency of clock which is 0 by default but can be changed using constraint) + hold + Phase Shift(clock time period defined in constraint file)+Uncertainty =  $0 + 0.047 + 0.1 = 0.147$  ns Arrival time is computed using Forward Traversal of Timing Graph.

Arrival time = 0.361

Slack = Arrival Time - Required Time = 0.213

**Hold slack is same in both the analysis.**

## AREA

Inst Name	Module Name	Inst Count	Total Area	Buffer	Inverter	Combinational	Flop	Latch	Clock Gate	Macro
Physical 0.000	ticket_machine_fsm	439	3234.234	158.949	368.610	1757.522	949.153	0.000	0.000	0.000

### Area Report:

Area of Buffers: 158.949  $\mu\text{m}^2$

Area of Inverters: 368.610  $\mu\text{m}^2$

Area of flip flops: 949.153  $\mu\text{m}^2$

Area of Combinational cells: 1757.522  $\mu\text{m}^2$

Total Area: 3234.234  $\mu\text{m}^2$

## POWER

### Power Report:

**Internal power:** It is the power consumed within the confines of a cell, arises from the charging or discharging of internal capacitances during switching. The cumulative internal power dissipation is measured at 0.3470mW which is 33.8526 % of total consumed power.

**Switching power:** It refers to the energy consumed by a driving cell when it charges and discharges the load capacitance connected to its output. In this case, the overall switching power amounts to 0.6595mW which is 64.3320 % of total power.

**Leakage power:** This leakage current is the current that flows from VDD to GND when there is no switching. The total leakage power is 0.01861mW which is 1.8154 % of total power.

**Total power:** Total power is the sum of the all above powers which is 1.0251mW.

```

*-----*
*   Innovus 20.10-p004_1 (64bit) 05/07/2020 20:02 (Linux 2.6.32-431.11.2.el6.x86_64)
*
*   Date & Time:    2024-Nov-15 12:58:46 (2024-Nov-15 07:28:46 GMT)
*
*-----*
*
*   Design: ticket_machine_fsm
*
*   Liberty Libraries used:
*       view1: ../../lib/90/slow.lib
*
*   Power Domain used:
*       Rail:      VDD      Voltage:      0.9
*
*   Power View : view1
*
*   User-Defined Activity : N.A.
*
*   Activity File: N.A.
*
*   Hierarchical Global Activity: N.A.
*
*   Global Activity: N.A.
*
*   Sequential Element Activity: 0.200000
*
*   Primary Input Activity: 0.200000
*
*   Default icg ratio: N.A.
*
*   Global Comb ClockGate Ratio: N.A.
*
*   Power Units = 1mW
*
*   Time Units = 1e-09 secs
*
*   Temperature = 125
*
*   report_power -outfile 80_after_optimisation_reports/power.rpt -rail_analysis_format VS
*-----*

```

Cell	Internal Power	Switching Power	Total Power	Leakage Power	Cell Name
FE_OFC2_fare_6	0.001989	0.0196	0.02181	0.0002199	CLKBUFX12
FE_OFC11_state_4	0.001989	0.01957	0.02178	0.0002199	CLKBUFX12
FE_OFC8_fare_0	0.001992	0.01955	0.02176	0.0002199	CLKBUFX12
FE_OFC12_return_amt_1	0.001992	0.01953	0.02174	0.0002199	CLKBUFX12
FE_OFC17_state_1	0.001991	0.01953	0.02174	0.0002199	CLKBUFX12
FE_OFC18_fare_?	0.001991	0.01953	0.0217	0.0002199	CLKBUFX12

**Total Power**

Total Internal Power:	0.34704497	33.8526%
Total Switching Power:	0.65950922	64.3320%
Total Leakage Power:	0.01861048	1.8154%
Total Power:	1.02516467	

-----  
Ended Static Power Report Generation: (cpu=0:00:00, real=0:00:00,  
mem(process/total/peak)=1289.34MB/2837.14MB/1289.34MB)

g10121	2.497e-05	2.048e-05	7.145e-05	2.001e-05	NAND4XL
g10033	1.807e-05	2.181e-05	6.768e-05	2.78e-05	NAND4BXL
g9995	3.353e-05	1.156e-05	6.325e-05	1.815e-05	A0I21X1
g10080	1.102e-05	2.413e-05	6.295e-05	2.78e-05	NAND4BXL
g9889	2.981e-05	1.869e-05	6.151e-05	1.301e-05	CLKINVX1
g10119	1.249e-05	2.003e-05	6.032e-05	2.78e-05	NAND4BXL
g10042	3.052e-05	9.262e-06	5.982e-05	2.004e-05	NOR2BX1
g9993	1.78e-05	2.627e-05	5.708e-05	1.301e-05	CLKINVX1
g9926	2.939e-05	7.556e-06	5.51e-05	1.815e-05	A0I21X1
g9902	1.071e-05	3.045e-05	5.351e-05	1.236e-05	NOR2XL
g10001	1.165e-05	2.835e-05	5.302e-05	1.301e-05	CLKINVX1
g10073	2.252e-05	1.592e-05	5.08e-05	1.236e-05	NOR2XL
g10022	1.485e-05	2.291e-05	5.077e-05	1.301e-05	CLKINVX1
g10002	6.352e-06	3.434e-05	4.998e-05	9.289e-06	NAND2XL
g10008	2.595e-05	1.021e-05	4.914e-05	1.299e-05	OAI21X1
g9891	2.31e-05	7.074e-06	4.868e-05	1.851e-05	OAI32X1
g10037	1.215e-05	1.648e-05	4.858e-05	1.995e-05	A0I211X1
g10041	2.2e-05	5.806e-06	4.785e-05	2.004e-05	NOR2BX1
g9852	6.74e-06	2.937e-06	4.387e-05	3.419e-05	NAND3BX1
g9943	1.197e-05	1.125e-05	4.242e-05	1.92e-05	OAI2BB1XL
g9901	1.61e-05	8.024e-06	3.632e-05	1.22e-05	A0I21XL
g10004	8.439e-06	1.46e-05	3.54e-05	1.236e-05	NOR2XL
g9860	9.435e-06	6.728e-06	3.537e-05	1.92e-05	OAI2BB1XL
g10003	7.119e-06	1.496e-05	3.509e-05	1.301e-05	CLKINVX1
g9913	1.527e-05	6.675e-06	3.414e-05	1.22e-05	A0I21XL
g10005	9.679e-06	3.166e-06	3.377e-05	2.093e-05	NOR4X1
g9882	1.542e-05	4.562e-06	3.218e-05	1.22e-05	A0I21XL
g9900	1.358e-05	4.458e-06	3.102e-05	1.299e-05	OAI21X1
g9885	1.183e-05	3.765e-06	2.795e-05	1.236e-05	NOR2XL
g9914	1.008e-05	4.013e-06	2.708e-05	1.299e-05	OAI21X1
g9916	1.182e-05	2.678e-06	2.685e-05	1.236e-05	NOR2XL
g9886	5.965e-06	4.675e-06	2.467e-05	1.403e-05	NAND2X1
g9927	8.062e-06	2.825e-06	2.387e-05	1.299e-05	OAI21X1
g10078	9.121e-06	4.796e-06	2.385e-05	9.93e-06	NAND3XL
g9930	7.692e-06	2.787e-06	2.284e-05	1.236e-05	NOR2XL
g10036	5.326e-06	4.48e-06	2.282e-05	1.301e-05	CLKINVX1
g9856	8.065e-06	3.635e-06	2.043e-05	8.728e-06	OAI21XL
g9905	6.549e-06	1.474e-06	2.038e-05	1.236e-05	NOR2XL
g10072	4.494e-06	4.791e-06	1.857e-05	9.289e-06	NAND2XL
g10071	4.594e-06	3.6e-06	1.748e-05	9.289e-06	NAND2XL
g9850	4.351e-06	2.283e-06	1.592e-05	9.289e-06	NAND2XL
g9823	3.78e-06	2.681e-06	1.575e-05	9.289e-06	NAND2XL
g9917	2.94e-06	2.54e-06	1.477e-05	9.289e-06	NAND2XL
g9904	2.27e-06	1.711e-06	1.327e-05	9.289e-06	NAND2XL
g9829	1.797e-06	1.502e-06	1.259e-05	9.289e-06	NAND2XL
g9931	1.313e-06	1.106e-06	1.171e-05	9.289e-06	NAND2XL

---

Total ( 439 of 439 )	0.347	0.6595	1.025	0.01861
Total Capacitance	3.41e-11 F			
Power Density	*** No Die Area ***			

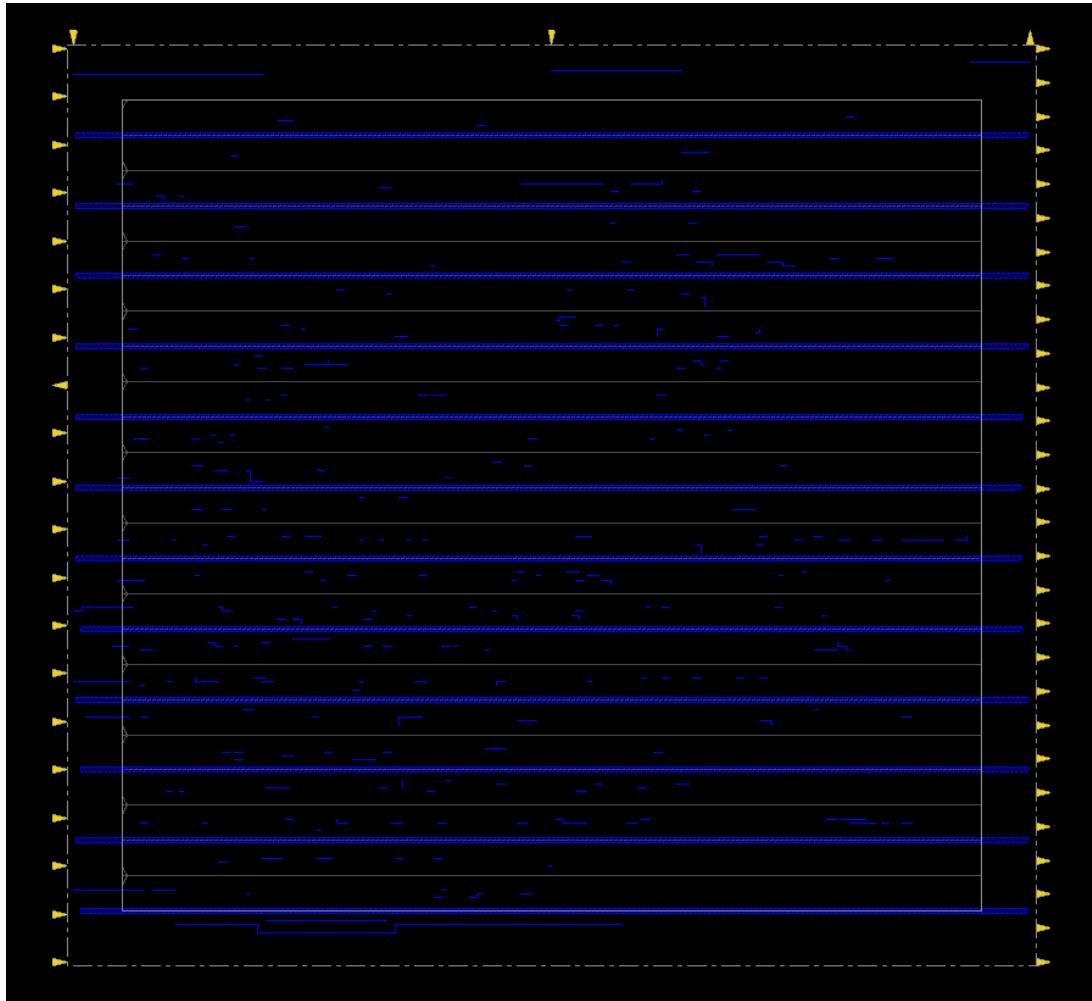
For 0.5 utilization:

Design Step	GBA Setup Slack (ns)	PBA Setup Slack (ns)	GBA Hold Slack (ns)	PBA Hold Slack (ns)	No. of cells	Power (mW)	Area of standard cells ( $\mu\text{m}^2$ )
Before physical Design	0.255	0.255	0.211	0.211	391	0.4409	2717
Before Placement	-4.457	-4.182	0.225	0.225	391	1.9319	3043.495
After Placement	-5.452	-5.108	0.291	0.291	391	2.1378	3043.495
After CTS (pre optimization)	0.003	0.046	0.223	0.223	435	1.0324	3263.752
After CTS (post optimization)	0.011	0.070	0.223	0.223	435	1.0313	3259.968
After Detailed Routing	0.012	0.068	0.224	0.224	435	1.0310	3259.968

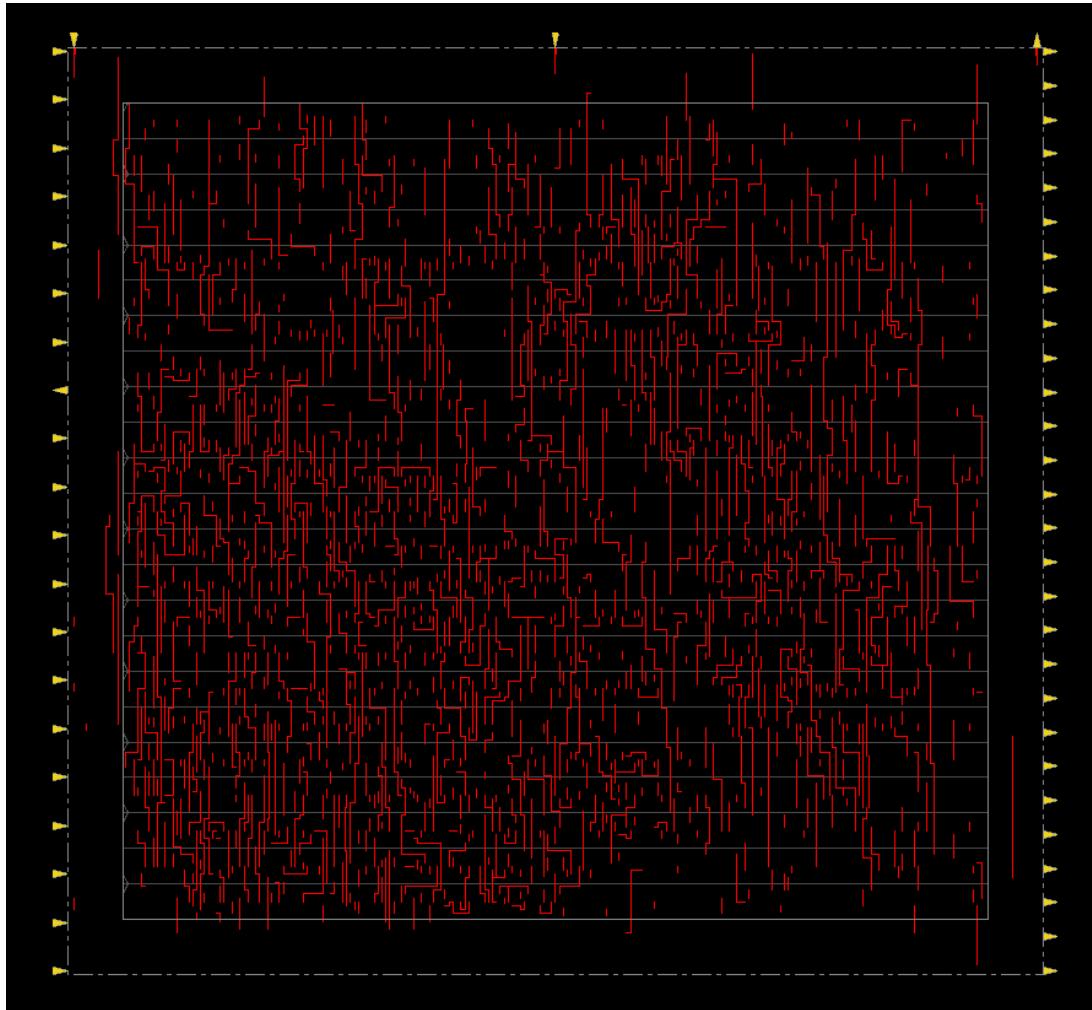
For 0.8 utilization:

Design Step	GBA Setup Slack (ns)	PBA Setup Slack (ns)	GBA Hold Slack (ns)	PBA Hold Slack (ns)	No. of cells	Power (mW)	Area of standard cells ( $\mu\text{m}^2$ )
Before Placement	-4.481	-4.209	0.252	0.252	391	1.9498	3043.495
After Placement	-5.267	-4.927	0.307	0.307	391	2.0815	3043.495
After CTS (pre optimization)	0.003	0.078	0.227	0.227	439	1.0423	3291.758
After CTS(post-optimization)	-0.028	0.05	0.213	0.213	439	1.0251	3234.234
After Detailed Routing	-0.026	0.057	0.213	0.213	439	1.02	3234.234

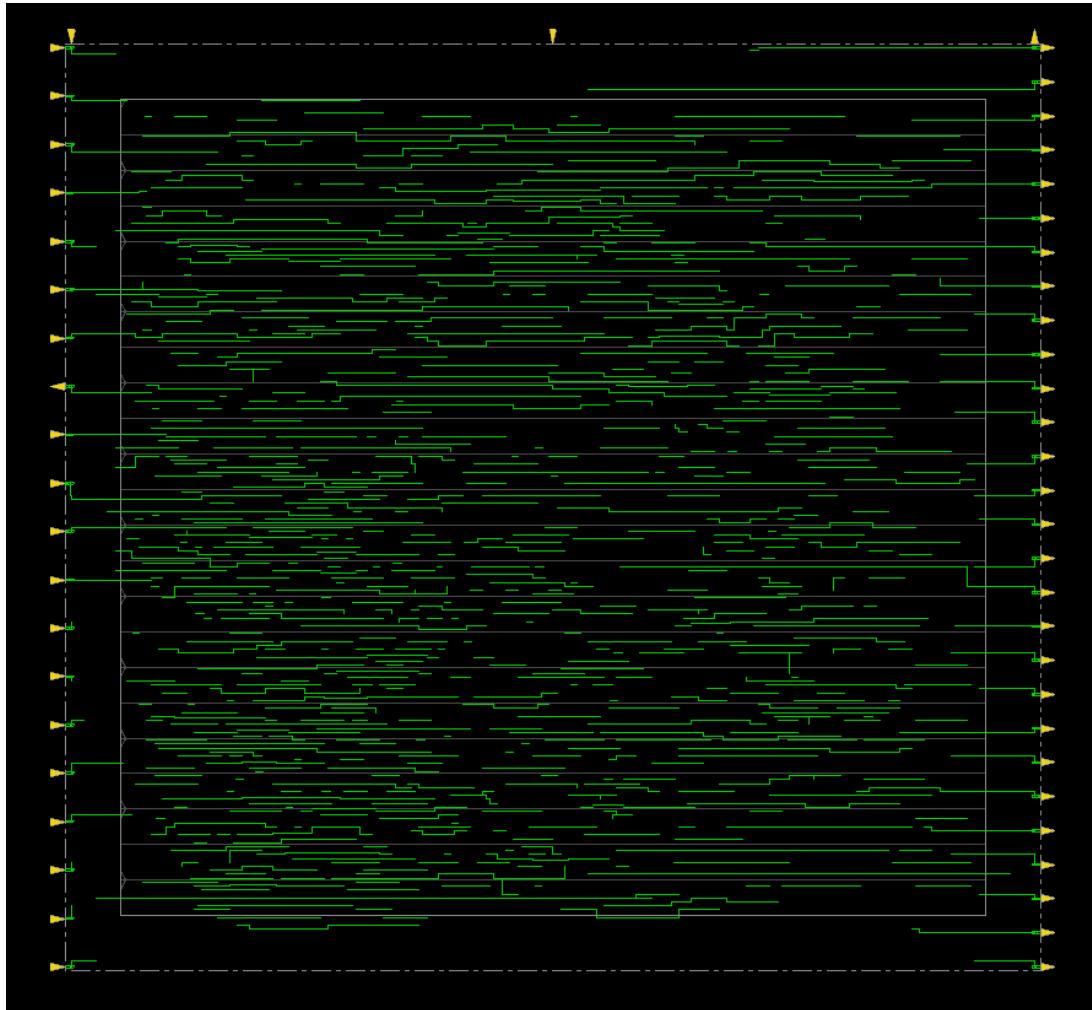
## METAL-1



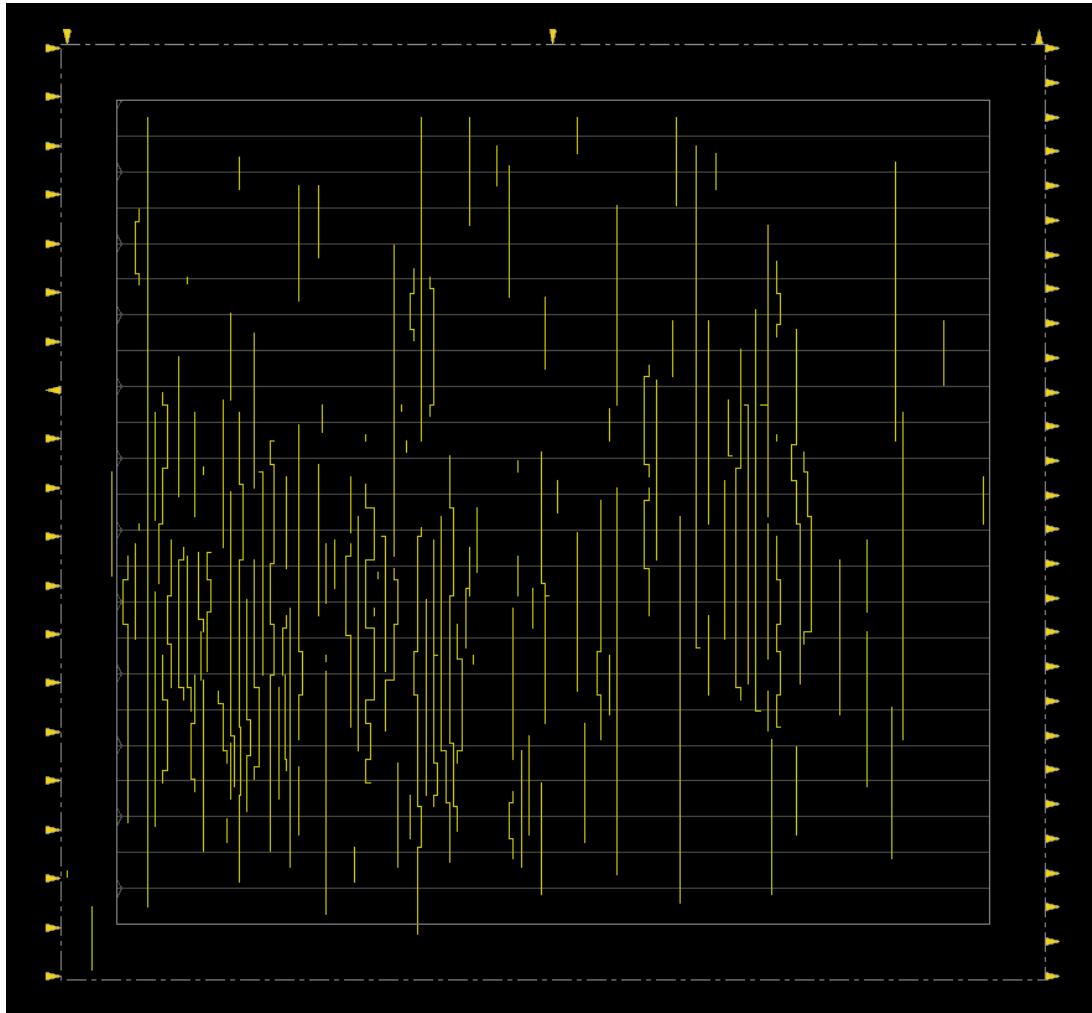
## METAL-2



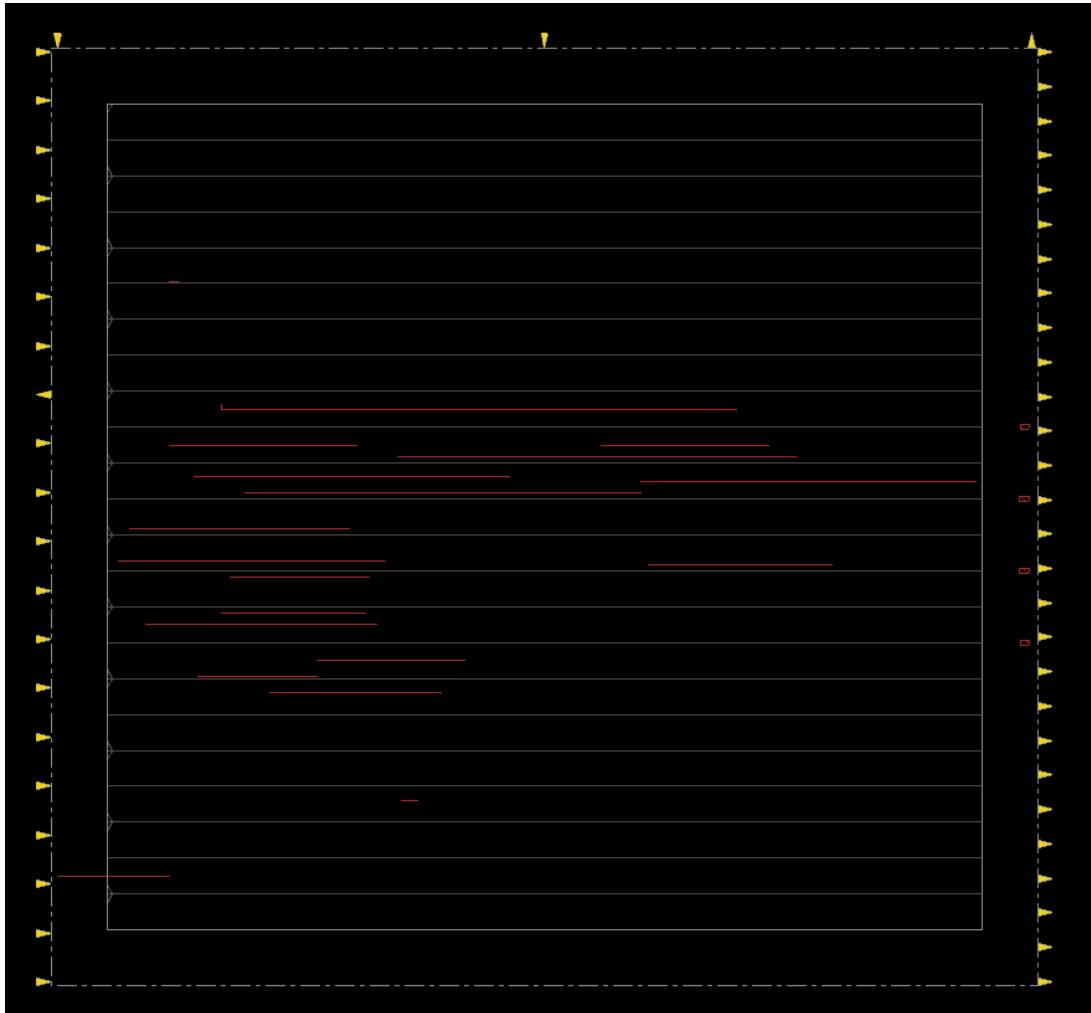
## METAL-3



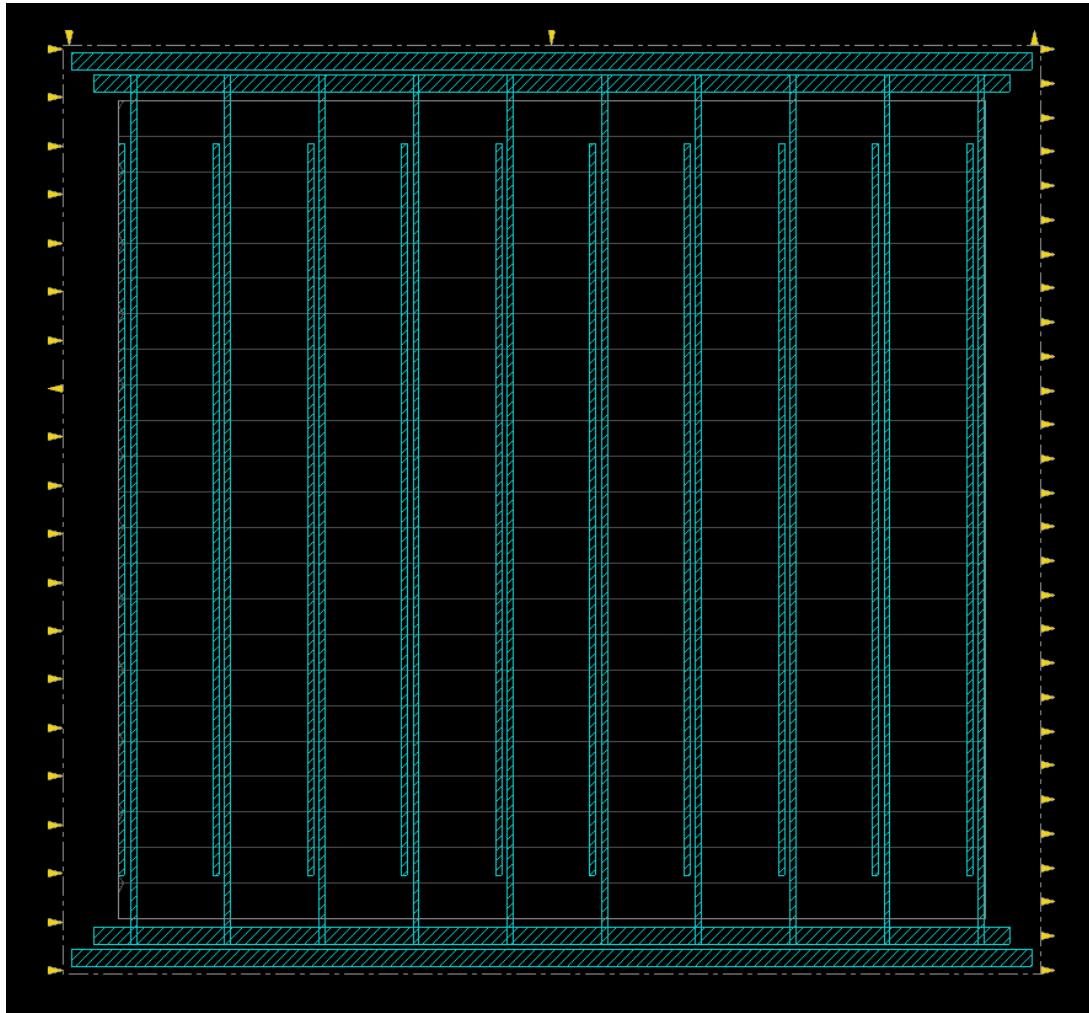
## METAL-4



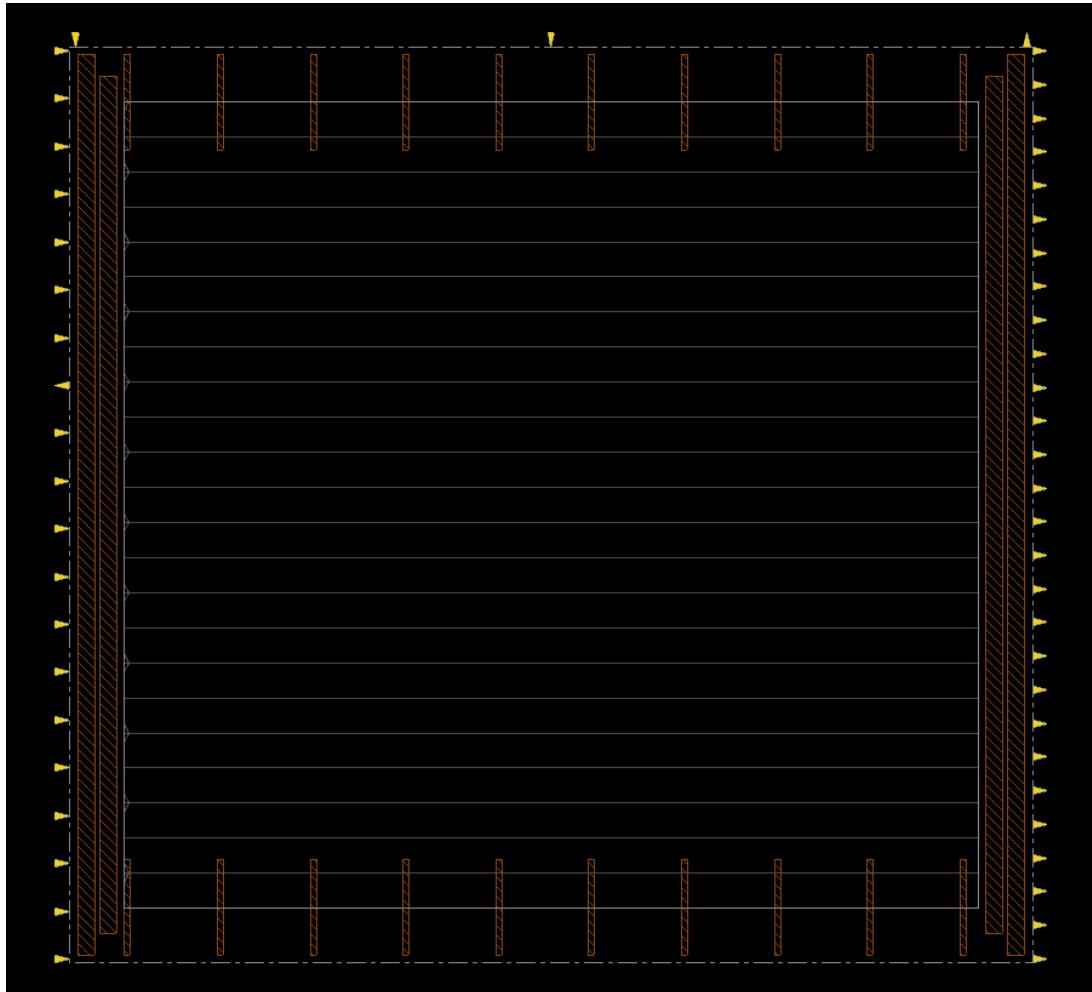
## METAL-5



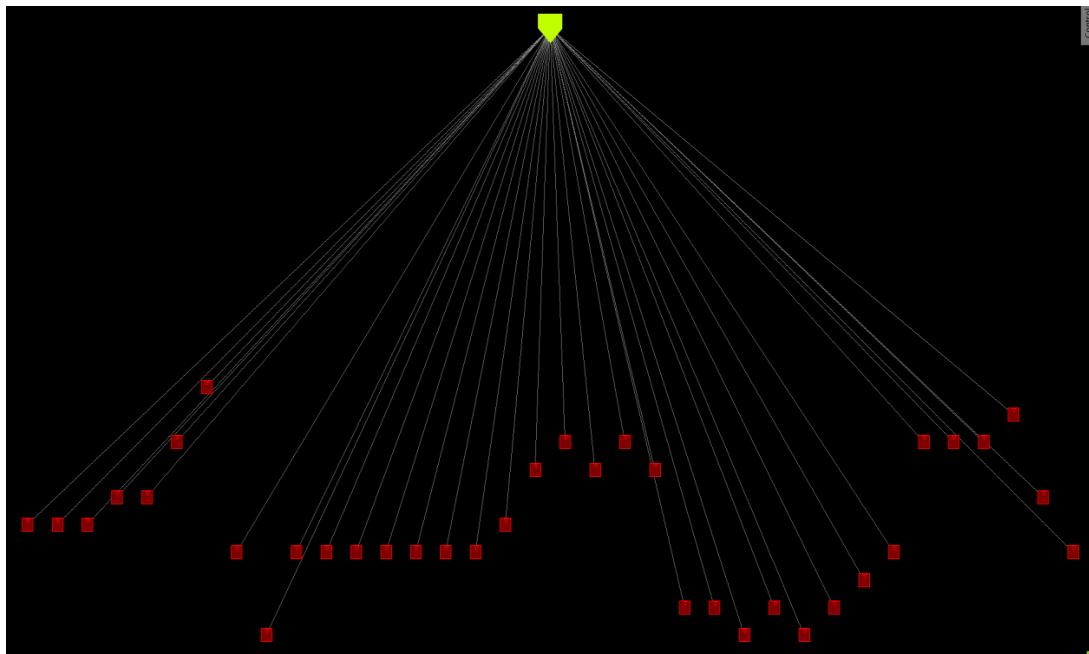
## METAL-8



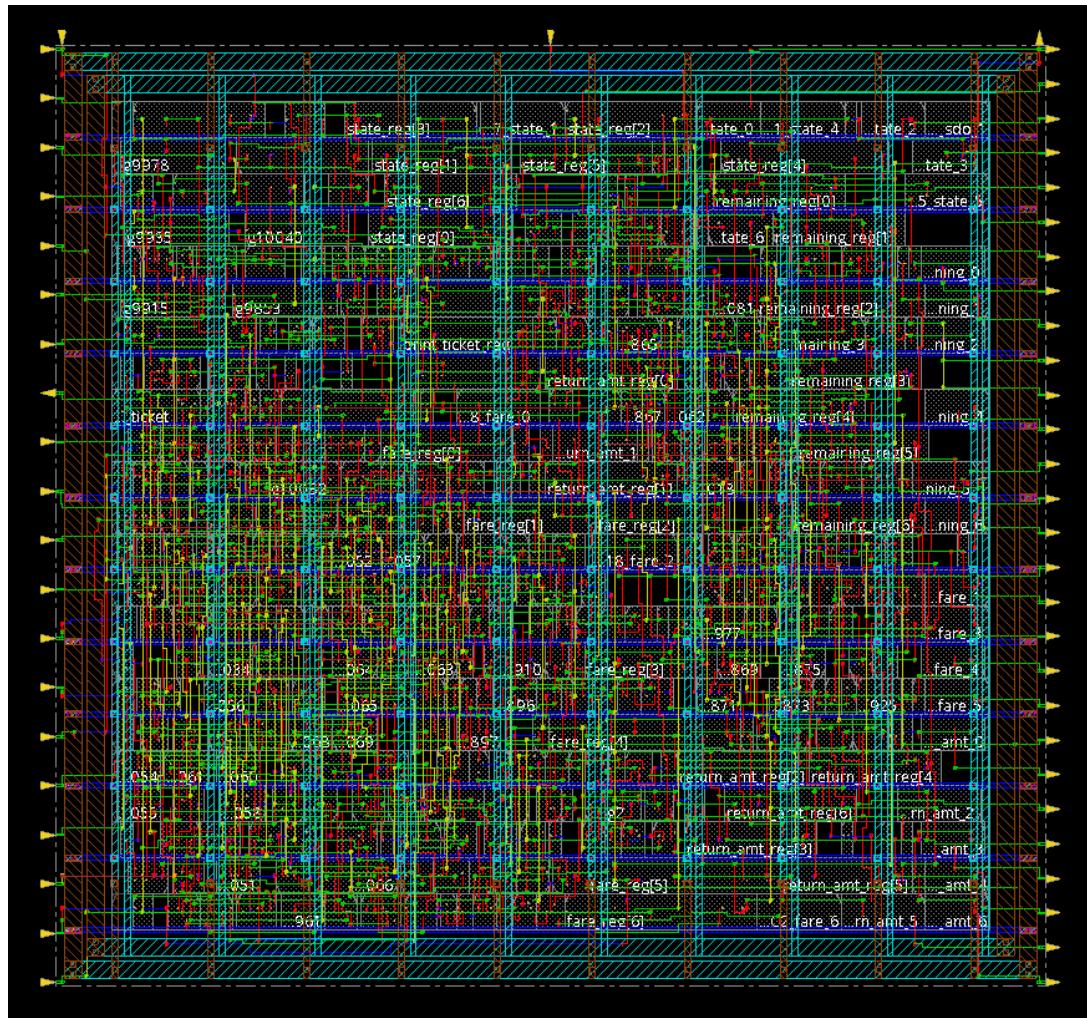
## METAL-9



CTS



## FINAL LAYOUT



## DRC VIOLATION

```
*** Starting Verify DRC (MEM: 1482.5) ***

VERIFY DRC ..... Starting Verification
VERIFY DRC ..... Initializing
VERIFY DRC ..... Deleting Existing Violations
VERIFY DRC ..... Creating Sub-Areas
VERIFY DRC ..... Using new threading
VERIFY DRC ..... Sub-Area: {0.000 0.000 71.630 68.150} 1 of 1
VERIFY DRC ..... Sub-Area : 1 complete 0 Viols.

Verification Complete : 0 Viols.

*** End Verify DRC (CPU: 0:00:00.1 ELAPSED TIME: 0.00 MEM: 0.0M) ***
```