CS 223 Computer Organization & Architecture

Lecture 37 [21.05.2020]

TCMP and NoC Design Principles

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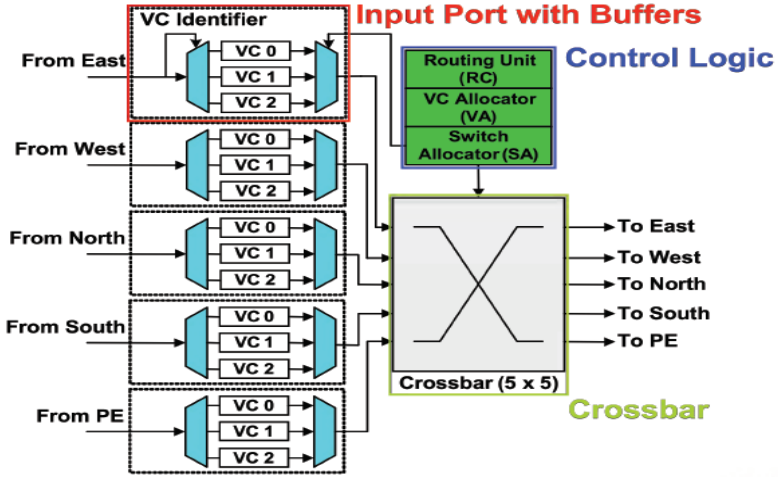
NoC Router Pipeline

- An NoC router does the following functions: VA: Virtual Channel Allocation, RC: Route computation, BW: Buffer Write, ST: Switch Traversal, SA: Switch Allocation. Write down the order of events.

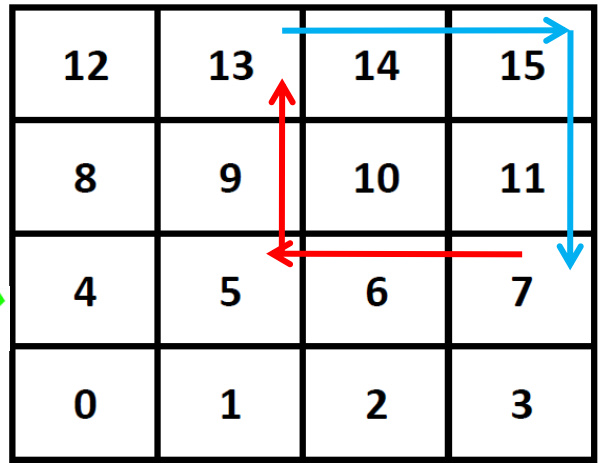
  - BW: Buffer Write
  - RC: Route computation
  - VA: Virtual Channel Allocation
  - SA: Switch Allocation
  - ST: Switch Traversal
  - LT: Link Traversal



BW	RC	VA	SA	ST		LT

NoC Routing

- A cache miss request packet P1 with a destination address 13 is injected into router 7 in a 4x4 mesh NoC that uses XY routing. State whether each of the following statement is True/False.
  - P1 while moving through the NoC takes a 90 degree turn at router 15. ✗
  - P1 moves through router 9. ✓
  - P1 takes 5 hops to reach its destination. ✗
  - Reply packet of P1 moves through router 14. ✓
  - Neither the request packet not the reply packet passes through router 10. ✓



NoC Routing

- Consider a 25 core machine in which cores are organized as regular square mesh topology. A packet P1 is generated from core number 18 destined to core 6. The system follows minimal north last routing. How many unique minimal paths are there from 18 to 6? List them.
  - 18-17-16-11-6
  - 18-17-12-11-6
  - 18-17-12-7-6
  - 18-13-12-11-6
  - 18-13-12-7-6
  - 18-13-8-7-6

20	21	22	23	24
15	16	17	18	19
10	11	12	13	14
5	6	7	8	9
0	1	2	3	4

NoC Router – Switch Arbitration

An input buffered NoC router R that uses age based switch allocation scheme (higher age has higher priority) and XY routing receives 4 packets at a given clock cycle. The details (packet number, age, source, destination) of the packets are <P1, 2, 15, 2>, <P2, 1, 10, 0>, <P3, 3, 11, 12> and <P4, 2, 9, 3>. State whether each of the following statement is True/False, if R is router 10 in a 4x4 mesh NoC?

Pkt	Age	S	D	IP	OP-req	OP- status
P1	2	15	2	N	S	S
P2	1	10	0	L	W	**** (BUFFER)
P3	3	11	12	E	W	W
P4	2	9	3	W	E	E

12	13	14	15
8	9	10	11
4	5	6	7
0	1	2	3

NoC Router – Switch Arbitration

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P2	1	10	0	L	W	**** (BUFFER)
P3	3	11	12	E	W	W
P4	2	9	3	W	E	E

12	13	14	15
8	9	10	11
4	5	6	7
0	1	2	3

- P4 enters R through its north input port. - False
- Both P2 and P3 wanted west output port at R. – True
- At the end of switch allocation phase P4 will remain in its buffer. - False
- There exits an output port conflict between P1 and P4 - - False
- At the end of switch allocation phase P1 gets south output port - True

Traffic Patterns and Packet Latency

Consider an 8x8 mesh NoC that uses a single flit packet scheme. Consider a 3 cycle router and 1cycle link for the NoC that uses XY routing. 3 packets P1, P2 and P3 were generated from routers 6, 24, and 50, respectively. If packet injection and ejection takes 2 cycles each, find the latency of P1, P2 and P3 if the packets follow

(a) transpose traffic pattern

(b) bit-complement traffic pattern

Traffic Patterns and Packet Latency

8x8 mesh NoC , XY routing
3 cycle router and 1cycle link.
P1 from 6, P2 from 24 and P3 from 50.
injection and ejection- 2 cycles each.

Lat = [hops x 4] + 4

56	57	58	59	60	61	62	63
48	49	50	51	52	53	54	55
40	41	42	43	44	45	46	47
32	33	34	35	36	37	38	39
24	25	26	27	28	29	30	31
16	17	18	19	20	21	22	23
8	9	10	11	12	13	14	15
0	1	2	3	4	5	6	7

Pkt	S	D_trans	Latency	D_bitrev	Lateny
P1	6	48	12x4+4 =52	57	12x4+4 =52
P2	24	3	6x4+4= 28	39	8x4+4=36
P3	50	22	8x4+4=36	13	8x4+4=36

TCMP Address Mapping

- Consider a TCMP system with a 8x8 mesh NoC where each tile consists of a superscalar processor a private L1 cache and a shared distributed L2 cache. Let T0, T1, T2... ,T63 corresponds to the tiles. The total L2 cache on the chip is 16MB and L2 uses 64B block and is 16-way associative. Each L2 cache on chip has all the 16 ways of the sets assigned to it. The L2 cache memory per tile division is such that total sets in L2 cache are uniformly partitioned across all tiles in sequential fashion as per SNUCA policy. The system uses a 32-bit physical address. Tile T52 generated a cache misses for the address 0x34120568 and tile T3 generated an L1 cache miss on the address 0xA02359A0. Where are these addresses mapped in TCMP?

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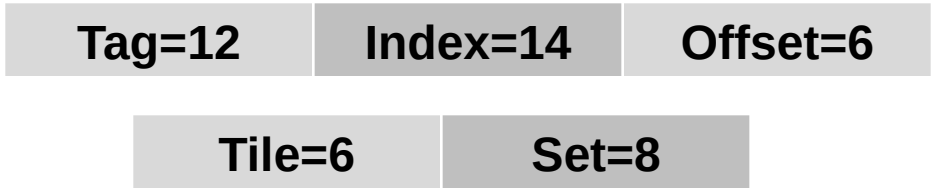
- Total L2- cache 16 MB, 64B block, 16 way
- #sets = $2^{24}/(2^6 \times 2^4) = 2^{14}$

  → 14 bits index.



TCMP Address Mapping

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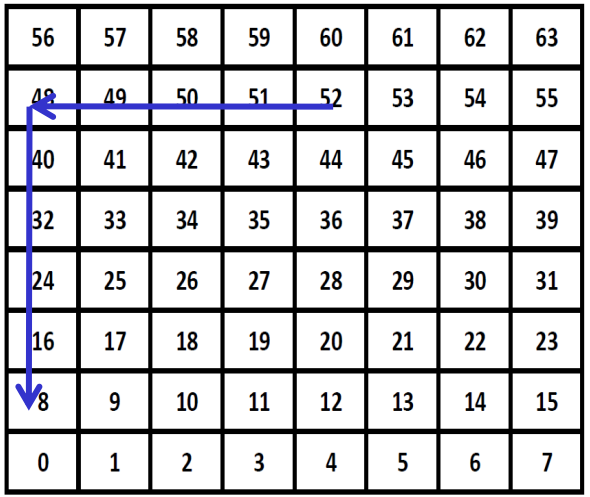
Tag=12	Index=14	Offset=6

Tile=6	Set=8

- Total L2- cache 16 MB, 64B block, 16 way
- #sets = 2^{14} → 14 bits index.
- **0x34120568 → 0x34120568**
- **0010 0000 0101 0110 1000**
- **0010 0000 0101 0110 1000**
- Tile 8 (T8) : Packet from T52 to T8



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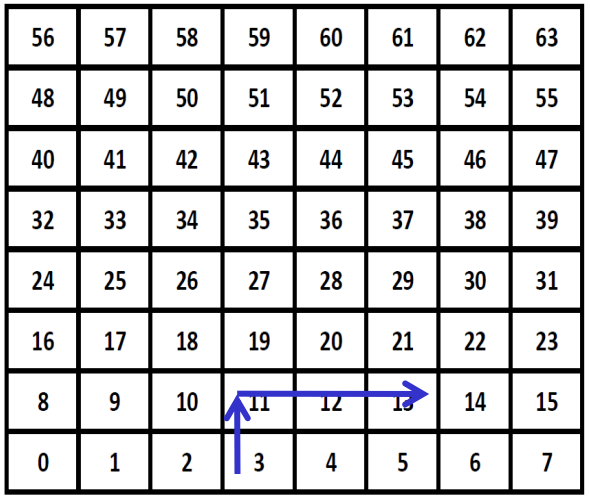
- Total L2- cache 16 MB, 64B block, 16 way
- #sets = 2^{14} → 14 bits index.
- **0xA02359A0 → 0xA02359A0**
- **0011 0101 1001 1010 0000**
- **0011 0101 1001 1010 0000**
- Tile 13 (T13) : Packet from T3 to T13



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