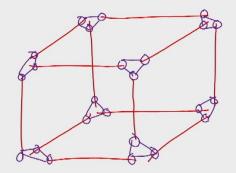
Recursive Structure Take an r-D Bfly Remove the rth col (a) (b) (b) (c) (c) (c) (d) Recursive Structure Take an Y-D Bfly 20 Remove the rth at 20

Wrapped Butterfly fusing the oth column & the rth column

Butterfly with the rows collapsed gives a hypercube Wrapped Butterfly is Hamiltonian

Cube Connected Cycle



3-D hypercube to 3-D CCC

Replace every hypercube node with a cycle of r hodes the hyper cube edges remain

(1) (b) (2) (c) (g)

if hode w & node w'
differ exactly in the
ith bit
then the ith vertex of cycle w

& ith vertex of cycle w'
are adjacent.

(w, i) typerale (w', i)

Where w & w' differ in ith lit

8 only in ith lit

(w, i) = (mod r)

each vertex has a degree of 3. Every hyper cube algorithm

that mus in T sleps Can be simulated on a CCC of dimension r un O(tr) Close relationship between a CCC and wrapped bfly CCC Wrapped bfly $\langle w,i \rangle$ $\langle w,i \rangle$ $\langle w,i \rangle$ $\langle w,i+1 \rangle$ $\langle w,i+1 \rangle$ $\langle w,i+1 \rangle$ An algorithm that nins in T sleps on CCC (resp. Woffy) can be run in O(T) steps on whfly (resp. ccc)

Butterfly ne twok

< w, 0> -(w, o)

agree on the ith bit

agree on the ith bit

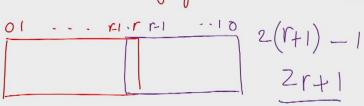
take the straight edge between

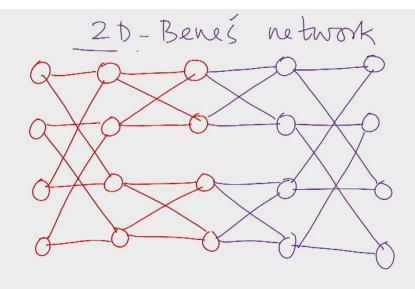
Columns if i+1

The diameter of a r-D bfly is O(r)The bisection width of an log N-dimensional bfly is $\Theta(N|\log N)$

Beneš Network

Paste two butterfligs back to back





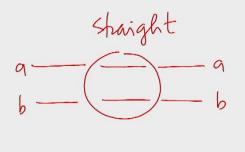
4 5 2 2 9 9

Rearrangeable Network

A network with n inputs & noutputs is a Reanaugeable network if for any permutation π of $\{1,...,n\}$, we can construct edge disjoint paths that connect input i to output π (i). for $1 \le i \le n$.

(4) (b) (2) (9) (9)

A Beneš Network is a rearrangeable network -----every node is a reconfigurable Switch



(4) (b) (2) (c) (g) (g)

r_D Beneš network has 2" inputs & 2" ontputs

Hypothesis

every (r-1) Dimensional Benes

network is

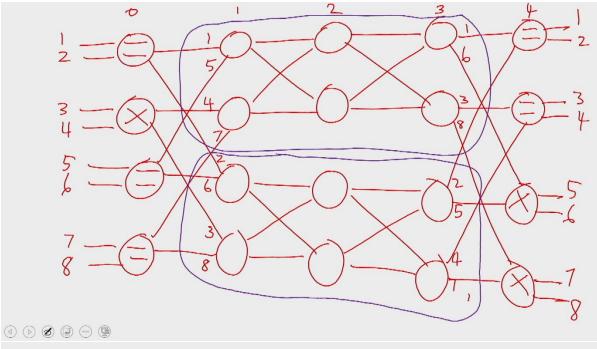
rearrangeable

Step

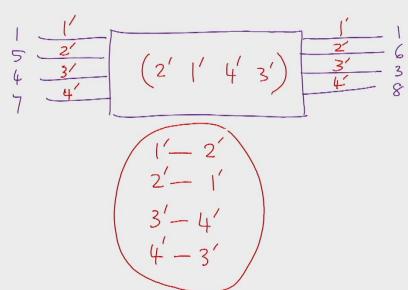
Consider II

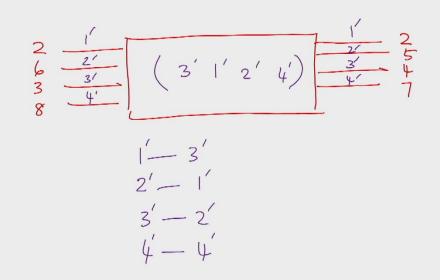
i 1 2 3 4 5 6 7 8

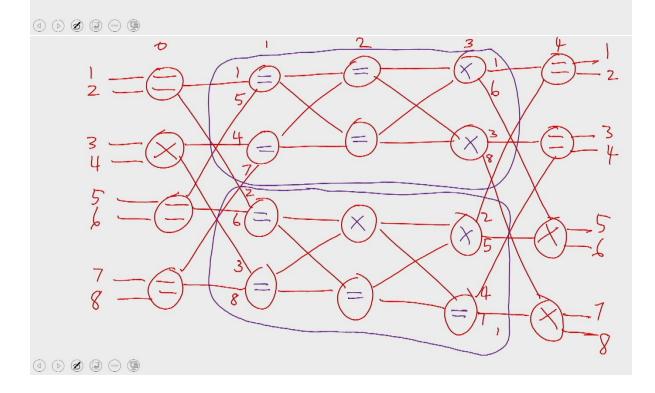
T(i) 6 4 5 8 1 2 3 7



(1) (b) (2) (c) (g)







Start any node i on the input side

Say i is paixed with i' choose a config. for the switch to which i & i' are connected = or x

(1) (b) (2) (d) (e) (e)

we know the half of input i.
Output T(i) should be connected to the same half
This gives as the configur for the switch T(i) is connected

Continue with the pair of T(i)

TT'(T(i)')

until we get back to the switch

to which input is

Connected.

④ ▷ Ø ඔ ◎ 몧

Why would we loop back?