भारतीय सूचना प्रौद्यागेकी संस्थान, नागपुर

Indian Institute of Information Technology, Nagpur

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Department of Electronics and Communication Engineering

Complementary Metal-Oxide Semiconductor (CMOS)

Project Title: Two-bit Carry Bypass Adder Design by using Universal Nand Gate Using CMOS Technology(90nm).

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Subject: CMOS

1. Introduction

In digital arithmetic, adders play a vital role in the design of arithmetic logic units (ALUs). Among various adder architectures, the Carry Skip Adder (CSA) provides an efficient trade-off between speed and complexity, reducing delay compared to Ripple Carry Adders (RCAs). This report presents the design and simulation of a Carry Skip Adder using CMOS technology (90nm) in Microwind, with a Full Adder constructed using only NAND gates—highlighting the universal gate's ability to simplify manufacturing and optimize transistor-level design.

2. Objective

- To design a Carry Skip Adder in Microwind using 90nm CMOS technology.
- To implement Full Adder logic solely with NAND gates.
- To compare the designed CSA with other adder architectures (RCA, Carry Look-Ahead Adder) in terms of delay, area, and power.

3. Design Methodology

3.1 NAND-Based Full Adder Design

A Full Adder has three inputs: A, B, Cin, and two outputs: Sum and Cout.

The Boolean expressions are:

- Sum = $A \oplus B \oplus Cin$
- Cout = $(A \cdot B) + (Cin \cdot (A \oplus B))$

Using NAND gates only:

- XOR using NANDs:
- $A \oplus B =$ (A NAND (A NAND B)) NAND (B NAND (A NAND B))
- Microwind logic schematic composed of 10-15 NAND gate stages for a single full adder.

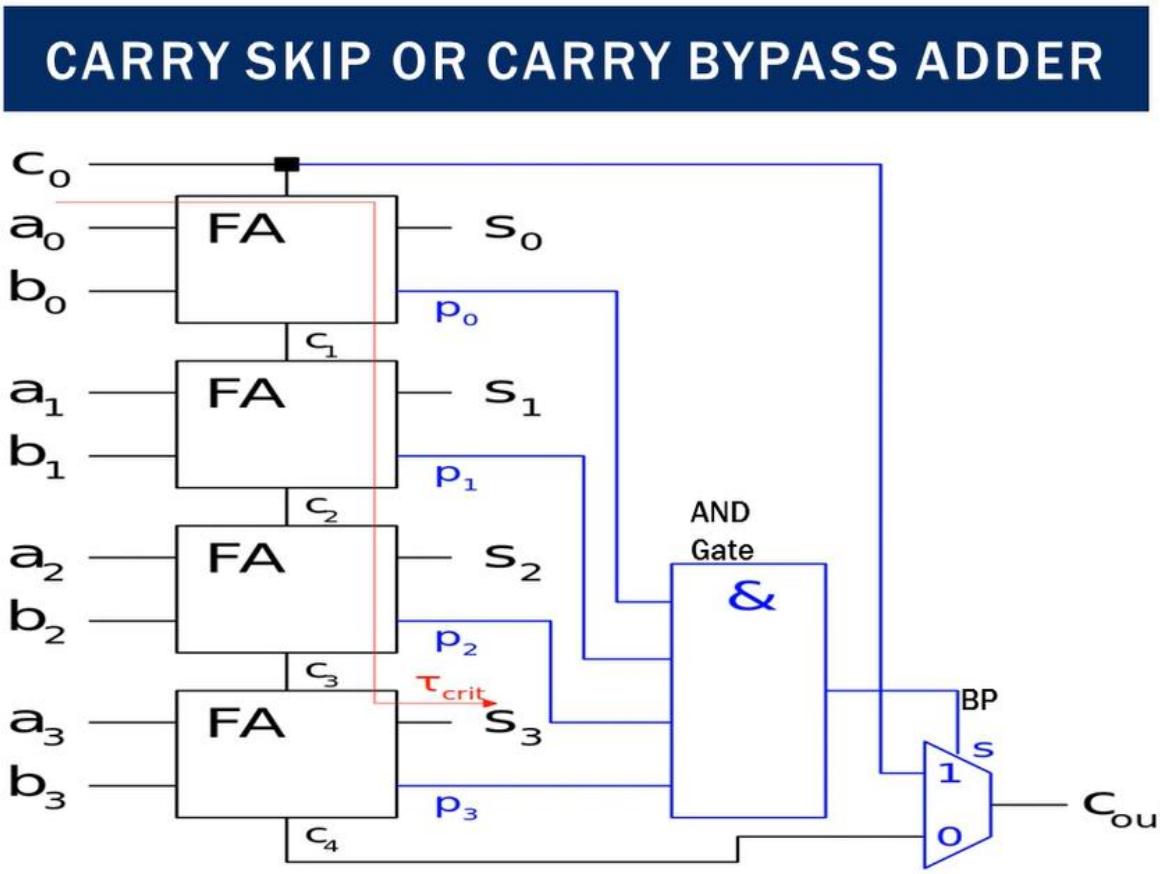
3.2 Carry Skip Adder (CSA)

- Groups of full adders are divided into blocks
- A skip logic (propagate logic) determines if carry can skip the block
- Propagate signal: Pi = Ai $\oplus$ Bi
- If all P[i] in block = 1, carry skips to next block directly
- Reduces critical path delay compared to RCA.

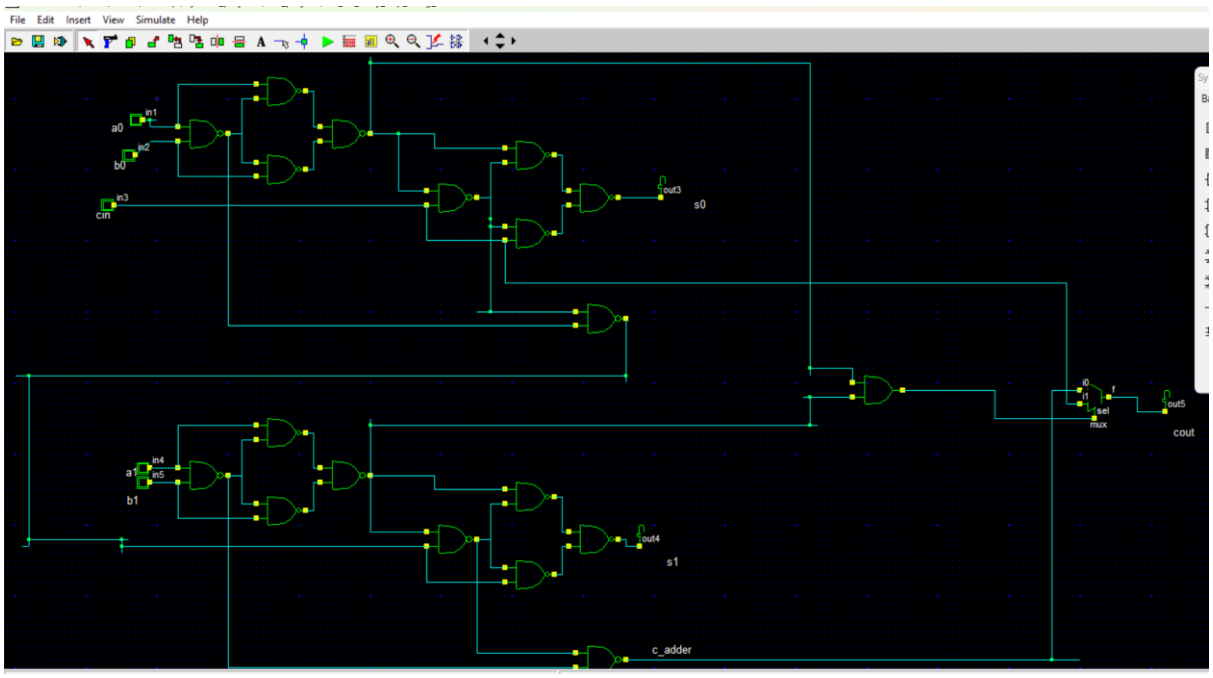
3.3 CMOS Layout in Microwind

- Used 90nm CMOS technology
- Implemented NAND gate design using PMOS and NMOS transistor combinations
- Designed Full Adder module, connected to form CSA block
- Verified functionality using timing simulations and logic analyzer.

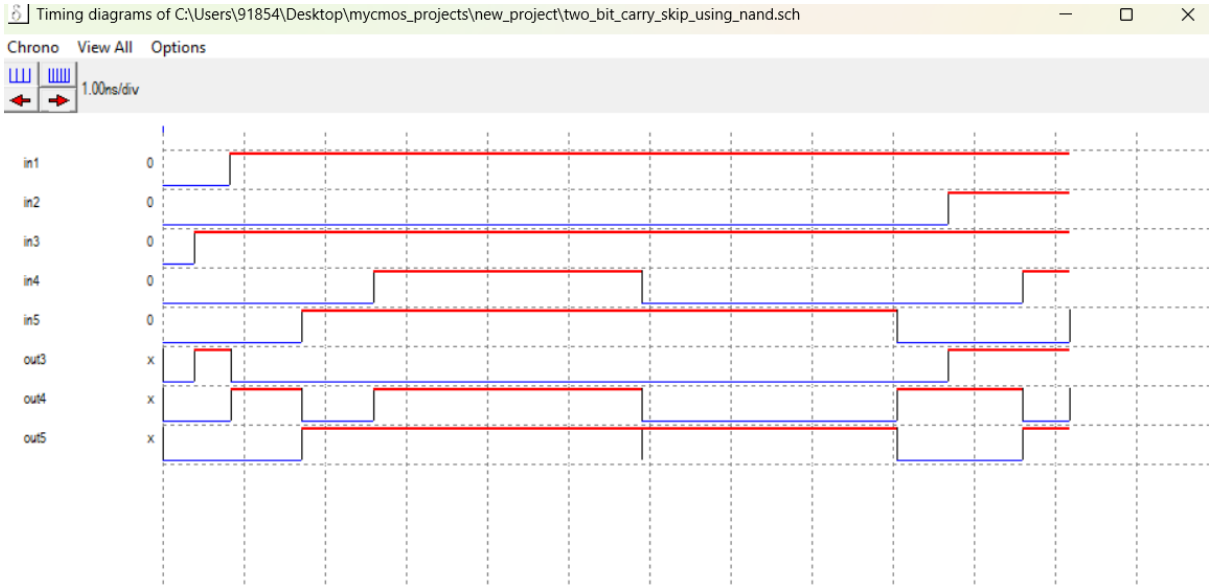
3. Circuit Diagram



4. DSCH SCHEMATIC DIAGRAM



DSCH_OUTPUT



5. NETLIST

two_bit carry skip adder using nand gate in 90nm cmos technology

.model pmod pmos level=54 version=4.7

.model nmod nmos level=54 version=4.7

.subckt nand_two a b out vdd vss

m1 out a vdd vdd pmod w=200u l=10u

m2 out b vdd vdd pmod w=200u l=10u

m3 out a net1 net1 nmod w=200u l=10u

m4 net1 b vss vss nmod w=200u l=10u

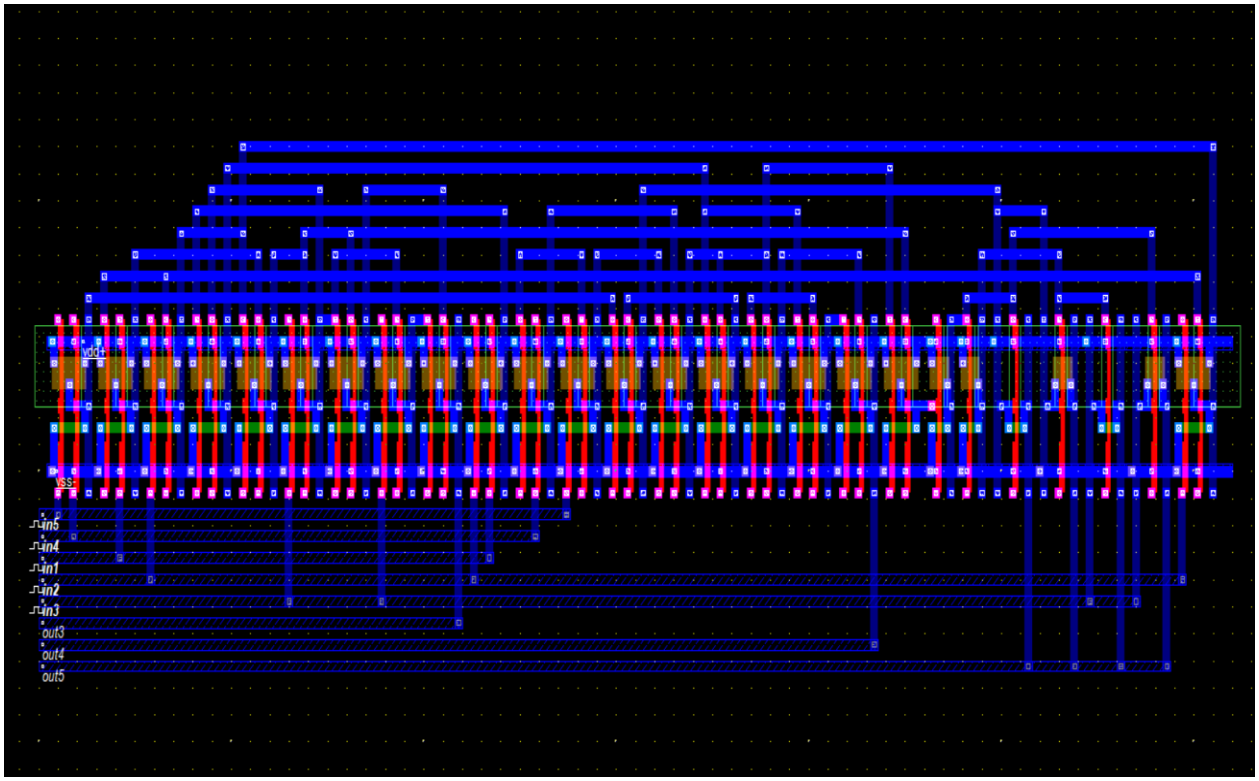
.ends

.subckt cmos_inver in out vdd vss

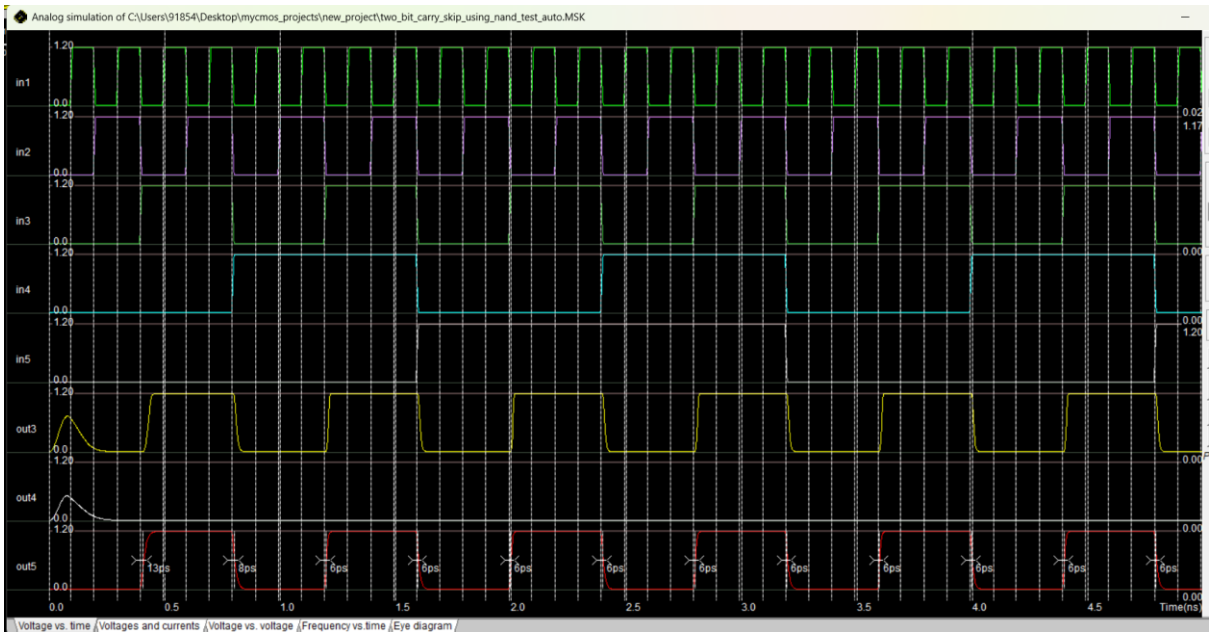
```
m1 out in vdd vdd pmod w=200u l=10u
m2 out in vss vss nmod w=100u l=10u
.ends

.subckt two_mux s_bar i0 s i1 out vdd vss
m1 n1 s_bar vdd vdd pmod w=400u l=10u
m2 n1 i0 vdd vdd pmod w=400u l=10u
m3 out s n1 n1 pmod w=400u l=10u
m4 out i1 n1 n1 pmod w=400u l=10u
m5 out s_bar n2 n2 nmod w=200u l=10u
m6 n2 i0 vss vss nmod w=200u l=10u
m7 out s n3 n3 nmod w=200u l=10u
m8 n3 i1 vss vss nmod w=200u l=10u
.ends

.subckt full_add a b cin sum cout p_out vdd vss
x1 a b n1 vdd vss nand_two
x2 a n1 n2 vdd vss nand_two
x3 n1 b n3 vdd vss nand_two
x4 n2 n3 p_out vdd vss nand_two
x5 p_out cin n4 vdd vss nand_two
x6 n4 p_out n5 vdd vss nand_two
x7 cin n4 n6 vdd vss nand_two
x8 n5 n6 sum vdd vss nand_two
```

```
x9 n4 n1 cout vdd vss nand_two
.ends

va0 25 0 pulse (0 1.8 0 1n 1n 10n 20n)
va1 26 0 pulse (0 1.8 0 1n 1n 20n 40n)
vb0 27 0 pulse (0 1.8 0 1n 1n 40n 80n)
vb1 28 0 pulse (0 1.8 0 1n 1n 80n 160n)
vcin 29 0 dc 0v
vdd 3 0 dc 1.8v

xfa1 25 27 29 32 30 34 3 0 full_add
xfa2 26 28 30 33 31 35 3 0 full_add
xn1 34 35 36 3 0 nand_two
xinv_top 36 37 3 0 cmos_inver
xmux_top 36 31 37 29 38 3 0 two_mux
.tran 0.1n 300n
.control
run
plot v(25) v(26) v(27) v(28) v(32) v(33) v(38)
.endc
.end
```

6. Generated layout



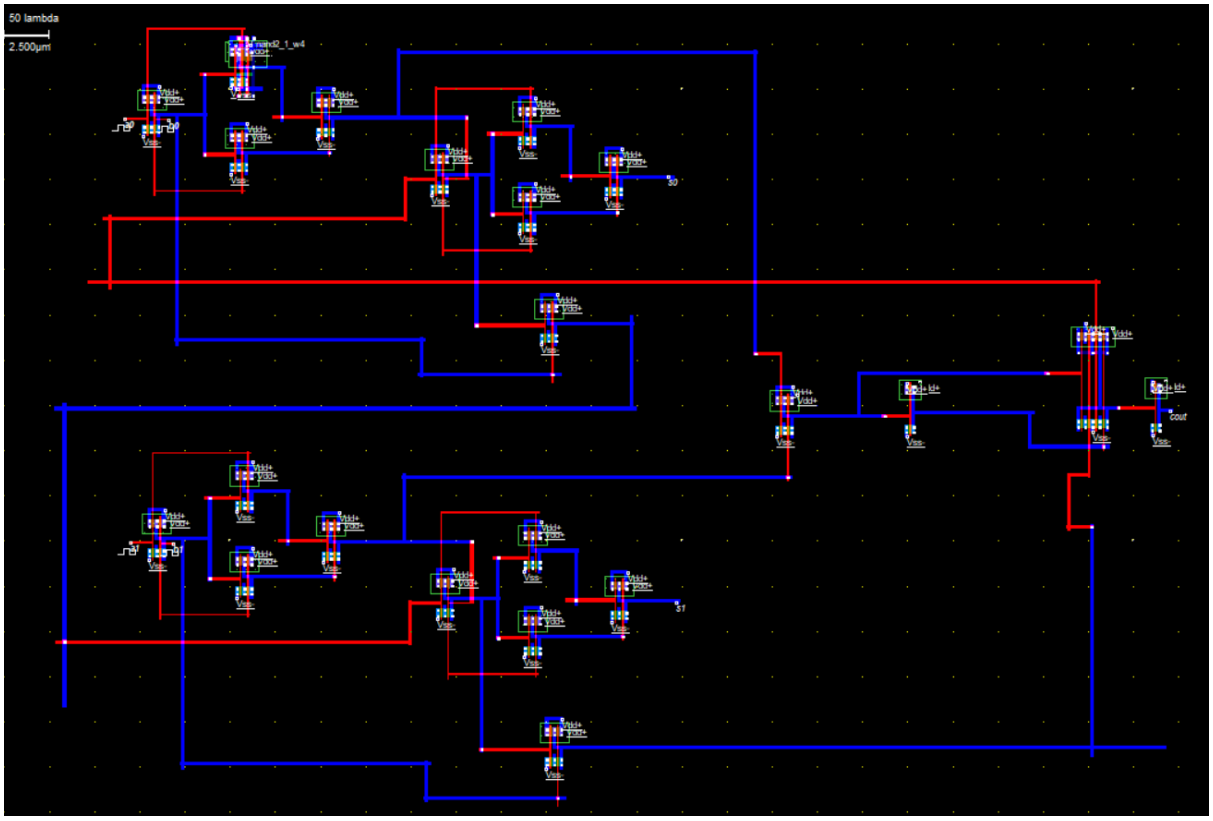
7. Auto Simulated



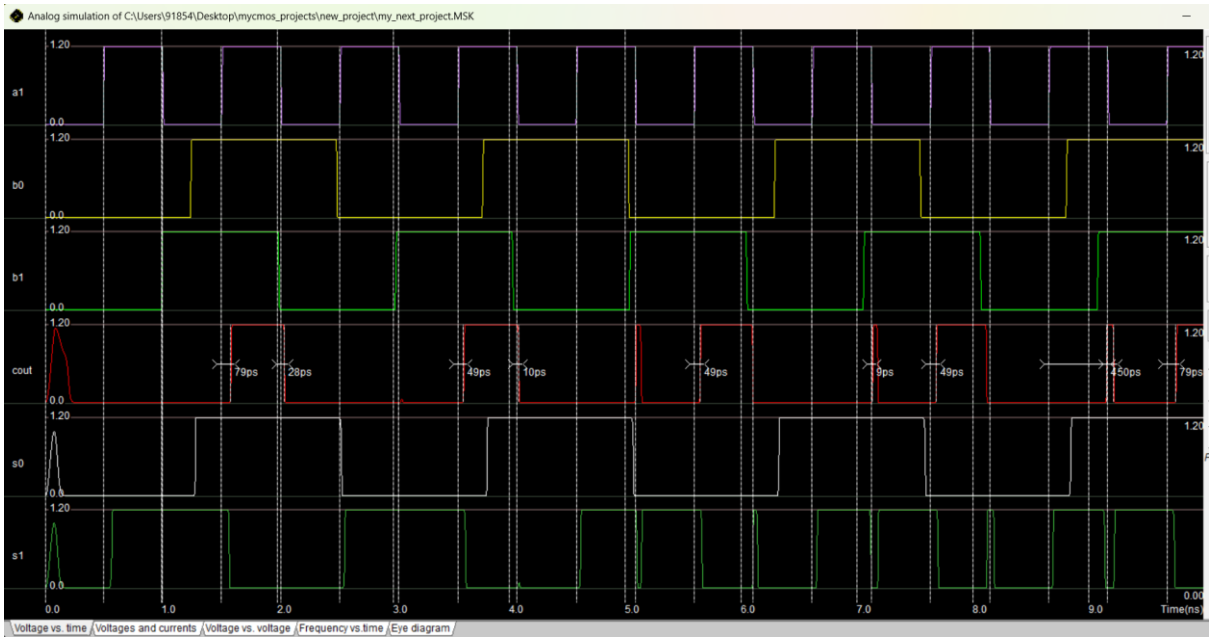
8. problems

Here Area is about 18.9% area used which makes size bigger of chip and create delay too.

9.Self_Layout_design



10.Simulated_output



11. Advantages of NAND-Only Design

- NAND is a universal gate, hence simplifies manufacturing
- Reduces standard cell library requirements
- Offers uniform transistor sizing
- Good for educational and academic implementations

4. Simulation and Results

Parameter	Ripple Carry Adder	Carry Skip Adder	Carry Look-Ahead Adder
Propagation Delay	High (~15ns)	Moderate (~8ns)	Low (~5ns)
Area (Microwind)	Low	Medium	High
Power Consumption	Low	Medium	High
Gate Count (for 4-bit)	16 Full Adders	16 FA + Skip	Complex logic
NAND Usage	Not fixed	Only NAND	Multi-gate

10. Applications

Carry Skip Adders (CSAs) are used in digital systems that require fast and efficient binary addition with moderate hardware complexity. The applications of the designed NAND-based CSA include**:**

1. **Arithmetic Logic Units (ALUs):**
    - Used in CPUs and DSPs for arithmetic operations.

- Offers a balance between delay and resource utilization.

2. **Embedded Systems:**
   - Suitable for low-power microcontrollers and IoT devices.
   - Efficient for tasks that require moderate-speed arithmetic.
3. **Digital Signal Processing (DSP):**
   - Used in filters, FFTs, and convolvers where addition speed is crucial.
   - Reduces computation bottlenecks in fixed-point operations**.**
4. **Image and Video Processing Units:**
   - Performs fast pixel-wise addition in hardware accelerators.
   - Useful in histogram equalization, blending, and filtering**.**
5. **Cryptographic Hardware:**
   - Fast adders are critical in algorithms like RSA, AES, ECC.
   - CSA offers secure and fast modular arithmetic support**.**

7. Conclusion

The Carry Skip Adder designed using NAND-only Full Adders in 90nm CMOS via Microwind offers a balanced trade-off between speed and complexity. This design is ideal for mid-performance, low-power ALU subsystems where delay is critical but full Carry Look-Ahead logic is too costly.