Digital Design and Computer Organisation Laboratory

UE22CS251A

3rd Semester, Academic Year 2023-24

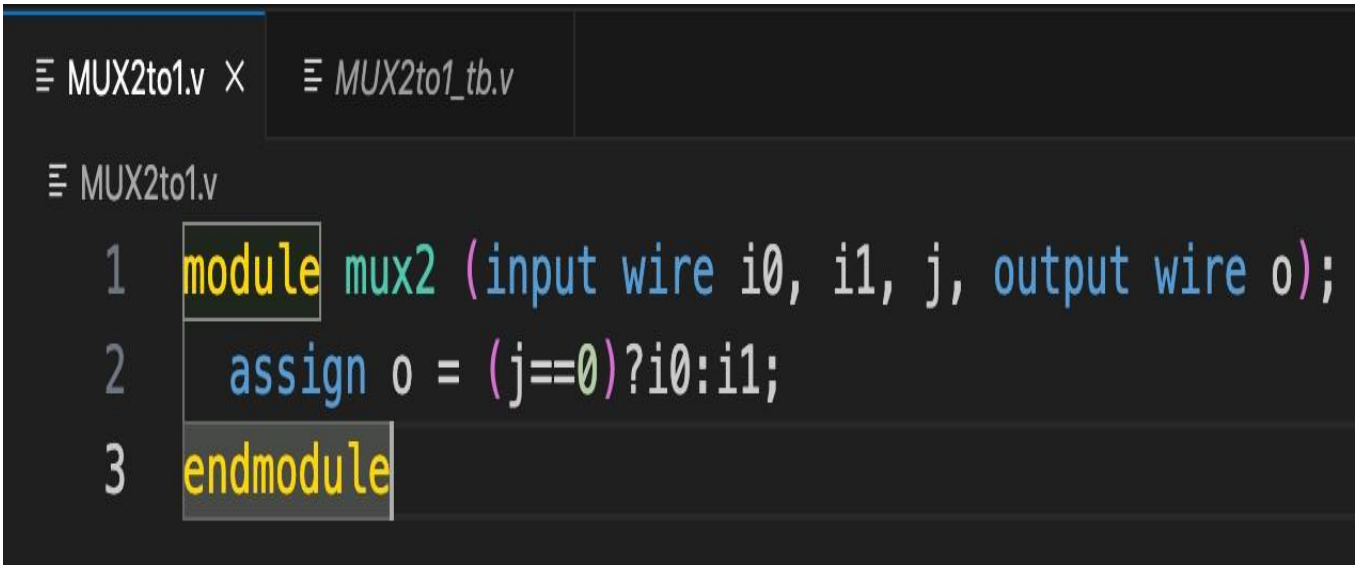
Date: 09/09/2024

Name: ABHISHEK P	SRN: PES2UG23AM002	Section: A

Week#____4_____ Program Number:_____1____

TITLE:

WRITE A VERILOG PROGRAM TO MODEL A 2: 1 MULTIPLEXER. GENERATE THE VVP OUTPUT AND SIMULATION WAVEFORM USING GTKWAVE. VERIFY THE OUTPUT AND WAVEFORM WITH THE TRUTH TABLE

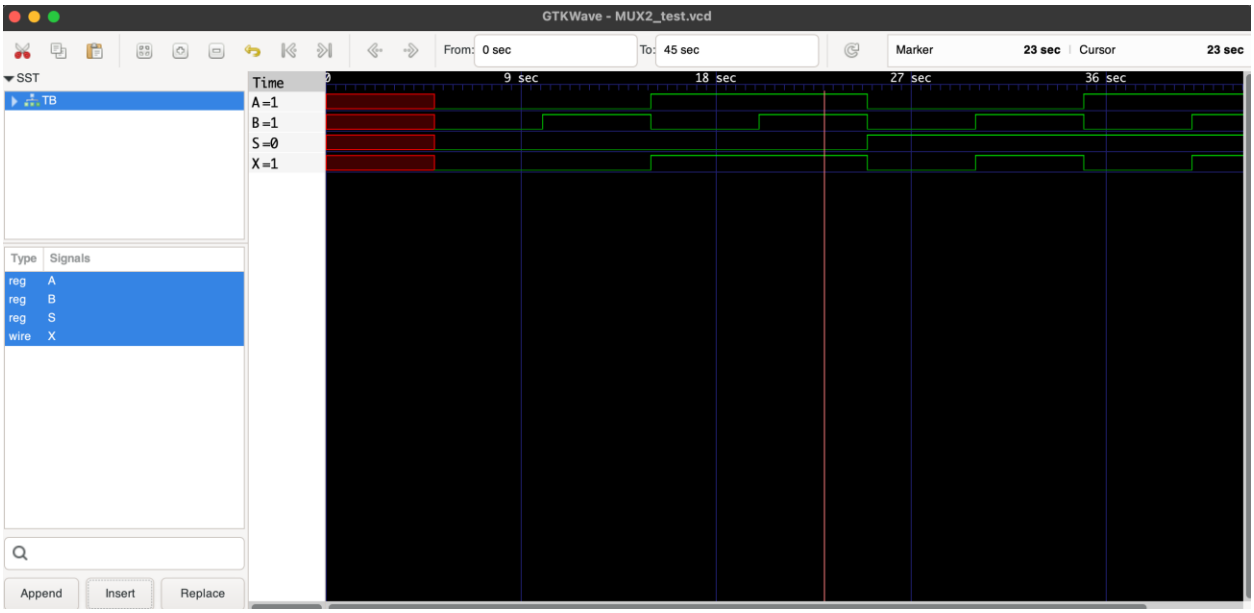


MUX2to1.v | MUX2to1_tb.v

MUX2to1_tb.v

```
module TB;
reg A,B,S;
wire X;
initial
begin
$dumpfile("MUX2_test.vcd");
$dumpvars(0,TB);
end
mux2 newMUX(.i0(A), .i1(B), .j(S), .o(X));
initial
begin
#5 S = 1'b0;
A = 1'b0;
B = 1'b0;
#5 S = 1'b0;A = 1'b0;
B = 1'b1;
#5
S = 1'b0;A = 1'b1;
B = 1'b0;
#5
S = 1'b0;A = 1'b1;
B = 1'b1;
#5
 S = 1'b1;
A = 1'b0;
B = 1'b0;
#5
 S = 1'b1;A = 1'b0;
B = 1'b1;
#5
 S = 1'b1;A = 1'b1;
B = 1'b0;
#5
 S=1'b1;A = 1'b1;
B = 1'b1;
#5;
end
always@(A or B or S)
$monitor("At time = %t,S=%b, A=%b, B=%b,Output = %b",$time,S,A,B, X);
endmodule
```

```
abhishekp@Abhisheks-MacBook-Air-3 ~ % cd Downloads
abhishekp@Abhisheks-MacBook-Air-3 Downloads % cd verilog
abhishekp@Abhisheks-MacBook-Air-3 verilog % iverilog -o dsn MUX2to1_tb.v MUX2to1.v
abhishekp@Abhisheks-MacBook-Air-3 verilog % vvp dsn
VCD info: dumpfile MUX2_test.vcd opened for output.
At time =                    5,S=0, A=0, B=0,Output = 0
At time =                   10,S=0, A=0, B=1,Output = 0
At time =                   15,S=0, A=1, B=0,Output = 1
At time =                   20,S=0, A=1, B=1,Output = 1
At time =                   25,S=1, A=0, B=0,Output = 0
At time =                   30,S=1, A=0, B=1,Output = 1
At time =                   35,S=1, A=1, B=0,Output = 0
At time =                   40,S=1, A=1, B=1,Output = 1
abhishekp@Abhisheks-MacBook-Air-3 verilog % gtkwave MUX2_test.vcd
```



Digital Design and Computer Organisation Laboratory

UE22CS251A

3rd Semester, Academic Year 2023-24

Date: 09/09/2024

Name: ABHISHEK P	SRN: PES2UG23AM002	Section: A

Week#____4_____ Program Number:_____2____

TITLE :

WRITE A VERILOG PROGRAM TO MODEL A 4:1 MULTIPLEXER USING 2:1 MULTIPLEXERS. GENERATE THE VVP OUTPUT AND SIMULATION WAVEFORM USING GTKWAVE. VERIFY THE OUTPUT AND WAVEFORM WITH THE TRUTH TABLE

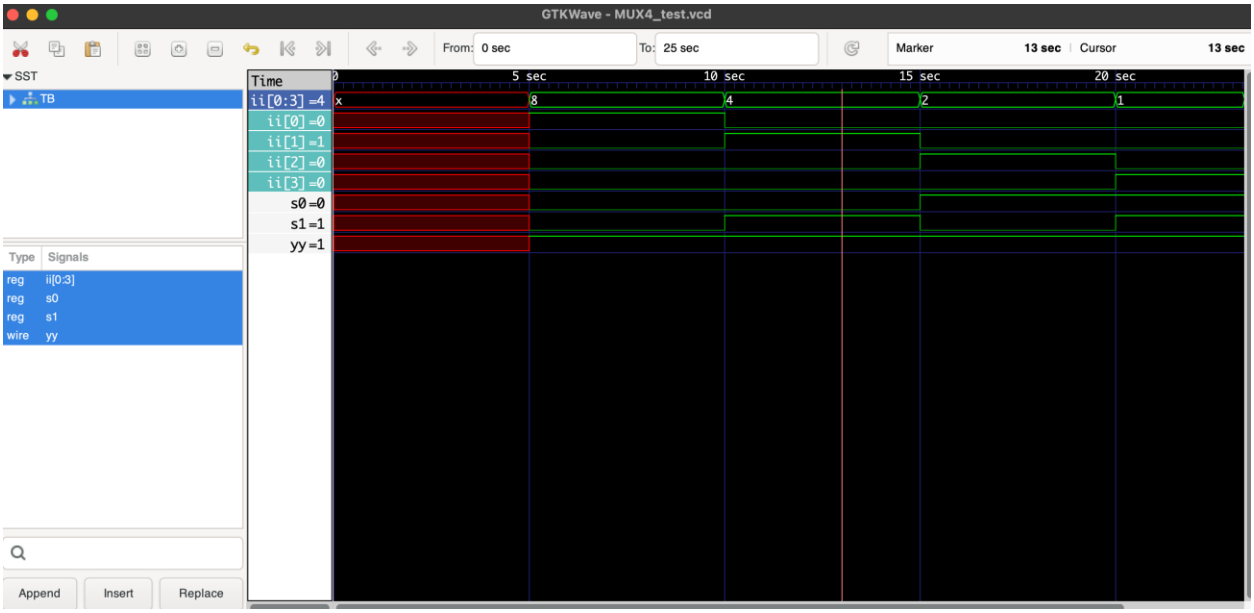
MUX4to1.v

```
1  module mux4 (input wire [0:3] i, input wire j1, j0, output wire o);
2    wire  t0, t1;
3    mux2 mux2_0 (i[0], i[1], j1, t0);
4    mux2 mux2_1 (i[2], i[3], j1, t1);
5    mux2 mux2_2 (t0, t1, j0, o);
6  endmodule
```

tb_MUX4to1.v

```
module TB;
reg [0:3]ii;
reg s0;
reg s1;
wire yy;
initial
begin
$dumpfile("MUX4_test.vcd");
$dumpvars(0, TB);
end
mux4 newMUX(.i(ii), .j0(s0),.j1(s1),.o(yy));
initial
begin
#5
      ii = 4'b1000;
s0=1'b0;
s1=1'b0;
#5
ii= 4'b0100;
s0=1'b0;
s1=1'b1;
#5
      ii = 4'b0010;
s0=1'b1;
s1=1'b0;
#5
      ii = 4'b0001;
s0=1'b1;
s1=1'b1;
#5;
end
always@(ii or s0 or s1)
$monitor("At time = %t,Inputs=%b, s0=%b, s1=%b,Output = %b",$time,ii,s0,s1, yy);
endmodule
```

```
abhishekp@Abhisheks-MacBook-Air-3 verilog % iverilog -o dsn MUX2to1.v MUX4to1.v tb_MUX4to1.v
abhishekp@Abhisheks-MacBook-Air-3 verilog % vvp dsn
VCD info: dumpfile MUX4_test.vcd opened for output.
At time =                    5,Inputs=1000, s0=0, s1=0,Output = 1
At time =                   10,Inputs=0100, s0=0, s1=1,Output = 1
At time =                   15,Inputs=0010, s0=1, s1=0,Output = 1
At time =                   20,Inputs=0001, s0=1, s1=1,Output = 1
abhishekp@Abhisheks-MacBook-Air-3 verilog % gtkwave MUX4_test.vcd
```



Digital Design and Computer Organisation Laboratory

UE22CS251A

3rd Semester, Academic Year 2023-24

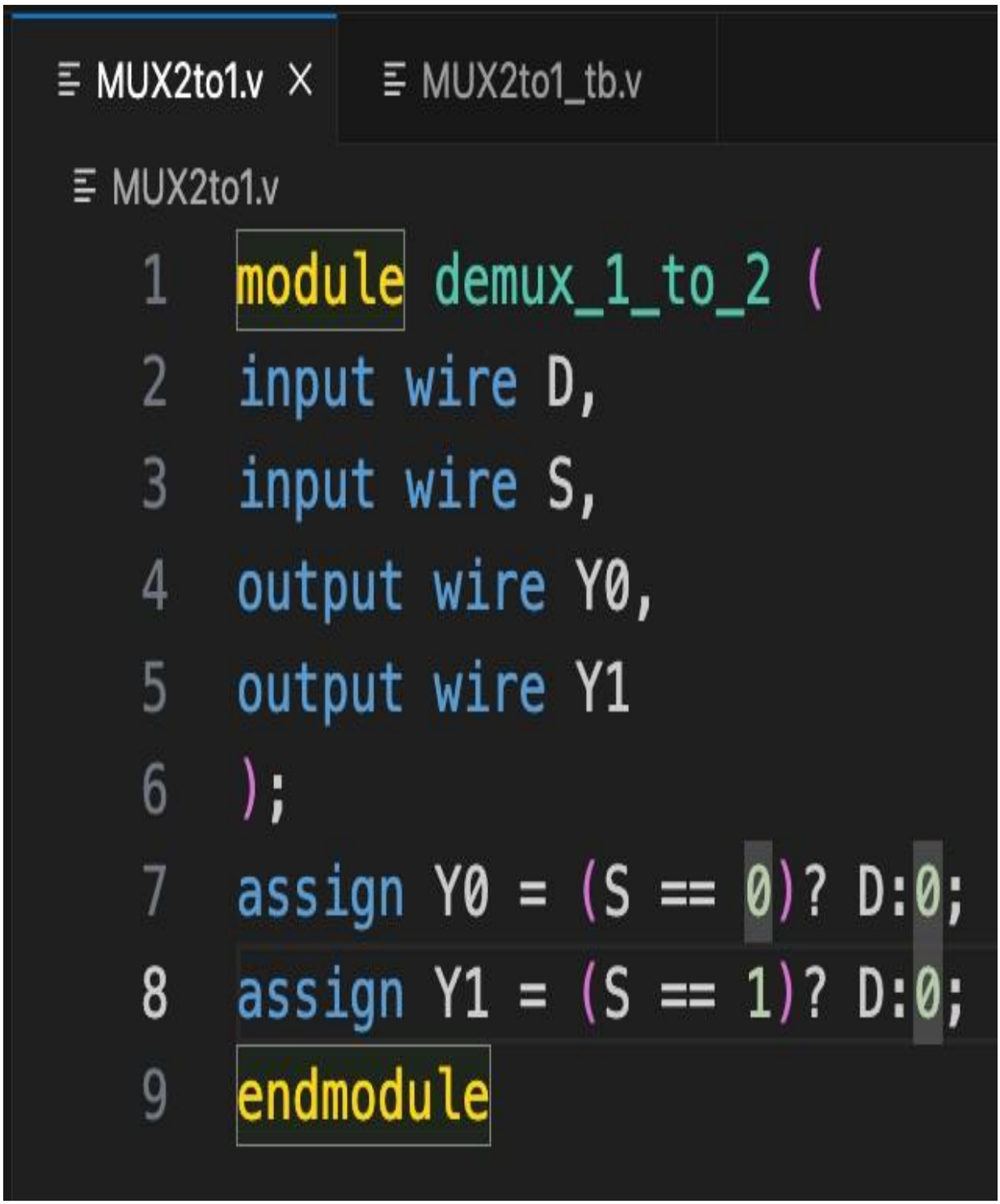
Date: 09/09/2024

Name: ABHISHEK P	SRN: PES2UG23AM002	Section: A

Week#____4_____ Program Number:_____3____

TITLE:

WRITE A VERILOG PROGRAM TO MODEL A 1:2 DEMULTIPLEXER.GENERATE THE VVP OUTPUT AND SIMULATION WAVEFORM USING GTKWAVE. VERIFY THE OUTPUT AND WAVEFORM WITH THE TRUTH TABLE

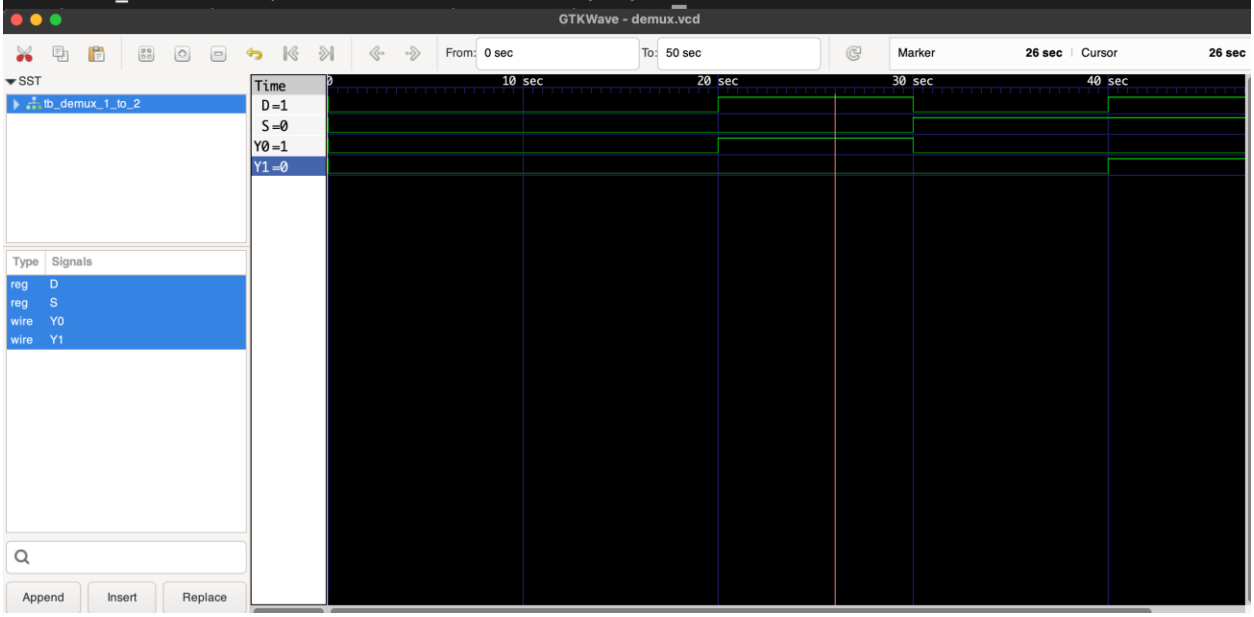

MUX2to1.v
MUX2to1_tb.v
MUX2to1.v
1 module demux_1_to_2 (
2 input wire D,
3 input wire S,
4 output wire Y0,
5 output wire Y1
6);
7 assign Y0 = (S == 0)? D:0;
8 assign Y1 = (S == 1)? D:0;
9 endmodule

MUX2to1.v | MUX2to1_tb.v ×

MUX2to1_tb.v

```
module tb_demux_1_to_2;
reg D;
reg S;
wire Y0;
wire Y1;
demux_1_to_2 uut (
.D(D),
.S(S),
.Y0(Y0),
.Y1(Y1)
);
initial begin
D = 0; S = 0;
#10;
D = 0; S = 0;
#10;
D= 1; S = 0;
#10;
D = 0; S = 1;
#10;
D= 1; S = 1;
#10;
$finish;
end
initial begin
$monitor("Time=%0t D=%b S=%b Y0=%b Y1=%b", $time, D, S, Y0, Y1);
end
initial begin
$dumpfile("demux.vcd");
$dumpvars(0, tb_demux_1_to_2);
end
endmodule
```

```
abhishekp@Abhisheks-MacBook-Air-3 ~ % cd Downloads
abhishekp@Abhisheks-MacBook-Air-3 Downloads % cd verilog
abhishekp@Abhisheks-MacBook-Air-3 verilog % iverilog -o dsn MUX2to1_tb.v MUX2to1.v
abhishekp@Abhisheks-MacBook-Air-3 verilog % vvp dsn
VCD info: dumpfile demux.vcd opened for output.
Time=0 D=0 S=0 Y0=0 Y1=0
Time=20 D=1 S=0 Y0=1 Y1=0
Time=30 D=0 S=1 Y0=0 Y1=0
Time=40 D=1 S=1 Y0=0 Y1=1
MUX2to1_tb.v:23: $finish called at 50 (1s)
```



Digital Design and Computer Organisation Laboratory

UE22CS251A

3rd Semester, Academic Year 2023-24

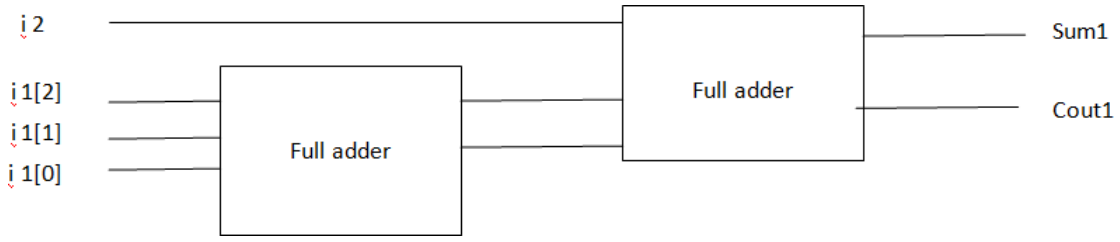
Date: 09/09/2024

Name: ABHISHEK P	SRN: PES2UG23AM002	Section: A

Week#____4_____ Program Number:_____4____

TITLE:

WRITE A VERILOG PROGRAM TO MODEL THE GIVEN CIRCUIT 3.GENERATE THE VVP OUTPUT AND SIMULATION WAVEFORM USING GTKWAVE. VERIFY THE OUTPUT AND WAVEFORM WITH THE TRUTH TABLE



MUX2to1.v × MUX2to1_tb.v

MUX2to1.v

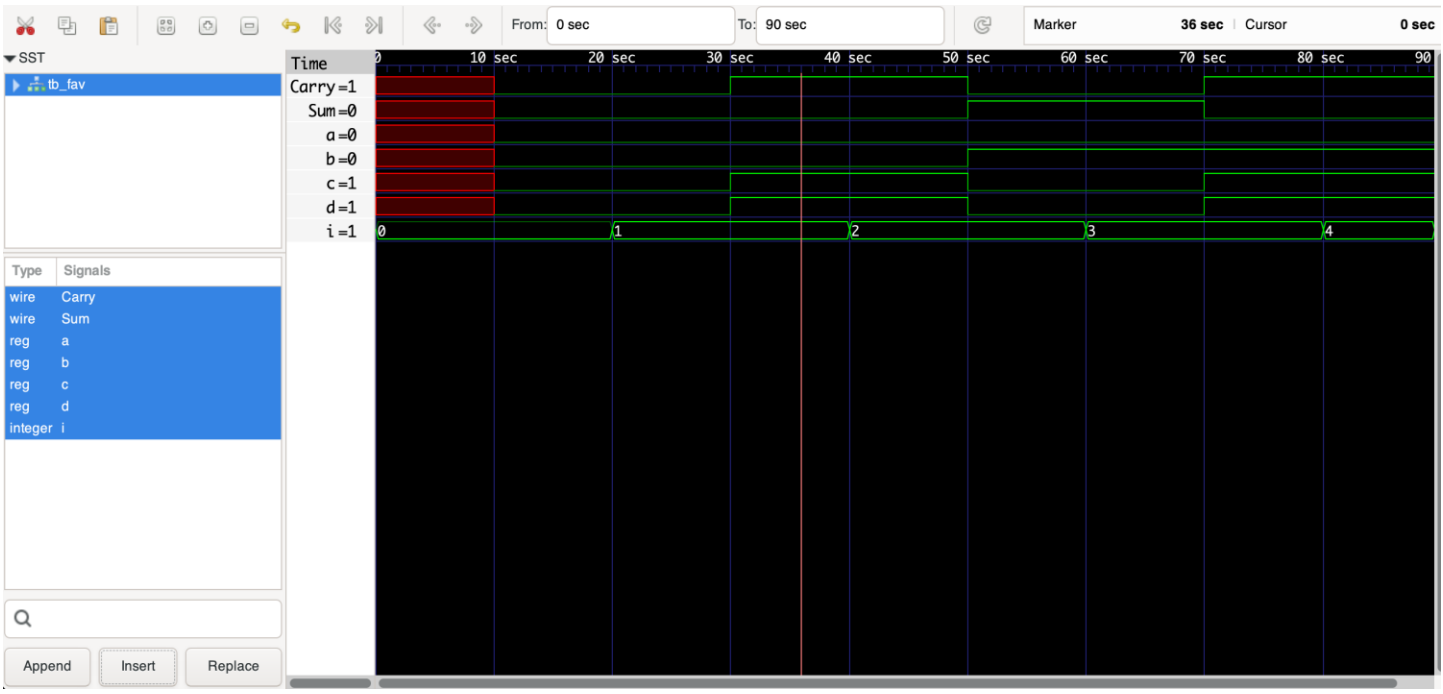
```
1   module andgate(a,b,c);
2   input a,b;
3   output c;
4   assign c=a*b;
5   endmodule
6   module xorgate(a,b,c);
7   input a,b;
8   output c;
9   assign c=a^b;
10  endmodule
11  module orgate(a,b,c);
12  input a,b;
13  output c;
14  assign c=a|b;
15  endmodule
16  module fulladder(a,b,c,sm, co);
17  input a,b,c;
18  output sm,co;
19  wire W1, W2, W3;
20  xorgate F1 (a,b,W1);
21  andgate F2 (a,b,W2);
22  xorgate F3 (W1,c,sm);
23  andgate F4 (W1,c,W3);
24  orgate F5 (W2,W3,co);
25  endmodule
26  module circuit2 (a,b,c,d, sum, carry);
27  input a,b,c,d;
28  output sum, carry;
29  wire ws,wc;
30  fulladder f1 (a,b,c, ws, wo);
31  fulladder f2 (ws, wo,d, sum, carry);
32  endmodule
```

MUX2to1.v | MUX2to1_tb.v

MUX2to1_tb.v

```
1  `define TESTVECS 4
2  module tb_fav;
3  reg a,b,c,d;
4  wire Sum;
5  wire Carry;
6  reg [3:0] test_vecs [0: (`TESTVECS)];
7  integer i;
8  initial begin
9      $dumpfile("fulladderv.vcd");
10     $dumpvars(0, tb_fav);
11 end
12 initial begin
13     test_vecs[0] = 4'b0000;
14     test_vecs[1] = 4'b0011;
15     test_vecs[2] = 4'b0100;
16     test_vecs[3] = 4'b0111;
17 end
18 circuit2 uut(a, b, c, d, Sum, Carry);
19 initial begin
20     for (i = 0; i < (`TESTVECS); i = i + 1) begin
21         #10 {a, b, c, d} = test_vecs[i];
22         $monitor("At time = %t, a = %b, b = %b, c = %b, d = %b, Sum = %b, Carry = %b",
23                  $time, a, b, c, d, Sum, Carry);
24     end
25     #10 $finish;
26 end
27 endmodule
```

```
abhishekp@Abhisheks-MacBook-Air-3 verilog % iverilog -o dsn MUX2to1_tb.v MUX2to1.v
abhishekp@Abhisheks-MacBook-Air-3 verilog % vvp dsn
VCD info: dumpfile fulladderv.vcd opened for output.
At time =                   10, a = 0, b = 0, c = 0, d = 0, Sum = 0, Carry = 0
At time =                   20, a = 0, b = 0, c = 1, d = 1, Sum = 0, Carry = 1
At time =                   30, a = 0, b = 1, c = 0, d = 0, Sum = 1, Carry = 0
At time =                   40, a = 0, b = 1, c = 1, d = 1, Sum = 0, Carry = 1
MUX2to1_tb.v:31: $finish called at 50 (1s)
```



Digital Design and Computer Organisation Laboratory

UE22CS251A

3rd Semester, Academic Year 2023-24

Date: 09/09/2024

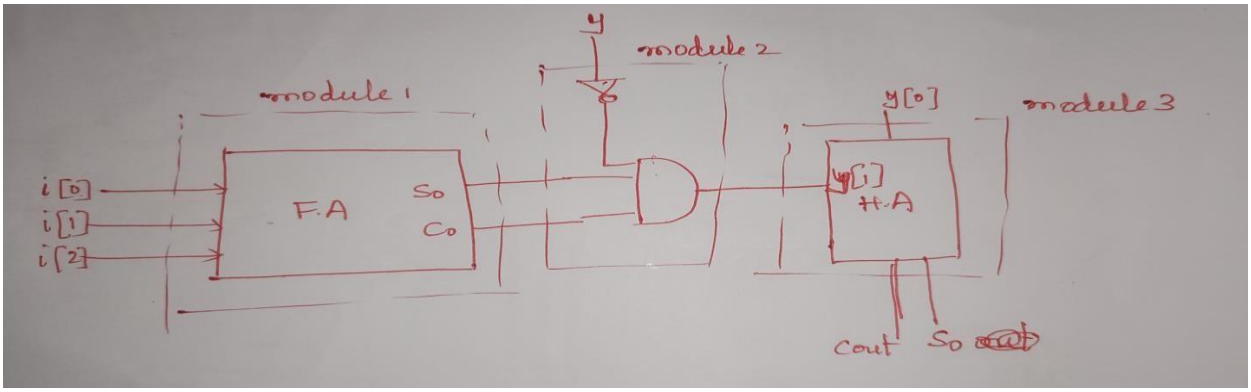
Name: ABHISHEK P	SRN: PES2UG23AM002	Section: A

Week#____4_____ Program Number:_____5____

TITLE:

WRITE A VERILOG PROGRAM TO MODEL THE GIVEN CIRCUIT 4.GENERATE THE VVP OUTPUT AND SIMULATION WAVEFORM USING

GTKWAVE. VERIFY THE OUTPUT AND WAVEFORM WITH THE TRUTH TABLE



MUX2to1.v × MUX2to1_tb.v

MUX2to1.v

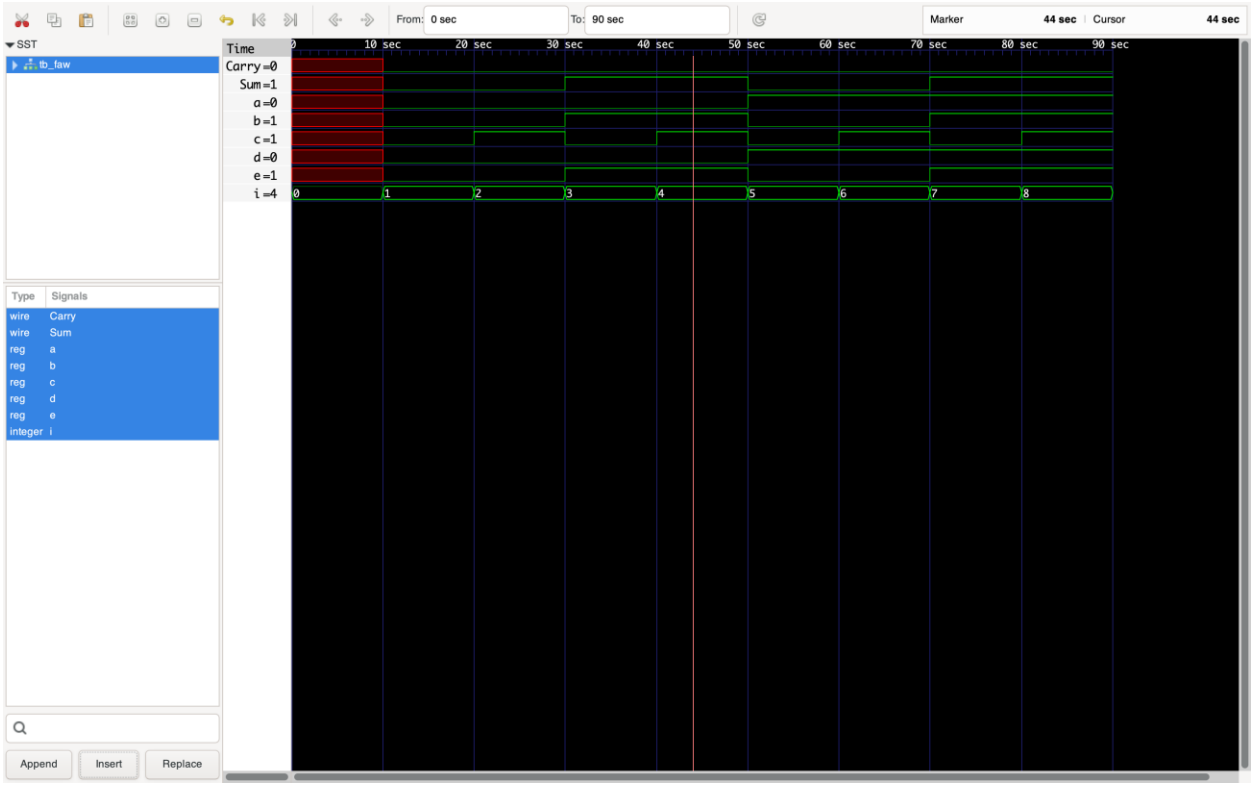
```
module andgate(a,b,c);
input a,b;
output c;
assign c = a * b;
endmodule
module and3gate(a,b,c,d);
input a,b,c;
output d;
assign d = a * b * c;
endmodule
module xorgate(a,b,c);
input a,b;
output c;
assign c = a ^ b;
endmodule
module orgate(a,b,c);
input a,b;
output c;
assign c = a | b;
endmodule
module notgate(
    input a,
    output y
);
assign y = !a;
endmodule
module fulladder (a, b, c, sm, co);
input a, b, c;
output sm, co;
wire W1, W2, W3;
xorgate F1(a, b, W1);
andgate F2(a, b, W2);
xorgate F3(W1, c, sm);
andgate F4(W1, c, W3);
orgate F5(W2, W3, co);
endmodule
module circuit2(a, b, c, d, e, sum, carry);
input a, b, c, d, e;
output sum, carry;
wire ws, wc, w1, W2;
fulladder f1(a, b, c, ws, wc);
notgate n1(d, w1);
and3gate a1(ws, wc, w1, W2);
fulladder f2(W2, e, 1'b0, sum, carry);
endmodule
```

MUX2to1.v | MUX2to1_tb.v

MUX2to1_tb.v

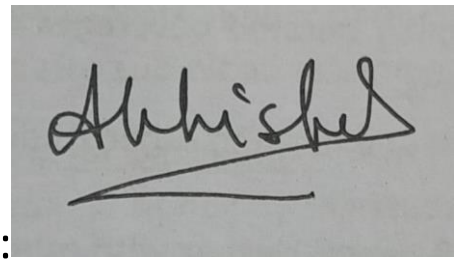
```
1  `define TESTVECS 8
2  module tb_faw;
3  reg a,b,c,d,e;
4  wire Sum;
5  wire Carry;
6  reg [4:0] test_vecs [0: (`TESTVECS-1)];
7  integer i;
8  initial begin
9  $dumpfile("fulladderw.vcd");
10 $dumpvars(0, tb_faw);
11 end
12 initial begin
13 test_vecs[0]= 5'b00000;
14 test_vecs[1]= 5'b00100;
15 test_vecs[2] = 5'b01001;
16 test_vecs[3]= 5'b01101;
17 test_vecs[4]= 5'b10010;
18 test_vecs[5]= 5'b10110;
19 test_vecs[6]= 5'b11011;
20 test_vecs[7]= 5'b11111;
21 end
22
23 circuit2 uut (a,b,c,d,e, Sum, Carry);
24 initial begin
25 for (i = 0; i < (`TESTVECS); i = i + 1) begin
26 #10 {a,b,c,d,e} = test_vecs[i];
27 $monitor("At time=%t, i1[0] %b, i1[1]%b, i1[2]= %b, Y1 = %b, Y2 =%b Sum = %b, Carry %b",
28 $time, a, b, c, d, e, Sum, Carry);
29 end
30 #10 $finish;
31 end
32 endmodule
```

```
abhishekp@Abhisheks-MacBook-Air-3 verilog % iverilog -o dsn MUX2to1_tb.v MUX2to1.v
abhishekp@Abhisheks-MacBook-Air-3 verilog % vvp dsn
VCD info: dumpfile fulladderw.vcd opened for output.
At time=                  10, i1[0] 0, i1[1]0, i1[2]= 0, Y1 = 0, Y2 =0 Sum = 0, Carry 0
At time=                  20, i1[0] 0, i1[1]0, i1[2]= 1, Y1 = 0, Y2 =0 Sum = 0, Carry 0
At time=                  30, i1[0] 0, i1[1]1, i1[2]= 0, Y1 = 0, Y2 =1 Sum = 1, Carry 0
At time=                  40, i1[0] 0, i1[1]1, i1[2]= 1, Y1 = 0, Y2 =1 Sum = 1, Carry 0
At time=                  50, i1[0] 1, i1[1]0, i1[2]= 0, Y1 = 1, Y2 =0 Sum = 0, Carry 0
At time=                  60, i1[0] 1, i1[1]0, i1[2]= 1, Y1 = 1, Y2 =0 Sum = 0, Carry 0
At time=                  70, i1[0] 1, i1[1]1, i1[2]= 0, Y1 = 1, Y2 =1 Sum = 1, Carry 0
At time=                  80, i1[0] 1, i1[1]1, i1[2]= 1, Y1 = 1, Y2 =1 Sum = 1, Carry 0
MUX2to1_tb.v:30: $finish called at 90 (1s)
```



Disclaimer:

- The programs and output submitted is duly written, verified and executed by me.
- I have not copied from any of my peers nor from the external resource such as internet.
- If found plagiarized, I will abide with the disciplinary action of the University.

Signature: 

Name: ABHISHEK P

SRN: PES2UG23AM002
Section: A
Date: 09/09/2024