Digital Design and Computer Organisation Laboratory

UE22CS251A

3rd Semester, Academic Year 2023-24

Name: ABHISHEK P	SRN: PES2UG23AM002	Section: A Date: 01/09/2024

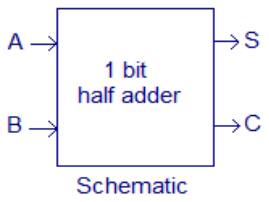
Week#____3_____ Program Number: ____1__

TITLE:

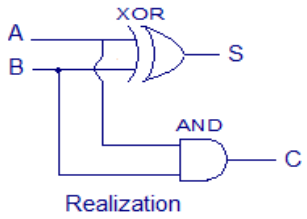
WRITE A VERILOG PROGRAM TO MODEL A HALF ADDER THAT CAN ADD TWO BITS. GENERATE THE VVP OUTPUT AND SIMULATION WAVEFORM USING GTKWAVE. VERIFY THE OUTPUT AND WAVEFORM WITH THE TRUTH TABLE

Inputs		Outputs	
A	B	S	C
0	0	0	0
1	0	1	0
0	1	1	0
1	1	0	1

Truth table



Schematic



Realization

Digital Design and Computer Organisation Laboratory

UE22CS251A

3rd Semester, Academic Year 2023-24

fulladd_tb.v | fulladd.v

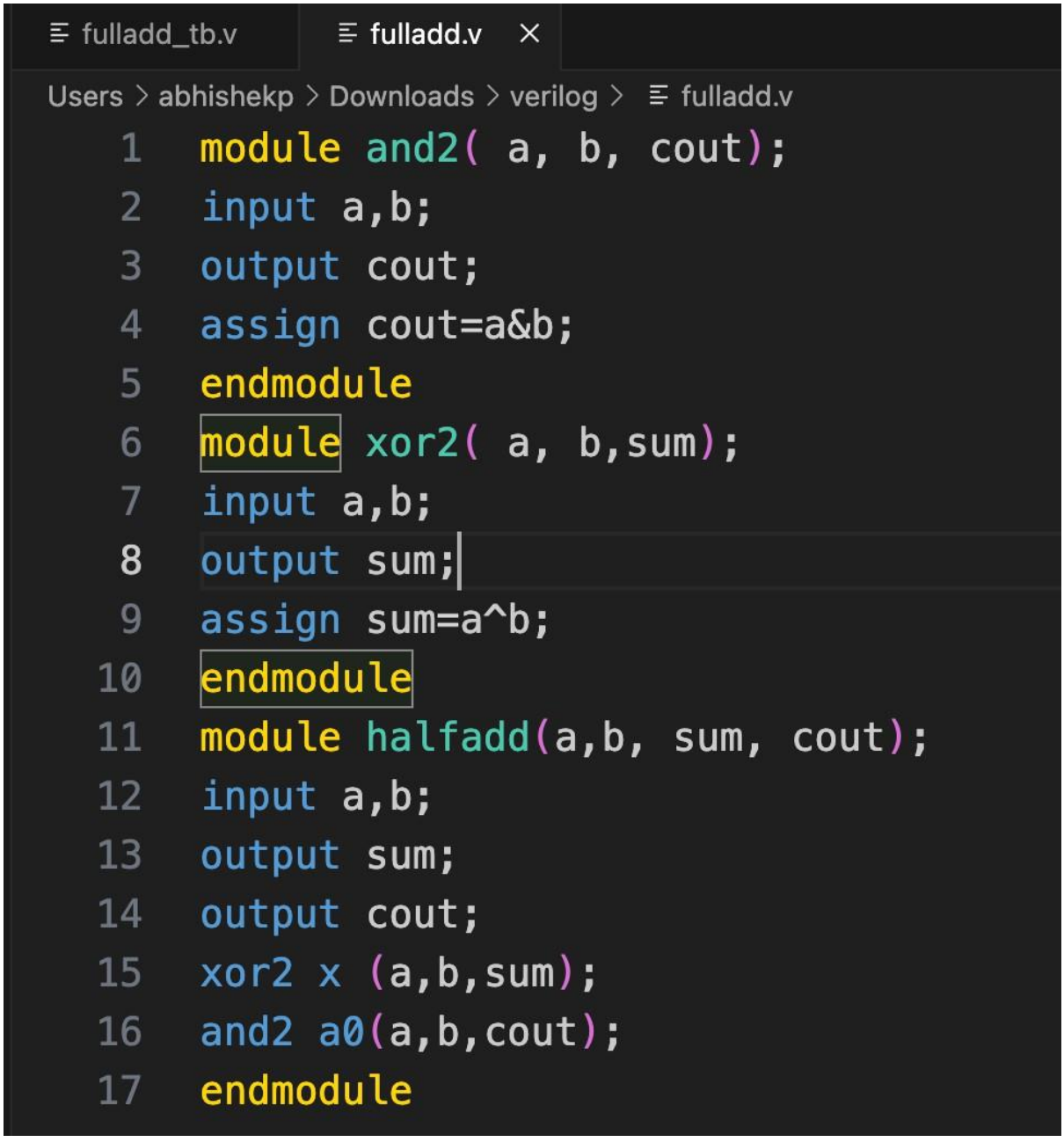
Users > abhishekp > Downloads > verilog > fulladd_tb.v

```
1  module halfadd_tb;
2  reg aa, bb;
3  wire ss,cy;
4  halfadd add1(.a(aa),.b(bb),.sum(ss),.cout(cy));
5  initial
6  begin
7  $dumpfile("halfadd_test.vcd");
8  $dumpvars(0, halfadd_tb);
9  end
10 initial
11 begin
12 $monitor($time, "A=%b, B=%b, SUM=%b, CARRY=%b", aa, bb,ss, cy);
13 aa=1'b0; bb=1'b0;
14 #5
15 aa=1'b0; bb=1'b1;
16 #5
17 aa=1'b1; bb=1'b0;
18 #5
19 aa=1'b1; bb=1'b1;
20 end
21 endmodule
```

Digital Design and Computer Organisation Laboratory

UE22CS251A

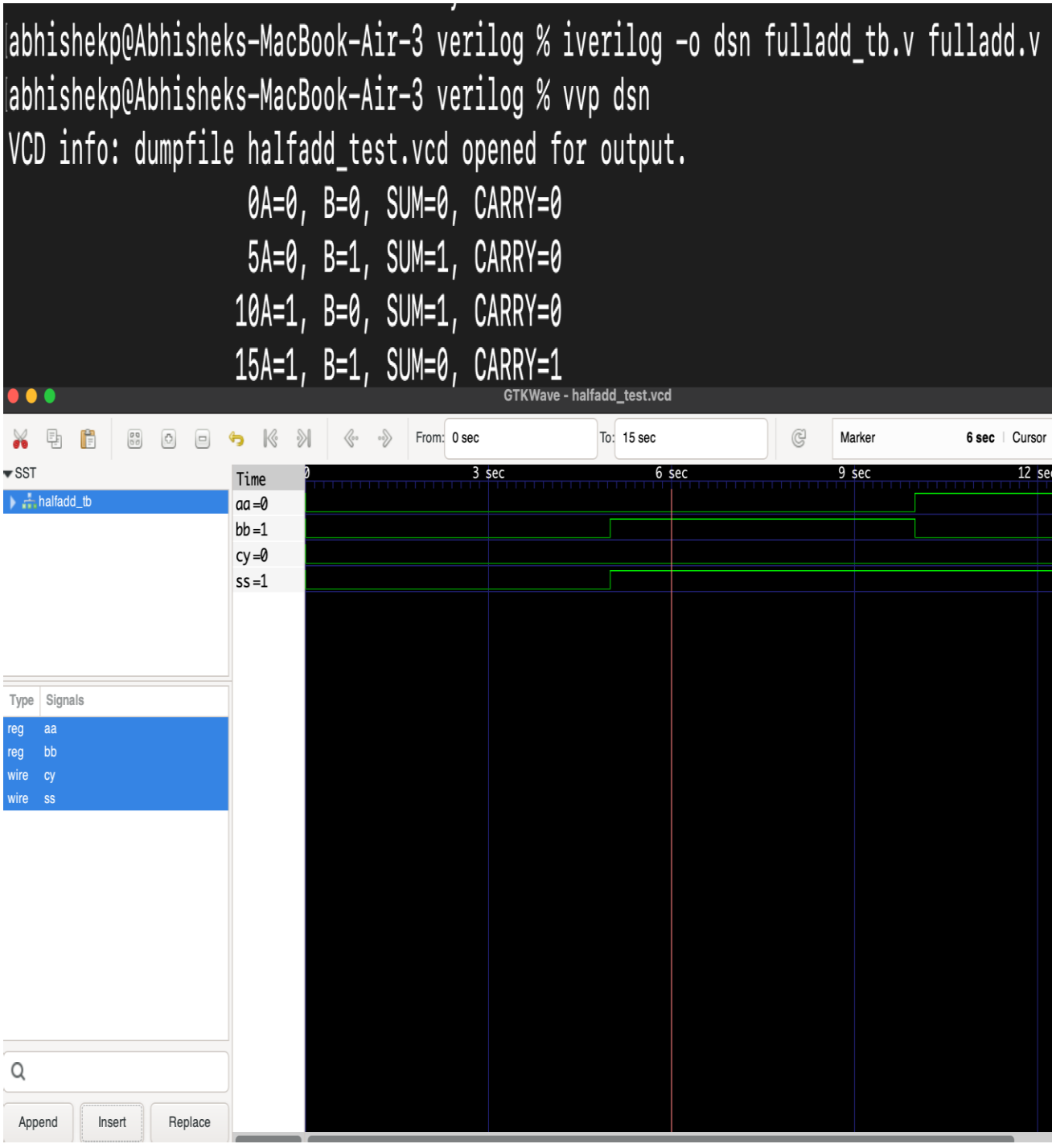
3rd Semester, Academic Year 2023-24



Digital Design and Computer Organisation Laboratory

UE22CS251A

3rd Semester, Academic Year 2023-24



Digital Design and Computer Organisation Laboratory

UE22CS251A

3rd Semester, Academic Year 2023-24

Name: ABHISHEK P	SRN: PES2UG23AM002	Section: A Date: 01/09/2024

Week#____3_____ Program Number: ____2__

TITLE :

WRITE A VERILOG PROGRAM TO MODEL A FULL ADDER THAT CAN ADD TWO BITS ALONG WITH AN INPUT CARRY. GENERATE THE VVP OUTPUT AND SIMULATION WAVEFORM USING GTKWAVE. VERIFY THE OUTPUT AND WAVEFORM WITH THE TRUTH TABLE

fulladd.v

```
1  module fulladd(input wire a, b, cin, output wire sum, cout);
2  wire [4:0] t;
3
4      xor2 x0(a, b, t[0]);
5      xor2 x1(t[0], cin, sum);
6
7      and2 a0(a, b, t[1]);
8      and2 a1(a, cin, t[2]);
9      and2 a2(b, cin, t[3]);
10
11     or2 o0(t[1], t[2], t[4]);
12     or2 o1(t[3], t[4], cout);
13 endmodule
14
```

Digital Design and Computer Organisation Laboratory

UE22CS251A

3rd Semester, Academic Year 2023-24

fulladd_tb.v

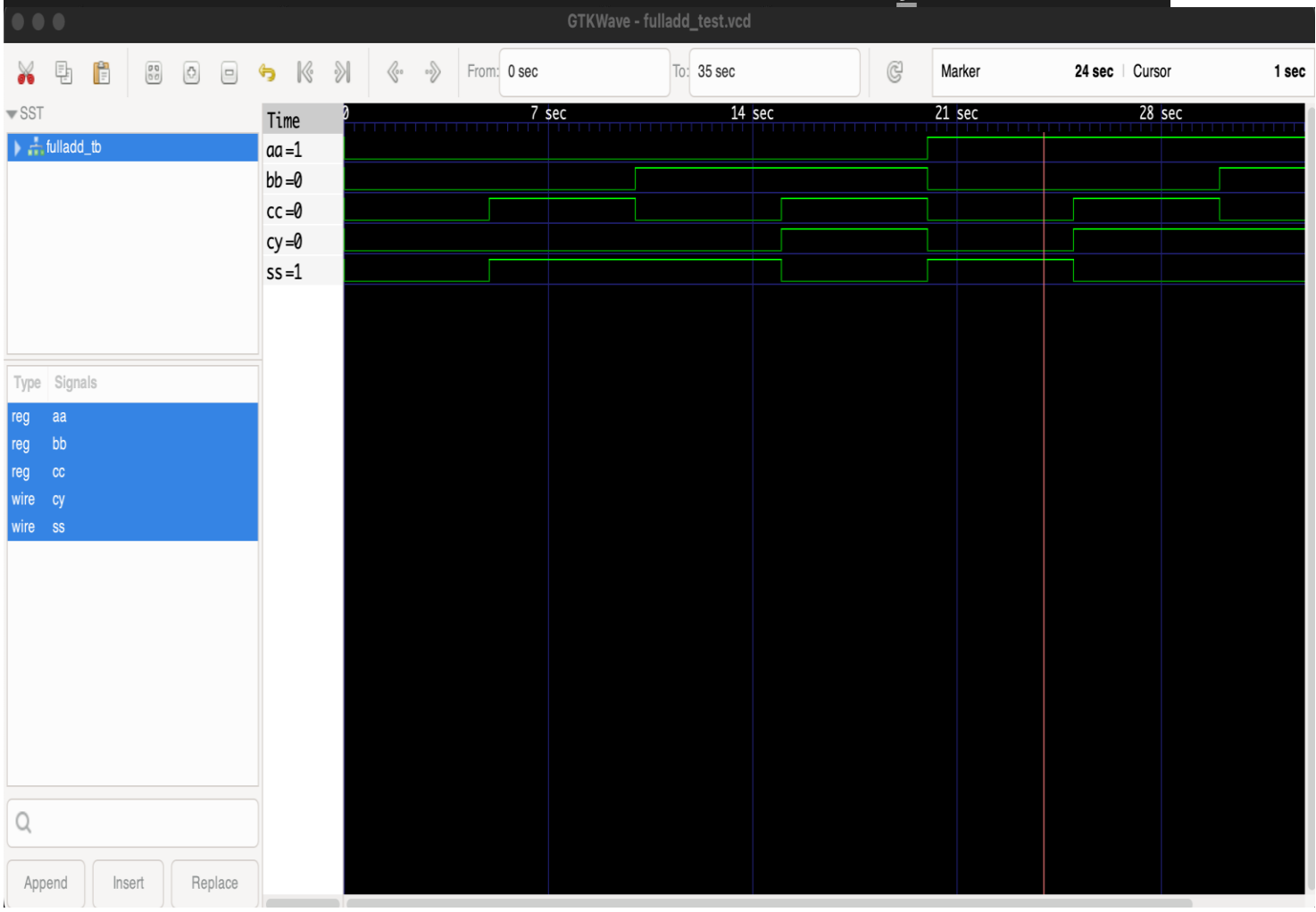
```
module fulladd_tb;

reg aa,bb,cc;

wire ss,cy;

fulladd add1(.a(aa), .b(bb), .cin(cc), .sum(ss), .cout(cy));

initial

begin

$dumpfile("fulladd_test.vcd");

$dumpvars(0, fulladd_tb);

end

initial
 begin
$monitor($time, "a=%b, b=%b, c=%b,sum=%b,carry=%b", aa,bb,cc,ss,cy);
aa = 1'b0;
bb = 1'b0;
cc=1'b0;

#5
  aa = 1'b0;
bb = 1'b0;
cc=1'b1;

#5
  aa = 1'b0;
bb = 1'b1;
cc=1'b0;

#5
  aa = 1'b0;
bb = 1'b1;
cc=1'b1;

#5
  aa = 1'b1;
bb = 1'b0;
cc=1'b0;

#5
  aa = 1'b1;
bb = 1'b0;
cc=1'b1;

#5
  aa = 1'b1;
bb = 1'b1;
cc=1'b0;

#5
  aa = 1'b0;
bb = 1'b1;
cc=1'b1;

end

endmodule
```

Digital Design and Computer Organisation Laboratory

UE22CS251A

3rd Semester, Academic Year 2023-24

```
abhishekp@Abhisheks-MacBook-Air-3 verilog % vvp dsn
VCD info: dumpfile fulladd_test.vcd opened for output.
                    0a=0, b=0, c=0,sum=0,carry=0
                    5a=0, b=0, c=1,sum=1,carry=0
                   10a=0, b=1, c=0,sum=1,carry=0
                   15a=0, b=1, c=1,sum=0,carry=1
                   20a=1, b=0, c=0,sum=1,carry=0
                   25a=1, b=0, c=1,sum=0,carry=1
                   30a=1, b=1, c=0,sum=0,carry=1
                   35a=0, b=1, c=1,sum=0,carry=1
```



Digital Design and Computer Organisation Laboratory

UE22CS251A

3rd Semester, Academic Year 2023-24

Name: ABHISHEK P	SRN: PES2UG23AM002	Section: A

Week#____1_____ Program Number: ____3__

TITLE:

WRITE A VERILOG PROGRAM TO MODEL A FOUR BIT FULL ADDER THAT GENERATES A FOUR BIT SUM AND A 1 BIT CARRY OUTPUT.GENERATE THE VVP OUTPUT AND SIMULATION WAVEFORM USING GTKWAVE. VERIFY THE OUTPUT AND WAVEFORM WITH THE TRUTH TABLE

rca.v

```
1  // Module 4-bit ripple carry adder.
2
3  module fulladdR(input wire [3:0] a, b, input wire cin, output wire [3:0] sum, output wire cout);
4
5      // Instantiate full adder modules here.
6  wire [2:0] c;
7    fulladd u0 (a[0], b[0], cin, sum[0], c[0]);
8    fulladd u1 (a[1], b[1], c[0], sum[1], c[1]);
9    fulladd u2 (a[2], b[2], c[1], sum[2], c[2]);
10   fulladd u3 (a[3], b[3], c[2], sum[3], cout);
11
12 endmodule
13
```

Digital Design and Computer Organisation Laboratory

UE22CS251A

3rd Semester, Academic Year 2023-24

basicfa.v | rca_tb.v

rca_tb.v

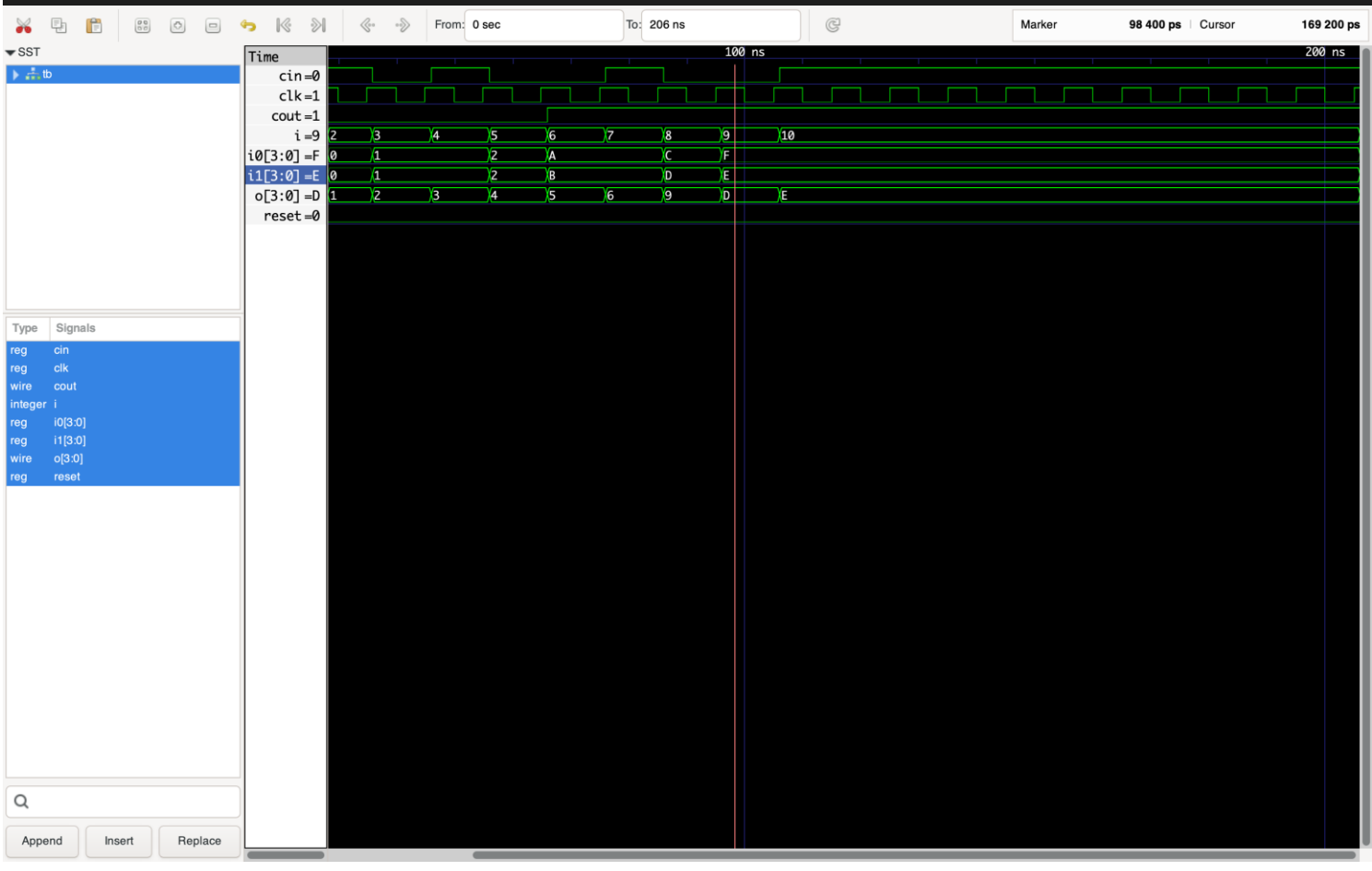
```
1   `timescale 1 ns / 100 ps
2
3   `define TESTVECS 10
4   module tb;
5
6   reg clk, reset;
7
8    reg [3:0] i0, i1;
9    reg cin;
10
11  wire [3:0] o;
12  wire cout;
13
14   reg [8:0] test_vecs [0:(`TESTVECS-1)];
15
16  integer i;
17
18   initial
19  begin
20  $dumpfile("rca_test.vcd");
21
22  $dumpvars(0,tb);
23
24   end
25
26  initial
27  begin
28   reset = 1'b1; #12.5 reset = 1'b0; end
29    initial clk = 1'b0; always #5 clk =~ clk;
30
31    initial begin
32
33   test_vecs[0] = 9'b000000000;
34
35   test_vecs[1] = 9'b000000001;
36
37   test_vecs[2] = 9'b000100010;
38
39    test_vecs[3] = 9'b000100011;
40
41  test_vecs[4] = 9'b001000100;
42
43    test_vecs[5] = 9'b101010110;
44
45    test_vecs[6] = 9'b101010111;
46
47     test_vecs[7] = 9'b110011010;
48
49  test_vecs[8] = 9'b111111100;
50
51  test_vecs[9] = 9'b111111101;
52
53
54   end
55    initial {i0, i1, cin, i} = 0;
56    fulladdR u0 (i0, i1, cin, o, cout);
57    initial begin
58      #6 for(i=0;i<`TESTVECS;i=i+1)
59        begin #10 {i0, i1, cin}=test_vecs[i]; end
60      #100 $finish;
61    end
62
63  always@(i0 or i1 or cin)
64  $monitor("At time = %t, i0=%b, i1=%b,cin=%b,Sum = %b,Carry %b", $time,i0,i1,cin,o,cout);
65
66
67  endmodule
68
```

Digital Design and Computer Organisation Laboratory

UE22CS251A

3rd Semester, Academic Year 2023-24

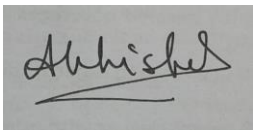
```
Last login: Wed Oct  2 19:07:14 on ttys000
abhishekp@Abhisheks-MacBook-Air-3 ~ % cd downloads
abhishekp@Abhisheks-MacBook-Air-3 downloads % iverilog -o dsn basicfa.v rca_tb.v rca.v
abhishekp@Abhisheks-MacBook-Air-3 downloads % vvp dsn
VCD info: dumpfile rca_test.vcd opened for output.
At time =                    0, i0=0000, i1=0000,cin=0,Sum = 0000,Carry 0
At time =                  260, i0=0000, i1=0000,cin=1,Sum = 0001,Carry 0
At time =                  360, i0=0001, i1=0001,cin=0,Sum = 0010,Carry 0
At time =                  460, i0=0001, i1=0001,cin=1,Sum = 0011,Carry 0
At time =                  560, i0=0010, i1=0010,cin=0,Sum = 0100,Carry 0
At time =                  660, i0=1010, i1=1011,cin=0,Sum = 0101,Carry 1
At time =                  760, i0=1010, i1=1011,cin=1,Sum = 0110,Carry 1
At time =                  860, i0=1100, i1=1101,cin=0,Sum = 1001,Carry 1
At time =                  960, i0=1111, i1=1110,cin=0,Sum = 1101,Carry 1
At time =                 1060, i0=1111, i1=1110,cin=1,Sum = 1110,Carry 1
rca_tb.v:60: $finish called at 2060 (100ps)
abhishekp@Abhisheks-MacBook-Air-3 downloads % gtkwave rca_test.vcd
```



Disclaimer:

- The programs and output submitted is duly written, verified and executed by me.
- I have not copied from any of my peers nor from the external resource such as internet.
- If found plagiarized, I will abide with the disciplinary action of the University.

Signature:



Name:
ABHISHEK P
SRN:
PES2UG23AM002
Section: ***A***