Digital Design and Computer Organization Laboratory

3rd Semester, Academic Year 2024-25

Date:22/08/2024

Name: ABHISHEK P	SRN: PES2UG23AM002	Section: A

Week#__2_____

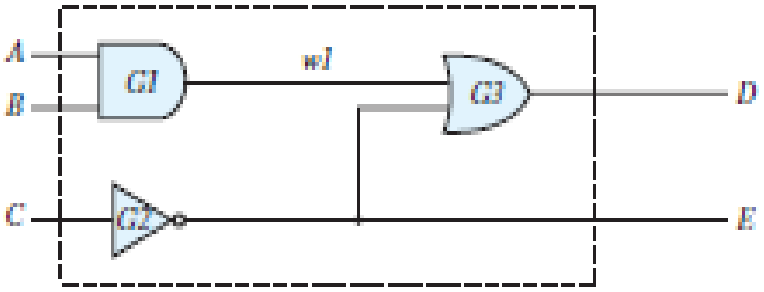
Program Number :___1____

Title of the Program

SIMPLE_CIRCUIT

Aim:

WRITE A VERILOG PROGRAM TO MODEL THE GIVEN SIMPLE CIRCUIT.GENERATE THE VVP OUTPUT AND VIEW THE SIMULATION WAVEFORM USING GTKWAVE.VERIFY THE OUTPUT AND WAVEFORM WITH THE RELEVANT TRUTH TABLE



```
1   module simple_circuit
2   (A,B,C,D,E);
3   output D,E;
4   input A,B,C;
5   wire w1;
6   and G1(w1,A,B);
7   not G2(E,C);
8   or G3(D,w1,E);
9   endmodule
10
```

```
abhishekp@Abhisheks-MacBook-Air-3 ~ % cd Downloads
abhishekp@Abhisheks-MacBook-Air-3 Downloads % cd verilog
abhishekp@Abhisheks-MacBook-Air-3 verilog % iverilog -o dsn and2.v and2_test.v
abhishekp@Abhisheks-MacBook-Air-3 verilog % vvp dsn
VCD info: dumpfile simple.vcd opened for output.
                  0 A=0, B=0, C=0, D=1, E=1
                 20 A=0, B=0, C=1, D=0, E=0
                 40 A=0, B=1, C=0, D=1, E=1
                 60 A=0, B=1, C=1, D=0, E=0
                 80 A=1, B=0, C=0, D=1, E=1
                100 A=1, B=0, C=1, D=0, E=0
                120 A=1, B=1, C=0, D=1, E=1
                140 A=1, B=1, C=1, D=1, E=0
and2_test.v:23: $finish called at 200 (1s)
abhishekp@Abhisheks-MacBook-Air-3 verilog %
```

Date:22/08/2024

Name: ABHISHEK P	SRN: PES2UG23AM002	Section: A

Week#__2_____

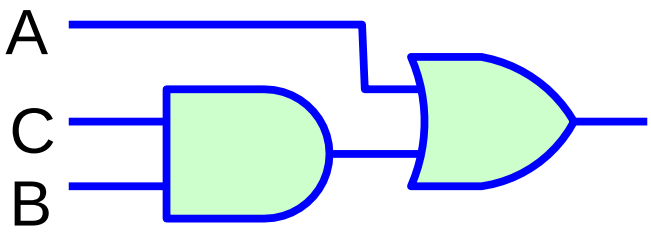
Program Number: ___2____

Title of the Program

CIRCUIT1

Aim:

WRITE A VERILOG PROGRAM TO MODEL THE GIVEN CIRCUIT1. GENERATE THE VVP OUTPUT AND VIEW THE SIMULATION WAVEFORM USING GTKWAVE.VERIFY THE OUTPUT AND WAVEFORM WITH THE RELEVANT TRUTH TABLE

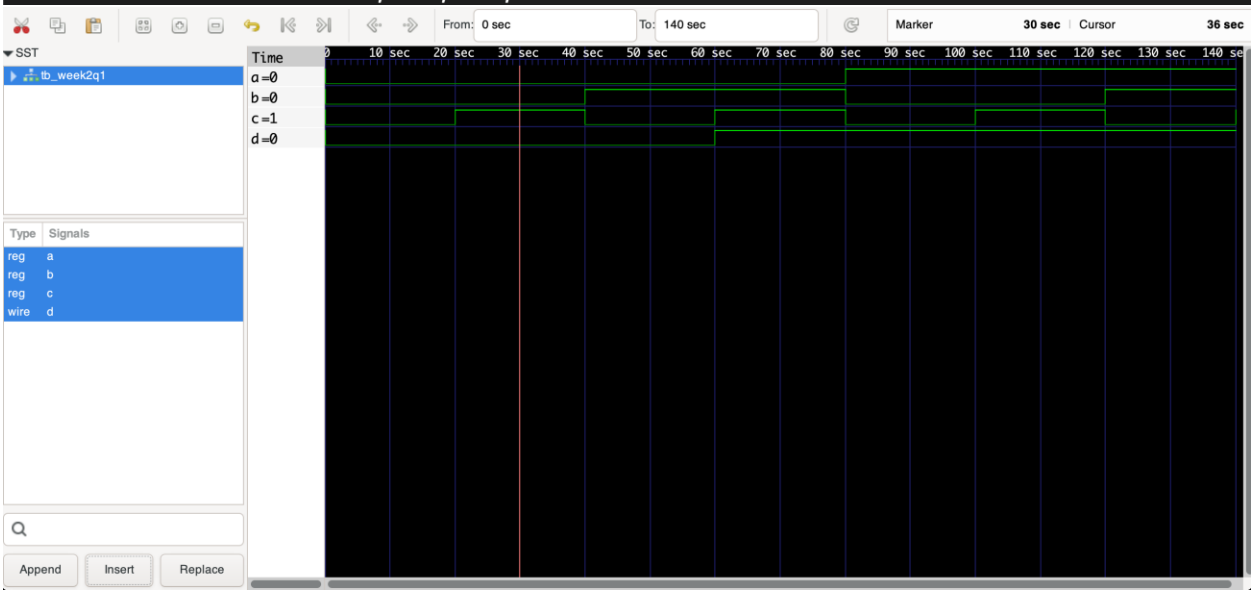


and2.v and2_test.v

and2_test.v

```
1  module tb_week2q1;
2  reg a,b,c;
3  wire d;
4  ckt M1(a,b,c,d);
5  initial
6  begin
7  #0
8  a=1'b0;b=1'b0;c=1'b0;
9  #20
10 a=1'b0;b=1'b0;c=1'b1;
11 #20
12 a=1'b0;b=1'b1;c=1'b0;
13 #20
14 a=1'b0;b=1'b1;c=1'b1;
15 #20
16 a=1'b1;b=1'b0;c=1'b0;
17 #20
18 a=1'b1;b=1'b0;c=1'b1;
19 #20
20 a=1'b1;b=1'b1;c=1'b0;
21 #20
22 a=1'b1;b=1'b1;c=1'b1;
23 end
24 initial
25 begin
26 $monitor($time,"a=%b,b=%b,c=%b,d=%b",a,b,c,d);
27 end
28 initial
29 begin
30 $dumpfile("test.vcd");
31 $dumpvars(0,tb_week2q1);
32 end
33 endmodule
```

```
abhishekp@Abhisheks-MacBook-Air-3 ~ % cd Downloads
abhishekp@Abhisheks-MacBook-Air-3 Downloads % cd verilog
abhishekp@Abhisheks-MacBook-Air-3 verilog % iverilog -o dsn and2.v and2_test.v
abhishekp@Abhisheks-MacBook-Air-3 verilog % vvp dsn
VCD info: dumpfile test.vcd opened for output.
                   0a=0,b=0,c=0,d=0
                  20a=0,b=0,c=1,d=0
                  40a=0,b=1,c=0,d=0
                  60a=0,b=1,c=1,d=1
                  80a=1,b=0,c=0,d=1
                 100a=1,b=0,c=1,d=1
                 120a=1,b=1,c=0,d=1
                 140a=1,b=1,c=1,d=1
```



Date:22/08/2024

Name: ABHISHEK P	SRN: PES2UG23AM002	Section: A

Week#__2_____

Program Number: ___3____

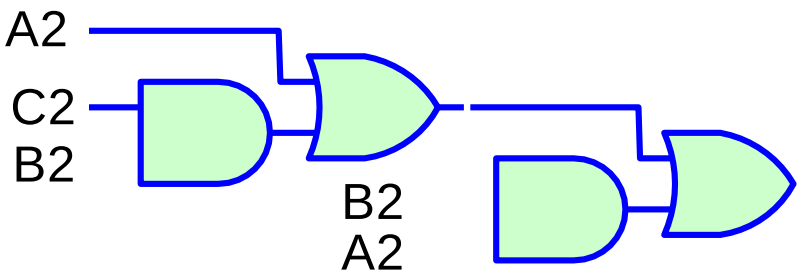
Title of the Program

CIRCUIT2

Aim:

WRITE A VERILOG PROGRAM TO MODEL THE GIVEN CIRCUIT2. GENERATE THE VVP OUTPUT AND VIEW THE SIMULATION WAVEFORM USING GTKWAVE.VERIFY THE OUTPUT AND WAVEFORM WITH THE RELEVANT TRUTH TABLE

CIRCUIT 2

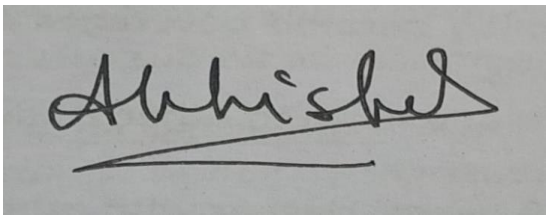


```
module tb_week2q2;
reg a2,b2,c2;
wire z;
ckt M1(a2,b2,c2,z);
initial
begin
#0
a2=1'b0;b2=1'b0;c2=1'b0;
#20
a2=1'b0;b2=1'b0;c2=1'b1;
#20
a2=1'b0;b2=1'b1;c2=1'b0;
#20
a2=1'b0;b2=1'b1;c2=1'b1;
#20
a2=1'b1;b2=1'b0;c2=1'b0;
#20
a2=1'b1;b2=1'b0;c2=1'b1;
#20
a2=1'b1;b2=1'b1;c2=1'b0;
#20
a2=1'b1;b2=1'b1;c2=1'b1;
end
initial
begin
$monitor($time,"a2=%b,b2=%b,c2=%b,z=%b",a2,b2,c2,z);
end
initial
begin
$dumpfile("test.vcd");
$dumpvars(0,tb_week2q2);
end
endmodule
```

```
abhishekp@Abhisheks-MacBook-Air-3 verilog % iverilog -o dsn and2.v and2_test.v
abhishekp@Abhisheks-MacBook-Air-3 verilog % vvp dsn
VCD info: dumpfile test.vcd opened for output.
                   0a2=0,b2=0,c2=0,z=0
                  20a2=0,b2=0,c2=1,z=0
                  40a2=0,b2=1,c2=0,z=0
                  60a2=0,b2=1,c2=1,z=1
                  80a2=1,b2=0,c2=0,z=1
                 100a2=1,b2=0,c2=1,z=1
                 120a2=1,b2=1,c2=0,z=1
                 140a2=1,b2=1,c2=1,z=1
```

Disclaimer:

- The programs and output submitted is duly written, verified and executed my me.
- I have not copied from any of my peers nor from the external resource such as internet.
- If found plagiarized, I will abide with the disciplinary action of the University.

Signature: 

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