Shahjalal University of Science and Technology

Department of Computer Science and Engineering

2nd Year 2nd Semester Final Examination-2022 (Session: 2020-21)

Course Code: EEE 201D **Credit: 3.0**

Course Title: Digital Logic Design

Time: 3 hours **Total Marks: 100**

Group – A

1. **Answer any FIVE of the following:** 5x2=10
   a. Using block diagram briefly explain how sequential circuits differ from combinational circuits.
   b. Describe why DRAMs are called dynamic RAM.
   c. Show that a positive logic NAND gate is a negative logic NOR gate and vice versa.
   d. Define multiplexers. Also, draw the two-to-one line multiplexer using only AND, OR and inverter gate
   e. Using minimum number of NAND gates, implement XOR gate.
   f. Express the following function as a sum of minterms:
   $$F(A,B,C,D) = B'D + A'D + BD$$
   g. Obtain a truth table for the following function: $F(x,y,z) = (xy + z)(y + xz)$.
   h. Find the Boolean expression for the logic circuit in figure 1.1.

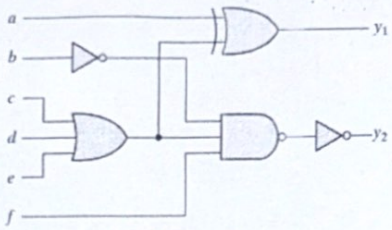

Figure: 1.1

2. **Answer any FOUR questions of the following:** 4x5=20
   a. Implement a 32x1 multiplexer using 8x1 multiplexer. You may use basic gates if necessary.
   b. Design and implement a binary full subtractor.
   c. Draw block diagram of a four-bit binary ripple carry adder and explain its working principle.
   d. Simplify the following Boolean function to minimized SOP and POS from-
   $$F(w,x,y,z) = \Sigma(1,3,7,11,15) + \sum_d (0,2,5)$$
   e. Simplify the following functions and implement them with two-level NOR gate circuits:
      1. $F = wx' + y'z' + w'yz'$
      2. $F = (w, x, y, z) = \Sigma(0, 3, 12, 15)$
   f. Implement J-K flip-flop using D flip-flop.
3. **Answer any TWO questions of the following:** 2x10=20
   a. In excess-3 code, numbers are represented as decimal digits, and each digit is represented by four bits as the digit value plus 3. i) Make a truth table for a BCD to excess-3 converter, ii) Find the Boolean expressions in minimized SOP form, ii) implement the logic circuit using minimum number of basic gates.
   b. Implement a full adder with two 4×1 multiplexers
   c. Design a four-input priority encoder with input D_0 having the highest priority and input D_3 the lowest priority.

Group – B

4. **Answer any FIVE questions of the following:** 5x2=10
   a. Define decoder and encoder.
   b. Explain the differences between a truth table, a state table, a characteristic table and an excitation table
   c. Differentiate between serial mode and parallel transfer mode of register.
   d. Briefly explain your understanding on excitation table.
   e. Write the characteristic and excitation table of a T flip-flop.
   f. A memory unit is specified by $1G \times 32$. Find how many address lines, input lines, output lines are required. Also find the capacity of the memory.

g. What is a register? Draw the logic diagram of a four-bit register
h. Determine the Q output waveform if the inputs shown in Figure: 4.1 are applied to a gated S-R latch that is initially RESET.

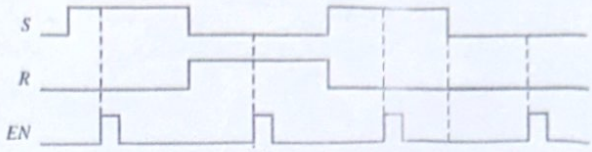

Figure: 4.1

5. **Answer any FOUR questions of the following** 4x5=20
a. Using proper block diagram, explain the differences among combinational programmable logic devices.
b. Draw logic circuit of a bi-directional shift register and briefly explain its operation.
c. From the state diagram, obtain the logic diagram of BCD ripple counter.
d. Draw logic diagram and timing diagram of Johnson counter. Briefly describe its operation.
e. Draw logic circuit of master-slave J-K flip-flop and briefly explain its operation.
f. Reduce the state diagram shown in figure 4.2 and draw the reduced diagram.

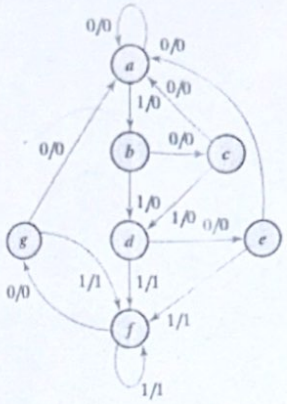

Figure: 4.2

6. **Answer any TWO questions of the following:** 2x10=20
a. Tabulate the truth table for an 8 * 4 ROM that implements the following Boolean functions-

$$A(x,y,z) = \sum(0,3,4,6)$$

$$B(x,y,z) = \sum(0,1,4,7)$$

$$C(x,y,z) = \sum(1,5)$$

$$D(x,y,z) = \sum(0,1,3,5,7)$$

Draw the fusing map of the ROM logic circuit. Considering now the ROM as a memory, specify the memory contents at addresses 1 and 4.
b. Implement the following Boolean function F, together with the don't-care conditions d, using no more than two NOR gates:

$$F(A, B, C, D) = \Sigma(2, 4, 10, 12, 14)$$

$$d(A, B, C, D) = \Sigma(0, 1, 5, 8)$$

~~Draw the fusing map of the ROM logic circuit. Considering now the ROM as a memory, specify the memory contents at addresses 1 and 4.~~
c. Tabulate the PLA programming table for the four Boolean functions listed below. Minimize the number of product terms. Mark the fuse map in PLA diagram.

$$A(x,y,z) = \sum(1,3,5,6)$$
$$B(x,y,z) = \sum(0,1,6,7)$$
$$C(x,y,z) = \sum(3,5)$$
$$D(x,y,z) = \sum(1,2,4,5,7)$$