## Dept. of Electronics and Electrical Communication Engineering Indian Institute of Technology Kharagpur

**VLSI DESIGN LABORATORY(EC69216)**

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Title:

**TWO-STAGE DIFFERENTIAL AMPLIFIER**

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# Objective:

Design and Analysis of TWO STAGE- Differential Amplifier for the given specifications.

* Vdd = 1.8V
* Av >= 1000, 60dB
* Phase Margin>=600
* CL = 2pF
* ICMR (+) = 1.6V
* ICMR (-) = 0.8V
* Slew Rate = 20V/usec
* Power dissipation < 0.3 mW
* GBW >= 30MHz

# Introduction:

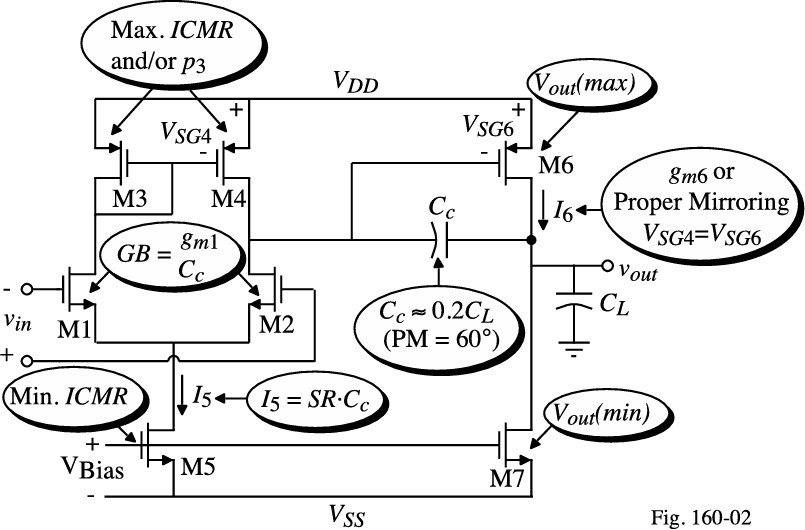
* A two-stage differential amplifier is a type of electronic amplifier that amplifies the difference between two input signals while suppressing any voltage common to both inputs.
* A two-stage amplifier can provide high gain and high output swing. The first stage is a differential amplifier, an Analog circuit with two inputs (Vin+ and Vin-) and one output (Vout), which is proportional to the difference between the two inputs. The second stage is a Common Source Amplifier.

**Two-Stage Configuration:**

* In a two-stage differential amplifier, two operational amplifiers (op-amps) are used in sequence. The first stage is typically a non-inverting amplifier, and the second stage is a differential amplifier. This configuration increases the gain and input resistance of the amplifier.

***First Stage: Non-Inverting Amplifier:***

* The first stage amplifies the input signal without inverting it. The gain of this stage is determined by the feedback resistors used in the circuit. The output of the first stage becomes the input for the second stage.



BIAS is done by the current mirror circuit

* Gain of the differential amplifier is the product of transconductance of M1 and Rout Ad = gm2 { rds2 || rds4 }
* While that of CS stage is Av = gm6 { rds6 || rds7

# Circuit Diagram:

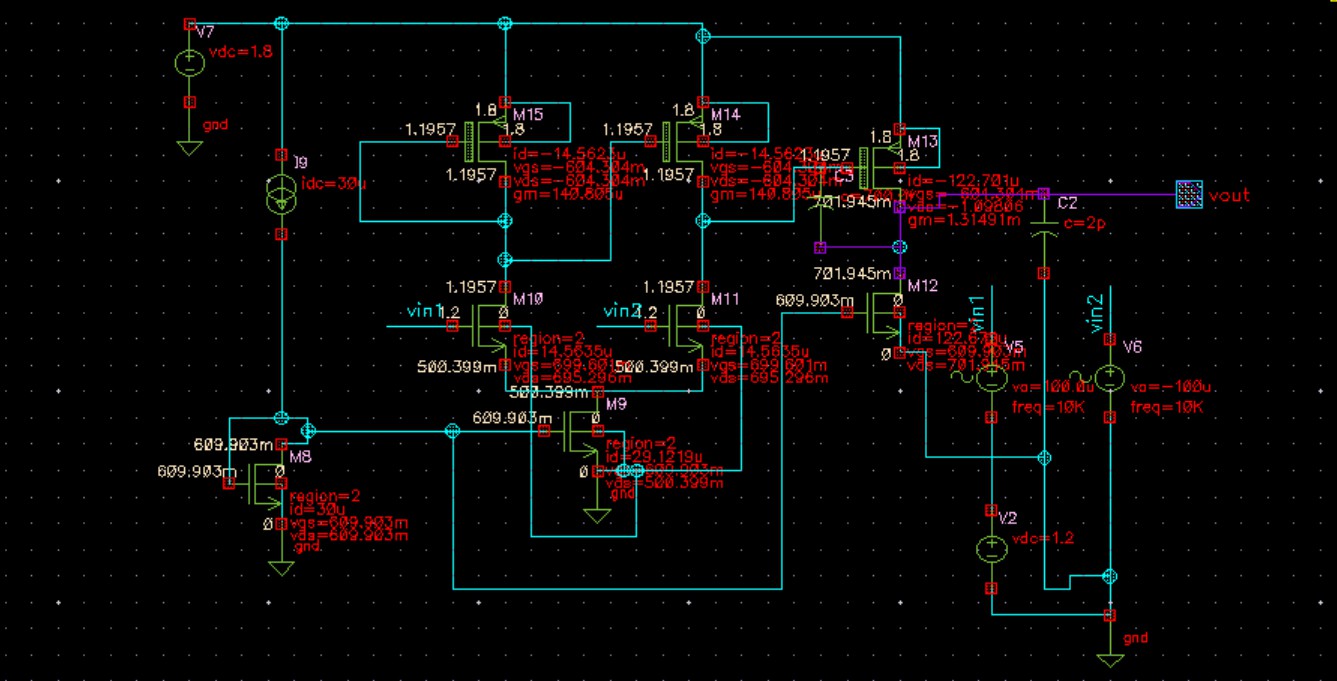
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Figure: 2-stage differential amplifier

# Plots:

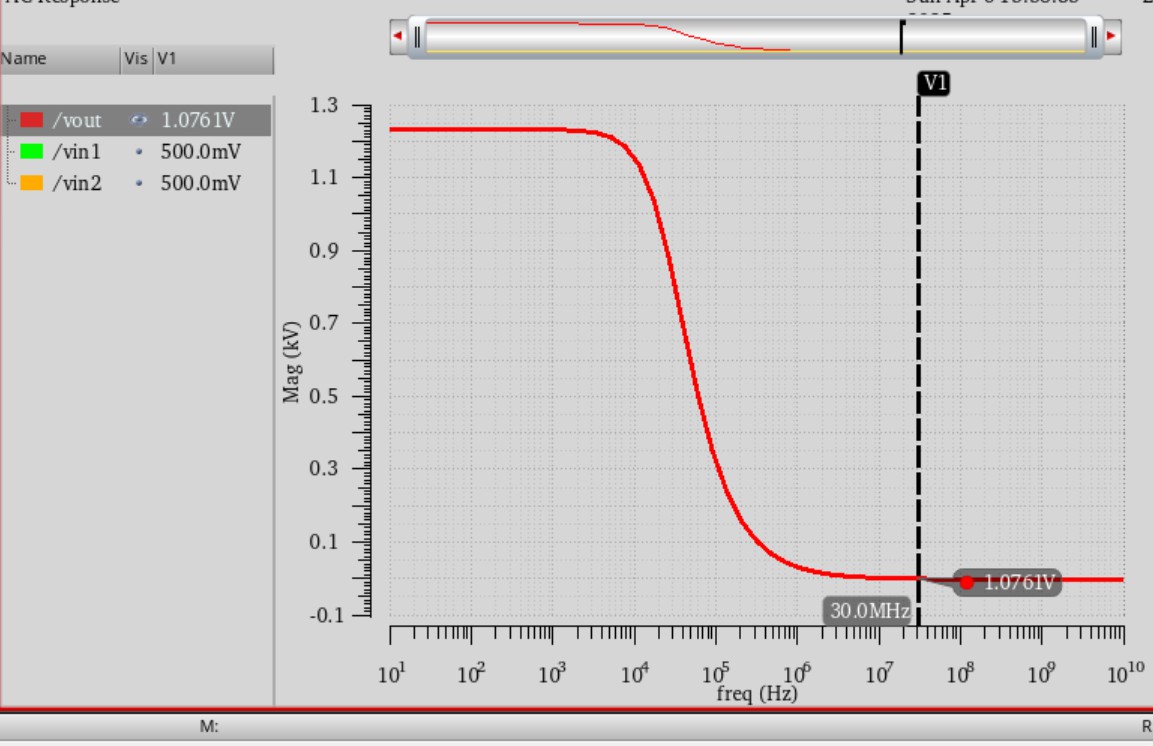
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Figure: GAIN PLOT FOR DIFFERENTIAL MODE

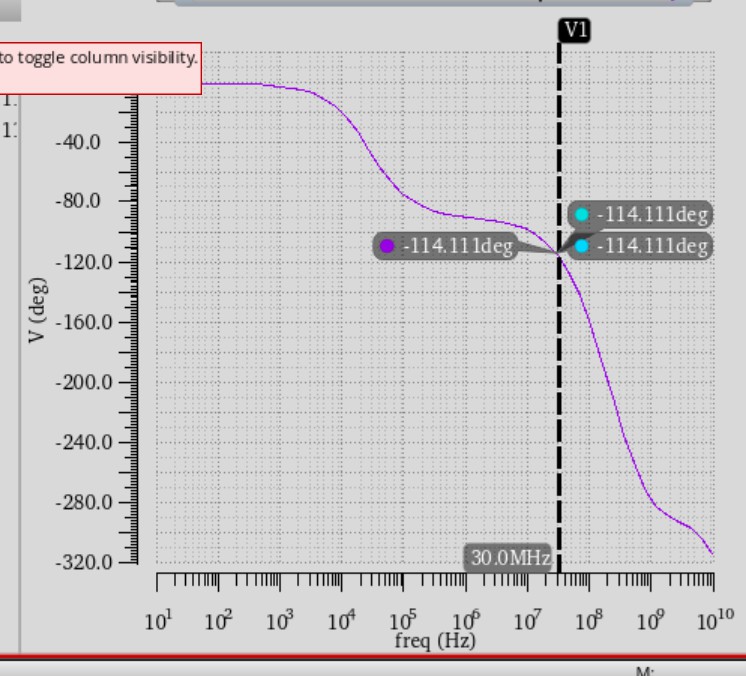


FIGURE: PHASE PLOT FOR DIFFERENTIAL MODE

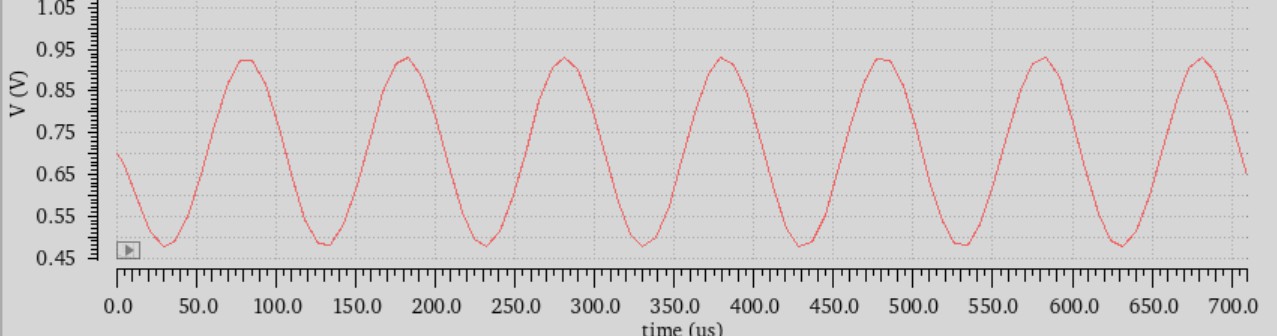


FIGURE:TRANSIENT ANALYSIS

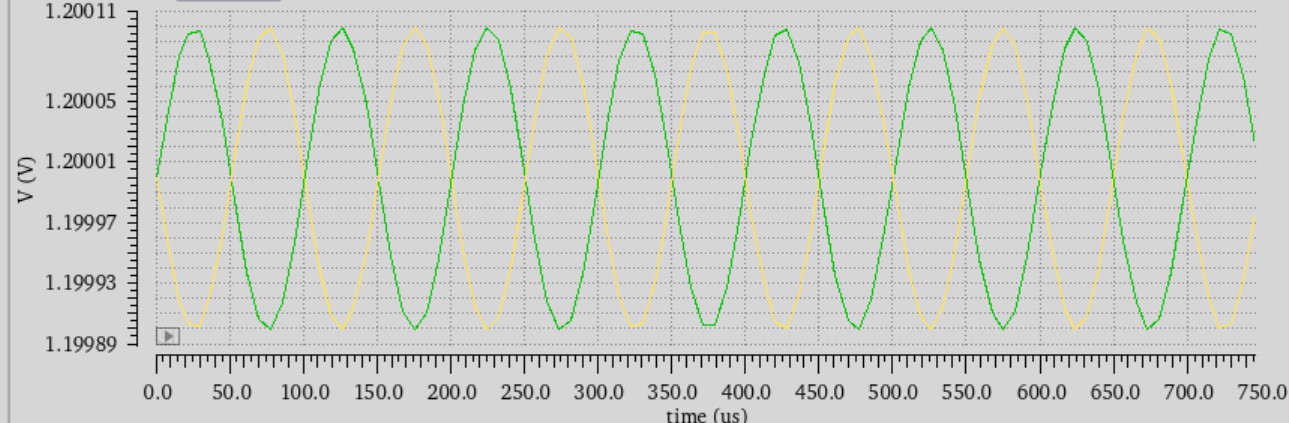


FIGURE:TRANSIENT ANALYSIS FOR VIN AS DIFFERENTIAL MODE

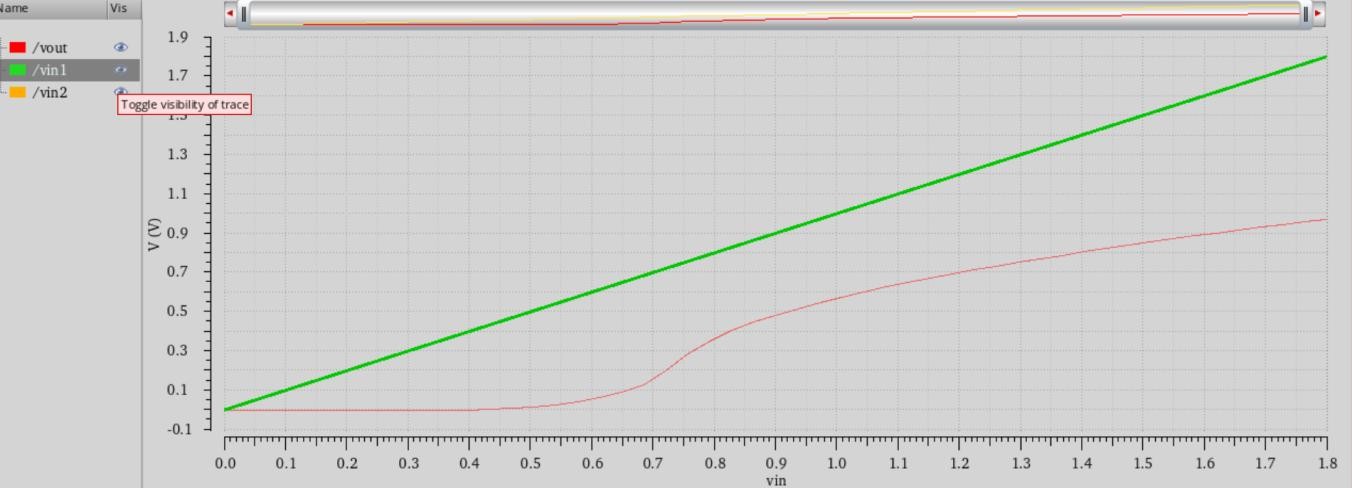


Figure: DC ANALYSIS

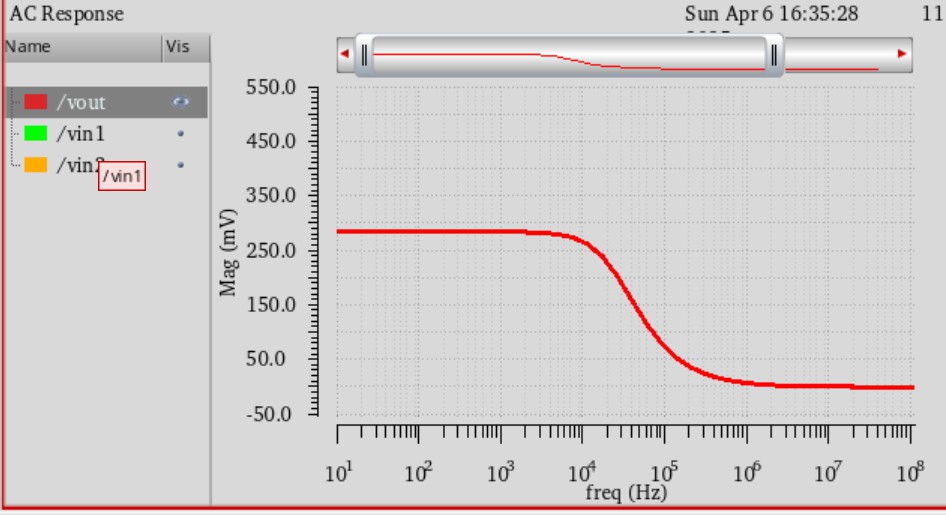


Figure: COMMON MODE GAIN

# Results and Calculations:

## From the circuit diagram, the theoretical and practical values are

|  |  |  |
| --- | --- | --- |
| * **Parameter** | * **Theoretical** | * **Practical** |
| * (W/L)9 | * 2.1/0.2 | * 2.1/0.2 |
| * (W/L)8 | * 2.1/0.2 | * 2.1/0.2 |
| * (W/L)10 | * 1.6/0.2 | * 1.8/0.4 |
| * (W/L)11 | * 1.6/0.2 | * 1.8/0.4 |
| * (W/L)15,14 | * 2.6/0.2 | * 6/0.4 |
| * (W/L)13 | * 2.6\*8/0.2 | * 3\*8/0.2 |
| * (W/L)12 | * 2.1\*4/0.2 | * 2.1\*4/0.2 |
| * Cc | * 0.7p F | * 0.7p F |
| * I tail | * 30u A | * 29.129u A |

|  |  |  |
| --- | --- | --- |
| * Gm1 | * 131.85u | * 158.138u |
| * Gm2 | * 1.048m | * 1.32902m |

Calcualtions:

