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 Computer Science & IT (CS)

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COMPUTER ORGANIZATION AND ARCHITECTURE (GATE 2023) - REPORTS

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ALL(33) CORRECT(19) INCORRECT(14) SKIPPED(0)

Q. 11
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Consider a system A with byte addressable main memory of size 1 MB. It has 64 registers. It uses 32 bit instruction format and there are two types of instructions available. First type of instruction contains an opcode, a register name and an address of main memory. Second type of instruction contains an opcode and three register names. There are 60 first type of instructions and n second type of instructions in system. The maximum possible value of n is _____.

 1024

 Your answer is **Correct** 1024

Solution :
 1024

$$\begin{aligned} \text{Memory address length (MAL)} &= \log_2 \left(\frac{\text{Memory size}}{\text{Addressable size}} \right) \\ &= \log_2 \left(\frac{1 \text{ MB}}{1 \text{ B}} \right) = \log_2 (2^{20}) = 20 \text{ bits} \end{aligned}$$

$$\text{Register name length (RL)} = \log_2 (\text{Number of register}) = \log_2 (64) = 6 \text{ bits}$$

1st type instruction:

20 bits for MAL and 6 bits for RL. Now 6 bits left for opcode.

 Maximum instruction possible of type first = $2^6 = 64$

But system has 60 instructions of first type.

 So, $64 - 60 = 4$ instruction left for opcode of 6 bit

2nd type instruction:
 $6 \times 3 = 18$ bits for 3 registers. Now 14 bits remains for opcode.

For 6 most-significant bits of opcode, we have only 4 instructions (shown above). Now, you have 4 instructions and 8 bits.

 So, total instructions possible for 2nd type = $4 \times 2^8 = 210$ 1024

 So, $n = 1024$
 QUESTION ANALYTICS

Q. 12
[Solution Video](#)
[Have any Doubt ?](#)


Consider a 5 stage pipeline with delays of 700, 800, 400, 500 and 450 pico seconds from first stage to last stage. To increase the performance, first stage divided into two parts of delays 350 and 350 pico seconds, and stage second divided into two parts of delays 400 and 400 pico seconds. Performance gain in the enhanced pipeline is _____.

 1.6

 Your answer is **Correct** 1.6

Solution :
 1.6

Old pipeline:

$$\text{Time to execute } n \text{ instructions} = (4 + n) 800 \text{ ps}$$

$$1 \text{ instruction execution time} = \frac{n}{(4+n)800} = \frac{1}{800} \text{ (for large } n\text{)}$$

New pipeline:

$$\text{Time to execute } n \text{ instructions} = (7 + n) 500 \text{ ps}$$

$$1 \text{ instruction execution time} = \frac{n}{(7+n)500} = \frac{1}{500} \text{ (for large } n\text{)}$$

$$\text{Performance gained} = \frac{\frac{1}{500}}{\frac{1}{800}} = \frac{800}{500} = 1.6$$

 QUESTION ANALYTICS

Q. 13
[Solution Video](#)
[Have any Doubt ?](#)


Consider a program requires 1000 memory references on a system with L_1 and L_2 cache. On execution of this program on system, there are 50 misses in L_1 cache and 10 misses in L_2 cache. Hit time of L_1 and L_2 cache are 2 cycles and 15 cycles respectively, and miss penalty of L_2 cache is 150 cycles. Which of the following is/are correct?

 A L_1 hit ratio = 0.95

 Your option is **Correct**

B L_2 hit ratio = 0.99

C L_2 miss ratio = $4 \times (L_1 \text{ miss ratio})$

Your option is Correct

D Average access cycles = 4.25 cycles

Your option is Correct

YOUR ANSWER - a,c,d

CORRECT ANSWER - a,c,d

STATUS - ✓

Solution :

(a, c, d)

$$L_1 \text{ miss ratio} = \frac{50}{1000} = 0.05$$

$$L_1 \text{ hit ratio} = 1 - L_1 \text{ miss ratio} = 0.95$$

$$L_2 \text{ miss ratio} = \frac{\text{Misses on } L_2}{\text{Misses on } L_1} = \frac{10}{50} = 0.2$$

$$L_2 \text{ hit ratio} = 1 - L_2 \text{ miss ratio} = 0.8$$

$$\begin{aligned} \text{Average access cycle} &= \text{Hit time}_{L_1} + \text{Miss rate}_{L_1} [\text{Hit time}_{L_2} + (\text{Miss rate}_{L_2} \times \text{Miss penalty}_{L_2})] \\ &= 2 + 0.5 [15 + (0.2 \times 150)] \\ &= 4.25 \text{ cycles} \end{aligned}$$

 QUESTION ANALYTICS

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Q. 14

 Solution Video

 Have any Doubt ?

Bookmark

Which of the following is incorrect?

A Memory and I/O devices have their own separate control lines in isolated I/O addressing mode.

B I/O modules signals an interrupt to processor on data line.

Your answer is Correct

Solution :

(b)

An interrupt can be signaled only on control lines.

C In interrupt-driven I/O technique, the data transferred from memory to I/O device or from I/O device to memory must pass through the processor.

D DMA technique is more efficient than interrupt-driven I/O and programmed I/O for transferring large amount of data from I/O device to memory or vice-versa.

 QUESTION ANALYTICS

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Q. 15

 Solution Video

 Have any Doubt ?

Bookmark

Consider a PC relative branch instruction which is 4 byte long. The address of this instruction is 12340567 in decimal. If the displacement in instruction is 2023 (in decimal), then the branch target address of this instruction is _____ (in decimal). [Assume memory is byte addressable]

12342594

Correct Option

Solution :

12342594

Address of this instruction = 12340567

Size of this instruction = 4 bytes

PC register contains address of next instruction to be executed. Address of next instruction to this instruction is $12340567 + 4 = 12340571$.

On execution of this instruction, PC will contain, address of next instruction.

So, $\text{PC} = 12340571$

Memory is byte-addressable.

So, Branch target address = $\text{PC} + \text{Displacement value}$
 $= 12340571 + 2023 = 12342594$

●

Your Answer is 12342591

 QUESTION ANALYTICS

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Q. 16

 Solution Video

 Have any Doubt ?

Bookmark

Consider the following code segment running on a pipelined processor with one branch delay slot:

I_1 : LOAD \$ r_2 , (1000)
 I_2 : LOAD \$ r_3 , (1020)
 I_3 : ADD \$ r_3 , \$ r_2 , \$ r_3
 I_4 : MUL \$ r_1 , \$ r_3 , \$ r_2
 I_5 : ADD \$ r_4 , \$ r_3 , \$ r_2
 I_6 : SUB \$ r_3 , \$ r_4 , \$ r_6
Jmp to label if ($r_1 == 0$)

Which instruction can occupy the delay slot without any modification in state or output of program?

A Only I_2

B Only I_5

Your answer is Correct

Solution :
(b)

C Either I_3 or I_5

D Either I_6 or I_3

QUESTION ANALYTICS

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Q. 17

Solution Video

Have any Doubt ?



Consider the following sequence of micro-operations (μO) on a system used for instruction fetch:

$\mu O1$: MAR \leftarrow PC
 $\mu O2$: MBR \leftarrow Mem[MAR]
 $\mu O3$: PC \leftarrow PC + 1
 $\mu O4$: IR \leftarrow MBR

where MAR is memory address register, PC is program counter, MBR is memory buffer register and IR is instruction register. And Mem[MAR] means reading data from memory location provided in MAR. Assume each μO takes 1 cycle. Which of the following μO 's can execute parallelly without conflict.

A $\mu O1$ and $\mu O2$

Your answer is IN-CORRECT

B $\mu O2$ and $\mu O4$

Your answer is IN-CORRECT

C $\mu O2$ and $\mu O3$

Your answer is Correct

D $\mu O3$ and $\mu O4$

Correct Option

YOUR ANSWER - a,b,c

CORRECT ANSWER - c,d

STATUS - ✘

Solution :

(c, d)
 $\mu O1$ and $\mu O2$ using MAR, so $\mu O2$ must after $\mu O1$.
 $\mu O1$ and $\mu O3$ have no common operands, so they can execute parallel. $\mu O3$ and $\mu O4$ have no common operand, so they can execute parallelly.
 $\mu O2$ and $\mu O4$ have MBR as common operand, so cannot execute parallelly.

QUESTION ANALYTICS

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Q. 18

Solution Video

Have any Doubt ?



Following is sequence of four instructions:

I_1 : ADD r_3 , r_2 , r_1 // $r_3 \leftarrow r_2 + r_1$
 I_2 : SUB r_2 , r_3 , r_1 // $r_2 \leftarrow r_3 - r_1$
 I_3 : ADD r_2 , r_3 , r_4 // $r_2 \leftarrow r_3 + r_4$
 I_4 : SUB r_5 , r_2 , r_4 // $r_5 \leftarrow r_2 - r_4$

Consider the following statements:

S_1 : There are true dependency in instruction pairs (I_1 , I_2) and (I_3 , I_4).
 S_2 : There is an output dependency between I_2 and I_3 .
 S_3 : There are anti dependency in instruction pairs (I_1 , I_2), (I_3 , I_4).

Which of the above statements are correct?

A Only S_2 and S_3

B Only S_1 , S_2

Your answer is Correct

Solution :

(b) True dependency:

 $I_1 \cdot r_3$ and $I_2 \cdot r_3$ $I_3 \cdot r_2$ and $I_4 \cdot r_2$

Output dependency:

 $I_1 \cdot r_2$ and $I_3 \cdot r_2$

Anti dependency:

 $I_1 \cdot r_2$ and $I_2 \cdot r_2$ $I_1 \cdot r_2$ and $I_3 \cdot r_2$ **C** Only S_2 **D** All S_1, S_2, S_3

QUESTION ANALYTICS

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Q. 19

Solution Video

Have any Doubt ?



Consider an instruction pipeline has 5 stages, namely Instruction fetch (IF), Instruction decode and register fetch (ID), ALU execution (EX), Memory access (MEM) and Register write-back (WB). Stages IF, ID, EX and WB takes 1 cycle in every type of instruction. If an instruction need to access the memory then stage MEM takes two cycles, otherwise one cycle. Consider the following sequence of instructions:

$$\begin{aligned} I_1 &: \text{LOAD } r_1, (1000) \quad // r_1 \leftarrow \text{Memory}[1000] \\ I_2 &: \text{LOAD } r_2, (1020) \quad // r_2 \leftarrow \text{Memory}[1020] \\ I_3 &: \text{ADD } r_3, r_1, r_2 \quad // r_3 \leftarrow r_1 + r_2 \\ I_4 &: \text{ADD } r_4, r_3, r_1 \quad // r_4 \leftarrow r_3 + r_1 \end{aligned}$$

The number of cycles required to execute above sequence of instruction on given pipeline without forwarding and with forwarding respectively are

A 14 cycles and 11 cycles**B** 14 cycles and 10 cycles**C** 16 cycles and 11 cycles

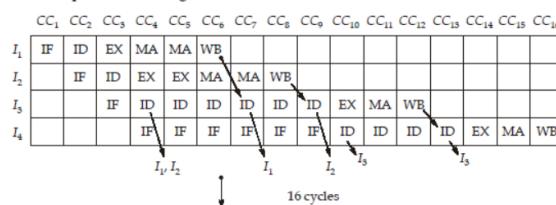
Your answer is Correct

Solution :

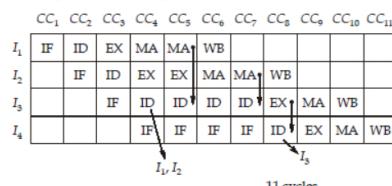
(c)

	IF	ID	EX	MA	WB
I_1	1	1	1	2	1
I_2	1	1	1	2	1
I_3	1	1	1	1	1
I_4	1	1	1	1	1

Without operand forwarding:



With operand forwarding:

**D** 15 cycles and 13 cycles

QUESTION ANALYTICS

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Q. 20

Solution Video

Have any Doubt ?



Consider a disk with 64 recording surfaces (0 – 63) having 2048 cylinders (0 – 2047), each track has 128 sectors (0 – 127), and each sector capacity is 512 bytes. Address format of a sector is <cylinder no., surface no., sector no.>, such that first and second sectors address are <0, 0, 0> and <0, 0, 1> respectively, and so on. Assume a file stored in disk in contiguous manner. Address of first and last sector of file are <15, 31, 64> and <20, 2, 3> respectively (both sectors inclusive). Approximate size of file is _____ KB.

Solution :
18954

A sector capacity = 2^9 B
A track capacity = Sectors per track × Sector size = $2^7 \times 2^9 = 2^{16}$ B
A cylinder size = Number of surfaces × Track capacity = $2^6 \times 2^{16} = 2^{22}$ B
(i) For 15th cylinder and 31st surfaces, size for 64 sectors from 64 to 127 = $2^6 \times 2^9 = 2^{15}$ B
(ii) On 15th cylinder 32 surfaces from 32 to 63 = $2^5 \times 2^{16} = 2^{21}$ B
(iii) 4 cylinders from 16 to 19 = $2^2 \times 2^{22} = 2^{24}$ B
(iv) On 20th cylinder 2 surfaces 0 to 1 = $2 \times 2^{16} = 2^{17}$ B
(v) On 20th cylinder 2nd surface 4 sectors from 0 to 3 = $4 \times 2^9 = 2^{11}$ B
Total file size = $(2^{14} + 2^{11} + 2^7 + 2^5 + 2^1) \times 2^{10}$ B = 18594 KB

Your Answer is 171646

 QUESTION ANALYTICS

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