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COMPUTER ORGANIZATION AND ARCHITECTURE (GATE 2023) - REPORTS

OVERALL ANALYSIS COMPARISON REPORT **SOLUTION REPORT**

ALL(33) CORRECT(19) INCORRECT(14) SKIPPED(0)

Q. 1

 Solution Video

 Have any Doubt ?



Which of the following method/process used by instruction scheduling technique to reduce data and control hazards?

A Use special hardware to detect hazard and issue instruction when possible.

B Schedule the execution of instruction only if there is no hazard.

C Compiler move the instructions around to fill the LOAD?Branch delay slots with meaningful instructions.

Your answer is **Correct**

Solution :

(c)

Instruction scheduling is a compiler technique in which instructions moved around with correct dependency to fill the delayed slots with meaningful instructions.

D If there is a hazard then stall the pipeline.

 QUESTION ANALYTICS



Q. 2

 Solution Video

 Have any Doubt ?



Consider a disk has average seek time of 10 ms and it rotates at 10000 revolutions per minute. There are 64 sectors per track and each sector capacity is 512 bytes. The average access time (with complete read) of a sector is _____ ms. [Rounded off upto 2 decimal places]

13.09

Your answer is **Correct** 13.09

Solution :

13.09

10000 revolutions take time = 60 sec

$$1 \text{ revolution take time} = \frac{60}{10000} \text{ sec} = 6 \text{ ms}$$

$$\text{Average rotational latency} = \frac{6}{2} = 3 \text{ ms}$$

$$\text{Read time for a sector} = \frac{\text{Revolution time}}{\text{Number of sectors}} = \frac{6 \text{ ms}}{64} = 0.09 \text{ ms}$$

$$\begin{aligned} \text{A sector access time} &= \text{Seek time} + \text{Average rotational latency} + \text{Read time} \\ &= 10 + 3 + 0.09 = 13.09 \text{ ms} \end{aligned}$$

 QUESTION ANALYTICS



Q. 3

 Solution Video

 Have any Doubt ?



Which of the following is incorrect for cache memory and main memory?

A If cache uses write-through technique, then main memory always remains valid.

B Dirty bit required for each cache line in write-through based cache memory.

Correct Option

Solution :

(b)

Dirty bit required in write-back method.

C If dirty bit of a cache block is set, then data in this block may be different than data in corresponding block in main memory.

Your answer is **IN-CORRECT**

D If cache uses write-back technique, then I/O modules can access main-memory only through the cache.

 QUESTION ANALYTICS



Q. 4

▶ Solution Video

⌚ Have any Doubt ?



Consider the following statements:

 S_1 : Conflict misses can be reduced by increasing value of cache associativity. S_2 : On increasing block size of cache, miss penalty also increases. S_3 : Increasing in block size of cache always decrease miss rate.

Which of the above statements are false?

 A Only S_3

Your answer is Correct

Solution :

(a)

On continuous increase in block size leads to less cache lines. And it increases the competition for cache lines, which can result as high miss rate. Also, if block is too big then on a miss it replace block of size greater than spatial locality and unnecessary locations loaded in cache. If block size is large, then replacement will also take more time, so high miss penalty. Small increment in block size can be beneficial. But, after a limit, it will lead to high miss rate. And, question mentioned always.

 B Only S_2 C Only S_1 and S_3 D None of the statement is false

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Q. 5

▶ Solution Video

⌚ Have any Doubt ?

Consider a system in which an instance value in register R_1 is 2000 and value at in memory location 2000 (in decimal) is 3000. Consider the following instruction used register indirect addressing mode:**LOAD R_2 , (R_1)**Let x is effective address for above instruction in decimal and y is value in register R_2 just after completion of above instruction. The value of $x + y$ is _____. (R_2 is destination register in above instruction) 5000

Your answer is Correct5000

Solution :

5000

Instruction used register indirect addressing mode, so

$$R_2 \leftarrow \text{Memory}[R_1]$$

$$R_2 \leftarrow \text{Memory}[2000]$$

$$R_2 \leftarrow 3000$$

So,

$$R_2 = 3000 = y$$

Here effective address is value in R_1 , which is 2000, so

$$x = 2000$$

So,

$$x + y = 2000 + 3000 = 5000$$

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Q. 6

? FAQ

▶ Solution Video

⌚ Have any Doubt ?



Consider a system with 16 bit physical address space and uses memory-mapped I/O configuration. Assume that at current instance system has 8 interface units and each unit with 6 registers. Address space with value 11 (in binary number) in two highest order bits (most significant bits) is reserved for I/O interfaces. Assume each interface does not need any other space other than 6 registers. Which of the following allocated address range is valid for above given interfaces? (address range in hexadecimal and memory is word-addressable)

 A 0000 to 003F

Your answer is IN-CORRECT

 B C000 to C007 C C000 to C03F

Correct Option

Solution :

(c)

Memory-mapped I/O used, so a registers of interfaces is actually a word in memory.

Bits required for interface identity

$$= \log_2 (\text{Number of interfaces})$$

$$= \log_2 (8) = 3 \text{ bits}$$

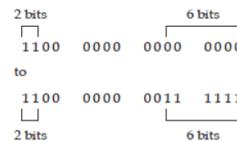
Bits required for particular register in an interface

$$= \lceil \log_2 (\text{Number of register}) \rceil$$

$$= \lceil \log_2 (6) \rceil = 3 \text{ bits}$$

For current system, interfaces need 6 bits for uniqueness in I/O operations. (11)₂ in two-highest order bits is necessary as it is allocated for I/O.

Address range:



So, C000 to C03F is correct.

- (d) and (b) has less address space.
- (a) is allocated for main-memory.

D FFF8 to FFFF

QUESTION ANALYTICS

Q. 7

Solution Video

Have any Doubt ?



Which of the following methods can be used to reduce impact of hazards in pipeline of a processor?

A Use data forwarding in pipeline

Your option is Correct

B Instruction scheduling by compiler

Your option is Correct

C Register renaming

Your option is Correct

D Separate instruction memory and data memory

Your option is Correct

YOUR ANSWER - a,b,c,d

CORRECT ANSWER - a,b,c,d

STATUS -

Solution :

- (a, b, c, d)
- (a) From data hazards
- (b) Mainly for data hazards
- (c) For data hazards
- (d) For structure hazards

QUESTION ANALYTICS



Q. 8

Solution Video

Have any Doubt ?



Consider a 2-way set associative cache memory with 32 blocks and uses first-in-first-out (FIFO) replacement algorithm. Initially the cache is empty. A program access following physical blocks in given order:

16, 1, 17, 15, 31, 0, 17, 32, 47, 1, 0, 16
Which of the following is correct?

A Compulsory misses = 6
Conflict misses = 3

B Compulsory misses = 7
Conflict misses = 2

C Compulsory misses = 8
Conflict misses = 1

Your answer is Correct

Solution :

(c)

$$\text{Number of sets} = \frac{\text{Number of blocks}}{\text{Associativity}} = \frac{32}{2} = 16$$

So, sets are from 0 to 15.

Set number	16	17	15	31	0	17	32	47	1	0	16
0											
1											
...											
15											

$C_1 \Rightarrow$ Compulsory misses

$C_2 \Rightarrow$ Conflict misses

16	1	17	15	31	0	17	32	47	1	0	16
C_1	C_1	C_1	C_1	C_1	C_1	Hit	C_1	C_1	Hit	Hit	C_2

Number of $C_1 = 8$
Number of $C_2 = 1$

D Compulsory misses = 8
Conflict misses = 2

QUESTION ANALYTICS

Q. 9

Solution Video

Have any Doubt?



Consider a non-pipelined processor with clock rate of 3 GHz and an average cycles per instruction (CPI) of 3. To upgrade this processor, a 6 stage pipeline introduced. But, due to internal pipeline delays, clock rate of new processor has reduced to 2.67 GHz. The speedup achieved by new processor for a program with large number of instructions is _____ (approx). [Upto two decimal places]

2.67 [2.66 - 2.68]

Correct Option

Solution :

2.67 [2.66 - 2.68]

Let a program has n instructions.

Non-pipelined:

$$\begin{aligned} \text{CPI} &= 3 \\ \text{Rate} &= 3 \text{ GHz} \end{aligned}$$

$$\begin{aligned} \text{Time for } n \text{ instructions} &= \frac{\text{CPI}}{\text{Rate}} \times n \\ &= \frac{3}{3 \text{ GHz}} \times n \\ &= 10^{-9} \times n \text{ sec} \end{aligned}$$

Pipelined (6 stage = k)

$$\text{Time for } n \text{ instructions} = (k + n - 1) \times \text{Clock period}$$

$$= (6 + n - 1) \times \frac{1}{2.67 \text{ GHz}}$$

$$\text{Speedup} = \frac{\text{Time taken by non-pipelined}}{\text{Time taken by pipelined}}$$

$$= \frac{10^{-9} \times n}{(5 + n) \frac{1}{2.67 \text{ GHz}}}$$

For large n speedup = 2.67

Your Answer is 2.67

QUESTION ANALYTICS

Q. 10

Solution Video

Have any Doubt?



Consider the following load instruction in a system with indirect addressing mode:

load \$r_1, @ (2023)

where r_1 is register, and 2023 is memory address. IR is instruction register and IR (address field) is value in address field of IR. Assume above instruction is already in IR, so IR (address field) value is 2023.

Which of the following sequence of micro-operation perform the task of above given instruction in IR?

A MAR $\leftarrow r_1$
MBR \leftarrow Memory
MAR \leftarrow MBR
MBR \leftarrow Memory
 $r_1 \leftarrow$ MBR

B MAR \leftarrow IR (address field)
MBR \leftarrow Memory
 $r_1 \leftarrow$ MBR

C MAR \leftarrow PC
MBR \leftarrow Memory
MAR \leftarrow MBR
MBR \leftarrow Memory
 $r_1 \leftarrow$ MBR

D MAR \leftarrow IR (address field)
MBR \leftarrow Memory
MAR \leftarrow MBR

Your answer is Correct

MBR \leftarrow Memory
 $r_1 \leftarrow$ MBR

Solution :

(d)

For load $\$r_1, @ (2023)$ with indirect addressing

$r_1 = \text{Memory}[\text{Memory}[2023]]$... (a)

Steps for (a)

- (i) $[2023] == \text{MAR} \leftarrow \text{IR} \text{ (address field)}$
- (ii) $\text{Mem}[2023] == \text{MBR} \leftarrow \text{Memory}$
- (iii) $[\text{Mem}[2023]] == \text{MAR} \leftarrow \text{MBR}$
- (iv) $\text{Mem}[\text{Mem}[2023]] == \text{MBR} \leftarrow \text{Memory}$
- (v) $r_1 = \text{Mem}[\text{Mem}[2023]] == r_1 \leftarrow \text{MBR}$

 QUESTION ANALYTICS

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