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COMPUTER ORGANIZATION AND ARCHITECTURE (GATE 2023) - REPORTS

[OVERALL ANALYSIS](#) [COMPARISON REPORT](#) **SOLUTION REPORT**

ALL(33) CORRECT(19) INCORRECT(14) SKIPPED(0)

Q. 21

 [Solution Video](#)

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Consider a processor with clock rate of 12.6 MHz. This processor executes average 0.4 instructions per clock cycle if there is no memory access in instructions. Assume a program X in which 20% instructions require only one memory access and 5% instructions require two memory accesses. Assume a one-cycle delay for each memory access. The performance of this processor on execution of program X is _____ MIPS.

4.5

Correct Option

Solution :

4.5

Instructions per cycle (IPC) = 0.4

$$CPI = \frac{1}{IPC} = \frac{1}{0.4} = 2.5$$

$$\begin{aligned} \text{Average memory access per instruction} &= \frac{20}{100} \times 1 + \frac{5}{100} \times 2 \\ &= 0.2 + 0.1 = 0.3 \end{aligned}$$

Cycles required for 0.3 memory access = $0.3 \times 1 = 0.3$ cycles

So, an instruction requires 0.3 extra for memory access other than execution.

Cycle per instruction without memory access = 2.5

Cycle per instruction with memory access in program X = $2.5 + 0.3 = 2.8$ CPI

$$\text{MIPS} = \frac{\text{Clock rate}}{\text{CPI} \times 10^6} = \frac{12.6 \times 10^6}{2.8 \times 10^6} = 4.5$$

Your Answer is 105

 [QUESTION ANALYTICS](#)



Q. 22

 [Solution Video](#)

 [Have any Doubt ?](#)



Consider a system has 8 registers, a shifter with 8 operations, and an ALU (Arithmetic Logic Unit) with 16 operations, all connected to common bus system. System uses three-address format and assume micro-programmed control word for micro-operation contains bits only for registers, ALU, and shifter. The length of the micro-programmed control-word in this system is

A 10 bits

Your answer is IN-CORRECT

B 16 bits

Correct Option

Solution :

(b)

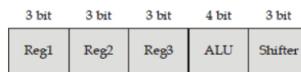
Register address = \log_2 (Number of registers) = $\log_2 (8) = 3$

Micro-programming is used, so

Bits for ALU micro-operation = \log_2 (Number of micro-operations) = $\log_2 (16) = 4$

Bits for shifter micro-operations = $\log_2 (8) = 3$

System uses 3-address format, an instruction needs 3 registers. So, control word will be



Length of control word = $3 + 3 + 3 + 4 + 3 = 16$ bits

C 32 bits

D 14 bits

 [QUESTION ANALYTICS](#)



Q. 23

 [Solution Video](#)

 [Have any Doubt ?](#)



Consider a DMA controller has data count register of size 16 bits. The memory of system is byte addressable. Processor need to transfer a 2023 KBytes size file to a I/O device through DMA. How many minimum number of times DMA takes control over system bus to transfer this file?

Solution :

32

Data register size is 16 bits, so maximum data transfer possible in one DMA request
 $= 2^{16} \text{ bytes} = 64 \text{ KBytes}$
 Minimum number of DMA requests to send 2023 KB size file = $\left\lceil \frac{2023 \text{ KB}}{64 \text{ KB}} \right\rceil = 32$

Q. 24**Solution Video****Have any Doubt ?****QUESTION ANALYTICS****A** 3454 B**B** 4864 B**C** 4224 B

Your answer is IN-CORRECT

D 4352 B

Correct Option

Solution :

(d)

$$\begin{aligned}\text{Block offset} &= \log_2 (\text{Data block size}) \\ &= \log_2 (32) = 5 \text{ bits} \\ \text{Set length} &= \log_2 \left(\frac{\text{Number of cache blocks}}{\text{Associativity}} \right) \\ &= \log_2 \left(\frac{128}{4} \right) = 5 \text{ bits} \\ \text{Physical address length} &= \log_2 \left(\frac{\text{Memory size}}{\text{Addressable size}} \right) \\ &= \log_2 \left(\frac{16 \text{ MB}}{1 \text{ B}} \right) = 24 \text{ bits} \\ \text{Tag field length} &= \text{Physical address length} - \text{Set length} - \text{block offset} \\ &= 24 - 5 - 5 = 14 \text{ bits} \\ \text{One block size} &= \left(\frac{\text{Tag bits} + \text{Extra bits}}{8} \right) + \text{Data size} \\ &= \left(\frac{14+2}{8} \right) + 32 \text{ Bytes} \\ &= 2 + 32 = 34 \text{ Bytes} \\ \text{Total cache size (128 blocks)} &= 34 \times 128 \text{ bytes} = 4352 \text{ B} \\ &= 4.25 \text{ KB}\end{aligned}$$

QUESTION ANALYTICS**Q. 25****Solution Video****Have any Doubt ?**

Consider a magnetic disk in which seek time of disk is T_s , rotation speed is R in revolutions per second, N_t is number of bytes per track, and N_s is number of bytes per sector. The average time required to read two adjacent sectors on a single track is (assume a track has more than two sectors)

A $T_s + \frac{1}{2R} + \frac{2 \times N_s}{R \times N_t}$

Your answer is Correct

Solution :

(a)

Time to reach a track (seek time) = T_s ... (i)
 R revolutions per second.

So, $\frac{1}{R}$ seconds per revolution.

Average rotation time (to reach a sector) = $\frac{1}{2} \times (1 \text{ revolution time}) = \frac{1}{2R}$... (ii)

In one revolution, disk reads whole track,

$$N_t \text{ bytes readable in } = \frac{1}{R} \text{ seconds}$$

$$N_s \text{ bytes readable in } = \frac{N_s}{R \times N_t} \quad \dots \text{(iii)}$$

From (i), (ii), (iii)

Average time to read two adjacent tracks = Seek time + Average rotation time + Time to read two sectors

$$= T_s + \frac{1}{2R} + 2 \times \frac{N_s}{R \times N_t}$$

B $T_s + \frac{1}{R} + \frac{N_t}{R \times N_s}$

C $T_s + \frac{1}{R} + \frac{N_s}{R \times N_t}$

D $T_s + \frac{R}{2} + \frac{2 \times R \times N_s}{N_t}$

QUESTION ANALYTICS

Q. 26

Solution Video

Have any Doubt?



Consider a processor with clock rate of 1.8 MHz. This processor operates generally at 20 MIPS rating. What is the effective Cycles Per Instruction (CPI) of this processor? [Upto two decimal places]

A 0.09

Correct Option

Solution :
0.09

$$\text{MIPS} = \frac{\text{Clock rate}}{\text{CPI} \times 10^6}$$

$$\text{CPI} = \frac{\text{Clock rate}}{\text{MIPS} \times 10^6}$$

$$= \frac{1.8 \times 10^6}{20 \times 10^6} = 0.09$$

Your Answer is 11.11

QUESTION ANALYTICS

Q. 27

Solution Video

Have any Doubt?



Consider a 32 bit load instruction in a system. This instruction uses direct addressing and address field length is 16 bits. This instruction uses address value given in address field without any change in address, like shifting, rotating, etc. Use address value as it is in instruction. Address space of this system is 32 bit. Which of the following address cannot be used in above given load instruction? (Following address are in decimal)

A 65536

Your answer is Correct

Solution :

(a)

$2^{16} = 65536$ to represent 65536 in binary format 17 bits requires. But above instruction have only 16 bits for address field. Above instruction can access address from 0 to $2^{16} - 1$.

B 0

C 32768

D None of the above

QUESTION ANALYTICS

Q. 28

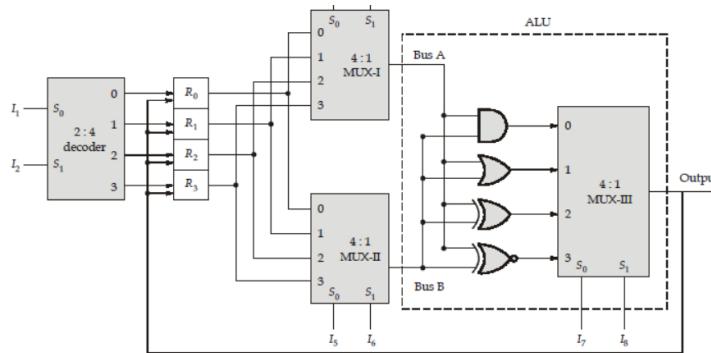
Solution Video

Have any Doubt?



Consider the following block diagram of part of a databath in a system:





Where R_0 , R_1 , R_2 and R_3 are registers, I_1 to I_8 are inputs to databath using control word. Selector S_0 is least significant in all mux and decoder. Assume control word consists only inputs given above. Following is 8 bit control word representation.

I_8	I_7	I_6	I_5	I_4	I_3	I_2	I_1
-------	-------	-------	-------	-------	-------	-------	-------

Which of the following is/are correct?

- A Control word 00010111 execute
 $R_3 \leftarrow R_1 \text{ AND } R_1$ Correct Option

B Control word 01111000 execute
 $R_0 \leftarrow R_2 \text{ OR } R_3$ Your option is Correct

C Control word 10000110 execute
 $R_2 \leftarrow R_1 \text{ XOR } R_0$ Correct Option

D Control word 11111101 execute
 $R_1 \leftarrow R_3 \text{ XNOR } R_3$ Correct Option

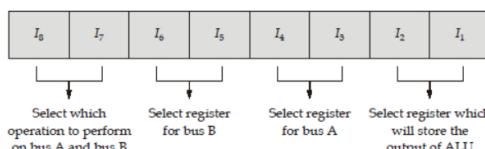
YOUR ANSWER - b

CORRECT ANSWER - a.b.c.d

STATUS -

Solution :

(a, b, c, d)
Control word:



I_2	I_1	Register for o/p
0	0	R_0
0	1	R_1
1	0	R_2
1	1	R_3

I_4	I_3	Bus A
0	0	R_0
0	1	R_1
1	0	R_2
1	1	R_3

I_6	I_5	Bus B
0	0	R_0
0	1	R_1
1	0	R_2
1	1	R

I_8	I_7	Operation in ALU
0	0	AND
0	1	OR
1	0	XOR
1	1	XNOR

Use above information to get answer.

 QUESTION ANALYTICS

30

 Solution Video

Have any Doubt ?

Consider a system has a 4 MBytes byte-addressable main-memory and a 4 KBytes 4-way setassociative cache memory with block size of 64 bytes. An array $A[.]$ has 350 elements and each element size is 8 bytes. Base address of $A[.]$ is 0x00000000 (in hexadecimal). Assume cache is initially empty and now array $A[.]$ is stored in cache. Find the number of sets in which three blocks of a particular set are occupied by element of $A[.]$?

Solution :

Correct Option

Solution :

$$\begin{aligned}\text{Address length} &= \log_2 \left(\frac{\text{Memory size}}{\text{Addressable size}} \right) \\ &= \log_2 \left(\frac{4 \text{ MB}}{1 \text{ KB}} \right) = 22 \text{ bits}\end{aligned}$$

$\sigma_2(1B) =$

$= \log_2 (64 \text{ Bytes}) = 6 \text{ bits}$
 Number of blocks in cache = $\frac{\text{Cache size}}{\text{Block size}} = \frac{4 \text{ KB}}{64 \text{ B}} = 64$
 Number of cache sets = $\frac{\text{Number of blocks}}{\text{Associativity}} = \frac{64}{4} = 16$
 Bits in set = $\log_2 (\text{Number of sets}) = \log_2 (16) = 4$
 Let array is $A[0, \dots, 349]$, number of array element per blocks
 $= \frac{\text{Block size}}{\text{Element size}} = \frac{64 \text{ B}}{8 \text{ B}} = 8$
 Address of array start from 0x000000, so following is the mapping
 (1) $A[0]$ to $A[7]$ in 1st block of set = 0
 (2) $A[8]$ to $A[15]$ in 1st block of set = 1
 :
 (16) $A[120]$ to $A[127]$ in 1st block of set = 15
 (17) $A[128]$ to $A[135]$ in 2nd block of set = 0
 :
 $A[248]$ to $A[255]$ in 2nd block of set = 15
 $A[256]$ to $A[263]$ in 3rd block of set = 0
 :
 $A[344]$ to $A[349]$ in 3rd block of set = 11
 So, set from 0 to 11 have three block in each set occupied by $A[]$.
 So, 12 sets is answer.

Your Answer is 14

QUESTION ANALYTICS

Q. 30

Solution Video

Have any Doubt?



Consider a system in which bus cycle takes 250 ns. Transfer of bus control in either direction, from processor to DMA controller or vice-versa, takes 100 ns. The system is byte addressable. Assume DMA transfer 1 byte in cycle stealing mode. What is the time in ns (nanoseconds) required to transfer 1 byte from memory to a I/O device using DMA in cycle stealing mode (time from the instance processor start to transfer control of system bus to DMA, to instance processor get back the control on system bus after data transfer)?

450

Your answer is Correct 450

Solution :

450

Total time to transfer 1 byte = Time taken to transfer control of system bus from processor to DMA + One bus cycle time + Time taken to transfer control of system bus from DMA to processor
 $= 100 + 250 + 100 = 450 \text{ ns}$
 In cycle stealing mode DMA use only one bus cycle of system bus.

QUESTION ANALYTICS

Item 21-30 of 33 « previous 1 2 3 4 next »