Abhrajyoti Kundu
Computer Science & IT (CS)

COMPUTER ORGANIZATION AND ARCHITECTURE-1 (GATE 2023) - REPORTS

OVERALL ANALYSIS | COMPARISON REPORT | SOLUTION REPORT

ALL(17) | CORRECT(14) | INCORRECT(2) | SKIPPED(1)

Q. 11 Solution Video | Have any Doubt ?

Consider an accumulator based architecture in which ADD, DIV, LOAD, SUB, MUL and STORE operations take memory address for operand field in instruction. Find the minimum number of instructions required for following expression in this architecture?

$$P = \left(\frac{Q+R}{S}\right)+T$$

Where *P, Q, R, S, T* are memory address?

A 4

B 5 — Correct Option

Solution :
(b)

ACC is accumulator register:

```
LOAD Q      //  ACC ← M[Q]
ADD R       //  ACC ← ACC + M[R]
DIV S       //  ACC ← ACC / M[S]
ADD T       //  ACC ← ACC + M[T]
STORE P     //  M[P] ← ACC
```

C 6

D 7 — Your answer is **IN-CORRECT**

QUESTION ANALYTICS +

Q. 12 Solution Video | See your Answers

Consider a pipelined processor with 5 stages: (i) Instruction fetch (IF), (ii) Instruction decode (ID), (iii) ALU execution (EXE), (iv) Memory access (MEM), (v) Write back to register (WB). Processor uses operand forwarding from EXE and MEM stages wherever operand available.
Consider the following sequence of instructions:

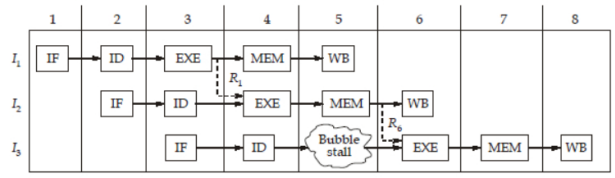
I_1 : ADD R_1, R_1, 100 // $R_1 \Leftarrow R_1 + 100$
I_2 : LOAD R_6, 0(R_1) // $R_6 \Leftarrow$ MEM[R_1 + 0]
I_3 : ADD R_4, R_6, R_5 // $R_4 \Leftarrow R_6 + R_5$

Assume every stage of above processor takes 1 cycle and memory is allowed to access only at MEM stage.
If we execute above sequence of instructions on given processor then number of cycles required are

A 7

B 8 — Your answer is **Correct**

Solution :
(b)



I[st] forwarding: Value of R_1 available after EXE stage
II[nd] forwarding: Value of R_6 of I_2 available after MEM stage, because in LOAD operation data come from memory.

C 9

D 10

QUESTION ANALYTICS +

Q. 13 Solution Video Have any Doubt ?

Consider a pipelined processor with 5 stages in pipeline and 1 cycle for each stage.
Assume a program with large number of instructions have 20% branch instructions. A branch instruction stalls 4 stages if processor run using without optimization and stalls 1 stage if processor run using with optimization. Speedup gain by with optimization over without optimization.

A 4.0

B 1.5 Your answer is Correct

Solution :
(b)
Time for n instructions without optimization.

$$t_{nf} = 5 - 1 + n + 0.2 \times n \times 4$$
$$= 4 + n + 0.8 \times n = 4 + 1.8\,n$$

Time for n instructions with optimization.

$$t_f = 5 - 1 + n + 0.2 \times n \times 1$$
$$= 4 + n + 0.2\,n = 4 + 1.2\,n$$

Speedup with optimization over without optimization.

$$s = \frac{t_{nf}}{t_f} = \frac{4+1.8n}{4+1.2n}$$

For large n

$$s = \lim_{n\to\infty} \frac{4+1.8n}{4+1.2n} = \lim_{n\to\infty} \frac{n\left(\frac{4}{n}+1.8\right)}{n\left(\frac{4}{n}+1.2\right)} = \frac{1.8}{1.2} = 1.5$$

C 1.14

D 1.11

QUESTION ANALYTICS +

Q. 14 Solution Video Have any Doubt ?

Consider a system with 16 bit instruction length and 32 registers. The instruction set have three categories of instructions. First category consists 30 instructions each with 2 registers as operands. Second category consists 3 instructions each with 1 register and a 8 bit immediate field as operands. Third category consists N instructions each with a 8 bit immediate field as operand field. Find maximum possible value of N.

40 Your answer is Correct40

Solution :
40
16 bit instruction length.
32 registers, so register address need 5 bit.

- **1st category instructions:** 30 instructions
  2 register operands, so 10 bits for operands and 6 bit left for opcode.
  For 6 bit opcode, 2^6 instructions possible. 1st category contains 30 instructions.
  Number of instruction for 6 bit opcode left after removing 1st category instructions.
  $= 2^6 - 30 = 64 - 30 = 34$ ...(1)
- **2nd category instructions:** 3 instructions
  5 bit for register and 8 bit for immediate operand, 3 bit left for opcode. But above we consider 6 bit opcode. Here we convert 3 bit opcode to 6 bit by considering total instruction in this category = Actual number of instructions $\times$ $2^{(6\text{ bit} - 3\text{ bit})}$
  $= 3 \times 2^3 = 24$ instructions
  we are doing this because $2^{(6\text{ bit} - 3\text{ bit})}$ instruction encoding is used by operands of this category (2^{nd}).

  So, now instruction left for 6 bit opcode after removing 1st and 2nd category
  $= 34 - 24 = 10$ ...(2)
- **3rd category:** 8-bit immediate operand, so 8-bit for opcode. But above we considered 6 bit for opcode. So, here we can add 2 more bits on opcode.
  From (2), 10 instruction left if we consider 6 bit opcode.
  Number of instructions after increment of 2 bits in opcode.
  $=$ (Old number of instructions) $\times$ 2^x
  where 'x' is bits increment in opcode
  $= 10 \times 2^2 = 40$ instructions
  So category three has 40 maximum possible instructions.

So, $N = 40$

QUESTION ANALYTICS +

Q. 15 Solution Video Have any Doubt ?

A processor consists 3 categories of instructions x, y and z with CPI (cycles per instruction) 1.4, 1.5 and 2.0 respectively. This processor runs at 3.2 GHz clock rate. A program has 25, 10 and 15 million instructions of category x, y and z respectively. Find the million instructions per second (MIPS) rating of processor for this program?

2000 — Your answer is **Correct** 2000

Solution :
2000

	x	y	z
CPI	1.4	1.5	2.0
Instruction count (in million)	25	10	15

$$\text{Average cycles per instruction } (CPI_{avg}) = \frac{25\times1.4+10\times1.5+15\times2.0}{25+10+15}$$

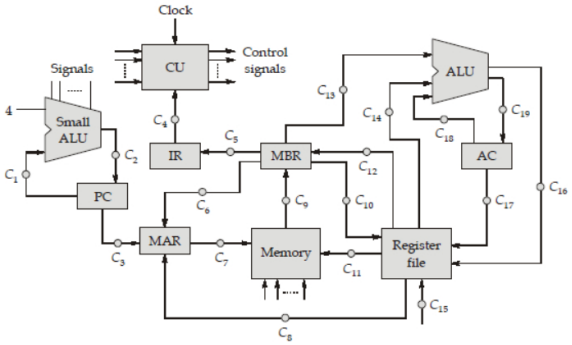
$$= \frac{35.0+15.0+30.0}{50} = \frac{80}{50} = 1.6 \text{ cycles/instruction}$$

$$MIPS = \frac{\text{Clock rate}}{CPI_{avg}\times10^6} = \frac{3.2\times10^9}{1.6\times10^6} = 2\times10^3 = 2000$$

QUESTION ANALYTICS +

Q. 16 — Solution Video — Have any Doubt ?

Consider the following data path with control signals for a system:



Following two micro-operations are executing parallely in above given system.
MBR ← Mem[MAR]
PC ← PC + 4
Where MBR is memory buffer register, MAR is memory address register, PC is program counter and Mem[MAR] read data from memory location in MAR.
Find active control signals from C_1 to C_{19} on executing above two micro-instructions parallely?

A C_1, C_2, C_{12}

B C_1, C_2 — Your option is **Correct**

C C_7, C_9, C_4

D C_7, C_9 — Your option is **Correct**

YOUR ANSWER - b,d | CORRECT ANSWER - b,d | STATUS - ✓

Solution :
(b, d)
C_1, C_2 used for PC ← PC + 1
C_7, C_9 used for MBR ← Mem[MAR]

QUESTION ANALYTICS +

Q. 17 — Solution Video — Have any Doubt ?

At a particular instance in a system R_1 = 2000, R_2 = 1000, content of memory location 1000 and 2000 is 2000 and 5 respectively, and PC = 1000. R_1 and R_2 are registers and PC is program counter of this system. Consider following conditions:

(i) x is effective address when R_1 is in instruction with register indirect addressing mode (AM).
(ii) y is effective address when R_2 is in instruction with indirect AM.
(iii) z is effective address when 2000 is in instruction with direct AM.
(iv) w is effective address when 2000 is in instruction with relative AM.

Which of the following is/are correct value for effective addresses?

x = 2000

A x = 2000 Your option is Correct

B y = 2000

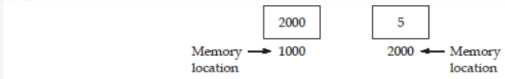
C z = 2000 Your option is Correct

D $w = 2000$

YOUR ANSWER - a,c | CORRECT ANSWER - a,c | STATUS -

Solution :

(a, c)



$R_1 = 2000, R_2 = 1000$

PC = 1000

(i) Register indirect AM

Effective address (EA) = Content of register (R_1)

= 2000

(iii) Direct AM

EA = Memory location in instruction

= 2000

(iv) Relative AM

EA = PC + Address in instruction

= 1000 + 2000 = 3000

QUESTION ANALYTICS +