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COMPUTER ORGANIZATION AND ARCHITECTURE (GATE 2023) - REPORTS

OVERALL ANALYSIS | COMPARISON REPORT | SOLUTION REPORT

ALL(33) | CORRECT(19) | INCORRECT(14) | SKIPPED(0)

Q. 31 Solution Video | Have any Doubt ?

Which of the following statement is false?

A. Loops in a program arises temporal locality.

B. In set-associative mapping, a main memory block can be placed in any block of cache. — Correct Option

Solution :
(b)
In set-associative mapping, a main-memory block can be placed in any block of selected set.

C. Sequential execution of a program arises spatial locality. — Your answer is **IN-CORRECT**

D. Fully-associative mapping requires associative memory for implementation.

QUESTION ANALYTICS +

Q. 32 Solution Video | Have any Doubt ?

Consider two systems A and B and a program X. System A and system B use 4 and 17 processors respectively. 80% and P% of program X can execute parallely on system A and B respectively. Speedup achieved by system B with respect to system A on executing program X is 2. Then the value of P is _____ (%).

85 — Correct Option

Solution :
85

$$\text{Speedup achieved by system } A \text{ w.r.t. single processor } (S_A) = \frac{1}{0.2+\frac{0.8}{4}} = \frac{1}{0.2+0.2} = 2.5$$

$$\text{Speedup achieved by system } B \text{ w.r.t. single processor } (S_B) = \frac{1}{\left(1-\frac{P}{100}\right)+\frac{\left(\frac{P}{100}\right)}{17}}$$

$$\Rightarrow \text{Speedup of system } B \text{ w.r.t. system } A \ (S_{B\to A}) = \frac{S_B}{S_A}$$

$$\Rightarrow 2 = \frac{\left[\frac{1}{\left(1-\frac{P}{100}\right)+\frac{\left(\frac{P}{100}\right)}{17}}\right]}{2.5}$$

$$\Rightarrow 1+\frac{P}{100}\left(\frac{1}{17}-1\right) = \frac{1}{5}$$

$$\Rightarrow \frac{P}{100}\left(1-\frac{1}{17}\right) = 0.8$$

$$\Rightarrow P = \frac{0.8\times 100}{16}\times 17 = 5\times 17 = 85$$

Your Answer is 17

QUESTION ANALYTICS +

Q. 33 Solution Video | Have any Doubt ?

A non-pipelined processor has average CPI of 3 cycles and clock rate of 2 GHz. After upgrade,processor converted to 5 stage pipeline to latencies 0.3 ns, 0.4 ns, 0.45 ns, 0.75 ns, 0.55 ns. Consider a program has 30% branch instruction and it lead to 2 stage penalty. All other instruction have no penalties. Assume program has large number of instructions. Approximate speedup achieved by new processor over old processor on execution of this program is

A. 1.5

B 2.0

C 2.5

D 1.25 Your answer is **Correct**

Solution :
(d)
For large n instructions:
Time taken by non-pipelined

$$= \text{CPI} \times \text{Clock period} \times n$$

$$= 3 \times \frac{1}{2\ \text{GHz}} \times n = (1.5 \times n)\ \text{ns}$$

Time taken by pipelined

$$= (5 + n - 1 + 0.3 \times n \times 2) \times 0.75\ \text{ns}$$

$$= (4 + 1.6 \times n) \times 0.75\ \text{ns}$$

$$\text{Speedup} = \lim_{n \to \infty} \frac{1.5 \times n}{(4 + 1.6 \times n)0.75} \approx \frac{1.5}{1.6 \times 0.75} = 1.25$$

QUESTION ANALYTICS +