



**Abhrajyoti Kundu**  
 Computer Science & IT (CS)

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## COMPUTER ORGANIZATION AND ARCHITECTURE-2 (GATE 2023) - REPORTS

[OVERALL ANALYSIS](#) [COMPARISON REPORT](#) **SOLUTION REPORT**

ALL(17) CORRECT(13) INCORRECT(4) SKIPPED(0)

**Q. 1**

 [Solution Video](#)

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Consider a system with byte addressable main memory and size of all instructions are 32 bit.

Consider following instructions:

**ADD R<sub>1</sub>, A**      //  $R_1 = R_1 + \text{Mem}[A]$

where  $R_1$  is register and  $A$  is a memory address and  $\text{Mem}[A]$  is reading value of memory address  $A$ . This instruction stored at memory location 2460 H and  $A$  is a memory location with address 4408 H, both are in hexadecimal notation.

What are the values of Program Counter (PC) and Memory Address Register (MAR) during execution of this instruction but after calculating effective address?

**A** PC = 2464 H, MAR = 4408 H

Your answer is Correct

**Solution :**

(a)

Just before fetching given instruction PC = 2460 H

Just after fetching given instruction PC = PC + 4 = 2460 + 4 = 2464 H because instruction size is 4 bytes (32 bits).

Mem[A] is using direct addressing mode.

So, Effective address = A = 4408 H

Now to read value of location A system has to make MAR = A = 4408 H.

**B** PC = 2460 H, MAR = 4400 H

**C** PC = 2464 H, MAR = 4400 H

**D** PC = 2460 H, MAR = 4408 H

 [QUESTION ANALYTICS](#)



**Q. 2**

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Consider the following table for two systems A and B:

	Word size	Main memory (MM)	Addressability
System A	4 bytes	4 GB	Byte addressable
System B	4 bytes	16 GB	Word addressable

$x$  and  $y$  are number of bits used to represent address of a memory location in system A and B respectively. Value of  $x$  and  $y$  are

**A**  $x = 32, y = 32$

Your answer is Correct

**Solution :**

(a)

**System A:**

It is byte addressable and 4 GB in size of memory.

So number of addressable locations in memory

$$= \frac{\text{Memory size}}{\text{Addressable size}} = \frac{4 \text{ GB}}{1 \text{ byte}} = 4 \text{ GB} = 2^{32}$$

Number of bits required for  $2^{32}$  locations =  $\log_2 (2^{32}) = 32$  bits

So,  $x = 32$

**System B:**

It is word addressable, word size is 4 bytes and 16 GB in size of memory, so number of addressable locations in memory

$$= \frac{16 \text{ GB}}{4 \text{ bytes}} = 4 \text{ GB} = 2^{32}$$

Number of bits required for  $2^{32}$  locations =  $\log_2 (2^{32}) = 32$  bits

So,  $y = 32$

**B**  $x = 32, y = 34$

**C**  $x = 30, y = 32$

**D**  $x = 34, y = 34$

 [QUESTION ANALYTICS](#)



Q. 3

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What is the use of Program Counter (PC) in a system?

- A PC contains address of the next instruction to be executed.

Your answer is **Correct**

**Solution :**  
(a)

- B PC contains address of current instruction that is being executed.

- C PC is number of processes running in a system at a particular instance.

- D PC contains effective address that calculated for operand of current executing instruction.

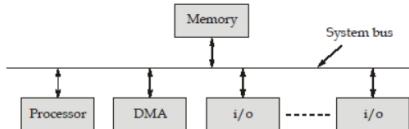
QUESTION ANALYTICS



Q. 4

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Below diagram shows single bus detached DMA configuration for a system. How many times system bus used for a single data transfer using DMA (consider only data transfer, not command or status transfer).



- A 1

Your answer is **IN-CORRECT**

- B 2

Correct Option

**Solution :**  
(b)

One access of system bus for data transfer from i/o to DMA and other for data transfer from DMA to memory.

- C 3

- D 0

QUESTION ANALYTICS



Q. 5

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Consider a system with 4 GB main memory with word size of 32 bits. Main memory is half word addressable. Then size of Memory Address Register (MAR) and Memory Data Register (MDR) for this system are respectively.

- A 32 bits, 30 bits

- B 31 bits, 32 bits

Your answer is **Correct**

**Solution :**  
(b)

Word size is 32 bit, so MDR size is 32 bits.

$$\begin{aligned} \text{Size of MAR} &= \log_2 \left( \frac{\text{Main memory size}}{\text{Addressable size}} \right) \\ &= \log_2 \left( \frac{4 \text{ GB}}{16 \text{ bits}} \right) \quad (\because \text{Here half word} = 16 \text{ bits}) \\ &= \log_2 \left( \frac{4 \times 2^{30} \times 8}{16} \right) = \log_2 (2^{31}) = 31 \text{ bits} \end{aligned}$$

- C 32 bits, 31 bits

- D 30 bits, 32 bits

Q. 6

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A hard disk has 32 recording surfaces, 256 cylinders, 512 sectors per track and sector size is 1 KB. Find the total size of this hard disk in GB \_\_\_\_\_.  
(Rounded off upto 1 decimal place)

4.0

Your answer is Correct4.0

**Solution :**

4.0

$$\begin{aligned} \text{Number of tracks} &= \text{Number of cylinders} \\ \text{Total size} &= (\text{Number of surfaces}) \times (\text{Number of tracks per surface}) \times (\text{Number of sectors per track}) \times (\text{Size of a sector}) \\ &= 32 \times 256 \times 512 \times 1024 \text{ bytes} \\ &= 2^5 \times 2^8 \times 2^9 \times 2^{10} \text{ bytes} \\ &= 2^{32} \text{ bytes} = 4 \text{ GB} \end{aligned}$$

Q. 7

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Consider a system with 32 bit physical address has data cache of size 16 Kbytes. Cache block size is 256 bytes. Cache is using fully associative mapping. x is tag field length in bits and y is set field length in bits for this cache system. Find value of  $x - y$  \_\_\_\_\_.  
\_\_\_\_\_

24

Your answer is Correct24

**Solution :**

24

$$\text{Block size (BS)} = 256 \text{ bytes} = 2^8 \text{ B}$$

$$\text{Block offset (BO)} = \log_2(2^8) = 8 \text{ bits}$$

In fully associative mapping physical address divided into tag field and block offset, so set field length = 0 bits.

$$\text{Tag field length} = \text{Physical address length} - \text{Block offset}$$

$$= 32 - 8 = 24 \text{ bits}$$

So,  $x = 24, y = 0$

$$x - y = 24$$

Q. 8

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Which i/o technique uses interrupts to take attention of CPU/processor?

**A** Programmed i/o**B** Interrupt driven i/o

Your option is Correct

**C** Direct memory access (DMA)

Your option is Correct

**D** None of the above

YOUR ANSWER - b,c

CORRECT ANSWER - b,c

STATUS - ✓

**Solution :**

(b, c)

In interrupt driven i/o, device interrupt CPU before data transfer.

And DMA interrupt CPU at the end of i/o operation.

Q. 9

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For a cache memory system, if we change the cache block size then in which of the following cache mapping method the tag field length cannot change. Assume, after change in the block size the number of sets in direct mapped and k associative cache must be greater than 1.

A Direct mapped cache

Correct Option

B *k* associative cache

Your option is Correct

C Fully associative cache

D None of the above

YOUR ANSWER - b

CORRECT ANSWER - a,b

STATUS -

#### Solution :

(a,b)

Fully associative cache contains only tag field and block offset, so if we change block size then it will effect tag field.

Direct mapped and *k* associative cache have tag field, set field and block offset. Here block offset will affect only set field, but not tag field.

QUESTION ANALYTICS

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Q. 10

Solution Video

Have any Doubt ?

Bookmark

A hard disk has 100 cylinders, 16 recording surfaces, 32 sectors per track and 512 bytes per sector. Address of a byte is represented by  $\langle c, s, r, b \rangle$ , where *c* is cylinder number, *s* is surface, *r* is sector number and *b* is byte number. Thus, 0th byte represented as  $\langle 0, 0, 0, 0 \rangle$ , 1<sup>st</sup> byte represented as  $\langle 0, 0, 0, 1 \rangle$  and so on. The head of disk starts reading the disk sequentially from  $\langle 0, 0, 0, 0 \rangle$  and reached at  $\langle 8, 8, 16, 127 \rangle$ . How many bytes have the head read, including the byte with address  $\langle 8, 8, 16, 127 \rangle$ .

A  $2^{21} + 2^{16} + 2^{13} + 128$  bytes

B  $2^{21} + 2^{17} + 2^{12} + 127$  bytes

C  $2^{20} + 2^{17} + 2^{12} + 128$  bytes

D  $2^{21} + 2^{17} + 2^{13} + 128$  bytes

Your answer is Correct

#### Solution :

(d)

Current address of head  $\langle 8, 8, 16, 127 \rangle$ .

Head have read 8 cylinders from 0 to 7, so

$$\begin{aligned} \text{Bytes for 8 cylinders} &= (\text{Number of cylinders}) \times (\text{Number of surfaces}) \times (\text{Number of sectors} \\ &\quad \text{per track}) \times (\text{Bytes per sector}) \\ &= 8 \times 16 \times 32 \times 512 \text{ bytes} \\ &= 2^3 \times 2^4 \times 2^5 \times 2^9 = 2^{21} \text{ bytes} \end{aligned} \quad \dots(i)$$

On 8<sup>th</sup> cylinder, head completed 8 surfaces from 0 to 7, so

$$\begin{aligned} \text{Bytes for 8 surfaces} &= (\text{Number of surfaces}) \times (\text{Number of sectors per track}) \times (\text{Bytes} \\ &\quad \text{per sector}) \\ &= 8 \times 32 \times 512 = 2^3 \times 2^5 \times 2^9 = 2^{17} \text{ bytes} \end{aligned} \quad \dots(ii)$$

On 8<sup>th</sup> surface of 8<sup>th</sup> cylinder, head completed 16 sectors from 0 to 15, so

$$\begin{aligned} \text{Bytes for 16 Sectors} &= (\text{Number of sectors}) \times (\text{Bytes per sector}) \\ &= 16 \times 512 = 2^4 \times 2^9 = 2^{13} \text{ bytes} \end{aligned} \quad \dots(iii)$$

On 16<sup>th</sup> sector of 8<sup>th</sup> surface on 8<sup>th</sup> cylinder, head completed 128 bytes from 0 to 127, so

On this sector bytes read = 128 bytes ...(iv)

From (i), (ii), (iii) and (iv) total bytes read by head.

$$= 2^{21} + 2^{17} + 2^{13} + 128 \text{ bytes}$$

QUESTION ANALYTICS

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