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COMPUTER ORGANIZATION AND ARCHITECTURE-2 (GATE 2023) - REPORTS

OVERALL ANALYSIS | COMPARISON REPORT | SOLUTION REPORT

ALL(17) | CORRECT(13) | INCORRECT(4) | SKIPPED(0)

Q. 11

Solution Video | Have any Doubt ?

A system has 4 GB byte-addressable main-memory and 128 Kbytes data cache memory with block size of 64 bytes. Tag field length is 16 bits in cache. Which of the following cache mapping used in this system?

A Direct mapped

B 2-way set associative — Your answer is Correct

Solution :
(b)

$$4\text{ GB} = 2^{32}\text{ bytes}$$

and memory is byte addressable, so address length is 32 bit

$$\text{Block size (BS)} = 64\text{ bytes} = 2^6\text{ B}$$

$$\text{Block offset (BO)} = \log_2(2^6) = 6\text{ bit}$$

$$\text{Number of cache blocks} = \left(\frac{\text{Cache size}}{\text{Block size}}\right) = \frac{128\text{ KB}}{2^6\text{ B}} = 2^{11}\text{ blocks}$$

$$\text{Length of set field} = \text{Address length} - \text{Block offset} - \text{Tag length}$$
$$= 32 - 6 - 16 = 10\text{ bit}$$

$$\text{Length of set field} = \log_2\left(\frac{\text{Number of cache blocks}}{\text{Associativity}}\right)$$

$$10 = \log_2\left(\frac{2^{11}}{x}\right)$$

$$\frac{2^{11}}{x} = 2^{10}$$

$$x = 2$$

So, cache is 2 way set associative.

C 4-way set associative

D Fully associative

QUESTION ANALYTICS +

Q. 12

Solution Video | Have any Doubt ?

Let R_1, R_2 and R_3 are 4 bit registers in a system. R_1 = 0011 and R_2 = 0101 in 2's complement binary format. System execute following instruction

SLT R_3, R_1, R_2

where SLT is 'set less than' operation in which R_3 = 0001 if $R_1 < R_2$ else R_3 = 0000, values in 2's complement binary number. What are the values of states bits overflow (V), zero (Z), negative (N) and half carry (H) after executive above instruction? Assume system uses 2's complement addition and subtraction.

A V = 0, Z = 0, N = 1, H = 0 — Your answer is Correct

Solution :
(a)

SLT operation actually implemented using subtraction, as shown below:
For SLT a, b, c

$$a = \begin{cases} 0, & \text{if } b - c \geq 0 \\ 1, & \text{if } b - c < 0 \end{cases}$$

So, here use $R_1 - R_2$

$$R_2 = 0101$$
$$-R_2 = 2\text{'s complement of } R_2 = 1011$$
$$R_1 - R_2 = R_1 + (-R_2)$$
$$= 0011 + 1011 = 1110$$

1110 is negative number in 2's complement.
So, N = 1
1110 is non zero, so Z = 0
No overflow in above operation,
So , V = 0
No half carry, so H = 0

B V = 0, Z = 1, N = 1, H = 0

C V = 1, Z = 1, N = 0, H = 1

D V = 1, Z = 0, N = 1, H = 0

QUESTION ANALYTICS +

Q. 13 Solution Video | Have any Doubt ?

Consider 4 ns CLK cycle processor which consumes 6 cycles for data transfer, 8 cycles for ALU and 4 cycles for branch instructions. Relative frequencies of these instructions are 40%, 30% and 30% respectively. What is the average instruction execution time?

A 20 ns

B 6 ns

C 4 ns

D 24 ns — Your answer is **Correct**

Solution :
(d)

$$\begin{aligned}\text{Average instruction execution time} &= \sum(IC_i \times CPI_i) \times \text{Cycle time} \\ &= ((0.4 \times 6) + (0.3 \times 8) + (0.3 \times 4))\ 4 \text{ ns} \\ &= 24 \text{ ns}\end{aligned}$$

QUESTION ANALYTICS +

Q. 14 Solution Video | Have any Doubt ?

A system has L_1 and L_2 cache with access time of 10 ns and 100 ns respectively.
Main memory access time is 1 µs.
Miss rates of L_1 and L_2 are $\frac{1}{100}$.
Find average memory access time for this system in ns. (Rounded upto one decimal place)

11.1 — Your answer is **Correct**11.1

Solution :
11.1

Average memory access time (AMAT) = (L_1 access time) + Miss rate of L_1 × [L_2 access time + Miss rate L_2 × Memory access time]

$$\begin{aligned}&= 10 \text{ ns} + \frac{1}{100} \times \left[100 \text{ ns} + \frac{1}{100} \times 1000 \text{ ns}\right] \\ &= 11.1 \text{ ns}\end{aligned}$$

QUESTION ANALYTICS +

Q. 15 Solution Video | Have any Doubt ?

A disk has seek time of 50 ms, 64 sectors per track, 512 bytes per sector and rotate at 600 rounds per minute. A file of size 48 Kbytes sequentially stored in two consecutive adjacent tracks, but starting point of file on both tracks can be anywhere on tracks. Negligible time spend on moving from one track to its adjacent track. Find the average time required to access and read the whole file in ms?

300 — Correct Option

Solution :
300

$$\begin{aligned}600 \text{ rounds in} &= 1 \text{ minute} = 60 \text{ sec} \\ 1 \text{ round in} &= \frac{60}{600} = \frac{1}{10} = 100 \text{ ms} = \text{rotation time} \\ \text{Bytes read in 1 round} &= \text{Bytes in a track} \\ &= (\text{Number of sectors per track}) \times (\text{Bytes per sector}) \\ &= 64 \times 512 = 2^6 \times 2^9 = 215 \text{ bytes}\end{aligned}$$

Time to access 1st track of file = Seek time
= 50 ms ...(i)

Time to access starting point of file on 1st track = Average rotational latency

$$= \frac{\text{Rotation time}}{2} = \frac{100}{2} = 50 \text{ ms} \quad \text{...(ii)}$$

Let x bytes of file stored on 1st track, then

$$\text{Time to record } x \text{ bytes} = x \times \frac{\text{Rotation time}}{\text{Bytes in 1 rotation}}$$

$$= x \cdot \frac{100}{2^{15}} \cdot \text{ms} \quad \text{...(iii)}$$

Negligible time on moving from 1st track to its adjacent track which contain other part of file.
Time to access starting point of file on 2nd track = Average rotational latency

$$= \frac{\text{Rotation time}}{2} = \frac{100}{2} = 50 \text{ ms} \quad \text{...(iv)}$$

1st track has x bytes of file, so 2nd track has (48 KB – x) bytes.
Time to read (48 KB – x) bytes from 2nd track

$$= (48 \text{ KB} - x \text{ bytes}) \times \frac{\text{Rotation time}}{\text{Bytes in 1 rotation}}$$

$$= (48 \text{ KB} - x \text{ bytes}) \frac{100}{2^{15}} \text{ ms} \quad \text{...(iv)}$$

Add (i), (ii), (iii), (iv) and (v) for total time to access and read given file.

$$\text{Total time} = 50 \text{ ms} + 50 \text{ ms} + x \cdot \frac{100}{2^{15}} \text{ ms} + 50 \text{ ms} + (48 \text{ KB} - x) \frac{100}{2^{15}} \text{ ms}$$

$$= 100 \text{ ms} + \frac{100}{2^{15}}(x + 48 \text{ KB} - x) + 50 \text{ ms}$$

$$= 150 \text{ ms} + \frac{100}{2^{15}} \times 48 \times 2^{10}$$

$$= 150 \text{ ms} + \frac{100}{32} \times 48$$

$$= 150 \text{ ms} + 150 \text{ ms} = 300 \text{ ms}$$

Your Answer is 200.05

QUESTION ANALYTICS +

Q. 16

Solution Video | Have any Doubt ?

Consider two systems A and B, each system contains byte addressable main memory of size 4 GB and "2-way set associative" cache memory of size 128 KBytes. System A has cache block of size 128 bytes and system B has cache block of size 256 bytes. x is difference of tag field lengths of system A and B. y is difference of set field lengths of system A and B. Find value of x and y?

A $x = 0$ — Your option is **Correct**

B $y = 1$ — Your option is **Correct**

C $x = 1$

D y = 0

YOUR ANSWER - a,b | CORRECT ANSWER - a,b | STATUS -

Solution :

(a, b)

Main memory (MM) address length = $\log_2$ (MM size) = $\log_2$ (4 GB) = $\log_2$ (2^{32}) = 32 bits

System A:

$$\text{Number of cache blocks} = \frac{\text{Cache size}}{\text{Block size}} = \frac{128 \text{ KB}}{128 \text{ B}} = 1 \text{ K} = 2^{10}$$

$$\text{Set numbers} = \frac{\text{Blocks}}{\text{Associativity}} = \frac{2^{10}}{2} = 2^9$$

$$\text{Set field length} = \log_2 (\text{Set numbers}) = \log_2 (2^9) = 9 \text{ bits}$$

$$\text{Block offset} = \log_2 (\text{Block size}) = \log_2 (2^7) = 7 \text{ bits}$$

$$\text{Tag field length} = \text{Address length} - \text{Set length} - \text{Block offset}$$

$$= 32 - 9 - 7 = 16 \text{ bits}$$

System B:

$$\text{Number of cache blocks} = \frac{128 \text{ KB}}{256 \text{ B}} = 2^9$$

$$\text{Set numbers} = \frac{2^9}{2} = 2^8$$

$$\text{Set field length} = \log_2 (2^8) = 8 \text{ bits}$$

$$\text{Block offset} = \log_2 (256) = \log_2 (2^8) = 8 \text{ bits}$$

$$\text{Tag field length} = 32 - 8 - 8 = 16 \text{ bits}$$

$$x = \text{Tag length of A} - \text{Tag length of B}$$

$$= 16 - 16 = 0$$

$$y = \text{Set length of A} - \text{Set length of B}$$

$$= 9 - 8 = 1$$

QUESTION ANALYTICS +

Q. 17

Solution Video | Have any Doubt ?

A system with 8 blocks of cache memory which is 2 way set associative mapped. Cache memory using LRU replacement algorithm. A process referencing following main memory blocks in given order:
10, 11, 12, 18, 5, 11, 6, 7, 10, 15, 11, 5
Assume cache is initially empty. Which of the following is/are true?

A 4 conflict misses

B 8 compulsory misses — Your option is **Correct**

C 0 capacity misses — Your option is **Correct**

D 2 hits — Correct Option

YOUR ANSWER - b,c | CORRECT ANSWER - b,c,d | STATUS - ✗

Solution :

(b, c, d)

$C_1 \rightarrow$ Conflict miss
$C_2 \rightarrow$ Compulsory miss
$C_3 \rightarrow$ Capacity miss
$H \rightarrow$ Hit

10	11	12	18	5	11	6	7	10	15	11	5
C_2	C_2	C_2	C_2	C_2	H	C_2	C_2	C_1	C_2	C_1	H

0	12
1	5
2	~~10~~ ~~18~~ 6 10
3	~~11~~ ~~7~~ 15 11

Number of C_1 = 2
Number of C_2 = 8
Number of C_3 = 0
Number of H = 2

QUESTION ANALYTICS +