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COMPUTER ORGANIZATION AND ARCHITECTURE-1 (GATE 2023) - REPORTS

OVERALL ANALYSIS | COMPARISON REPORT | SOLUTION REPORT

ALL(17) CORRECT(14) INCORRECT(2) SKIPPED(1)

Q. 1 Solution Video | Have any Doubt ?

Consider a system with some machine instructions of following format:
OP R_i, R_j, R_k
where OP is operation to be performed on contents of register R_j and R_k and result stored in R_i.
Consider following sequence of instructions:
I_1 : DIV R_1, R_2, R_3
I_2 : ADD R_2, R_4, R_6
I_3 : SUB R_3, R_2, R_1
I_4 : ADD R_2, R_4, R_1
Consider the following statements:
S_1 : True-dependency exists in above instructions.
S_2 : Anti-dependency exists in above instructions.
S_3 : Output-dependency does not exist in above instructions.
Which of the statements are true?

Ⓐ S_2

Ⓑ S_1, S_2, S_3

Ⓒ S_1, S_3

Ⓓ S_1, S_2 — Your answer is **Correct**

Solution :
(d)
- Anti-dependencies:
  1. R_2 of I_1 and I_2
  2. R_2 of I_1 and I_4
  3. R_3 of I_1 and I_3
  4. R_2 of I_3 and I_4

  So, S_2 is true.
- True-dependency:
  1. R_1 of I_1 and I_3 } Non adjacent dependencies are
  2. R_1 of I_1 and I_4 } eliminated through adjacent dependency
  3. R_2 of I_2 and I_3

  So, S_1 is true.
- Output-dependency
  1. R_2 of I_2 and I_4

  So, S_3 is false.

QUESTION ANALYTICS +

Q. 2 Solution Video | Have any Doubt ?

Match **List-I** with **List-II** and select the correct answer using the codes given below the lists:

	List-I		List-II
A.	ADD R_1, R_2, R_3	1.	Three address instruction
B.	PUSH X	2.	Two address instruction
C.	ADD	3.	One address instruction
D.	SUB R_1, R_2	4.	Zero address instruction

Where R_1, R_2, R_3 are registers and X is memory address.
Codes:

	A	B	C	D
(a)	1	3	4	2
(b)	4	3	4	3
(c)	2	3	1	4
(d)	1	4	4	2

Ⓐ a — Correct Option

Solution :
(d)
1. ADD R_1, R_2, R_3 is equivalent to $R_1 \Leftarrow R_2 + R_3$ and it is three address instruction.
2. PUSH X it is one-address instruction, operand in address X pushed into stack.
3. ADD zero-address instruction, pop two elements from stack, add them and push the result

into stack.

4. SUB R_1, R_2 is equivalent is $R_1 \Leftarrow R_1 + R_2$ it is two-address instruction.

B b

C c

D d — Your answer is **IN-CORRECT**

QUESTION ANALYTICS +

Q. 3

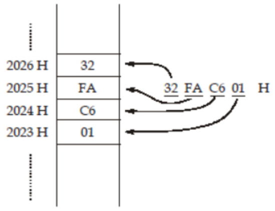
Solution Video | Have any Doubt ?

Consider a 32 bit number 32FAC601 H in hexadecimal notation stored at memory location 2023 H in little endian format and memory is byte addressable. The value of byte stored at location 2023 H and 2025 H.

A 01 and 56

B 01 and FA — Your answer is **Correct**

Solution :
(b)
For little endian



C 32 and FA

D 32 and C6

QUESTION ANALYTICS +

Q. 4

Solution Video | Have any Doubt ?

A load-store architecture in which memory operation applied only on LOAD and STORE instructions and other all operations are REG-REG instructions. Find the minimum number of instructions required to execute the expression X = $\frac{(A+B)-(C+D)}{E}$ in this load store architecture, where *A, B, C, D, E* and *X* are memory locations and expression evaluated on operands stored in these locations. Result stores in memory location *X*. Assume three address architecture.

A 10 — Correct Option

Solution :
(a)

1. LOAD R_1, A // $R_1 \Leftarrow A$
2. LOAD R_2, B // $R_2 \Leftarrow B$
3. ADD R_1, R_1, R_2 // $R_1 \Leftarrow A - B$
4. LOAD R_3, C // $R_3 \Leftarrow C$
5. LOAD R_4, D // $R_4 \Leftarrow D$
6. ADD R_3, R_3, R_4 // $R_3 \Leftarrow C + D$
7. SUB R_1, R_1, R_3 // $R_1 \Leftarrow (A + B) - (C + D)$
8. LOAD R_5, E // $R_5 \Leftarrow E$
9. DIV R_1, R_1, R_5 // $R_1 \Leftarrow \frac{(A+B)-(C+D)}{E}$
10. STORE R_1, X

B 11

C 5

D 4

QUESTION ANALYTICS +

Q. 5 ▶ Solution Video Have any Doubt ?

A program of 300 instructions running on a system whose clock rate is 2.1 GHz. Average cycles per instruction for the program is 1.4. Find the execution time of program in nano seconds.

A 102

B 450

C 882

D 200 Your answer is **Correct**

Solution :
(d)

$$\begin{aligned}\text{Number of instructions} &= 300\\ \text{Cycle per instruction (CPI)} &= 1.4\\ \text{Clock rate} &= 2.1\text{ GHz}\\ \text{Execution time} &= \frac{\text{Number of instruction} \times \text{CPI}}{\text{Clock rate}}\\ &= \frac{300 \times 1.4}{2.1 \times 10^9} = 200\text{ ns}\end{aligned}$$

QUESTION ANALYTICS +

Q. 6 ▶ Solution Video Have any Doubt ?

Assume a system with machine instructions of two word long. How many memory accesses require for following instruction in this system?

I_1 : ADD $r_1, r_2, (r_3)$ // register indirect addressing
I_2 : SUB r_4, r_5, r_6 // register addressing
I_3 : ADD $r_7, r_8,$ [1000] // direct addressing
I_4 : ADD r_9, r_{10} @ 2000 // memory indirect addressing

Assume memory is word addressable.

● 12 Your answer is **Correct**12

Solution :
12

Instructions are two word long, so every instruction reading needs 2 memory access (MA).

	MA for instruction reading	Other memory access for addressing
I_1	2	1
I_2	2	0
I_3	2	1
I_4	2	2
Total	8	4

$\therefore$ Total memory access = 8 + 4 = 12

QUESTION ANALYTICS +

Q. 7 ▶ Solution Video Have any Doubt ?

Consider a system with *n* processors. A program with 80% parallel part and 20% sequential part. There is a speedup of 4 when we run this program on given system with *n* processors as compare to single processor system. The value of *n* is

● 16 Your answer is **Correct**16

Solution :
16

Using Amdahl's law

$$\Rightarrow \quad \text{Speedup} = \frac{1}{\text{Sequential part} + \dfrac{\text{Parallel part}}{\text{Number of processors}}}$$

$$\Rightarrow \quad 4 = \frac{1}{0.2 + \dfrac{0.8}{n}}$$

$\Rightarrow \quad 0.2+\frac{0.8}{n} = \frac{1}{4} = 0.25$

$\Rightarrow \quad \frac{0.8}{n} = 0.05$

$\Rightarrow \quad n = \frac{0.8}{0.05} = 16$

QUESTION ANALYTICS +

Q. 8

Solution Video | Have any Doubt ?

A system architecture has 203 control signals. X and Y are the number of bits required for control field in control word for horizontal and vertical microprogramming respectively. Value of X and Y are

A $X = 256$

B $Y = 203$

C $X = 203$ Your option is Correct

D $Y = 8$ Your option is Correct

YOUR ANSWER - c,d

CORRECT ANSWER - c,d

STATUS - ✓

Solution :

(c, d)

Horizontal micro-programming use 1 bit for each signal, so, 203 bits.

Vertical micro-programming uses $\lceil \log_2 n \rceil$ bits for n signals,

So, $Y = \lceil \log_2 203 \rceil = 8$

QUESTION ANALYTICS +

Q. 9

? FAQ | Solution Video | Have any Doubt ?

Which of the following methods can be used to handle hazards in pipelining?

A Static branch prediction Your option is Correct

B Dynamic branch prediction Your option is Correct

C Register renaming Your option is Correct

D Delayed branching Your option is Correct

YOUR ANSWER - a,b,c,d

CORRECT ANSWER - a,b,c,d

STATUS - ✓

Solution :

(a, b, c, d)

QUESTION ANALYTICS +

Q. 10

Solution Video | Have any Doubt ?

Consider the following sequence of instructions for a pipelined processor with one branch delay slot:

I_1 LABEL : ADD $r_3 \leftarrow r_3 + 1$
I_2 DIV $r_2 \leftarrow r_2 / r_6$
I_3 SUB $r_1 \leftarrow r_2 - 1$
I_4 If $r_1 \leq 0$ then BRANCH to LABEL
I_5 SUB $r_3 \leftarrow r_3 - r_7$

Which of the following is true after filling the branch delay slot using ‘Delayed branching’ method without changing the actual result of program when the condition is true?

A No change in order of instructions, because I_5 will definitely execute on loop termination.

B I_1 shifted to branch delay slot and now label pointing to I_3.

C I_2 shifted to branch delay slot.

D I_1 shifted to branch delay slot and now LABEL pointing to I_2.

Your answer is **Correct**

Solution :
(d)
Branching condition is independent of I_1 and I_1 will definitely execute whether branch taken or not. Branching condition is also independent of I_5, but I_5 will execute only if branch not taken.

QUESTION ANALYTICS +

Item **1-10** of 17 « previous 1 2 next »