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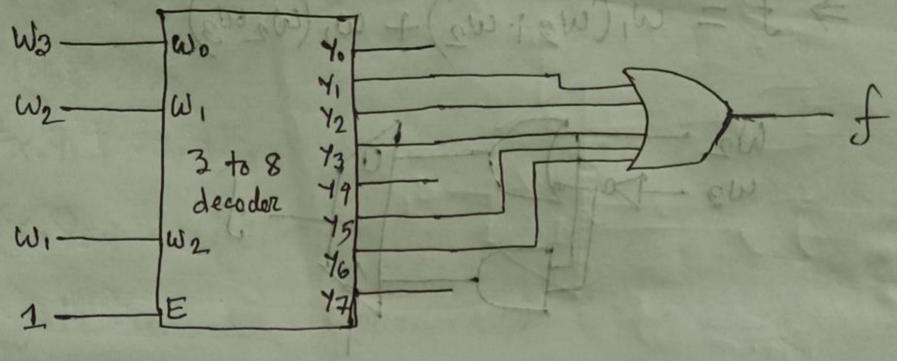
Assignment - 8

Problem - 4.2

Soln:



Problem - 4.3

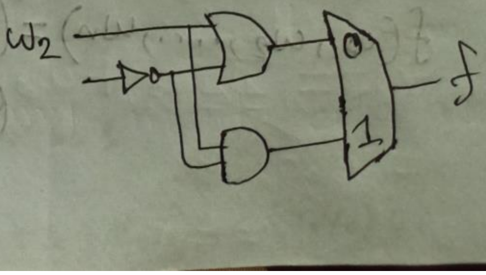
Soln:

w_1	w_2	w_3	f
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

$\Rightarrow w_2 + \overline{w}_3$

$\Rightarrow w_2 \overline{w}_3$

w_1	f
0	$w_2 + \overline{w}_3$
1	$w_2 \overline{w}_3$

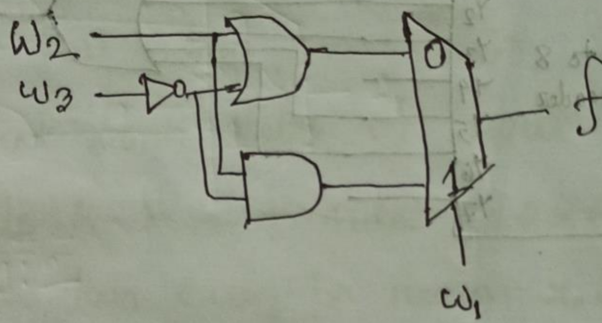


Problem - 4.5

Soln: $f = \bar{w}_1\bar{w}_2\bar{w}_3 + \bar{w}_1 w_2 \bar{w}_3 + \bar{w}_1 w_2 w_3 +$
$w_1 w_2 \bar{w}_3$

The expansion in term of w_1 gives,

$\Rightarrow f = \bar{w}_1(\bar{w}_3 + w_2) + w_1(w_2\bar{w}_3)$.



Problem- 4.10

Soln: $f(w_1, w_2, \dots, w_n) = \bar{w}_1 f(0, w_2, \dots, w_n) +$
$w_1 f(1, w_2, \dots, w_n)$

By duality:

$f(w_1, w_2, \dots, w_n) = (w_1 + f(0, w_2, \dots, w_n))$
$(\bar{w}_1 + f(1, w_2, \dots, w_n))$.

Problem - 4.12

Solⁿ: Refer to figure 3.15.

$$S_0 = x_0 \oplus y_0 \oplus C_0 \quad \text{——} \quad ①$$

$$C_1 = P_0 C_0 + g_0 \quad \text{——} \quad ②$$

From eqⁿ ①

$$S_0 = (x_0 \oplus y_0) \oplus C_0$$

$$= (x_0 \bar{y}_0 + \bar{x}_0 y_0)\bar{C}_0 + (\bar{x}_0 \bar{y}_0 + x_0 y_0) C_0$$

$$= (x_0 \bar{y}_0 + \bar{x}_0 y_0)\bar{C}_0 + \overline{(x_0 \bar{y}_0 + \bar{x}_0 y_0)} C_0$$

The XOR gate can be implemented using a MUX is shown in Figure 1.

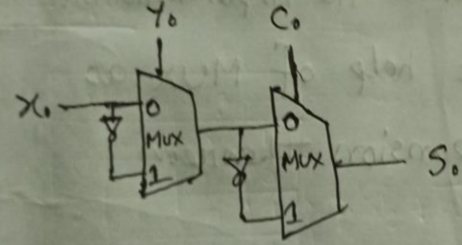


Fig: 1.

In the figure 1, the XOR of 'x' and 'y' is implemented using the 1st MUX and the outcome of it is again XORed with the 'C' using the second MUX resulting in $S_0 = x_0 \oplus y_0 \oplus C_0$

From eqⁿ ②,

$$C_1 = P_0 C_0 + g_0 = (x_0 + y_0) C_0 + x_0 y_0 . 1$$

$$= (x_0 + y_0) C_0 + x_0 y_0 (C_0 + \bar{C}_0) = (x_0 + y_0 + x_0 y_0) C_0 + (x_0 y_0) \bar{C}_0$$

Simplify further,

$$C_1 = (x_0 + y_0(1+x_0))C_0 + (x_0 y_0)\overline{C_0}$$

$$= (x_0+y_0)C_0 + (x_0 y_0)\overline{C_0}$$

The simplified carry expression is implemented using MUX is shown in figure-2

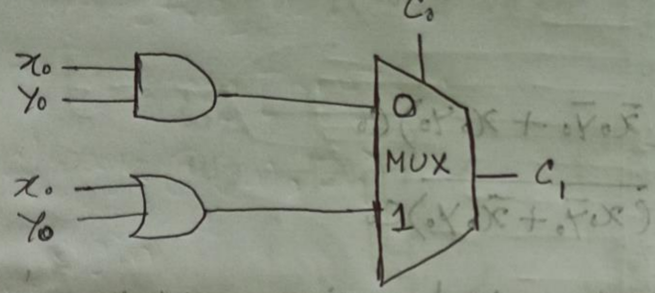


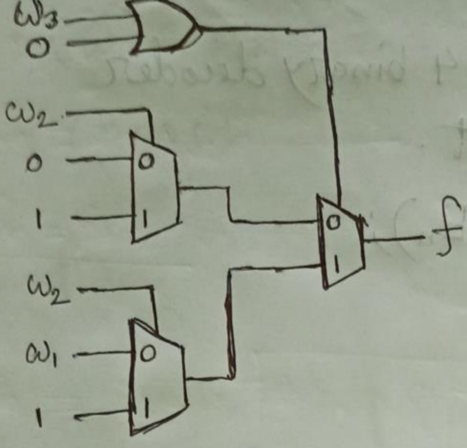
Fig:2

Thus figure 1 and figure 2 show the implementation of sum and carry with the help of MUX as described by Shannon's Expansion Theorem respectively.

Problem-4.16

Sol^n: $f = w_2\overline{w_3} + w_1 w_3 + \overline{w_2} w_3$

$$\Rightarrow f = \overline{w_3}(w_2) + w_3(w_1 + \overline{w_2})$$



Problem– 4.18

Soln: The given verilog code in the question is a 2-to-4 decoder with an Enable input.

It's not a good style of programming. This code is not easy to read. Again, in this code, here 'if' statement are used. But, the verilog compiler often turns if statements into multiplexer in which case the resulting decoder may have multiplexers controlled by the Enable signal on the output side.

Problem- 4.26

Solnº: Verilog module - 2 to 4 binary decoder using an if else statement.

```
module: if 2 to 4(W, Y, En);
input En;
input [1:0] W;
output reg [0:3] Y;
always @(W, En)
  begin
if (En == 0)
  Y = 4'b0000;
else
if (W == 00)
  Y = 4'b1000;
  Y = 4'b0100;
else if (w == 10)
  Y = 4'b0010;
  Y = 4'b1000;
else if (W == 01)
  Y = 4'b0100;
else if (W == 10)
```

```
  Y = 4'b0010;
else if (w == 11)
  Y = 4'b0001;
end;
end module;
```

Verilog module - 3to 8 binary decoder using two instances of the if 2to4 module.

```
module h3 to 8 (w,y,En)
input [2:0] w;
input En;
output [0:7] y;
wire [0:1] m;
if 2 to 4 dec1(w[0:1],y[0:3],(w[2],En));
if 2 to 4 dec2(w[0:1], y[4:7],(w[2],En));

end module;
```