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Assignment-6

Problem-3.5

Soln: (i)

$$\begin{array}{rl} & 00110110 \rightarrow (+54)_{10} \\ + & 01000101 \rightarrow (+69)_{10} \\ \hline & 01111011 \rightarrow (123)_{10} \end{array}$$

When the result of an arithmetic operation requires n+1 bits, but operating on n-bit no. then an $\boxed{\text{overflow occurs}}$ or If result exceeds the range 0 to 2^{n-1} an overflow occurs.

For 8 bits range 0 to 255

Carry out	Sign bit	
0	0	→ No overflow.
1	1	
0	1	→ Overflow
1	0	→ under

Carry in sign bit = 0

Carry out of sign bit = 0

So $\boxed{\text{No overflow}}$.

(ii) 01110101 → $(117)_{10}$

(+) 11011110 → $(222)_{10}$

01010011 → $(339)_{10}$

Carry in sign bit = 1

Carry out of sign bit = 0

$\boxed{\text{No overflow}}$

(iii) 00110110 → $(+54)_{10}$

00101011 → $(-43)_{10}$

Binary of 43 → 00101011

1st complement → 11010100

2nd complement → +1 (2's complement)

= 11010101

$(+54)_{10}$ = 00110110

$(-43)_{10}$ = 11010101

(+11) = 100001011 → mag. representation

Carry in sign bit → 1

Carry out sign bit → 1

$\boxed{\text{No overflow}}$

(iv) 01110101 → $(+117)_{10}$

(−) 11010110 → $(+214)_{10}$

Binary of 214 = 11010110

1st complement → 00101001

2's complement → 11010110

−214 = 00101010

01110101 → $(+117)_{10}$

00101010 → $(-214)_{10}$

10011111 → $-(97)_{10}$

Carry in sign bit → 1

carry out of sign bit → 0

$\boxed{\text{overflow}}$

(v) 11010011 → $(+211)_{10}$

(−) 11101100 → $(-236)_{10}$

Binary of 226 → 11101100

1's complement → 00010011

2's " → 11101100

(−236) = 00010100

$$
\begin{array}{rl}
 & 11010011 \rightarrow (+211)_{10} \\
(+) & 00010100 \rightarrow (-236)_{10} \\
\hline
 & 11100111 \rightarrow -(25)_{10}
\end{array}
$$

Carry in sign bit = 0

Carry out " " = 0

$\boxed{\text{No overflow}}$

(vi)

$$
\begin{array}{rl}
 & 11011111 \rightarrow (223)_{10} \\
(+) & 10111000 \rightarrow (184)_{10} \\
\hline
 & \underbrace{10010111}_{\text{magnitude rep.}} \rightarrow \underbrace{(407)}_{\text{Decimal in sign}}{}_{10}
\end{array}
$$

Carry in sign bit → 1

Carry out " " → 1

$\boxed{\text{No overflow}}$

Problem - 3.7

Soln:

Fig: 3.3(a) →

C_i	x_i	y_i	$C_{out} = C_{i+1}$	S_i	
0	0	0	0	0	0
0	0	1	0	1	1
0	1	0	0	1	2
0	1	1	1	0	3
1	0	0	0	1	4
1	0	1	1	0	5
1	1	0	1	0	6
1	1	1	1	1	7

C_i \ x_iy_i	00	01	11	10
$\bar{C_i}$ 0		1		1
C_i 1	1		1	

C_i \ $AB=x_iy_i$	00	01	11	10
$\bar{C_i}$ 0			1	
C_i 1		1	1	1

Sop

$S_i = x_i \oplus y_i \oplus C_i$ — (i)

$C_{out} = x_iC_i + x_iy_i + y_iC_i$

$= x_iy_i + x_iC_i + y_iC_i$

$= x_iy_i + C_i(x_i \oplus y_i)$

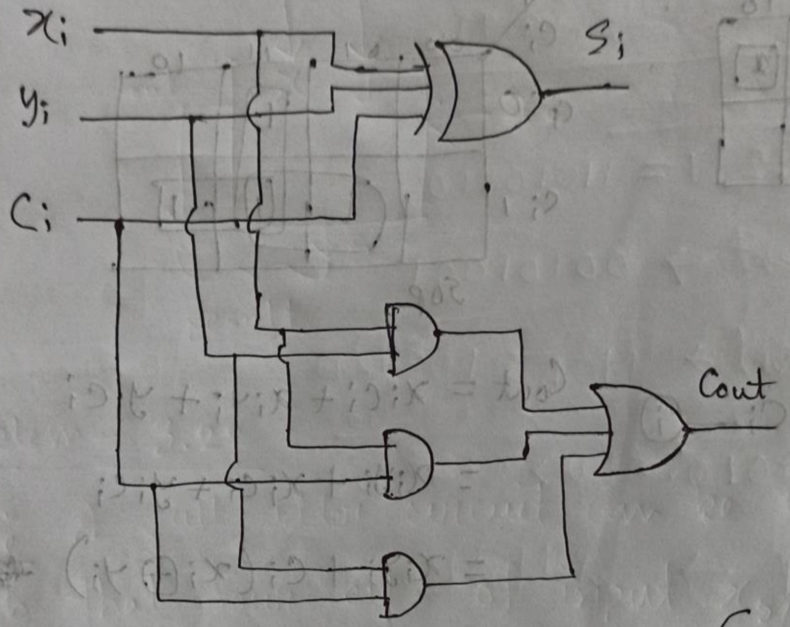
Again, we use the k-map,

C_i \ x_iy_i	00	01	11	10
$\bar{C_i}$ 0			1	
C_i 1		1	1	1

New, $C_{out} = x_iy_i + \bar{x}_iy_iC_i + x_i\bar{y}_iC_i$

$= x_iy_i + C_i(\bar{x}_iy_i + x_i\bar{y}_i)$

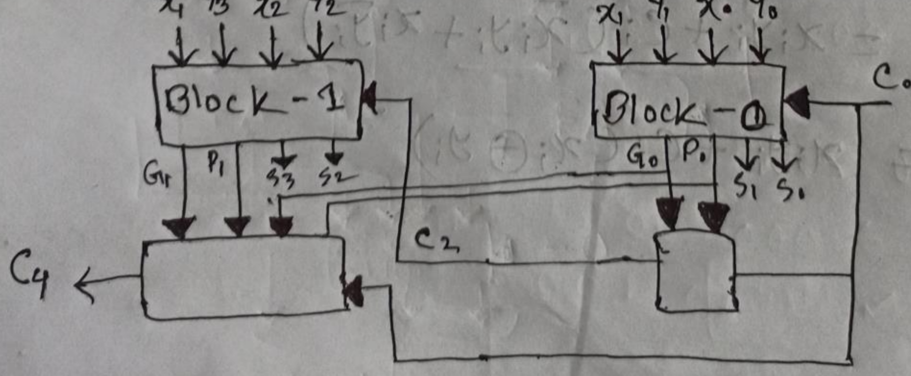
$\therefore C_{out} = x_iy_i + C_i(x_i \oplus y_i)$



(showed)

Problem - 3.14

Soln: The circuits for a 4-bit version of the adder on the hierarchial structure in Fig: 3.17 is constructed as follows:



Block 0 & 1 the structure to the circuit in Fig 3.17. The overall circuit is given by the expression,

$P_1 = x_1 + y_1$

$g_1 = x_1 y_1$

$P_0 = P_1 P_0$

$G_0 = g_1 + P_1 g_0$

$P_1 = P_3 P_2$

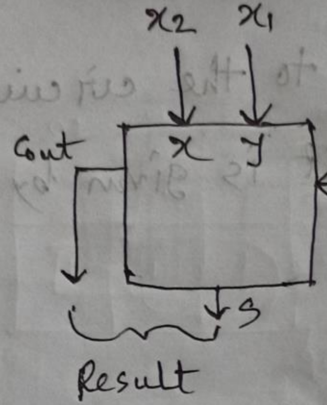
$G_1 = g_3 + P_3 g_2$

$C_2 = G_0 + P_0 C_0$

$C_4 = G_1 + P_1 G_0 + P_1 P_0 \cdot C_0$

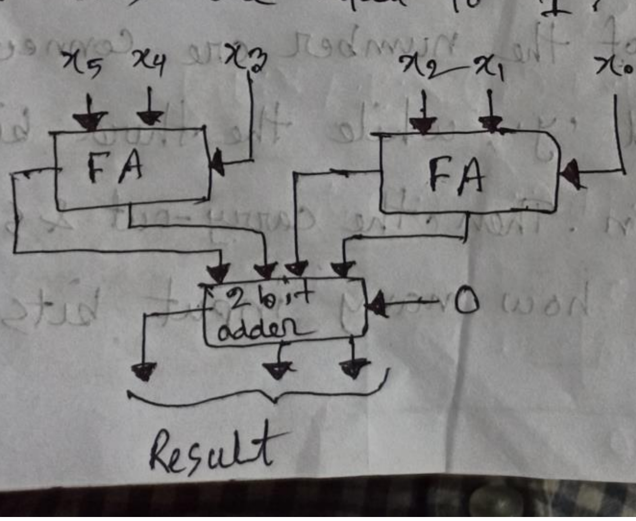
Problem - 3.21

Soln: A full adder circuit can be used such that two of bits of the number are connected as inputs 'x' and 'y', while the third bit is connected as carry-in. Then the carry-out & sum bit will be indicate how many input bits are equal to 1.



Problem- 3.22

Soln: A full adder circuit can be used, such that four bits of input x_5, x_4 in one side & another side $x_2 \& x_1$. While there we have two carry-in region x_0 & x_3 respectively, Then, output coming out from two full adder is connected with 2-bit adder. Now, the carry out & sum bit will indicate how many input bits are equal to 1.


x_5
x_4
x_3
x_2
x_1
x_0
FA
FA
2 bit adder
0
Result