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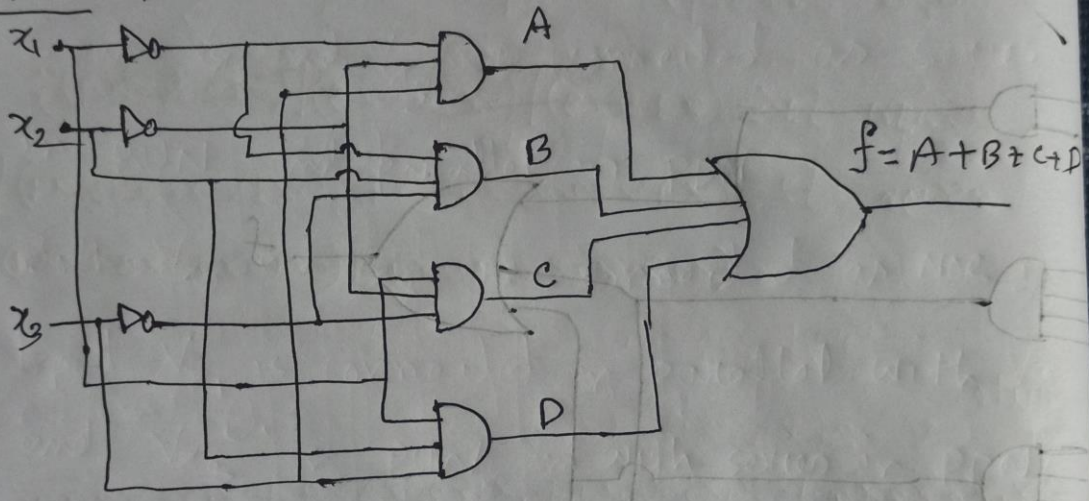
Assignment-7

Problem-B.1

Soln: a)



$A = \bar{x}_1 \bar{x}_2 x_3$

$B = \bar{x}_1 x_2 \bar{x}_3$

$C = x_1 \bar{x}_2 \bar{x}_3$

$D = x_1 x_2 x_3$

x_1	x_2	x_3	A	B	C	D	$f = A+B+C+D$
0	0	0	0	0	0	0	0
0	0	1	1	0	0	0	1
0	1	0	0	1	0	0	1
0	1	1	0	0	0	0	0
1	0	0	0	0	1	0	1
1	0	1	0	0	0	0	0
1	1	0	0	0	0	0	0
1	1	1	0	0	0	1	1

b) From part (a), There are 3 NOT gates. So $3 \times 2 = 6$ transistors need to build 3 NOT gates.

There are 4 3 input AND gates which requires 8 transistors.

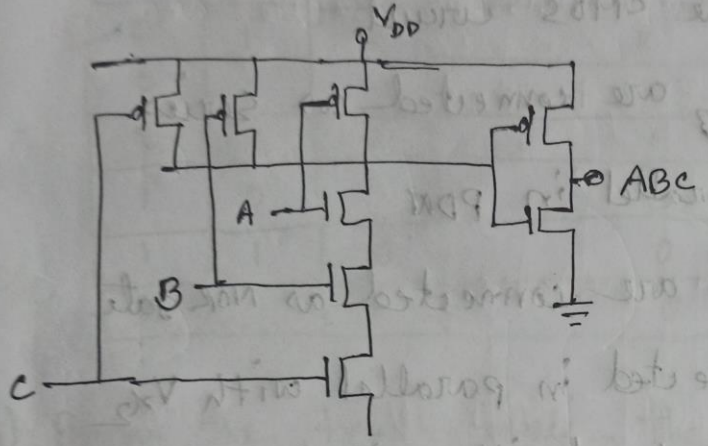


Fig: 4-3 input AND gates requires 8 Transistors

Therefore 4 3-input AND require $4 \times 8 = 32$ transistors and 4-input OR gate requires 10 transistors.

Gate	NOT	3-input AND	4-input OR
Number of Gates	3	4	1
Number of Transistors per gate	2	8	10

∴ Total number of transistors $= 2 \times 3 + 8 \times 4 + 10 \times 1 = 48$

Problem - B.6

Soln^n: a) Inputs for the circuit in Figure PB.4 are $V_{x_1}, V_{x_2}, V_{x_3}$. and output is V_f

Let us consider the CMOS circuit.

- Inputs V_{x_2} and V_{x_3} are connected as series in PUN and parallel in PDN
- Both V_{x_2} and V_{x_3} are connected as NOR gate
- Input V_{x_1} is connected in parallel with V_{x_2} and V_{x_3} in PUN and with series in PDN.

Therefore logical NAND operation is performed with V_{x_1} and $(V_{x_2} + V_{x_3})$

Hence,

$$V_f = \overline{V_{x_1} \cdot (V_{x_2} + V_{x_3})}$$

$$= \overline{V_{x_1}} + \overline{V_{x_2} + V_{x_3}}$$

$$= \overline{V_{x_1}} + \overline{V_{x_2}} \cdot \overline{V_{x_3}}$$

Truth Table

V_{x_1}	V_{x_2}	V_{x_3}	$V_f = \overline{V_{x_1}} + \overline{V_{x_2}} \cdot \overline{V_{x_3}}$
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

b) From the truth table, the canonical sum-of-products expression can be derived as,

$$V_f = \overline{V_{x_1}}\,\overline{V_{x_2}}\,\overline{V_{x_3}} + \overline{V_{x_1}}\,\overline{V_{x_2}}\,V_{x_3} + \overline{V_{x_1}}\,V_{x_2}\,\overline{V_{x_3}} + V_{x_1}\,\overline{V_{x_2}}\,\overline{V_{x_3}} + \overline{V_{x_1}}\,V_{x_2}\,V_{x_3}$$

So we require,

Five 3-input AND gate

Three NOT Gate

5-input OR gate

A three-input AND gate need 8 transistors
A NOT gate need 2 transistors.
A five-input OR gate need 12 transistors.

∴ The number of transistors required is

$= 5 \times 8 + 3 \times 2 + 1 \times 12$

$= 40 + 6 + 12$

$= 58$ transistors.

Problem - 3.8

Soln: The output of given digital circuit is,

$$V_f = V_{x_2} + V_{x_1} \cdot V_{x_3}$$

The complement of the output is,

$$\overline{V_f} = \overline{V_{x_2} + V_{x_1} \cdot V_{x_3}} = \overline{V_{x_2}} \cdot \overline{V_{x_1} \cdot V_{x_3}}$$

$$= \overline{V_{x_2}} \left(\overline{V_{x_1}} + \overline{V_{x_3}} \right)$$

Therefore the other half of the circuit will be,

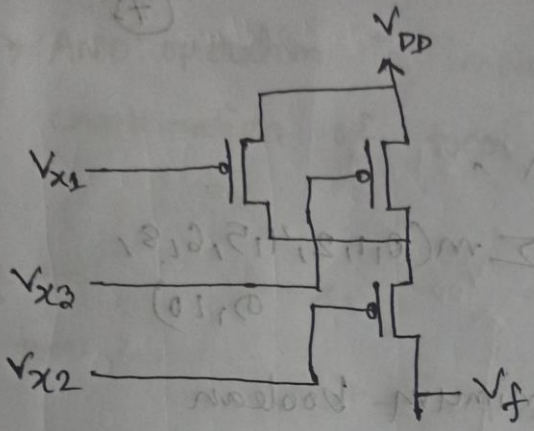


Fig- The other half of the circuit containing only PMOS transistors.

The complete circuit is shown below,

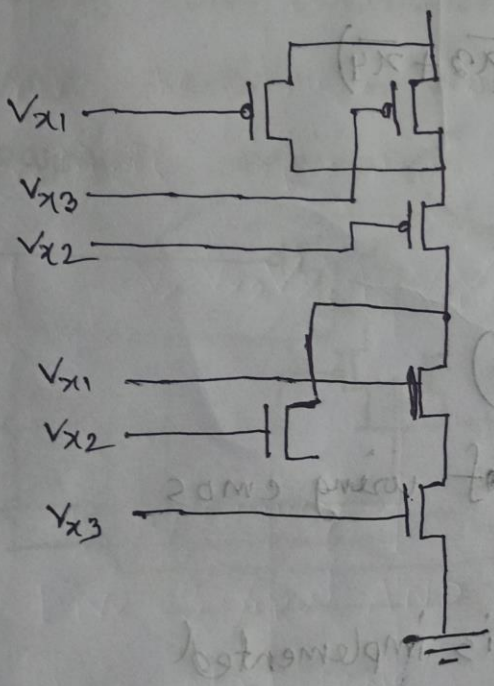


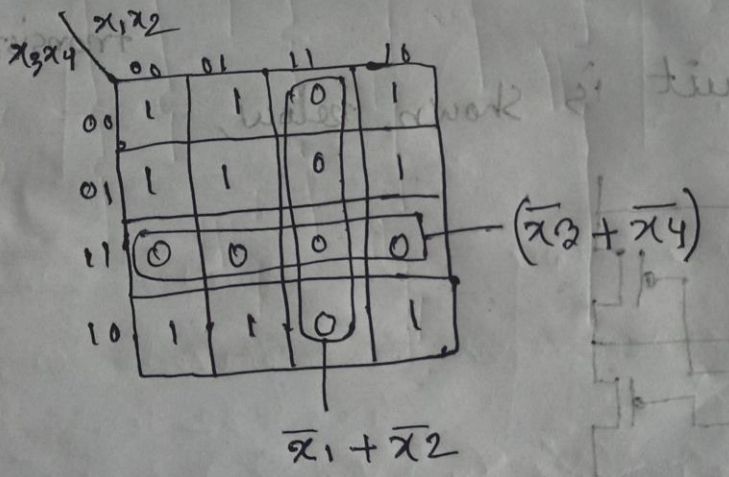
Fig. The complete circuit.

Problem - B.10

Soln: Given logic function,

$$f(x_1, x_2, x_3, x_4) = \sum m(0,1,2,4,5,6,8,9,10)$$

Convert & reduce to minimum boolean algebra using k-map.

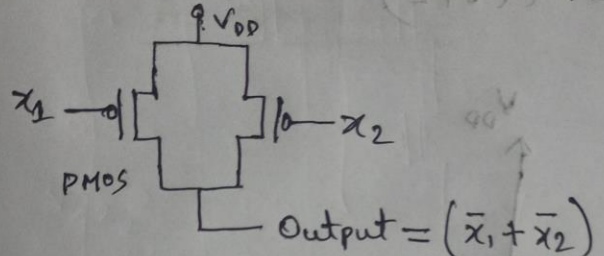


$$\therefore f = (\bar{x}_1 + \bar{x}_2) \cdot (\bar{x}_3 + \bar{x}_4)$$

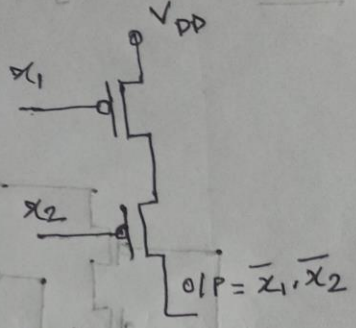
Now implement the output of using cmos logic gate.

→ In PMOS, OR operation is implemented using parallel combination of two PMOS.

→ AND operation is implemented by series combination of two PMOS.



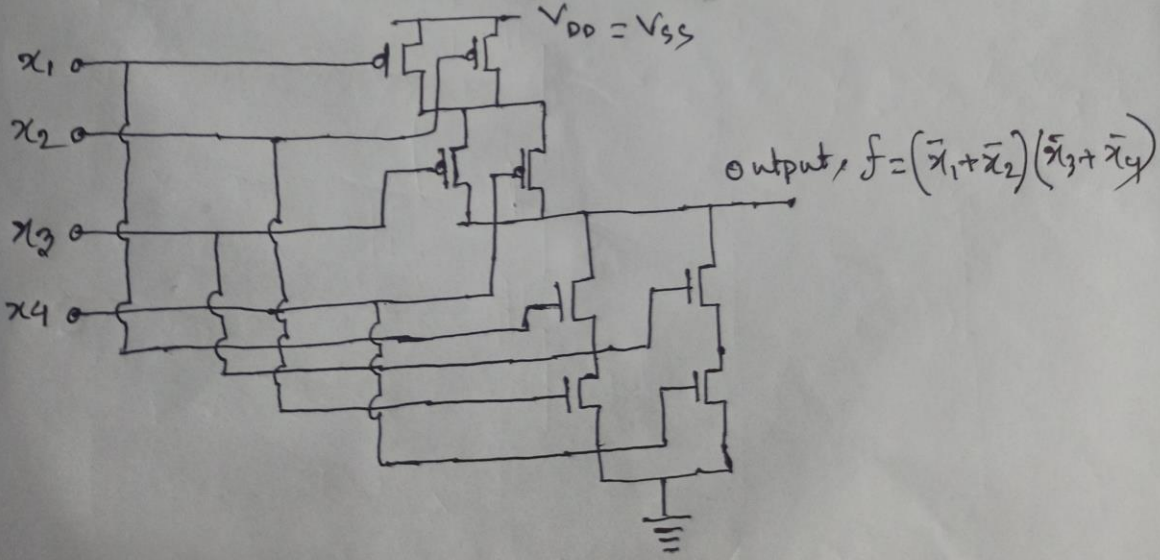
Parallel combination



Series combination

→ In case of NMOS, OR operation is implemented using series combination of two NMOS.

→ AND operation in NMOS is implemented using parallel combination of two series NMOS.



Problem – B.12

Soln: $f = xy + xz = x(y+z)$