PROJECT OVERFLOW

Problem Statement

C-Class core performance analysis: Stage0 (PCGen, Branch Predictor). Vary some configuration knobs in the parameter files and evaluate on risc-v benchmarks, coremark and other microbenchmarks given by Shakti team. Compare performance across configs. Extra credit: Performance analysis on FPGA.

Phase 1:

In c class,core64.yaml we change the parameters of stage0 like pcgen,branch predictor.First have baseline numbers,vary the configurations and evaluate the results based on our observation.To implement this,our first step is to build and run c class and run it in bluespec Verilog.