### **4-BIT COMPARATOR:**

### **AIM:**

To design a four-bit comparator using Modelsim and Verilog HDL

### **TOOLS:**

Modelsim

# **MAIN CODE:**

```
C:\intelFPGA_lite\17.1\bit_4_comparator.v
File Edit View Tools Bookmarks Window Help
C:\intelFPGA_lite\17.1\bit_4_comparator.v - Default =
  ////100 Days of RTL////
         ////Abilash////
         ////4 Bit Comparator////
      module bit_4_comparator (a_in, b_in, a_less_b, a_great_b, a_equal_b);
         input [3:0]a_in, b_in;
output reg a_less_b, a_great_b, a_equal_b;
  always @ (a_in, b_in)
       begin
           if(a_in<b_in)
         begin

a_less_b = 1;

a_great_b = 0;

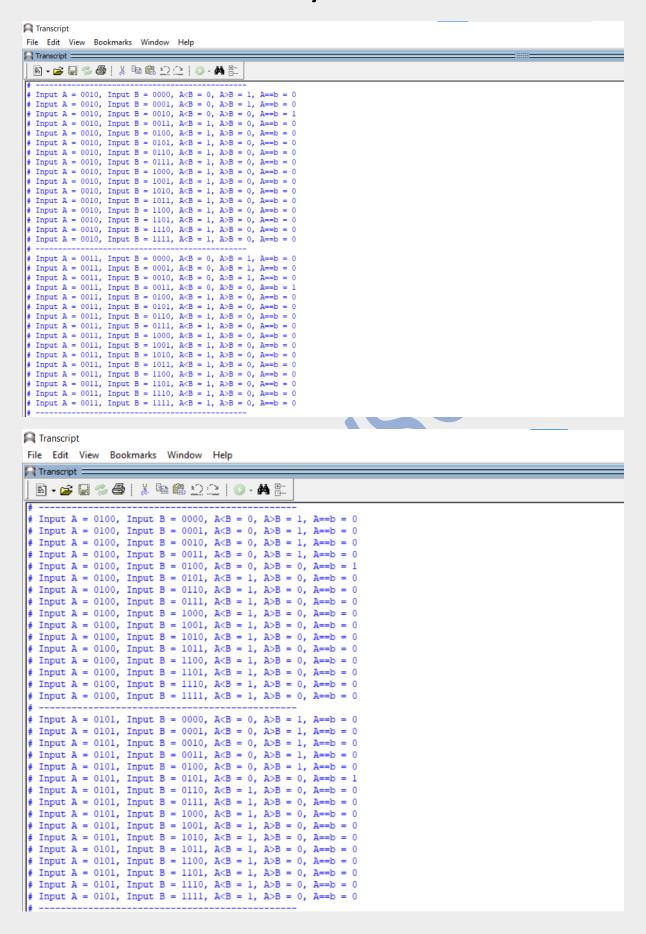
a_enual_b = 0;
              a_equal_b = 0;
           else if (a_in>b_in)
           begin
              a_less_b = 0;
a_great_b = 1;
a_equal_b = 0;
              begin
              a_less_b = 0;
a_great_b = 0;
a_equal_b = 1;
         endmodule
           ı
```

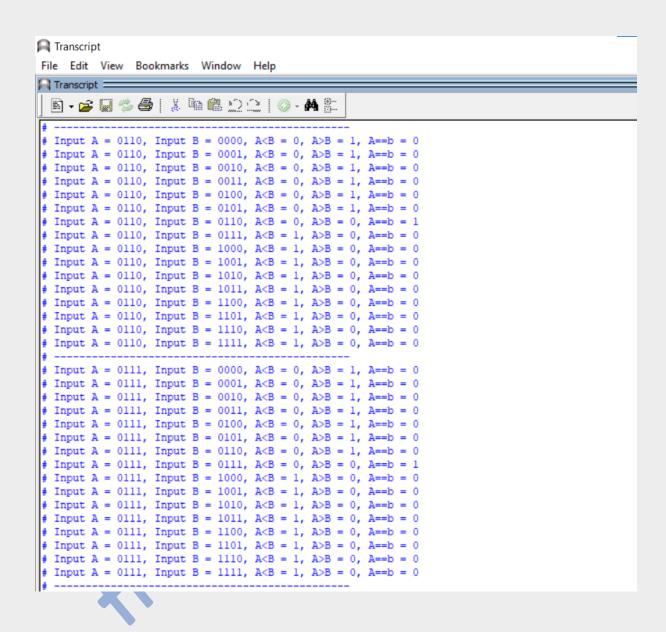
# **TESTBENCH CODE:**

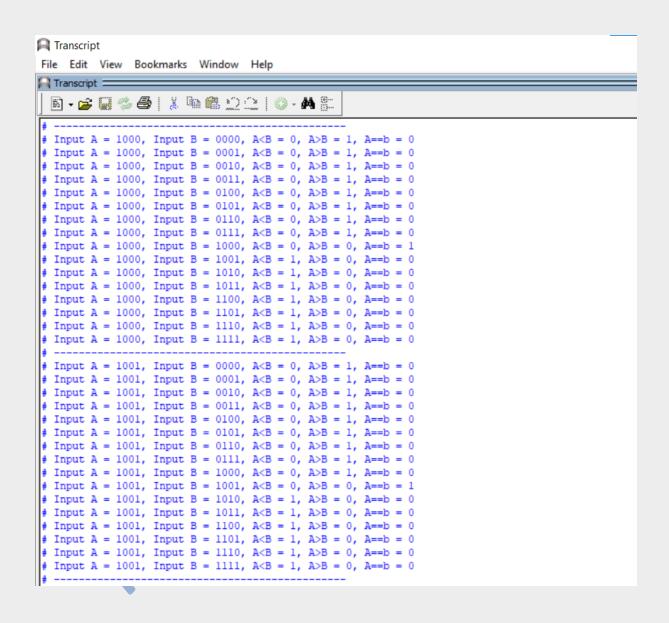
```
C:/intelFPGA_lite/17.1/bit_4_comparator_tb.v
File Edit View Tools Bookmarks Window
C:/intelFPGA_lite/17.1/bit_4_comparator_tb.v - Default =
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          ///100 Days of RTL Challenge///
          ///Abilash P///
          ///4 bit comparator///
        pmodule bit_4_comparator_tb ();
          reg [3:0]a_in,b_in;
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          wire a_less_b, a_great_b, a_equal_b;
          bit_4_comparator DUT (.a_in(a_in), .b_in(b_in), .a_less_b(a_less_b), .a_great_b(a_great_b), .a_equal_b(a_equal_b));
          integer i;
          initial
        🛱 begin
          a_in = 4'b 0000;
b_in = 4'b 0000;
          end
          initial
        pegin
            for(i=0; i<256; i=i+1)</pre>
           begin
              {a_in,b_in} = i;
if(b_in == 0)
                 $display("-
              #20;
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          end
          initial
                   or("Input A = %b, Input B = %b, A<B = %b, A>B = %b, A==b = %b", a_in,b_in,a_less_b,a_great_b, a_equal_b);
          endmodule
```

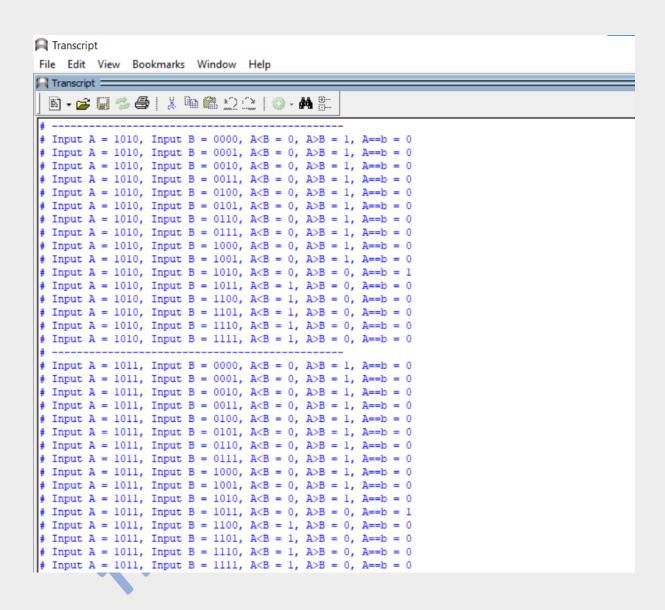
# **Results:**

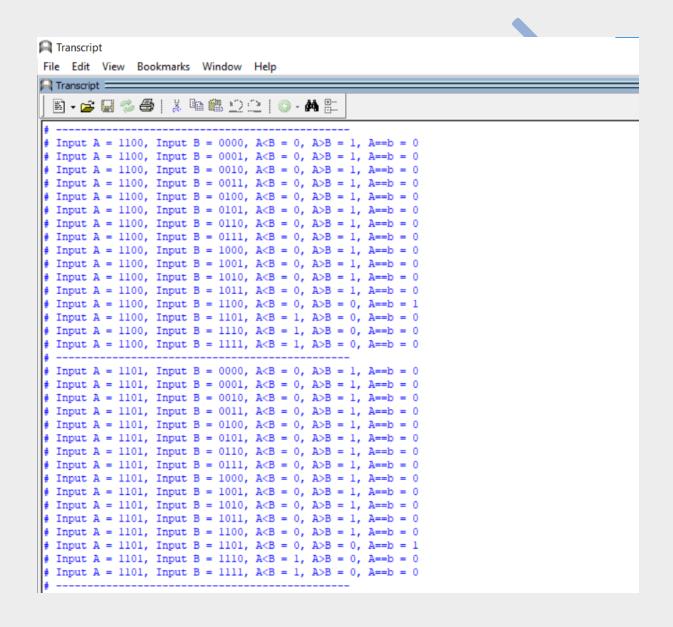
```
| Time comparison | Time compa
```





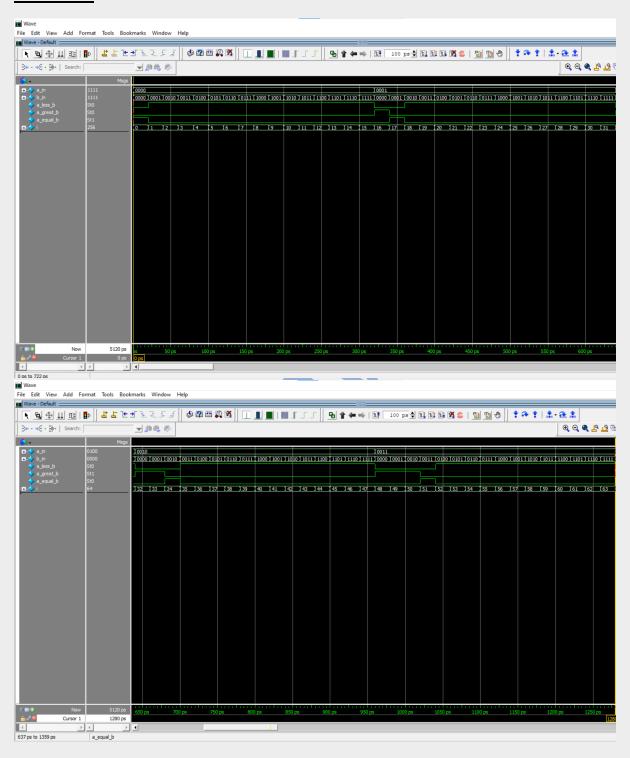


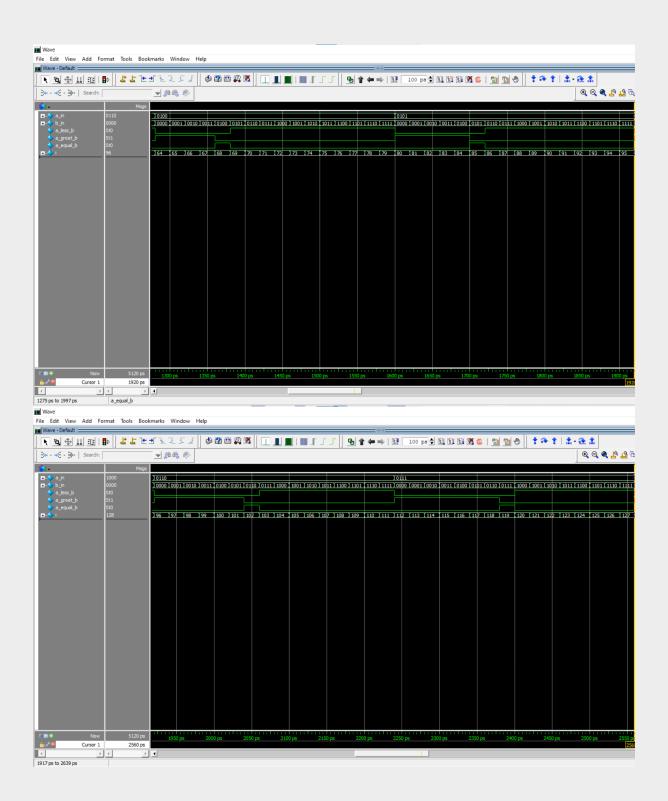


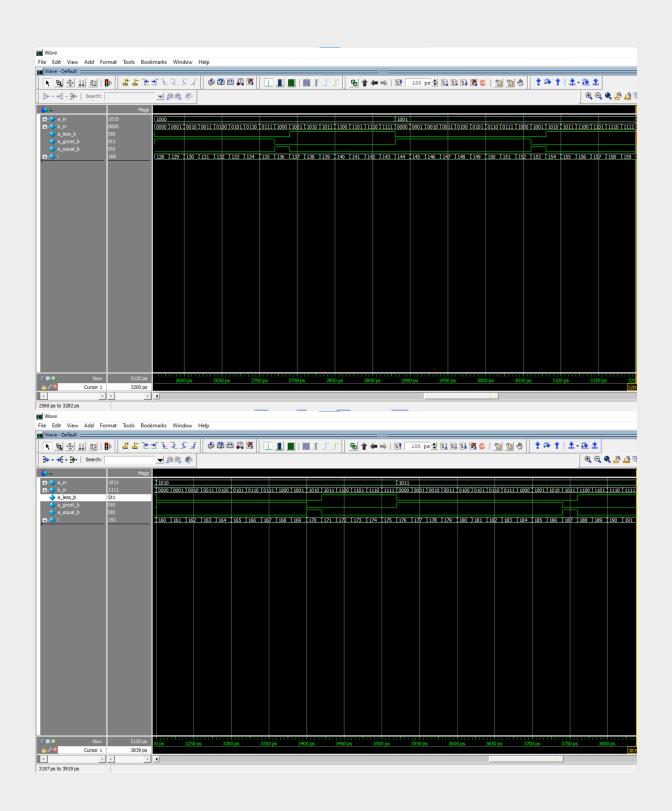


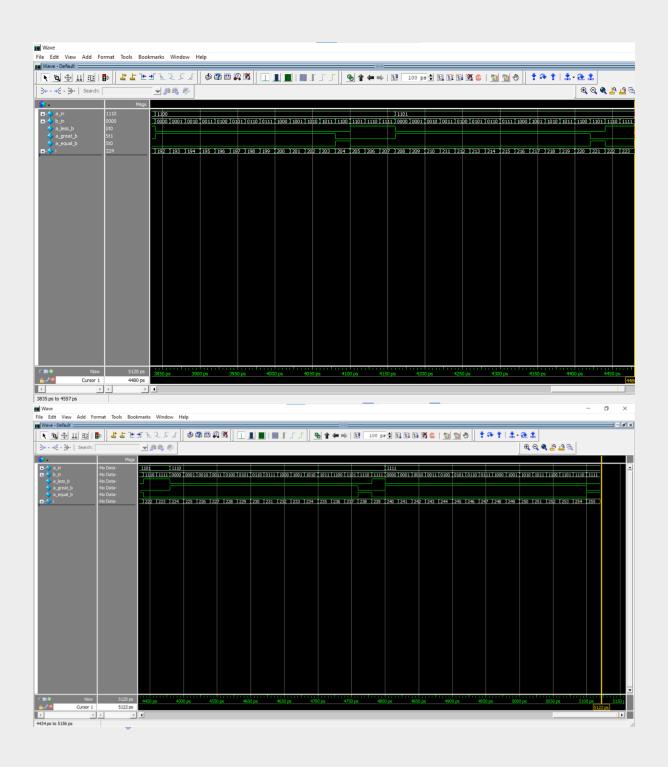
```
# Input A = 1110, Input B = 0000, A<B = 0, A>B = 1, A==b = 0
 Input A = 1110, Input B = 0001, A<B = 0, A>B = 1, A==b = 0
# Input A = 1110, Input B = 0010, A<B = 0, A>B = 1, A==b = 0
# Input A = 1110, Input B = 0011, A<B = 0, A>B = 1, A==b = 0
# Input A = 1110, Input B = 0100, A<B = 0, A>B = 1, A==b = 0
# Input A = 1110, Input B = 0101, A<B = 0, A>B = 1, A==b = 0
# Input A = 1110, Input B = 0110, A<B = 0, A>B = 1, A==b = 0
# Input A = 1110, Input B = 0111, A<B = 0, A>B = 1, A==b = 0
# Input A = 1110, Input B = 1000, A<B = 0, A>B = 1, A==b = 0
# Input A = 1110, Input B = 1001, A<B = 0, A>B = 1, A==b = 0
# Input A = 1110, Input B = 1010, A<B = 0, A>B = 1, A==b = 0
# Input A = 1110, Input B = 1011, A<B = 0, A>B = 1, A==b = 0
# Input A = 1110, Input B = 1100, A<B = 0, A>B = 1, A==b = 0
# Input A = 1110, Input B = 1101, A<B = 0, A>B = 1, A==b = 0
# Input A = 1110, Input B = 1110, A<B = 0, A>B = 0, A==b = 1
# Input A = 1110, Input B = 1111, A<B = 1, A>B = 0, A==b = 0
# Input A = 1111, Input B = 0000, A<B = 0, A>B = 1, A==b = 0
# Input A = 1111, Input B = 0001, A<B = 0, A>B = 1, A==b = 0
# Input A = 1111, Input B = 0010, A<B = 0, A>B = 1, A==b = 0
# Input A = 1111, Input B = 0011, A<B = 0, A>B = 1, A==b = 0
# Input A = 1111, Input B = 0100, A<B = 0, A>B = 1, A==b = 0
# Input A = 1111, Input B = 0101, A<B = 0, A>B = 1, A==b = 0
# Input A = 1111, Input B = 0110, A<B = 0, A>B = 1, A==b = 0
# Input A = 1111, Input B = 0111, A<B = 0, A>B = 1, A==b = 0
# Input A = 1111, Input B = 1000, A<B = 0, A>B = 1, A==b = 0
# Input A = 1111, Input B = 1001, A<B = 0, A>B = 1, A==b = 0
# Input A = 1111, Input B = 1010, A<B = 0, A>B = 1, A==b = 0
# Input A = 1111, Input B = 1011, A<B = 0, A>B = 1, A==b = 0
# Input A = 1111, Input B = 1100, A<B = 0, A>B = 1, A==b = 0
# Input A = 1111, Input B = 1101, A<B = 0, A>B = 1, A==b = 0
# Input A = 1111, Input B = 1110, A<B = 0, A>B = 1, A==b = 0
# Input A = 1111, Input B = 1111, A<B = 0, A>B = 0, A==b = 1
VSIM 5>
```

### **Waves:**









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