MPU-6880
Register Map and Descriptions
Revision 1.0

CONTENTS

1 Revision History

Revision Date	Revision	Description
12/12/2013	1.0	Initial Release

2 Purpose and Scope

This document provides preliminary information regarding the register map and descriptions for the Motion Processing Unit™ MPU-6880™. This document should be used in conjunction with the MPU-6880 Product Specification (PS-MPU-6880A-00) for detailed features, specifications, and other product information.

3 Register Map

The MPU-6880 has two modes of operation in terms of device programmability:

- MPU-6880 mode
  - This is the default manner of operation.
- MPU-6050C compatible mode
  - If this mode is desired, please contact your local InvenSense representative as this would require a change in the device trim setting.

The following table lists the register map for the MPU-6880 mode. All the registers affected by the differences between the two modes are marked by an asterisk (*) in the register name column in the table below and are explained separately below.

Addr (Hex)	Addr (Dec.)	Register Name	Serial I/F	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00	0	SELF_TEST_X_GYRO	R/W	XG_ST_DATA [7:0]							
01	1	SELF_TEST_Y_GYRO	R/W	YG_ST_DATA [7:0]							
02	2	SELF_TEST_Z_GYRO	R/W	ZG_ST_DATA [7:0]							
0D	13	SELF_TEST_X_ACCEL	R/W	XA_ST_DATA [7:0]							
0E	14	SELF_TEST_Y_ACCEL	R/W	YA_ST_DATA [7:0]							
0F	15	SELF_TEST_Z_ACCEL	R/W	ZA_ST_DATA [7:0]							
13	19	XG_OFFSET_H	R/W	X_OFFS_USR [15:8]							
14	20	XG_OFFSET_L	R/W	X_OFFS_USR [7:0]							
15	21	YG_OFFSET_H	R/W	Y_OFFS_USR [15:8]							
16	22	YG_OFFSET_L	R/W	Y_OFFS_USR [7:0]							
17	23	ZG_OFFSET_H	R/W	Z_OFFS_USR [15:8]							
18	24	ZG_OFFSET_L	R/W	Z_OFFS_USR [7:0]							
19	25	SMPLRT_DIV	R/W	SMPLRT_DIV[7:0]							
1A	26	CONFIG	R/W	-	FIFO_MODE	EXT_SYNC_SET[2:0]			DLPF_CFG[2:0]		
1B	27	GYRO_CONFIG	R/W	XG_ST_EN	YG_ST_EN	ZG_ST_EN	GYRO_FS_SEL [1:0]		-	FCHOICE_B[1:0]	
1C	28	ACCEL_CONFIG	R/W	XA_ST_EN	YA_ST_EN	ZA_ST_EN	ACCEL_FS_SEL[1:0]		-		
1D	29	ACCEL_CONFIG 2	R/W	-				ACCEL_FCHOICE_B	A_DLPF_CFG		
1E	30	LP_ACCEL_ODR *	R/W	-				LPOSC_CLKSEL [3:0]			
1F	31	WOM_THR	R/W	WOM_THRESHOLD [7:0]							
23	35	FIFO_EN	R/W	TEMP_FIFO_EN	GYRO_XOUT	GYRO_YOUT	GYRO_ZOUT	ACCEL	-	-	-
37	55	INT_PIN_CFG	R/W	ACTL	OPEN	LATCH_INT_EN	INT_ANYRD_2CLEAR	ACTL_FSYNC	FSYNC_INT_MODE_EN	-	-
38	56	INT_ENABLE	R/W	-	WOM_EN	-	FIFO_OFLOW_EN	FSYNC_INT_EN	-	-	DATA_RDY_EN
3A	58	INT_STATUS	R	-	WOM_INT	-	FIFO_OFLOW_INT	FSYNC_INT	-	-	DATA_RDY_INT
3B	59	ACCEL_XOUT_H	R	ACCEL_XOUT_H[15:8]							
3C	60	ACCEL_XOUT_L	R	ACCEL_XOUT_L[7:0]							
3D	61	ACCEL_YOUT_H	R	ACCEL_YOUT_H[15:8]							
3E	62	ACCEL_YOUT_L	R	ACCEL_YOUT_L[7:0]							
3F	63	ACCEL_ZOUT_H	R	ACCEL_ZOUT_H[15:8]							
40	64	ACCEL_ZOUT_L	R	ACCEL_ZOUT_L[7:0]							
41	65	TEMP_OUT_H	R	TEMP_OUT_H[15:8]							

Addr (Hex)	Addr (Dec.)	Register Name	Serial I/F	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
42	66	TEMP_OUT_L	R	TEMP_OUT_L[7:0]							
43	67	GYRO_XOUT_H	R	GYRO_XOUT_H[15:8]							
44	68	GYRO_XOUT_L	R	GYRO_XOUT_L[7:0]							
45	69	GYRO_YOUT_H	R	GYRO_YOUT_H[15:8]							
46	70	GYRO_YOUT_L	R	GYRO_YOUT_L[7:0]							
47	71	GYRO_ZOUT_H	R	GYRO_ZOUT_H[15:8]							
48	72	GYRO_ZOUT_L	R	GYRO_ZOUT_L[7:0]							
68	104	SIGNAL_PATH_RESET	R/W	-	-	-	-	-	GYRO_RST	ACCEL_RST	TEMP_RST
69	105	ACCEL_INTEL_CTRL	R/W	ACCEL_INTEL_EN	ACCEL_INTEL_MODE	-		-		-	
6A	106	USER_CTRL	R/W	-	FIFO_EN	-	I2C_IF_DIS	-	FIFO_RST	-	SIG_COND_RST
6B	107	PWR_MGMT_1	R/W	H_RESET	SLEEP	CYCLE	GYRO_STANDBY	TEMP_DIS	CLKSEL[2:0]		
6C	108	PWR_MGMT_2 *	R/W	-		DIS_XA	DIS_YA	DIS_ZA	DIS_XG	DIS_YG	DIS_ZG
72	114	FIFO_COUNTH	R/W	-			FIFO_CNT[12:8]				
73	115	FIFO_COUNTL	R/W	FIFO_CNT[7:0]							
74	116	FIFO_R_W	R/W	D[7:0]							
75	117	WHO_AM_I	R	WHOAMI[7:0]							

Table 1 MPU-6880 mode register map

The table below lists the registers in the MPU-6050C compatible mode register map that are different from the MPU-6880 mode.

Addr (Hex)	Addr (Dec.)	Register Name	Serial I/F	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
6	6	XA_OFFSET_H	R/W	XA_OFFSET [14:7]							
7	7	XA_OFFSET_L	R/W	XA_OFFSET [6:0]							-
8	8	YA_OFFSET_H	R/W	YA_OFFSET [14:7]							
9	9	YA_OFFSET_L	R/W	YA_OFFSET [6:0]							-
A	10	ZA_OFFSET_H	R/W	ZA_OFFSET [14:7]							
B	11	ZA_OFFSET_L	R/W	ZA_OFFSET [6:0]							-
6C	108	PWR_MGMT_2	R/W	LP_WAKE_CTRL[1:0]		DIS_XA	DIS_YA	DIS_ZA	DIS_XG	DIS_YG	DIS_ZG

Table 2 MPU-6050C compatible mode register map

Note: Register Names ending in _H and _L contain the high and low bytes, respectively, of an internal register value.

In the detailed register tables that follow, register names are in capital letters, while register values are in capital letters and italicized. For example, the ACCEL_XOUT_H register (Register 59) contains the 8 most significant bits, *ACCEL_XOUT*[15:8], of the 16-bit X-Axis accelerometer measurement, *ACCEL_XOUT*.

The reset value is 0x00 for all registers other than the registers below, also the self-test registers contain pre-programmed values and will not be 0x00 after reset.

- Register 107 (0x01) Power Management 1
- Register 117 (0x78) WHO_AM_I

4 Register Descriptions

This section describes the function and contents of each register within the MPU-6880. All the descriptions relate to the default MPU-6880 mode of operation. Any differences specific to the MPU-6050C mode of operation are described in the specific register sections below.

Note: The device will come up in active mode upon power-up.

4.1 Registers 0 to 2 – Gyroscope Self-Test Registers

Serial IF: R/W

Reset value: 0x00

REGISTER	BITS	FUNCTION
SELF_TEST_X_GYRO	XG_ST_DATA[7:0]	The value in this register indicates the self test output generated during manufacturing tests. This value is to be used to check against subsequent self test outputs performed by the end user.
SELF_TEST_Y_GYRO	YG_ST_DATA[7:0]	The value in this register indicates the self test output generated during manufacturing tests. This value is to be used to check against subsequent self test outputs performed by the end user.
SELF_TEST_Z_GYRO	ZG_ST_DATA[7:0]	The value in this register indicates the self test output generated during manufacturing tests. This value is to be used to check against subsequent self test outputs performed by the end user.

Gyroscope Hardware Self-Test: Relative Method

Gyroscope self-test permits users to test the mechanical and electrical portions of the gyroscope.

When self-test is activated, the on-board electronics will actuate the appropriate sensor. Please refer to register 27 for the corresponding bits to activate the self-test. This actuation will vibrate the sensor's proof masses over a distance equivalent to a pre-defined Coriolis force. This proof mass vibration results in a change in the sensor output, which is reflected in the output signal. The output signal is used to observe the self-test response.

The self-test response (STR) is defined as follows:

$$SelfTest\ Response =$$

$$Gyroscope\ Output\ with\ Self\text{-}Test\ Enabled - Gyroscope\ Output\ with\ Self\text{-}Test\ Disabled$$

This self-test response is used to determine whether the part has passed or failed self-test by finding the change from factory trim of the self-test response as follows:

$$Change\ from\ Factory\ Trim\ of\ the\ Self\text{-}Test\ Response(\%) = \frac{(STR - FT)}{FT}$$

where,

$$FT = Factory\ trim\ value\ of\ selftest\ response$$

This change from factory trim of the self-test response must be within the limits provided in the MPU-6880 Product Specification document for the part to pass self-test. Otherwise, the part is deemed to have failed self-test.

Obtaining the Gyroscope Factory Trim (FT) Value

The procedure detailed below can be followed to obtain the Factory trim value of the self-test response (FT) mentioned above.

The Factory trim value of the self-test response (FT) is calculated as shown below. FT[Xg], FT[Yg], and FT[Zg] refer to the factory trim (FT) values for the gyroscope X, Y, and Z axes, respectively. XG_TEST is the decimal version of XG_ST_DATA[7-0], YG_TEST is the decimal version of YG_ST_DATA[7-0], and ZG_TEST is the decimal version of ZG_ST_DATA[7-0].

When performing self-test for the gyroscope, the full-scale range should be set to ±250dps.

$$FT[Xg] = 20 * 1.01^{(XG\_TEST-1)} \quad \text{if XG\_TEST} \neq 0$$

$$FT[Yg] = 20 * 1.01^{(YG\_TEST-1)} \quad \text{if YG\_TEST} \neq 0$$

$$FT[Zg] = 20 * 1.01^{(ZG\_TEST-1)} \quad \text{if ZG\_TEST} \neq 0$$

If XG_TEST, YG_TEST, or ZG_TEST is 0, it indicates no FT data. Relative method does not apply in this case.

4.2 Registers 13 to 15 – Accelerometer Self-Test Registers

Serial IF: R/W

Reset value: 0x00

REGISTER	BITS	FUNCTION
SELF_TEST_X_ACCEL	XA_ST_DATA[7:0]	The value in this register indicates the self test output generated during manufacturing tests. This value is to be used to check against subsequent self test outputs performed by the end user.
SELF_TEST_Y_ACCEL	YA_ST_DATA[7:0]	The value in this register indicates the self test output generated during manufacturing tests. This value is to be used to check against subsequent self test outputs performed by the end user.
SELF_TEST_Z_ACCEL	ZA_ST_DATA[7:0]	The value in this register indicates the self test output generated during manufacturing tests. This value is to be used to check against subsequent self test outputs performed by the end user.

Accelerometer Hardware Self-Test: Relative Method

Accelerometer self-test permits users to test the mechanical and electrical portions of the accelerometer. Code for operating self-test is included within the MotionApps software provided by InvenSense. Please refer to the next section (titled Obtaining the Accelerometer Factory Trim (FT) Value) if not using MotionApps software.

When self-test is activated, the on-board electronics will actuate the appropriate sensor. Please refer to register 28 for the corresponding bits to activate the self-test. This actuation simulates an external acceleration. The actuated sensor, in turn, will produce a corresponding output signal. The output signal is used to observe the self-test response.

The self-test response (STR) is defined as follows:

$$\begin{aligned} &SelfTest\ Response \\ &= Accelerometer\ Output\ with\ Self\text{-}Test\ Enabled \\ &- Accelerometer\ Output\ with\ Self\text{-}Test\ Disabled \end{aligned}$$

This self-test response is used to determine whether the part has passed or failed self-test by finding the change from factory trim of the self-test response as follows:

$$Change\ from\ Factory\ Trim\ of\ the\ Self\text{-}Test\ Response(\%) = \frac{(STR - FT)}{FT}$$

where,

$$FT = Factory\ trim\ value\ of\ selftest\ response$$

This change from factory trim of the self-test response must be within the limits provided in the MPU-6880 Product Specification document for the part to pass self-test. Otherwise, the part is deemed to have failed self-test.

Obtaining the Accelerometer Factory Trim (FT) Value

If InvenSense MotionApps software is not used, the procedure detailed below should be followed to obtain the Factory trim value of the self test response (FT) mentioned above.

The Factory trim value of the self test response (FT) is calculated as shown below. FT[Xa], FT[Ya], and FT[Za] refer to the factory trim (FT) values for the accelerometer X, Y, and Z axes, respectively. XA_TEST is the decimal version of XA_ST_DATA[7-0], YA_TEST is the decimal version of YA_ST_DATA[7-0], and ZA_TEST is the decimal version of ZA_ST_DATA[7-0].

When performing accelerometer self test, the full-scale range should be set to ±8*g*.

$$\mathrm{FT[Xa]} = 0.16 * 1.01^{(XA\_TEST-1)} \quad \text{if XA\_TEST} \neq 0$$

$$\mathrm{FT[Ya]} = 0.16 * 1.01^{(YA\_TEST-1)} \quad \text{if YA\_TEST} \neq 0$$

$$\mathrm{FT[Za]} = 0.16 * 1.01^{(ZA\_TEST-1)} \quad \text{if ZA\_TEST} \neq 0$$

If XA_TEST, YA_TEST, or ZA_TEST is 0, it indicates no FT data. Relative method does not apply in this case.

4.3 Registers 19 to 24 – Gyro Offset Registers

Serial IF: R/W

Reset value: 0x00

BIT	NAME	FUNCTION

BIT	NAME	FUNCTION
[7:0]	X_OFFS_USR[15:8]	High byte, Low byte in USR register (14h) **OffsetLSB=** X_OFFS_USR * 4 / 2^FS_SEL **OffsetDPS=** X_OFFS_USR * 4 / 2^FS_SEL / Gyro_Sensitivity Nominal FS_SEL = 0 Conditions Gyro_Sensitivity = 2^16 LSB / 500dps Max 999.969 dps Min -1000 dps Step 0.0305 dps
[7:0]	X_OFFS_USR[7:0]	Low byte, High byte in USR register (13h)
[7:0]	Y_OFFS_USR[15:8]	High byte, Low byte in USR register (16h) **OffsetLSB=** Y_OFFS_USR * 4 / 2^FS_SEL **OffsetDPS=** Y_OFFS_USR * 4 / 2^FS_SEL / Gyro_Sensitivity Nominal FS_SEL = 0 Conditions Gyro_Sensitivity = 2^16 LSB / 500dps Max 999.969 dps Min -1000 dps Step 0.0305 dps
[7:0]	Y_OFFS_USR[7:0]	Low byte, High byte in USR register (15h)
[7:0]	Z_OFFS_USR[15:8]	High byte, Low byte in USR register (18h) **OffsetLSB=** Z_OFFS_USR * 4 / 2^FS_SEL **OffsetDPS=** Z_OFFS_USR * 4 / 2^FS_SEL / Gyro_Sensitivity Nominal FS_SEL = 0 Conditions Gyro_Sensitivity = 2^16 LSB / 500dps Max 999.969 dps Min -1000 dps Step 0.0305 dps
[7:0]	Z_OFFS_USR[7:0]	Low byte, High byte in USR register (17h)

These registers are used to remove DC bias from the gyro sensor data output for X, Y and Z axes. The values in these registers are subtracted from the gyro sensor values before going into the sensor registers. Please refer to registers 67 to 72 for units.

4.4 Register 25 – Sample Rate Divider

Serial IF: R/W

Reset value: 0x00

BIT	NAME	FUNCTION
[7:0]	SMPLRT_DIV[7:0]	Divides the internal sample rate (see register CONFIG) to generate the sample rate that controls sensor data output rate, FIFO sample rate. NOTE: This register is only effective when Fchoice = 2'b11 (fchoice_b register bits are 2'b00), and (0 < dlpf_cfg < 7), such that the average filter's output is selected (see chart below). This is the update rate of sensor register. **SAMPLE_RATE=** Internal_Sample_Rate / (1 + SMPLRT_DIV)

Data should be sampled at or above sample rate; SMPLRT_DIV is only used for1kHz internal sampling.

4.5 Register 26 – Configuration

BIT	NAME	FUNCTION
[7]	Reserved	
[6]	FIFO_MODE	When set to '1', when the fifo is full, additional writes will not be written to fifo. When set to '0', when the fifo is full, additional writes will be written to the fifo, replacing the oldest data.
[5:3]	EXT_SYNC_SET[2:0]	Enables the FSYNC pin data to be sampled. **EXT_SYNC_SET** / **FSYNC bit location** 0 – function disabled 1 – TEMP_OUT_L[0] 2 – GYRO_XOUT_L[0] 3 – GYRO_YOUT_L[0] 4 – GYRO_ZOUT_L[0] 5 – ACCEL_XOUT_L[0] 6 – ACCEL_YOUT_L[0] 7 – ACCEL_ZOUT_L[0] Fsync will be latched to capture short strobes. This will be done such that if Fsync toggles, the latched value toggles, but won't toggle again until the new latched value is captured by the sample rate strobe. This is a requirement for working with some 3rd party devices that have fsync strobes shorter than our sample rate.
[2:0]	DLPF_CFG[2:0]	For the DLPF to be used, fchoice[1:0] must be set to 2'b11, fchoice_b[1:0] is 2'b00.

		See table 3 below.

The DLPF is configured by *DLPF_CFG*, when *FCHOICE_B* [1:0] = 2b'00. The gyroscope and temperature sensor are filtered according to the value of *DLPF_CFG* and *FCHOICE_B* as shown in the table below. Note that FCHOICE mentioned in the table below is the inverted value of *FCHOICE_B* (e.g. FCHOICE=2b'00 is same as FCHOICE_B=2b'11).

FCHOICE		DLPF_CFG	Gyroscope			Temperature Sensor	
<1>	<0>		Bandwidth (Hz)	Delay (ms)	Fs (kHz)	Bandwidth (Hz)	Delay (ms)
x	0	x	8800	0.064	32	4000	0.04
0	1	x	3600	0.11	32	4000	0.04
1	1	0	250	0.97	8	4000	0.04
1	1	1	184	2.9	1	188	1.9
1	1	2	92	3.9	1	98	2.8
1	1	3	41	5.9	1	42	4.8
1	1	4	20	9.9	1	20	8.3
1	1	5	10	17.85	1	10	13.4
1	1	6	5	33.48	1	5	18.6
1	1	7	3600	0.17	8	4000	0.04

4.6 Register 27 – Gyroscope Configuration

Serial IF: R/W

Reset value: 0x00

BIT	NAME	FUNCTION
[7]	XG_ST_EN	X Gyro self-test
[6]	YG_ST_EN	Y Gyro self-test
[5]	ZG_ST_EN	Z Gyro self-test
[4:3]	GYRO_FS_SEL[1:0]	Gyro Full Scale Select: 00 = ±250dps 01= ±500dps 10 = ±1000dps 11 = ±2000dps
[2]	-	Reserved
[1:0]	FCHOICE_B[1:0]	Used to bypass DLPF as shown in table 1 above. NOTE: Register is FCHOICE_B (inverted version of FCHOICE), table 1 uses FCHOICE (which is the inverted version of this register).

4.7 Register 28 – Accelerometer Configuration

Serial IF: R/W

Reset value: 0x00

BIT	NAME	FUNCTION
[7]	XA_ST_EN	X Accel self-test
[6]	YA_ST_EN	Y Accel self-test
[5]	ZA_ST_EN	Z Accel self-test
[4:3]	ACCEL_FS_SEL[1:0]	Accel Full Scale Select: ±2g (00), ±4g (01), ±8g (10), ±16g (11)
[2:0]	Reserved	

4.8 Register 29 – Accelerometer Configuration 2

Serial IF: R/W

Reset value: 0x00

BIT	NAME	FUNCTION
[7:4]	Reserved	
[3]	ACCEL_FCHOICE_B	Used to bypass DLPF as shown in table 2 below. NOTE: This register contains ACCEL_FCHOICE_B (the inverted version of ACCEL_FCHOICE as described in the table below).
[2:0]	A_DLPFCFG	Accelerometer low pass filter setting as shown in table 2 below.

Accelerometer Data Rates and Bandwidths (Normal Mode)

ACCEL_FCHOICE	A_DLPF_CFG	Output			
		Bandwidth (Hz)	Delay (ms)	Noise Density (ug/rtHz)	Rate (kHz)
0	X	1.13 K	0.75	250	4
1	0	460	1.94	250	1
1	1	184	5.80	250	1
1	2	92	7.80	250	1

1	3	41	11.80	250	1
1	4	20	19.80	250	1
1	5	10	35.70	250	1
1	6	5	66.96	250	1
1	7	460	1.94	250	1

The data output rate of the DLPF filter block can be further reduced by a factor of 1/(1+SMPLRT_DIV), where SMPLRT_DIV is an 8-bit integer. Following is a small subset of ODRs that are configurable for the accelerometer in the normal mode in this manner (Hz):

3.91, 7.81, 15.63, 31.25, 62.50, 125, 250, 500, 1K

The following table lists the approximate accelerometer filter bandwidths available in the low-power mode of operation.

In the low-power mode of operation, the accelerometer is duty-cycled. ACCEL_FCHOICE=0 for all options.

Accelerometer Data Rates and Bandwidths (Low-Power Mode)

ACCEL_FCHOICE	ODR (Hz)	Output	
		Bandwidth (Hz)	Delay (ms)
0	0.24	1.1 k	1
0	0.49	1.1 k	1
0	0.98	1.1 k	1
0	1.95	1.1 k	1
0	3.91	1.1 k	1
0	7.81	1.1 k	1
0	15.63	1.1 k	1
0	31.25	1.1 k	1
0	62.50	1.1 k	1
0	125	1.1 k	1
0	250	1.1 k	1
0	500	1.1 k	1

As you can see from the tables above, some of the ODRs can be configured in the normal accelerometer mode as well as low power mode.

For further details on how to configure the individual ODRs, please refer to register 30 Low Power Accelerometer ODR Control.

4.9 Register 30 – Low Power Accelerometer ODR Control

Serial IF: R/W

Reset value: 0x00

BIT	NAME	FUNCTION
[7:4]	Reserved	
[3:0]	LPOSC_CLKSEL[3:0]	Sets the frequency of waking up the chip to take a sample of accel data – the low power accel Output Data Rate.

LPOSC_CLKSEL	Output Frequency (Hz)
0	0.24
1	0.49
2	0.98
3	1.95
4	3.91
5	7.81
6	15.63
7	31.25
8	62.50
9	125
10	250
11	500
12-15	Reserved

Please refer to the register 108 Power Management 2 for further details on the MPU-6050C compatible mode.

4.10 Register 31 – Wake-on Motion Threshold

Serial IF: R/W

Reset value: 0x00

BIT	NAME	FUNCTION
[7:0]	WOM_THRESHOLD	This register holds the threshold value for the Wake on Motion Interrupt for accel x/y/z axes. LSB = 4mg. Range is 0mg to 1020mg.

For more details on how to configure the Wake-on-Motion interrupt, please refer to section 5 in the MPU-6880 Product Specification document.

4.11 Register 35 – FIFO Enable

Serial IF: R/W

Reset value: 0x00

BIT	NAME	FUNCTION
[7]	TEMP_OUT	1 – Write TEMP_OUT_H and TEMP_OUT_L to the FIFO at the sample rate; If enabled, buffering of data occurs even if data path is in standby. 0 – function is disabled
[6]	GYRO_XOUT	1 – Write GYRO_XOUT_H and GYRO_XOUT_L to the FIFO at the sample rate; If enabled, buffering of data occurs even if data path is in standby. 0 – function is disabled
[5]	GYRO_YOUT	1 – Write GYRO_YOUT_H and GYRO_YOUT_L to the FIFO at the sample rate; If enabled, buffering of data occurs even if data path is in standby. 0 – function is disabled NOTE: Enabling any one of the bits corresponding to the Gyros or Temp data paths, data is buffered into the FIFO even though that data path is not enabled.
[4]	GYRO_ZOUT	1 – Write GYRO_ZOUT_H and GYRO_ZOUT_L to the FIFO at the sample rate; If enabled, buffering of data occurs even if data path is in standby. 0 – function is disabled
[3]	ACCEL	1 – write ACCEL_XOUT_H, ACCEL_XOUT_L, ACCEL_YOUT_H, ACCEL_YOUT_L, ACCEL_ZOUT_H, and ACCEL_ZOUT_L to the FIFO at the sample rate; 0 – function is disabled
[2:0]	-	Reserved

4.12 Register 55 – INT Pin Enable Configuration

Serial IF: R/W

Reset value: 0x00

BIT	NAME	FUNCTION
[7]	ACTL	1 – The logic level for INT pin is active low. 0 – The logic level for INT pin is active high.
[6]	OPEN	1 – INT pin is configured as open drain. 0 – INT pin is configured as push-pull.
[5]	LATCH_INT_EN	1 – INT pin level held until interrupt status is cleared. 0 – INT pin indicates interrupt pulse's is width 50us.
[4]	INT_ANYRD_2CLEAR	1 – Interrupt status is cleared if any read operation is performed. 0 – Interrupt status is cleared only by reading INT_STATUS register

BIT	NAME	FUNCTION
[3]	ACTL_FSYNC	1 – The logic level for the FSYNC pin as an interrupt is active low. 0 – The logic level for the FSYNC pin as an interrupt is active high.
[2]	FSYNC_INT_MODE_EN	1 – This enables the FSYNC pin to be used as an interrupt. A transition to the active level described by the ACTL_FSYNC bit will cause an interrupt. 0 – This disables the FSYNC pin from causing an interrupt.
[1-0]	Reserved	

4.13 Register 56 – Interrupt Enable

Serial IF: R/W

Reset value: 0x00

BIT	NAME	FUNCTION
[7]	Reserved	
[6]	WOM_EN	1 – Enable interrupt for wake on motion to propagate to interrupt pin. 0 – function is disabled.
[5]	Reserved	
[4]	FIFO_OVERFLOW_EN	1 – Enable interrupt for fifo overflow to propagate to interrupt pin. 0 – function is disabled.
[3]	FSYNC_INT_EN	1 – Enable Fsync interrupt to propagate to interrupt pin. 0 – function is disabled.
[2:1]	-	Reserved
[0]	DATA_RDY_EN	1 – Enable Raw Sensor Data Ready interrupt to propagate to interrupt pin. 0 – function is disabled.

4.14 Register 58 – Interrupt Status

Serial IF: R/C

Reset value: 0x00

BIT	NAME	FUNCTION
[7]	Reserved	
[6]	WOM_INT	1 – Wake on motion interrupt occurred.

BIT	NAME	FUNCTION
[5]	Reserved	
[4]	FIFO_OVERFLOW_INT	1 – Fifo Overflow interrupt occurred. Note that the oldest data is has been dropped from the fifo.
[3]	FSYNC_INT	1 – Fsync interrupt occurred.
[2]	Reserved	
[1]	Reserved	
[0]	DATA_RDY_INT	This bit automatically sets to 1 when a Data Ready interrupt is generated. The bit clears to 0 after the register has been read.

4.15 Registers 59 to 64 – Accelerometer Measurements

Name: ACCEL_XOUT_H

Serial IF: R

Reset value: 0x00 (if sensor disabled)

BIT	NAME	FUNCTION
[7:0]	ACCEL_XOUT_H[15:8]	High byte of accelerometer x-axis data.

Name: ACCEL_XOUT_L

Serial IF: R

Reset value: 0x00 (if sensor disabled)

BIT	NAME	FUNCTION
[7:0]	ACCEL_XOUT_L[7:0]	Low byte of accelerometer x-axis data.

Name: ACCEL_YOUT_H

Serial IF: R

Reset value: 0x00 (if sensor disabled)

BIT	NAME	FUNCTION
[7:0]	ACCEL_YOUT_H[15:8]	High byte of accelerometer y-axis data.

Name: ACCEL_YOUT_L

Serial IF: R

Reset value: 0x00 (if sensor disabled)

BIT	NAME	FUNCTION
[7:0]	ACCEL_YOUT_L[7:0]	Low byte of accelerometer y-axis data.

Name: ACCEL_ZOUT_H

Serial IF: R

Reset value: 0x00 (if sensor disabled)

BIT	NAME	FUNCTION
[7:0]	ACCEL_ZOUT_H[15:8]	High byte of accelerometer z-axis data.

Name: ACCEL_ZOUT_L

Serial IF: R

Reset value: 0x00 (if sensor disabled)

BIT	NAME	FUNCTION
[7:0]	ACCEL_ZOUT_L[7:0]	Low byte of accelerometer z-axis data.

4.16 Registers 65 and 66 – Temperature Measurement

Name: TEMP_OUT_H

Serial IF: R

Reset value: 0x00 (if sensor disabled)

BIT	NAME	FUNCTION
[7:0]	TEMP_OUT_H[15:8]	High byte of the temperature sensor output

Name: TEMP_OUT_L

Serial IF: R

Reset value: 0x00 (if sensor disabled)

BIT	NAME	FUNCTION
[7:0]	TEMP_OUT_L[7:0]	Low byte of the temperature sensor output **TEMP_degC** = ((TEMP_OUT – RoomTemp_Offset)/Temp_Sensitivity) + 25degC

4.17 Registers 67 to 72 – Gyroscope Measurements

Name: GYRO_XOUT_H

Serial IF: R

Reset value: 0x00 (if sensor disabled)

BIT	NAME	FUNCTION
[7:0]	GYRO_XOUT_H[7:0]	High byte of the X-Axis gyroscope output

Name: GYRO_XOUT_L

Serial IF: R

Reset value: 0x00 (if sensor disabled)

BIT	NAME	FUNCTION

BIT	NAME	FUNCTION
[7:0]	GYRO_XOUT_L[7:0]	Low byte of the X-Axis gyroscope output **GYRO_XOUT =** Gyro_Sensitivity * X_angular_rate Nominal FS_SEL = 0 Conditions Gyro_Sensitivity = 131 LSB/(°/s)

Name: GYRO_YOUT_H

Serial IF: R

Reset value: 0x00 (if sensor disabled)

BIT	NAME	FUNCTION
[7:0]	GYRO_YOUT_H[7:0]	High byte of the Y-Axis gyroscope output

Name: GYRO_YOUT_L

Serial IF: R

Reset value: 0x00 (if sensor disabled)

BIT	NAME	FUNCTION
[7:0]	GYRO_YOUT_L[7:0]	Low byte of the Y-Axis gyroscope output **GYRO_YOUT =** Gyro_Sensitivity * Y_angular_rate Nominal FS_SEL = 0 Conditions Gyro_Sensitivity = 131 LSB/(°/s)

Name: GYRO_ZOUT_H

Serial IF: R

Reset value: 0x00 (if sensor disabled)

BIT	NAME	FUNCTION
[7:0]	GYRO_ZOUT_H[7:0]	High byte of the Z-Axis gyroscope output

Name: GYRO_ZOUT_L

Serial IF: R

Reset value: 0x00 (if sensor disabled)

BIT	NAME	FUNCTION
[7:0]	GYRO_ZOUT_L[7:0]	Low byte of the Z-Axis gyroscope output **GYRO_ZOUT =** Gyro_Sensitivity * Z_angular_rate Nominal Conditions: FS_SEL = 0 Gyro_Sensitivity = 131 LSB/(°/s)

4.18 Register 104 – Signal Path Reset

SIGNAL_PATH_RESET

Serial IF: R/W

Reset value: 0x00

BIT	NAME	FUNCTION
[7:3]	Reserved	
[2]	GYRO_RST	Reset gyro digital signal path. Note: Sensor registers are not cleared. Use SIG_COND_RST to clear sensor registers.
[1]	ACCEL_RST	Reset accel digital signal path. Note: Sensor registers are not cleared. Use SIG_COND_RST to clear sensor registers.
[0]	TEMP_RST	Reset temp digital signal path. Note: Sensor registers are not cleared. Use SIG_COND_RST to clear sensor registers.

4.19 Register 105 – Accelerometer Interrupt Control

ACCEL_INTEL_CTRL

Serial IF: R/W

Reset value: 0x00

BIT	NAME	FUNCTION
[7]	ACCEL_INTEL_EN	This bit enables the Wake-on-Motion detection logic.
[6]	ACCEL_INTEL_MODE	This bit defines 1 = Compare the current sample with the previous sample. 0 = Not used.
[5:0]	Reserved	

Please refer to the Wake-on-Motion Interrupt section of the MPU-6880 Product Specification for additional details.

4.20 Register 106 – User Control

Name: USER_CTRL

Serial IF: R/W

Reset value: 0x00

BIT	NAME	FUNCTION
[7]	Reserved	
[6]	FIFO_EN	1 – Enable FIFO operation mode. 0 – Disable FIFO access from serial interface. To disable FIFO writes by dma, use FIFO_EN register.
[5]	-	Reserved
[4]	I2C_IF_DIS	1 – Reset I2C Slave module and put the serial interface in SPI mode only. This bit auto clears after one clock cycle of the internal 20MHz clock.
[3]	Reserved	
[2]	FIFO_RST	1 – Reset FIFO module. Reset is asynchronous. This bit auto clears after one clock cycle of the internal 20MHz clock.
[1]	-	Reserved
[0]	SIG_COND_RST	1 – Reset all gyro digital signal path, accel digital signal path, and temp digital signal path. This bit also clears all the sensor registers.

4.21 Register 107 – Power Management 1

Name: PWR_MGMT_1

Serial IF: R/W

Reset value: 0x01

BIT	NAME	FUNCTION
[7]	H_RESET	1 – Reset the internal registers and restores the default settings. Write a 1 to set the reset, the bit will auto clear.
[6]	SLEEP	When set, the chip is set to sleep mode.

BIT	NAME	FUNCTION
[5]	CYCLE	When set, and SLEEP and STANDBY are not set, the chip will cycle between sleep and taking a single sample at a rate determined by LP_ACCEL_ODR (MPU-6880 mode) or LP_WAKE_CTRL (MPU-6050C compatible mode) NOTE: When all accelerometer axis are disabled via PWR_MGMT_2 register bits and cycle is enabled, the chip will wake up at the rate determined by the respective registers above, but will not take any samples.
[4]	GYRO_STANDBY	When set, the gyro drive and pll circuitry are enabled, but the sense paths are disabled. This is a low power mode that allows quick enabling of the gyros.
[3]	TEMP_DIS	When set to 1, this bit disables the temperature sensor.
[2:0]	CLKSEL[2:0]	**Code** **Clock Source** 0 Internal 20MHz oscillator 1 Auto selects the best available clock source – PLL if ready, else use the Internal oscillator 2 Auto selects the best available clock source – PLL if ready, else use the Internal oscillator 3 Auto selects the best available clock source – PLL if ready, else use the Internal oscillator 4 Auto selects the best available clock source – PLL if ready, else use the Internal oscillator 5 Auto selects the best available clock source – PLL if ready, else use the Internal oscillator 6 Internal 20MHz oscillator 7 Stops the clock and keeps timing generator in reset

4.22 Register 108 – Power Management 2

Name: PWR_MGMT_2

Serial IF: R/W

Reset value: 0x00

BIT	NAME	FUNCTION
[7:6]	LP_WAKE_CTRL[1:0]	Specifies the frequency of wake-ups during Accelerometer Only Low Power Mode.
[5]	DISABLE_XA	1 – X accelerometer is disabled 0 – X accelerometer is on

BIT	NAME	FUNCTION
[4]	DISABLE_YA	1 – Y accelerometer is disabled 0 – Y accelerometer is on
[3]	DISABLE_ZA	1 – Z accelerometer is disabled 0 – Z accelerometer is on
[2]	DISABLE_XG	1 – X gyro is disabled 0 – X gyro is on
[1]	DISABLE_YG	1 – Y gyro is disabled 0 – Y gyro is on
[0]	DISABLE_ZG	1 – Z gyro is disabled 0 – Z gyro is on

MPU-6050C compatible mode:

In addition to the above default MPU-6880 mode, this register allows the user to configure the frequency of wake-ups in Accelerometer Only Low Power Mode using the *LP_WAKE_CTRL* bits.

The MPU-6880 can be put into Accelerometer Only Low Power Mode using the following steps:

(i) Set CYCLE bit to 1
(ii) Set SLEEP bit to 0
(iii) Set TEMP_DIS bit to 1
(iv) Set DIS_XG, DIS_YG, DIS_ZG bits to 1

The bits mentioned in the steps (i) to (iii) can be found in Power Management 1 register (Register 107).

In this mode, the device will power off all devices except for the primary I^2C interface, waking only the accelerometer at fixed intervals to take a single measurement. The frequency of wake-ups can be configured with *LP_WAKE_CTRL* as shown below.

LP_WAKE_CTRL	Wake-up Frequency
0	1.25 Hz
1	5 Hz
2	20 Hz
3	40 Hz

4.23 Register 114 and 115 – FIFO Count Registers

Name: FIFO_COUNTH

Address: 114

Serial IF: Read Only

Reset value: 0x00

BIT	NAME	FUNCTION
[7:5]	Reserved	
[4:0]	FIFO_CNT[12:8]	High Bits, count indicates the number of written bytes in the FIFO. Reading this byte latches the data for both FIFO_COUNTH, and FIFO_COUNTL.

FIFO_COUNTL

Address: 115

Serial IF: Read Only

Reset value: 0x00

BIT	NAME	FUNCTION
[7:0]	FIFO_CNT[7:0]	Low Bits, count indicates the number of written bytes in the FIFO. NOTE: Must read FIFO_COUNTH to latch new data for both FIFO_COUNTH and FIFO_COUNTL.

4.24 Register 116 – FIFO Read Write

Name: FIFO_R_W

Serial IF: R/W

Reset value: 0x00

BIT	NAME	FUNCTION
[7:0]	D[7:0]	Read/Write command provides Read or Write operation for the FIFO.

Description:

This register is used to read and write data from the FIFO buffer.

Data is written to the FIFO in order of register number (from lowest to highest).

The contents of the sensor data registers are written into the FIFO buffer when their corresponding FIFO enable flags are set to 1 in FIFO_EN (Register 35).

If the FIFO buffer has overflowed, the status bit *FIFO_OFLOW_INT* is automatically set to 1. This bit is located in INT_STATUS (Register 58). When the FIFO buffer has overflowed, the oldest data will be lost and new data will be written to the FIFO unless register 26 CONFIG, bit[6] FIFO_MODE = 1.

If the FIFO buffer is empty, reading this register will return the last byte that was previously read from the FIFO until new data is available. The user should check *FIFO_COUNT* to ensure that the FIFO buffer is not read when empty.

4.25 Register 117 – Who Am I

Name: WHOAMI

Serial IF: Read Only

Reset value: 0x78

BIT	NAME	FUNCTION
[7:0]	WHOAMI	Register to indicate to user which device is being accessed.

This register is used to verify the identity of the device. The contents of *WHO_AM_I* is an 8-bit device ID. The default value of the register is 0x78. This is different from the I2C address of the device as seen on the slave I2C controller by the applications processor. The I2C address of the MPU-6880 is 0x68 or 0x69 depending upon the value driven on AD0 pin.

4.26 Registers 6, 7, 8, 9, 10, 11, Accelerometer Offset Registers

For MPU-6050C compatible mode only:

Name: XA_OFFS_H

Address: 6

Serial IF: R/W

Reset value: 0x00

BIT	NAME	FUNCTION
[7:0]	XA_OFFS[14:7]	Upper bits of the X accelerometer offset cancellation. +/- 16g Offset cancellation in all Full Scale modes, 15 bit 0.98-mg steps

Name: XA_OFFS_L

Address: 7

Serial IF: R/W

Reset value: 0x00

BIT	NAME	FUNCTION
[7:1]	XA_OFFS[6:0]	Lower bits of the X accelerometer offset cancellation. +/- 16g Offset cancellation in all Full Scale modes, 15 bit 0.98-mg steps
[0]	Reserved	

Name: YA_OFFS_H

Address: 8

Serial IF: R/W

Reset value: 0x00

BIT	NAME	FUNCTION
[7:0]	YA_OFFS[14:7]	Upper bits of the Y accelerometer offset cancellation. +/- 16g Offset cancellation in all Full Scale modes, 15 bit 0.98-mg steps

Name: YA_OFFS_L

Address: 9

Serial IF: R/W

Reset value: 0x00

BIT	NAME	FUNCTION
[7:1]	YA_OFFS[6:0]	Lower bits of the Y accelerometer offset cancellation. +/- 16g Offset cancellation in all Full Scale modes, 15 bit 0.98-mg steps
[0]	Reserved	

Name: ZA_OFFS_H

Address: 10

Serial IF: R/W

Reset value: 0x00

BIT	NAME	FUNCTION
[7:0]	ZA_OFFS[14:7]	Upper bits of the Z accelerometer offset cancellation. +/- 16g Offset cancellation in all Full Scale modes, 15 bit 0.98-mg steps

Name: ZA_OFFS_L

Address: 11

Serial IF: R/W

Reset value: 0x00

BIT	NAME	FUNCTION
[7:1]	ZA_OFFS[6:0]	Lower bits of the Z accelerometer offset cancellation. +/- 16g Offset cancellation in all Full Scale modes, 15 bit 0.98-mg steps

BIT	NAME	FUNCTION
[0]	Reserved	

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