MODULE 3
Array Processors

SIMD array processors

- Synchronous array of parallel processors is an array processor
  - Consists of multiple PEs under the supervision of one CU.

- Array processor handle SIMD streams (SIMD computers)
  - Designed to perform vector computations over matrices or arrays of data.

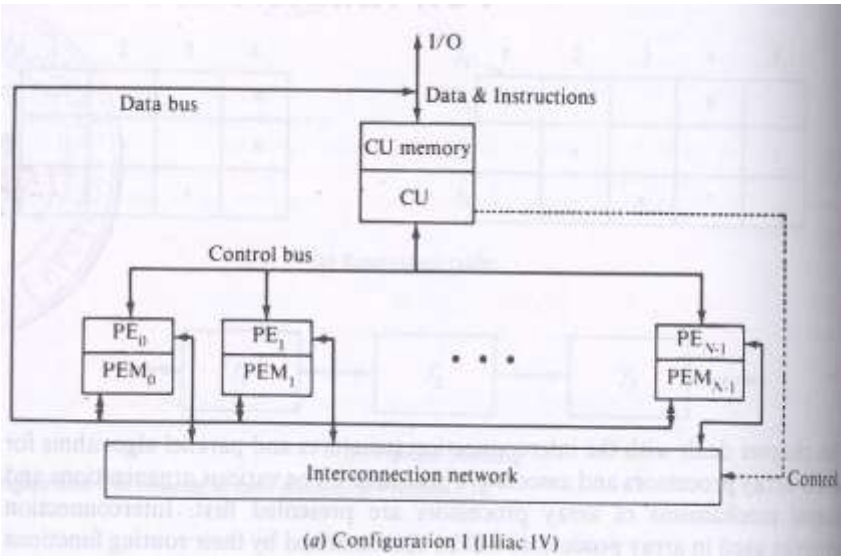
- SIMD computers - 2 basic architectural organizations:

  - **Array processors**, using random-access memory;

  - **Associative processors** using content addressable (or associative) memory.

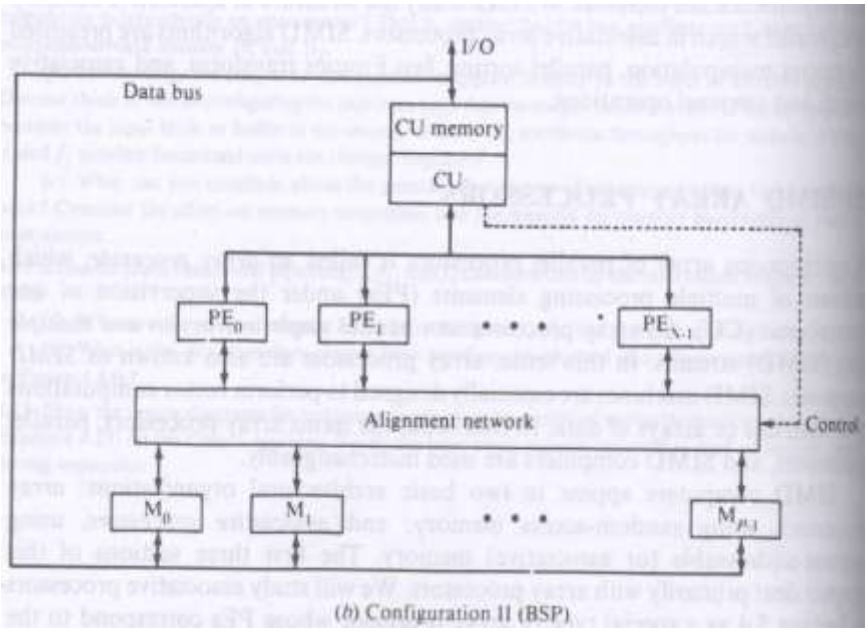
SIMD computer organization

Architectural configurations of SIMD array processors



(a) Configuration I (Illiac IV)

- Configuration1 is structured with N synchronized PEs, under the control of one CU.
- PEi is an ALU with attached **working registers and local memory PEMi**, for storage of distributed data.
- CU has its **main memory for the storage of programs**. The system/user programs are executed under the control of CU.
- User programs are loaded into the CU memory from an external source.
- Function of CU is to **decode instructions** and determine where the decoded instructions should be executed.
- Scalar/control type instructions are executed inside the CU.
- Vector operands are distributed to the PEMs before the parallel execution in the array of PEs.
- Distributed data can be loaded into the PEMs from an external source via the **system data bus**/ via CU in a broadcast mode using the **control bus**.
- PEs may be either ***active or disabled*** during an instruction cycle.
- **Masking vector** is used to control the status of PEs during the execution of a vector instruction. Only enabled PEs participate in the execution of a vector instruction.
- Data exchanges among PEs are done via an **inter PE communication network** (under the control of the control unit), which performs all data routing and manipulation functions.



(b) Configuration II (BSP)

Difference between the configurations --in two aspects

I - local memories attached to the PEs are replaced by ***parallel memory modules*** shared by all PEs through an alignment network.

II - inter PE permutation network is replaced by the inter PE ***memory alignment network*** which is again controlled by CU.

The alignment network is path-switching network between PEs and parallel memories.

- To allow conflict free accesses of the shared memories by as many PEs as possible.

SIMD computer C is characterized by the parameters:

C=<N, F, I, M>

N: no. of PEs. For eg for Illiac-IV has 64, BSP 16.

F: set of data routing functions

I: set of m/c instructions for scalar-vector, data-routing and the network-manipulation operations.

M: the set of masking schemes, where each mask partitions the set of PEs into the 2 disjoint subsets (enabled PEs and disabled PEs).

Masking and Data routing mechanisms

Components in a PE

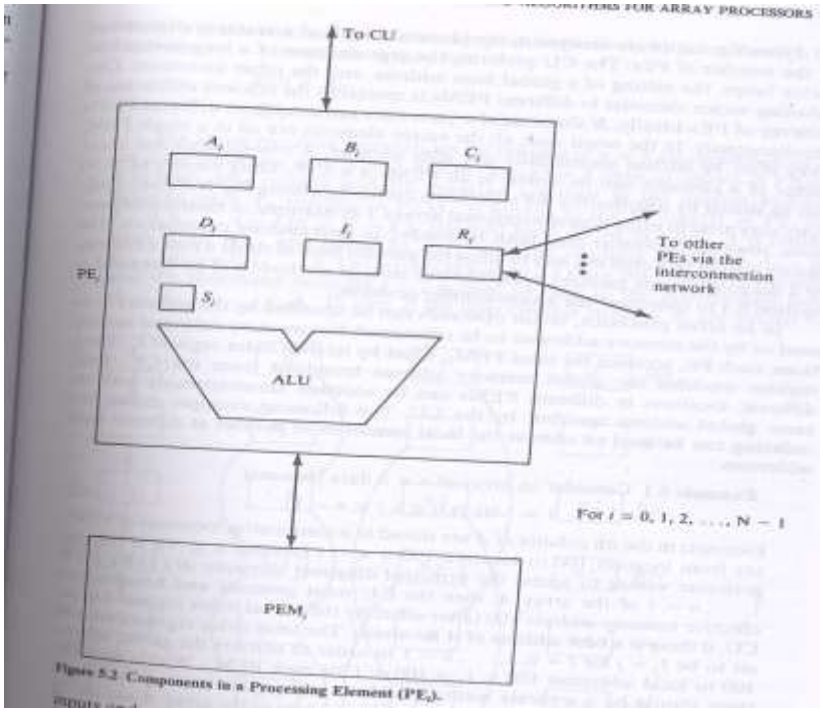


Figure 5.2 Components in a Processing Element (PE_i).

- Here each PE is a processor with its own memory PEM; a set of working registers and flags , namely A, B, C and S; an ALU; a local index register I; an address register D and a data routing register R.
- The R of each PE is connected to the R of other PE via the interconnection n/w.
- When data transfer among PEs occur contents of R registers are being transferred.

- PE is either in *active* or *inactive* mode during instruction cycle.
- If a PE is active, it executes the instruction broadcast to it by the CU otherwise it will not.
- Masking schemes are used to specify the status flag S of PE.

  S=1 indicate active PE and 0 for inactive PE.

Inter –PE communications

Network design is the fundamental decision in determining appropriate architecture of an interconnection network for an SIMD machine.

Decisions are to be made upon…..

Operation mode: 2 types of communication: ***synchronous* and *asynchronous*.**

Synchronous communication needed for establishing communication paths synchronously for either data manipulating function or for data instruction broadcast. **Asynchronous communication** is needed for multiprocessing in which connection requests are issued dynamically.

Control strategy: A typical interconnection n/w consists of a no. of switching elements and interconnecting links. Interconnection functions are realized by properly setting control of the switching elements.

Switching methodology:

Circuit switching and packet switching.

Circuit switching: physical path is established between source and destination.

Packet switching: data is put in a packet and routed through the interconnection n/w without establishing a physical connection path.

N/w topology:

N/w is depicted by a graph.

- Nodes represent switching points and edges represent communication links.

Topologies grouped into 2 categories:

- *Static and dynamic.*

Static topology*:* links between 2 processors are passive and dedicated buses cannot be reconfigured for direct connections to other processors.

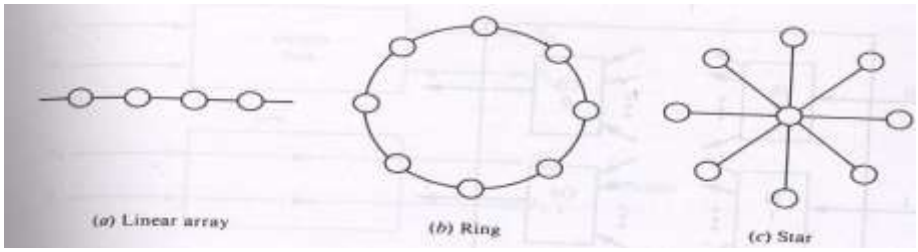
Links in the ***dynamic* category** can be reconfigured by setting the n/ws active switching elements.

SIMD interconnection n/ws

- Interconnection networks carry data between processors and to memory.
- Interconnects are made of switches and links (wires, fiber).
- SIMD interconnection n/ws are classified based on n/w topologies: ***static n/ws and dynamic n/ws.***

Static networks

- Consists of point-to-point communication links among processing nodes
- Also referred to as **direct** networks
- Topologies in the static n/ws can be classified according to the dimensions (1D, 2D, 3D and hypercube) required for layout.
- Eg of 1D : linear array
- 2D: ring, star, tree, mesh, and systolic array.
- 3D:completely connected, chordal ring, 3 cube, 3 cube connected cycle.
- A D dimensional W-wide hypercube contains W nodes in each dimension and there is a connection to a node in each dimension.
- Mesh and 3 cube are actually 2 and 3D hypercubes.



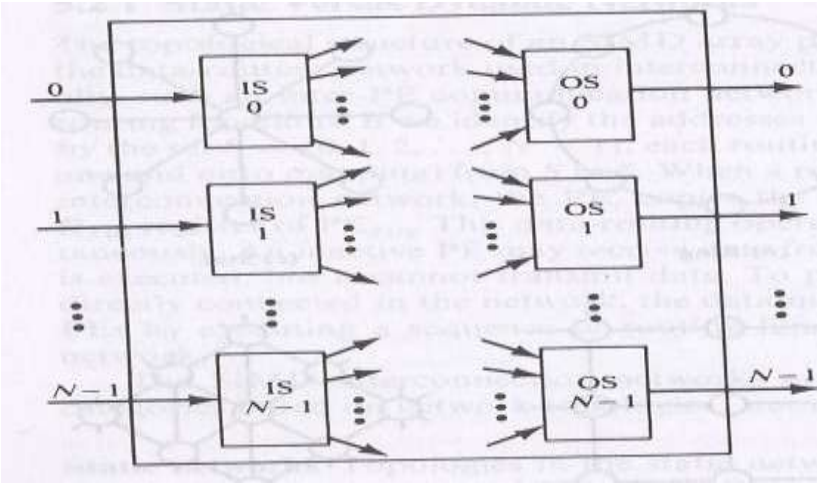
Dynamic networks

- Built using switches (switching element) and links
- Communication links are connected to one another dynamically by the switches to establish paths among processing nodes and memory banks.

Dynamic n/w: 2 classes

- Single stage v/s multistage
- **A single stage** n/w is a switching n/w with N i/p selectors (IS) and N o/p selectors (OS).

Conceptual view of a single stage interconnection n/w



IS is a 1 to D demultiplexer and OS is an M to1 multiplexer where 1<=D<=N and 1<=M<=N.

- Also called *recirculating n/w*.

  Data items may have to recirculate through the single stage several times before reaching their final destinations.The no. of recirculations needed depends on the connectivity in the single stage n/w.

Multistage n/w:

- Many stages of interconnected switches form a multistage SIMD network. Multistage n/ws are described by 3 characterizing features: switch box, network topology and control structure.
- Many switch boxes are used in a multistage n/w.
- Each box is an interchange device with 2 i/ps and 2 o/ps.
- **4 states of switch box**:

  Straight, exchange, upper broadcast and lower broadcast.

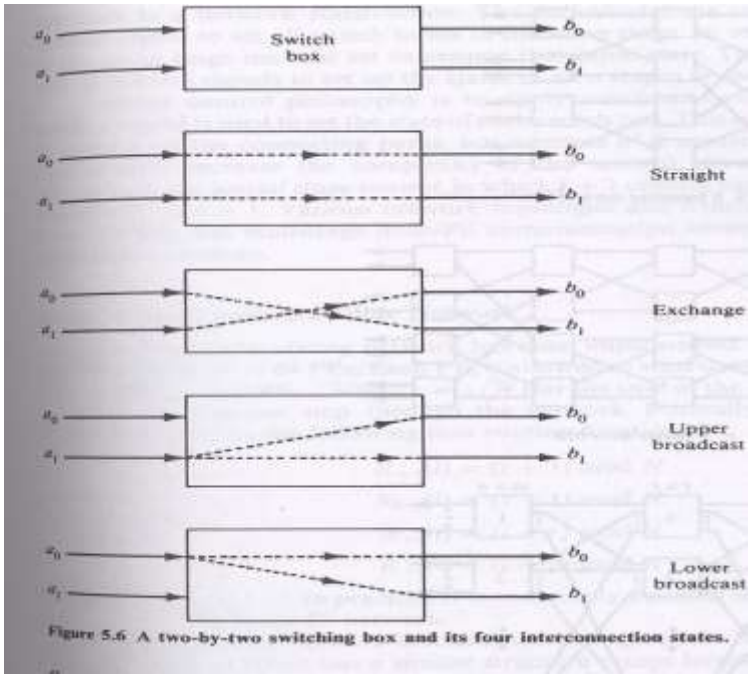


Figure 5.6 A two-by-two switching box and its four interconnection states.

- A multistage n/w is capable of connecting an arbitrary i/p terminal to an arbitrary o/p terminal.
- Multistage n/w can be **1 sided or 2 sided**.

  1 sided n/w, called *full switches* have i/p-o/p ports on the same side.

  2 sided multistage n/w usually have an i/p side and an o/p side, can be divided into 3 classes:

  Blocking, rearrangeable and nonblocking.

In blocking n/ws , simultaneous connections of more than one terminal pair may result in conflicts in the use of n/w communication links.
Eg : data manipulator, omega, flip, n cube and baseline.

Rearrangeable: if it can perform all possible connections between i/ps and o/ps by rearranging its existing connections so that a connection path for a new i/p-o/p pair can always be established.
eg Benes n/w

N/w which can handle all possible connections without blocking is called a **nonblocking n/w.**

- **Control structure** of a network determines how the states of the switch boxes will be set.

  -----2 types

  Individual stage control uses the same control signal to set all switch boxes in the same stage.

  Individual box control a separate control signal is used to set the state of each switch box.

Mesh-connected Illiac n/w

- Single stage recirculating n/w is implemented in Illiac-IV array processor with N=64 PEs.

- Each PEi is allowed to send data to any one of PE i+1, PEi-1, PEi+r, and PEi-r where r = √N in one circulation step through the n/w.

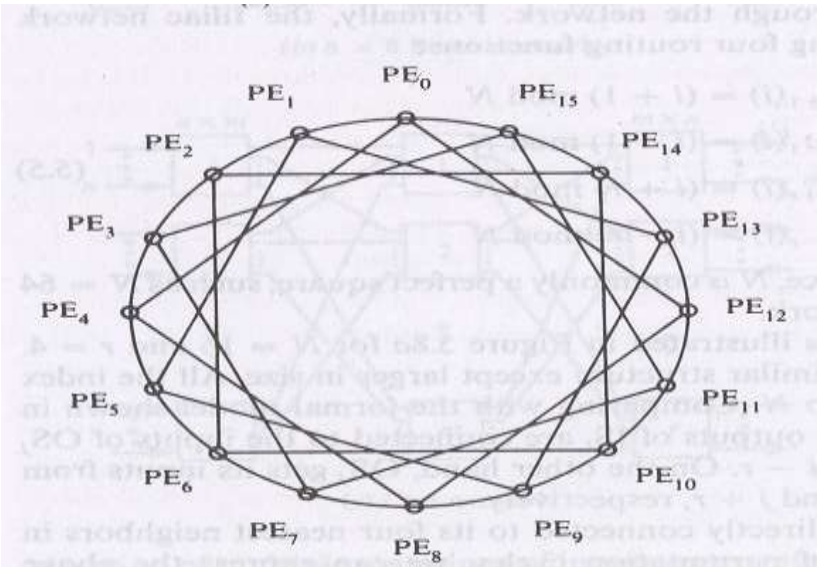
Illiac n/w is characterized by the following 4 routing functions:

$$R+1(i) = (i+1) \bmod N$$
$$R-1(i) = (i-1) \bmod N$$
$$R+r(i) = (i+r) \bmod N$$
$$R-r(i) = (i-r) \bmod N$$

Where 0<=i<=N-1. N is commonly a perfect square.

The o/ps of ISi are connected to the i/ps of OSj for j=i+1, i-1, i+r, i-r. On the other hand, OSj gets i/ps from ISi for i=j-1, j+1, j-r and j+r.

Each PEi is directly connected to its 4 nearest neighbours in the mesh n/w.

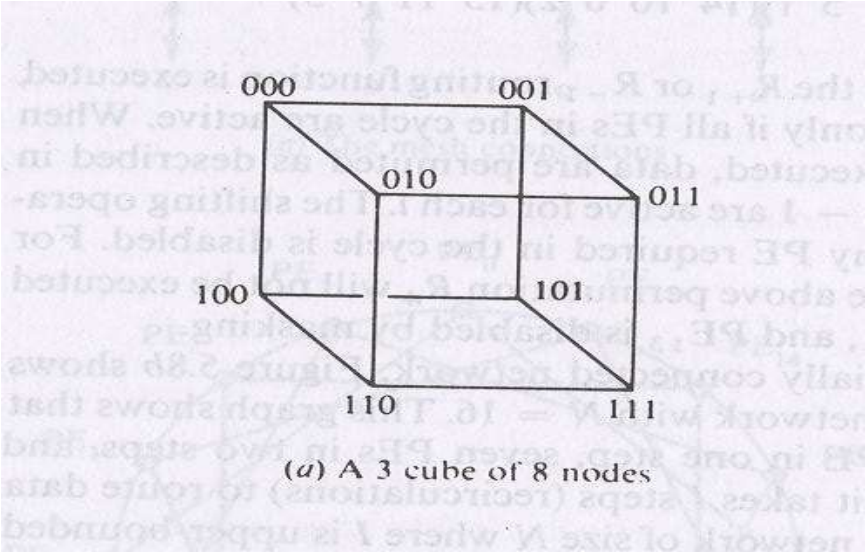


(*b*) The mesh redrawn

Cube interconnection n/ws

The cube can be implemented either as a recirculating n/w or as a multistage n/w for SIMD machines.

A 3D cube



(*a*) A 3 cube of 8 nodes

- Vertical lines connect vertices (PEs) whose address differs in the *most significant bit position*. Vertices at both ends of the diagonal lines differ in the middle bit position.

- Horizontal lines differ in the *least significant bit position*. This unit cube concept can be extended to an n dimensional unit space called an n cube with n bits per vertex.

- A cube n/w for a SIMD m/c with N PEs corresponds to an n cube where n=log2 N.

Barrel shifter and data manipulator

Barrel shifters are also known as plus-minus-2i (PM2I) networks.

This type of n/w is based on following routing functions:

$B+i(j) = (j+2i) \pmod N$
$B-i(j) = (j-2i) \pmod N$

Where $0<=j<=N-1$, $0<=i<=n-1$ and $n=\log_2 N$

The following equivalence is revealed when $r=\sqrt{N} = 2n/2$:

$B+0 = R+1$
$B-0 = R-1$
$B+n/2 = R+r$
$B-n/2 = R-r$

This implies Illiac routing functions are a subset of the barrel shifting functions. In addition to adjacent +-1 and fixed distance +-r shiftings, the barrel shifting functions allow either forward or backward shifting of distances which are the integer power of two, ie +-1, +-2,+-4,…+-2n/2,..,..,..+-2n-1.

Each PE in a barrel shifter is directly connected to 2(n-1)PEs.

- Connectivity in a barrel shifter is increased from Illiac n/w by having (2n-5). 2n-1 more links.

- Illiac n/w has 32 direct links and the same size barrel shifter has 56 links. The two n/ws are identical only when the size is reduced to be no greater than n=2 or N=5.

- The barrel shifter can be implemented as either recirculating single-stage n/w or as a multistage n/w.
- Interconnection patterns in a recirculating barrel shifter for N=8 is given as:

- The barrel shifting functions B+-0, B+-1 and B+-2 are executed by the interconnection patterns shown.
- For a single case barrel shifter of size N=2n, the minimum no. of recirculations B is upper bounded by

$$B <= \frac{\log 2N}{2}$$

- A barrel shifter has been implemented with multiple stages in the form of a data manipulator.

- The data manipulator consists of n stages of N cells is given

- Each cell is essentially a controlled shifter. This n/w is designed for implementing manipulating functions such as permuting, replicating, spacing, masking, and complementing.

- To implement a data manipulating function, proper control lines of the 6 groups (u12i, u22i, h12i, h22i, d12i, d22i) in each column must be properly set through the use of the control register and the associated decoder.

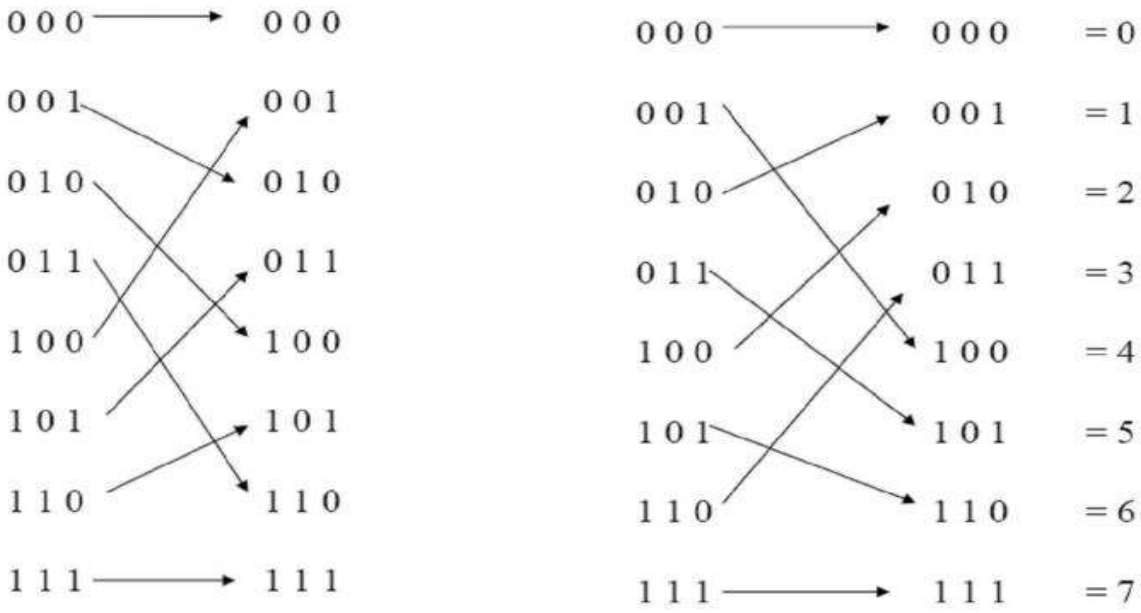
Shuffle Exchange and Omega networks

- The class of shuffle-exchange networks is based on 2 routing functions shuffle (S) and exchange (E). Let A = an-1…a1a0 be a PE address.

    - S(an-1…a1a0) = an-2…a1a0an-1
    - Where 0<=A<=N-1 and n=log2N.

- The cyclic shifting of the bits in A to the left for one bit position is performed by the S function. This action corresponds to perfectly shuffling a deck of N cards.

- The perfect shuffle cuts the deck into 2 halves from the center and intermixes them evenly.
- The inverse perfect shuffle does the opposite to restore the original ordering.



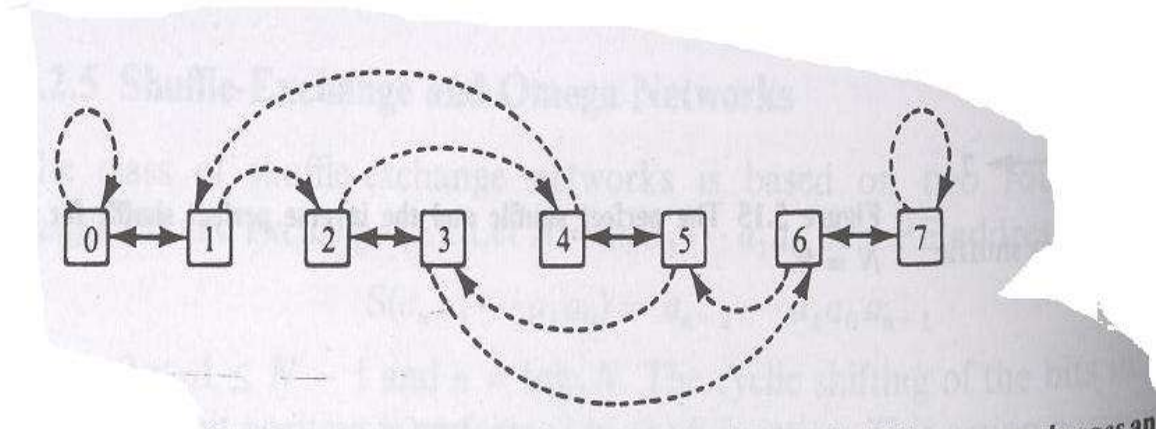
Perfect Shuffle

Inverse perfect shuffle

ure 16.13 (a) Perfect Shuffle and Inverse Perfect Shuffle for n = 8

- These shuffle exchange functions can be implemented as either a recirculating n/w or a multistage n/w.

For N=8, a single stage recirculating shuffle –exchange n/w is shown as:



Shuffle-exchange recirculating network for $N = 8$. (Solid lines are *exchanges* an are *shuffle*.)

- The use of recirculating shuffle-exchange n/w for parallel processing was proposed by Stone.

- A no. of parallel algorithms can be effectively implemented with the use of shuffle and exchange functions. The eg. include fast Fourier transform (FFT), polynomial evaluation, sorting, matrix transposition etc.

The shuffle exchange functions have been implemented with the multistage **Omega n/w** by Lawrie.

Omega n/w for N=8.

- An n X n Omega n/w consists of n identical stages.
- Between 2 adjacent stages is a perfect shuffle interconnection.
- Each stages has N/2 switch boxes under independent box control.
- Each box has 4 functions.
- The switch boxes can be repositioned.

The ncube network has the same interconnection topology as the repositioned Omega. The 2 n/w differ in 2 aspects.

1. The cube n/w uses 2 function switch boxes, whereas the Omega n/w uses 4 function switch boxes.
2. The data flow directions in the 2 n/ws are opposite to each other.