1.6 INDIAN CONTRIBUTIONS TO PARALLEL PROCESSING

India has made significant strides in developing high-performance parallel computers .Many Indians feel that the presence of these systems has helped create a high-performance computing culture in India, and has brought down the cost of equivalent international machines in the Indian marketplace. However, questions remain about the cost-effectiveness of the government funding for these systems, and about their commercial viability.

India's government decided to support the development of indigenous parallel processing technology. In August 1988 it set up the Centre for Development of Advanced Computing (C-DAC).

The C-DAC's First Mission was to deliver a 1 -Gflop parallel supercomputer by 1991. Simultaneously, the Bhabha Atomic Research Centre (BARC), the Advanced Numerical Research & Analysis Group (Anurag) of the Defence Research and Development Organization, the National Aerospace Laboratory WAL) of the Council of Scientific and Industrial Research, and the Centre for Development of Telematics (C-DOT) initiated complementary projects to develop high-performance parallel computers. Delivery of India's first-generation parallel computers started in 1991.

1. Param

The C-DAC's computers are named Param (parallel machine), which means "supreme" in Sanskrit. The first Param systems, called the 8000 series, used Innios 800 and 805 Transputers as computing nodes. Although the theoretical peak-performance of a 256-node Param was 1 Gflop (a single node T805 performs at 4.25 Mflops), its sustained performance in an actual application turned out to be between 100 and 200 Mflops. The C-DAC named the programming environment Pavas, after the mythical stone that can turn iron into gold by mere touch.

Early in 1992, the C-DAC realized that the Param 8000's basic compute node was underpowered, so it integrated Intel's i860 chip into the Param architecture. The objective

Was to preserve the same application programming environment and provide straightforward hardware upgrades by just replacing the Param 8000's compute- node boards. This resulted in the Param 8600, architecture with the i860 as a main processor and four Transputers as communication processors, each with four built-in links. The CDAC extended Paras to the Param 8600 to give a user view identical to that of the Param 8000. Param 8000 applications could easily port to the new machine.

The C-DAC claimed that the sustained performance of the 16-node Param 8600 ranged from 100 to 200 Mflops, depending on the application. Both the C-DAC and the Indian government considered that the First Mission was accomplished and embarked on the Second Mission, to deliver a teraflops range parallel system capable of addressing grand challenge problems. This machine, the Param 9000, was announced in 1994 and exhibited at Supercomputing '94. The C-DAC plans to scale it to teraflops- level performance.

The Param 9000's multistage interconnect network uses a packet-switching wormhole router as the basic switching element. Each switch can establish 32 simultaneous non-blocking connections to provide a sustainable bandwidth of 320 Mbytes per second. The communication links conform to the IEEE P13 55 standards for point-to-point links. The Param 9000 architecture emphasizes flexibility. The C-DAC hopes that, as new technologies in processors, memory, and communication links become available, those elements can be upgraded in the field. The first system is the Param 9000/SS, which is based on SuperSparc processors. A complete node is a 75-MHz SuperSparc I1 processor with 1 Mbyte of external cache, 16 to 12 8 Mbytes of memory, one to four communication links, and related I/O devices. When new MBus modules with higher frequencies become available, the computers can be field-upgraded. Users can integrate Sparc workstations into the Param 9000/SS by adding a Sbus-based network interface card. Each card supports one, two, or four communication links. The C-DAC also provides the necessary software drivers.

2. Anupam

The BARC, founded by Homi Bhabha and located in Bombay, is India's major centre for nuclear science and is at the forefront of India's Atomic Energy Program. Through 1991 and

1992, BARC computer facility members started interacting with the C-DAC to develop a high-performance computing facility. The BARC estimated that it needed a machine of 200 Mflops sustained computing power to solve its problems. Because of the importance of the BARC's program, it decided to build its own parallel computer. In 1992, the BARC developed the Anupam (Sanskrit for "unparalleled") computer, based on the standard Multibus I1 i860 hardware. Initially, it announced an eight-node machine, which it expanded to 16, 24, and 32 nodes. Subsequently, the BARC transferred Anupam to the Electronics Corporation of India, which manufactures electronic systems under the umbrella of India's Department of Atomic Energy.

System Architecture

Anupam has a multiple-instruction, multiple- data (MIMD) architecture realized through off-the-shelf Multibus I1 i860 cards and crates. Each node is a 64-bit i860 processor with a 64-Kbyte cache and a local memory of 16 to 64 Mbytes. A node's peak computing power is 100 Mflops, although the sustained power is much less. The first version of the machine had eight nodes in a single cluster (or Multibus I1 crate). There is no need for a separate host. Anupam scales to 64 nodes. The inter cluster message-passing bus is a 32-bit Multibus II backplane bus operating at 40 Mbytes peak. Eight nodes in a cluster share this bus. Communication between clusters travels through two 16-bit-wide SCSI buses that form a 2D mesh. Standard topologies such as a mesh, ring, or hypercube can easily map to the mesh.

3. Pace

Anurag, located in Hyderabad, focuses on R&D in parallel computing; VLSIs; and applications of high-performance computing in computational fluid dynamics, medical imaging, and other areas. Anurag has developed the Process- SOT for Aerodynamic Computations and Evaluation, a loosely-coupled, message passing parallel processing system. The PACE program began in August 1988. The initial prototypes used the 16.67-MHz Motorola MC 68020 processor. The first prototype had four nodes and used a VME bus for communication. The VME backplane works well with Motorola processors and provided the necessary bandwidth and operational flexibility. Later, Anurag developed an eight-node prototype

based on the 2s-MHz MC 68030. This cluster forms the backbone of the PACE architecture. The 128-node prototype is based on the 33-MHz MC 68030. To enhance the floating-point speed, Anurag has developed a floating-point processor, Anuco. The processor board has been specially designed to accommodate the MC 68881, MC 68882, or the Anuco floating-point accelerators. PACE+, the latest version, uses a 66- MHz HyperSparc node. The memory per node can expand to 256 MBytes.

4. Flosolver

In 1986, the NAL, located in Bangalore, started a project to design, develop, and fabricate suitable parallel processing systems to solve fluid dynamics and aerodynamics problems. The project was motivated by the need for a powerful computer in the laboratory and was influenced by similar international developments Flosolver, the NAL's parallel computer, was the first operational Indian parallel computer. Since then, the NAL has built a series of updated versions, including Flosolver Mkl and MklA, four-processor systems based on 16-bit Intel 8086 and 8087 processors, Flosolver MklB, an eight-processor system, Flosolver Mk2, based on Intel's 32-bit 80386 and 80387 processors, and the latest version, Flosolver Mk3, based on Intel's 1860 RISC processor.

5. Chipps

The Indian government launched the CDOT to develop indigenous digital switching technology. The C-DOT, located in Bangalore, completed its First Mission in 1989 by delivering technologies for rural exchanges and secondary switching areas. In February 1988, the C-DOT signed a contract with the Department of Science and Technology to design and build a 640-Mflop, 1,000- MIPS-peak parallel computer. The CDOT set a target of 200 Mflops for sustained performance.

System Architecture

C-DOTS High Performance Parallel Processing System (Chipps) is based on the single-algorithm, multiple-data architecture. Such architecture provides coarse-grain parallelism with barrier synchronization, and uniform start up and simultaneous data distribution across all configurations. It also employs off-the-shelf hardware and software. Chipps supports

large, medium, and small applications. The system has three versions: a 192-node, a 64-node, and a 16-node machine.

In terms of performance and software support, the Indian high-performance computers hardly compare to the best commercial machines. For example, the C-DAC's 16-node Param 9000/SS has a peak performance of 0.96 Gflops, whereas Silicon Graphics' 16-processor Power Challenge has a peak performance of 5.96 Gflops, and IBM's 16- processor Para2 model 590 has a peak performance of 4.22 Gflops. However, the C-DAC hopes that a future Param based on DEC Alpha processors will match such performance.