Master Slave Flip Flop

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Master Slave flip flop are the cascaded combination of two flip-flops among which the first is designated as master flip-flop while the next is called slave flip-flop (Figure 1). Here the master flip-flop is triggered by the external clock pulse train while the slave is activated at its inversion i.e. if the master is positive edge-triggered, then the slave is negative-edge triggered and vice-versa. This means that the data enters into the flip-flop at leading/trailing edge of the clock pulse while it is obtained at the output pins during trailing/leading edge of the clock pulse. Hence master-slave flip-flop completes its operation only after the appearance of one l...

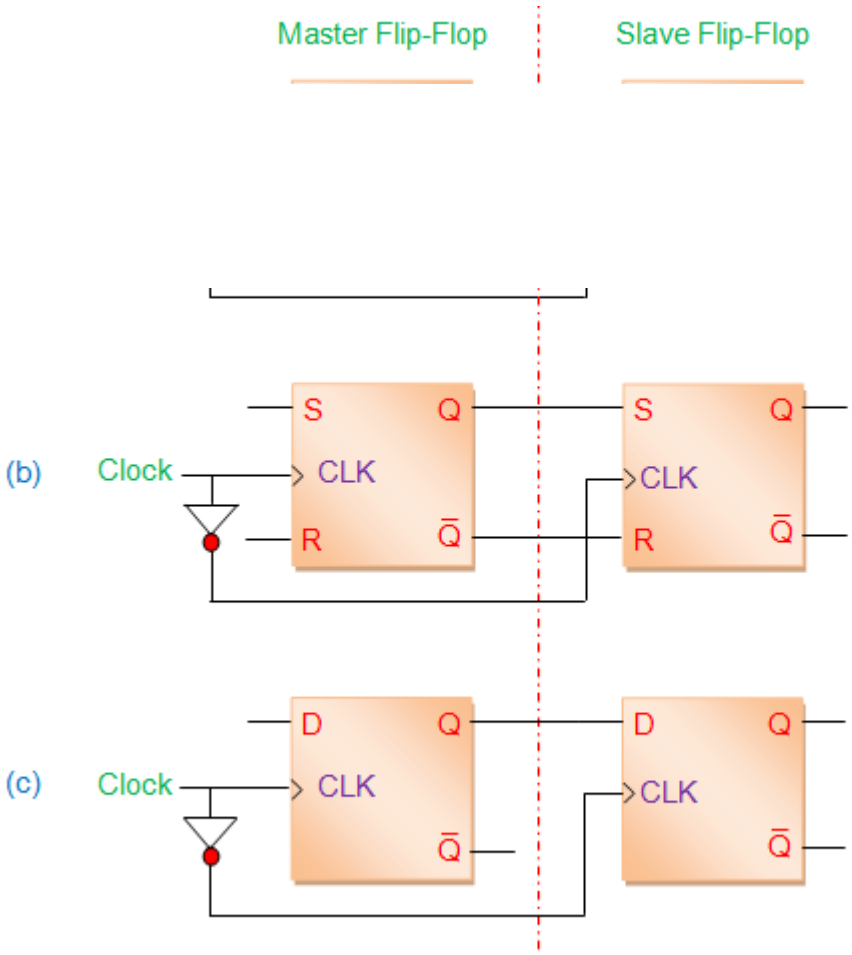

Figure 1 (a) Master-Slave JK flip-flop (b) Master-Slave SR flip-flop (c) Master-Slave D flip-flop

The internal structure of a master-slave JK flip-flop interms of NAND gates and an inverter (to complement the clock signal) is shown in Figure 2. Here it is seen that the NAND gate 1 (N_1) has three inputs viz., external clock pulse (Clock), input J and output $\bar{Q}$; while the NAND gate 2 (N_2) has external clock pulse (Clock), input K and output Q as its inputs.

Further the outputs of N_1 and N_2 gates are connected as the inputs for the criss-cross connected gates N_3 and N_4. These four gates together (N_1, N_2, N_3 and N_4) f the master-part of the flip-flop while a similar arrangement of the other four gates

N_5, N_6, N_7 and N_8 form the slave-part of it.

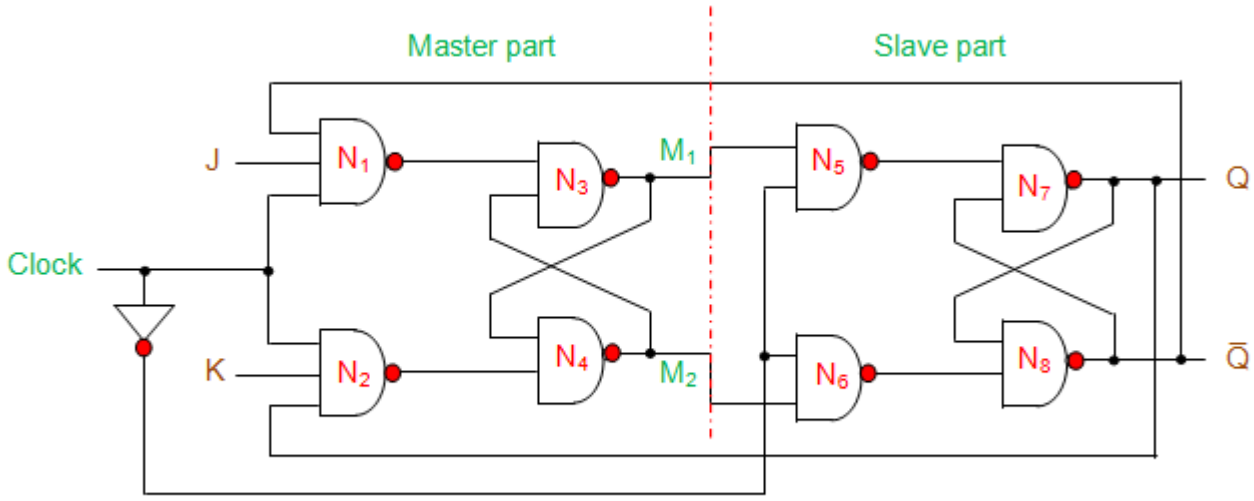

Figure 2 Master-Slave JK flip-flop realized using NAND gates and an inverter

From figure it is also evident that the slave is driven by the outputs of the master (M_1 and M_2), which is in accordance with its name **master-slave flip-flop**. Further the master is active during the positive edge of the clock due to which M_1 and M_2 change their states; depending on the values of J and K. However at this instant the outputs of the overall system (master-slave JK flip-flop) remains unchanged as the slave will be inactive due to positive-edge of the clock pulse. Similar to this, the slave decides on its outputs Q and $\bar{Q}$ depending on its inputs M_1 and M_2, during the negative edge of the clock during which the master will be inactive.

The truth table corresponding to the working of the flip-flop shown in Figure 2 is

(data enclosed in red boxes) appear during the positive-edge of the clock (red arrow). However at this instant the slave-outputs remain latched or unchanged. The same data is transferred to the output pins of the master-slave flip-flop (data enclosed in blue boxes) by the slave during the negative edge of the clock pulse (blue arrow). The same principle is further emphasized in the timing diagram of **master-slave flip-flop** shown by Figure 3. Here the green arrows are used to indicate that the slave-output is nothing but the master-output delayed by half-a-clock cycle.

Moreover it is to be noted that the working of any other type of master-slave flip-flop is analogous to that of the master slave JK flip-flop explained here.

Truth Table

Trigger	Inputs		Output						Inference
			Present State		Intermediate		Next State		
CLK	J	K	Q	$\bar{Q}$	M_1	M_2	Q	$\bar{Q}$	
↑	0	0	0	1	0	1	Latched		No Change
↓			0	1	Latched		0	1	
↑			1	0	1	0	Latched		
↓			1	0	Latched		1	0	
↑	0	1	0	1	0	1	Latched		Reset
↓			0	1	Latched		0	1	
↑			1	0	0	1	Latched		
↓			1	0	Latched		0	1	
↑	1	0	0	1	1	0	Latched		Set
↓			0	1	Latched		1	0	
↑			1	0	1	0	Latched		
↓			1	0	Latched		1	0	
↑	1	1	0	1	1	0	Latched		Toggles
↓			0	1	Latched		1	0	
↑			1	0	0	1	Latched		
↓			1	0	Latched		0	1	

Table I Truth table for master-slave JK flip-flop

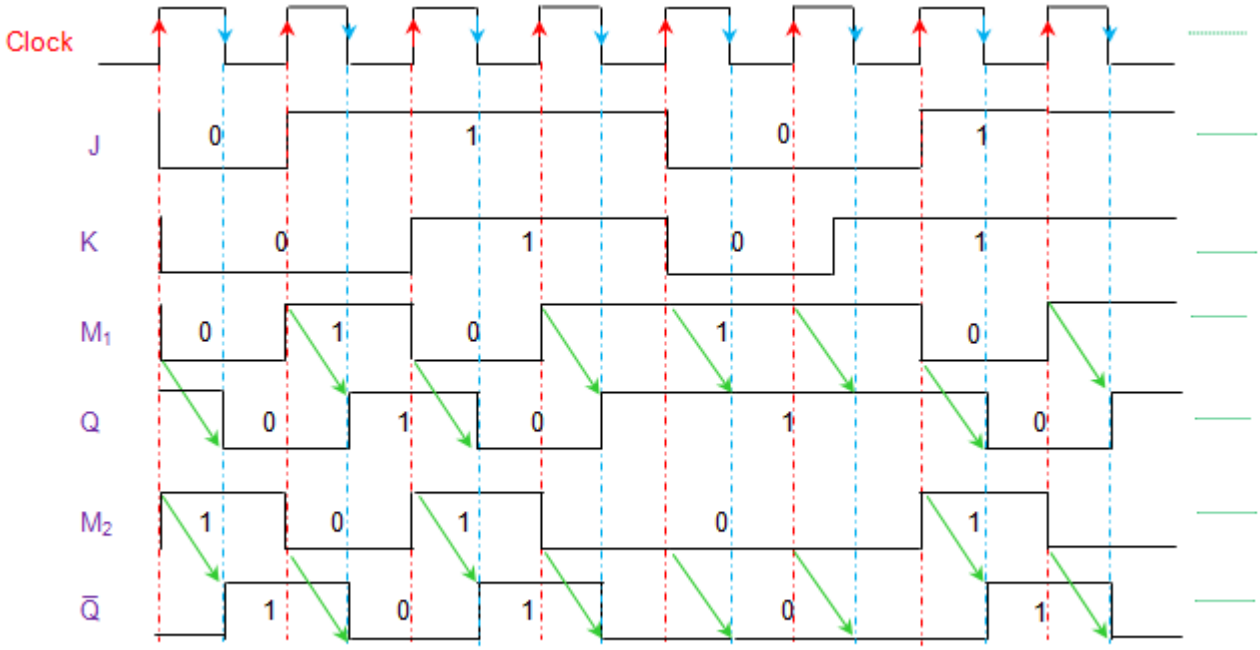

Figure 3 Timing diagram for master-slave JK flip-flop

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