

Logic Families

4.1 INTRODUCTION

Logic gates and memory devices are fabricated as *integrated circuits* (ICs) because the components used such as resistors, diodes, bipolar junction transistors and the insulated gate or metal-oxide semiconductor field-effect transistors are the integral parts of the chip. The various components are interconnected within the chip to form an electronic circuit during assembly. The ICs result in an increase in reliability and a reduction in weight and size.

Small Scale Integration (SSI) refers to ICs with fewer than 10 gates on the same chip. Medium Scale Integration (MSI) includes 12 to 100 gates per chip. Large Scale Integration (LSI) refers to more than 100 upto 5000 gates per chip. Very Large Scale Integration (VLSI) devices contain several thousand gates per chip.

Integrated circuits are classified into two general categories: (i) *Linear* and (ii) *Digital*. Linear integrated circuits operate with continuous signals and are used to construct electronic circuits such as amplifiers, voltage comparators, etc. Digital integrated circuits operate with binary signals and are invariably constructed with integrated circuits.

4.2 DIGITAL INTEGRATED CIRCUITS

The various logic families can be placed into two broad categories according to the IC fabrication process: (i) Bipolar and (ii) Metal-oxide semiconductor (MOS).

ICs come in the following types of packages:

- (i) Dual-in-Line Package (DIP)
- (ii) Leadless Chip Carrier (LCC)
- (iii) Plastic Leaded Chip Carrier (PLCC)
- (iv) Plastic Quad Flat Pack (PQFP) and
- (v) Pin Grid Array (PGA)

4.2.1 Bipolar Logic Families

The important elements of a bipolar IC are resistors, transistors and diodes (varactor diodes used as capacitors). Based on the two main operations of bipolar ICs, i.e., saturated and non-saturated, bipolar families are classified into

- (i) saturated logic and
- (ii) non-saturated logic.

The following are the saturated bipolar logic families:

1. Resistor–Transistor Logic (RTL)
2. Direct-coupled Transistor Logic (DCTL)
3. Diode–Transistor Logic (DTL)
4. High Threshold Logic (HTL)
5. Transistor–Transistor Logic (TTL)
6. Integrated-injection Logic (I^2L)

The following are the non-saturated logic families:

1. Schottky TTL
2. Emitter-coupled Logic (ECL)

4.2.2 MOS Families

The MOS families include

1. PMOS p -channel MOSFETs
2. NMOS n -channel MOSFETs
3. CMOS Complementary MOSFETs

4.3 CHARACTERISTICS OF DIGITAL ICs

Some of the important parameters or properties of various logic families are listed as follows:

1. Speed of operation (Propagation delays)
2. Power dissipation
3. Fan-in
4. Fan-out
5. Noise immunity
6. Operating temperature
7. Power supply requirements

The comparison of performance of digital ICs may be made with reference to the above properties.

4.3.1 Speed of Operation

The speed of operation of an IC is expressed in terms of propagation delay. *Propagation delay* is defined as the time taken for the output of a gate to change after the inputs have changed.

A logic signal always experiences a delay in going through a circuit. The two propagation delay times shown in Fig. 4.1 are defined as follows:

t_{PLH} : It is the propagation delay time in going from logical LOW (0 state) to logical HIGH (1 state).

t_{PHL} : It is the propagation delay time in going from logical HIGH (1 state) to logical LOW (0 state).

It is evident that t_{PHL} is the delay in the *output* response as it goes from LOW state to a HIGH state, and vice versa for t_{PLH} . The delay times are measured between the 50% voltage levels of the input and output waveforms. In general, the two delays t_{PHL} and t_{PLH} are not necessarily equal and will vary depending on load conditions. The values of propagation times are a measure of the relative speed of logic circuits. The average of the above two propagation delays $(t_{PLH} + t_{PHL})/2$ is called the *average propagation delay* and is used to rate the circuit. It is a function of the switching time of the individual transistors or MOSFETs in the circuit.

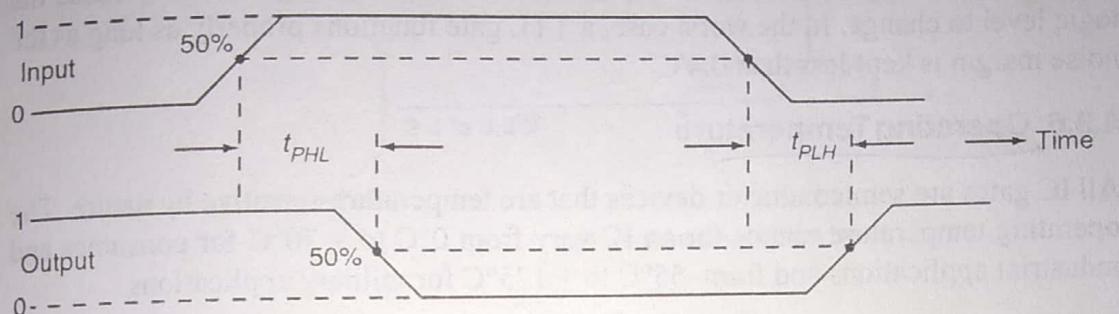


Fig. 4.1 Propagation delays

4.3.2 Power Dissipation

Power dissipation is a measure of the power consumed by the logic gate when fully driven by all its inputs, and it is expressed in milliwatts or nanowatts. The d.c. or average power dissipation is the product of d.c. supply voltage and the mean current taken from that supply.

4.3.3 Fan-in

The fan-in of a gate is the number of inputs connected to the gate without any degradation in the voltage levels. For example, an eight-input gate requires one Unit Load (UL) per input. Its fan-in is 8. This parameter determines the functional capabilities of a logic circuit.

4.3.4 Fan-out

Fan-out is the maximum number of similar logic gates that a gate can drive without any degradation in voltage levels. Very often a gate will drive several other gates. Each driven gate requires a certain current which must be supplied by the driving gate. The driving gate must be capable of supplying this current while maintaining the required voltage level. In part, this is a function of the output impedance of the driving gate and the input impedance of the driven gates. Usually, in a given logic family, gates drive others of the same type. If their output impedance is low while their input impedance is high, then one gate can often drive many others.

4.3.5 Noise Immunity or Noise Margin

The term noise denotes an unwanted signal voltage, e.g., hum, transients and glitches.

Noise can sometimes cause the input voltage of a logic gate to drop below V_{IH} (min) or rise above V_{IL} (max), which leads to unreliable operation. *Noise immunity* is the maximum noise voltage that may appear at the input of a logic gate without changing the logical state of its output. A quantitative measure of noise immunity is called *noise margin*.

The difference between the operating input-logic voltage level and the threshold voltage is called the noise margin of the circuit. The manufacturer usually quotes the noise margin, which refers to the amplitude of the noise voltage that may cause the logic level to change. In the worst case, a TTL gate functions properly as long as the noise margin is kept less than 0.4V.

4.3.6 Operating Temperature

All IC gates are semiconductor devices that are temperature-sensitive by nature. The operating temperature ranges for an IC vary from 0°C to + 70°C for consumer and industrial applications and from -55°C to + 125°C for military applications.

4.3.7 Power Supply Requirements

The amount of power and supply voltage required by an IC are the main parameters to be taken into consideration while choosing a proper power supply.

4.3.8 Current and Voltage Parameters

The following currents and voltages are very important in designing digital systems. The values given below are for TTL gates only.

High-level input voltage (V_{IH}) [$V_{in(1)}$] It is the minimum voltage level required for a logical 1 at an input. Its minimum value is 2V.

Low-level input voltage (V_{IL}) [$V_{in(0)}$] It is the maximum input voltage required for a logical 0 (LOW) at an input. Its maximum value is 0.8V.

High-level output voltage (V_{OH}) [$V_{out(1)}$] It is the minimum voltage required for a logical 1 state at the output. Its minimum value is 2.4V.

Low-level output voltage (V_{OL}) [$V_{out(0)}$] It is the maximum voltage available at the circuit's output corresponding to the logical 0 state. Its maximum value is 0.4V.

High-level input current (I_{IH}) [$I_{in(1)}$] The current that flows through an input when a specified high-level voltage is applied to that input.

Low-level input current (I_{IL}) [$I_{in(0)}$] The current that flows through an input when a specified low-level voltage is applied to that input.

High-level output current (I_{OH}) [$I_{out(1)}$] The current that flows from an output in the logical 1 state under specified load conditions.

Low-level output current (I_{OL}) [$I_{out(0)}$] The current that flows from an output in the logical 0 state under specified load conditions.

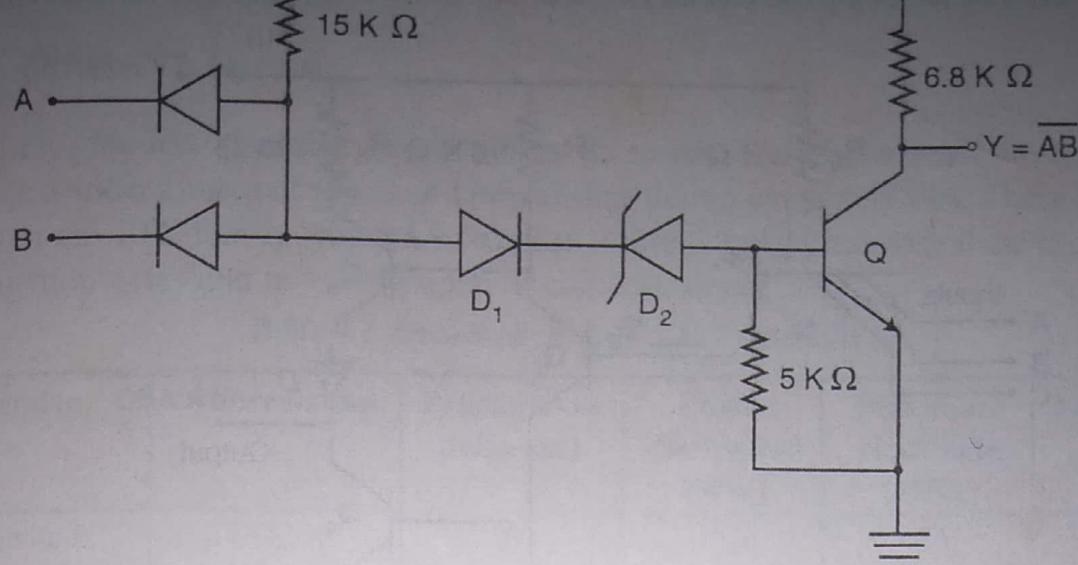


Fig. 4.5(b) Basic TTL NAND gate

4.9 TRANSISTOR-TRANSISTOR LOGIC (TTL or T²L)

The most commonly used saturating logic family called the Transistor-Transistor Logic, (TTL or T²L), has the fastest switching speed when compared to other logic families that utilize saturated transistors. The series 54/74 TTL family has grown and evolved into five major divisions:

- (i) standard (SN 54/74)
- (ii) high-speed (SN54H/74H)
- (iii) low-power (SN54L/74L)
- (iv) schottky-diode-clamped (SN54S/74S)
- (v) low power schottky. (SN54LS/74LS)

Although the high-speed and low-power series were designed for specific applications, all four families are compatible and are capable of interfacing directly with one another.

They have the following typical characteristics in common:

- (i) Supply voltage : 5.0V
- (ii) Logical 0 output voltage : 0V to 0.4V
- (iii) Logical 1 output voltage : 2.4V to 5V
- (iv) Logical 0 input voltage : 0V to 0.8V
- (v) Logical 1 input voltage : 2V to 5V
- (vi) Noise immunity : 0.4V

4.9.1 TTL NAND Gate

The basic circuit for the TTL logic family is the NAND gate. The TTL circuit uses a special single multi-emitter transistor that is fabricated with several emitters at its input. The number of emitters used depends on the desired fan-in of the circuit. Since

a multi-emitter transistor is smaller in area than the diodes it replaces, the yield from a wafer is increased. Moreover, smaller area results in lower capacitance to the substrate, thereby reducing the circuit rise and fall times and hence increasing its speed.

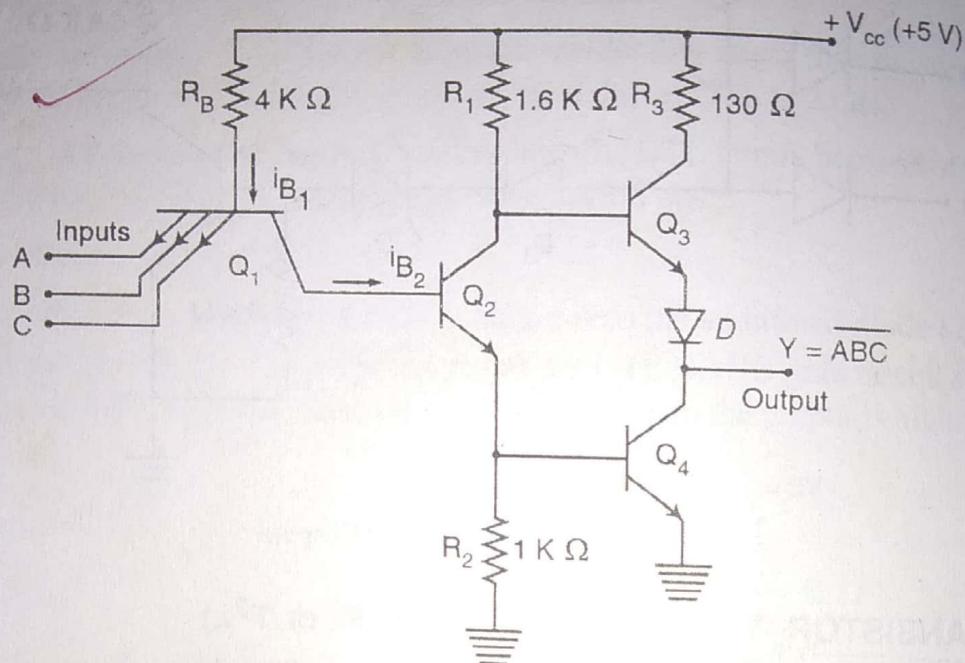


Fig. 4.6 3-input TTL NAND gate

Circuit operation The basic circuit of the TTL NAND gate is shown in Fig. 4.6. The output is taken from the collector of transistor Q_4 . Each emitter of Q_1 acts like a diode. Therefore, transistor Q_1 and the $4\text{k}\Omega$ resistor act like a 3-input AND gate and the rest of the circuit inverts the signal. Hence, the overall circuit acts like a 3-input NAND gate.

When either or all inputs (A , B and C) are at 0V (logic 0), the corresponding emitter-base junction of Q_1 becomes forward-biased. The value of R_B is selected so as to ensure that Q_1 is turned ON. However, the value of current i_{B_2} flowing through the base of Q_2 reduces the potential at the base of Q_2 , and hence transistors Q_2 and Q_4 are cutoff so that the output voltage is at V_{cc} (logic 1).

If all the inputs are high (logic 1), the emitter-base junction of Q_1 is reverse-biased so that it has no base current. Hence, Q_1 is OFF. However, its collector-base junction is forward-biased supplying base current i_{B_2} to Q_2 . The current i_{B_2} will be sufficiently large to saturate Q_2 . As a result, transistor Q_2 is turned ON and the drop across R_2 is sufficient to forward bias the base-emitter junction of Q_4 , thereby turning Q_4 ON. Hence, the output at its collector is low (logic 0). The function of diode D is to prevent both Q_3 and Q_4 from being ON simultaneously.

In the absence of diode D , the transistor Q_3 will conduct slightly when the output is LOW. In order to prevent this, the diode is connected between the emitter of Q_3 and the collector of Q_4 . The voltage drop across the diode keeps the base-emitter junction of Q_3 reverse-biased. In this way, transistor Q_4 only conducts when the output is LOW, which confirms the conditions for NAND operation.

As TTL input circuits require higher drive currents than DTL, they are designed to have high power output stages. The open collector gates are used in three major applications: driving a lamp and relay, performing a wired logic and for the construction of common bus system.

Also, the circuit is

Tri-state output A very popular output connection that incorporates the benefits of totem-pole and open-collector in the single circuit is the tri-state output connection.

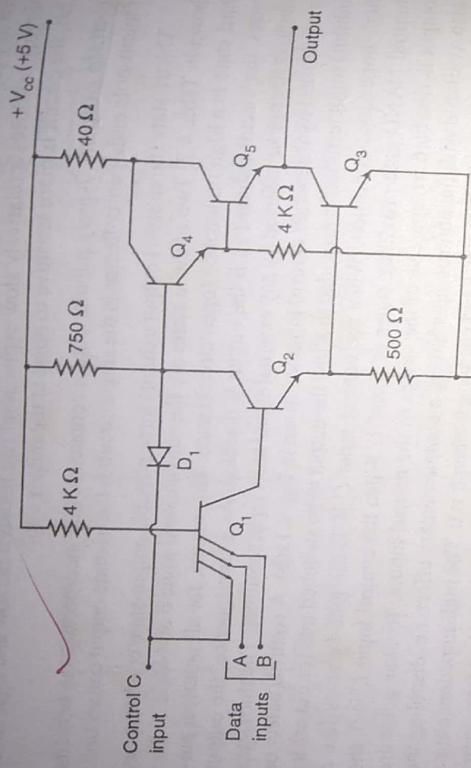
The tri-state (three state) output exhibits three possible output-state conditions as shown in Table 4.2. Two of these states are the conventional logic 0 and logic 1. The third state is a high impedance (open circuit) state. This means, for all practical purposes, the circuit behaves as if the output is disabled. As a consequence, the output cannot affect or be affected by any external signal at its input terminals. The third state is controlled by a separate control input as shown in Fig. 4.11(b). A control (Select or Inhibit) input terminal is provided to allow the output to be switched into (or out of) its high impedance condition. When the control input C is 1, the gate behaves like a normal NAND gate providing states of 0 and 1. When the control input C is 0, the output is disabled irrespective of the values of the normal inputs. Tri-state gates are also available with the control input having a complementary effect, i.e. disabling the gate when the control input is 1 and enabling it when it is 0. The high-impedance state of a tri-state gate allows the possibility of making a direct wire connection from many outputs to a common bus line, in which only one output line will be enabled while all other outputs are disabled by their respective control inputs.

Table 4.2 Truth table for tri-state TTL NAND gate

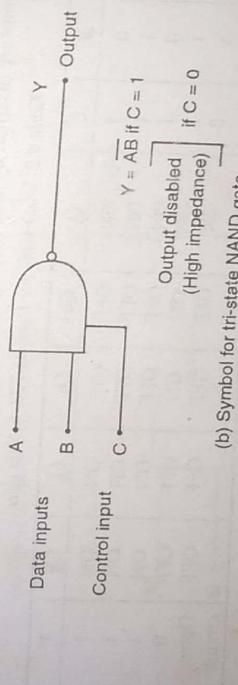
A	B	C	Q_1	Q_2	Q_3	Q_4	Q_5	Y
0	0	1	ON	OFF	OFF	ON	ON	1
0	1	1	ON	OFF	OFF	ON	ON	1
1	0	1	ON	OFF	OFF	ON	ON	1
1	1	1	OFF	ON	ON	OFF	OFF	0
X	X	0	ON	OFF	OFF	OFF	OFF	Open-circuit

Operation of tri-state TTL NAND gate Table 4.2 shows the truth table summarizing the operation of the tri-state NAND circuit of Fig. 4.11(a). When the control input C is HIGH (1) and any input A or B is LOW, Q_1 is ON and both Q_2 and Q_3 are OFF. Hence, Q_4 and Q_5 will be turned ON and the output will be at the HIGH level (nearly +3.6V). When the control input C is HIGH and both inputs A and B are HIGH, transistor Q_1 becomes OFF, and thereby drives both the transistors, Q_2 and Q_3 , ON. Hence, Q_4 and Q_5 are OFF and the output is LOW(0). Thus, when the control input C is HIGH, the circuit operates like a totem-pole output circuit. When the control input is in LOW state, then diode D_1 conducts and therefore the voltage at the base of transistor Q_4 is 0.7V which is not enough to make both the transistors, Q_4 and Q_5 , to switch to the ON state. Also, since Q_1 is conducting, the transistor Q_2 is in a cutoff state and therefore Q_3 is also OFF. So, neither the output transistor Q_5 nor Q_3 is ON and the

output is open circuited or in HIGH impedance state. Therefore, it is concluded that there are three states of the output—LOW, HIGH and Open circuit as determined by the inputs.



(a) Basic circuit of TTL NAND gate with tri-state (3-state) output



(b) Symbol for tri-state NAND gate

Fig. 4.11

4.9.4 TTL Parameters

only values to remember no derivation.
Series 54/7400 devices work reliably over a temperature range of 0 to 70°C and over a supply range of 4.75 to 5.25V.

Floating inputs When a TTL input voltage is HIGH (ideally +5V) as shown in Fig. 4.12(a), the emitter current is zero. When a TTL input is unconnected (floating) as shown in Fig. 4.12(b), there is no flow of emitter current because of the open circuit. Hence, a floating TTL input is equivalent to a high input.

Also, when an input terminal is left open, it acts like a small antenna and picks up stray electromagnetic noise voltages leading to malfunctioning or erroneous operation of the gate. Therefore, it is a must to connect the unused TTL inputs either to the

ground or to the V_{CC} , depending upon the gate. For example, in AND and NAND gates, the unused input must be connected to V_{CC} , while in OR and NOR gates the unused inputs should be connected to ground.

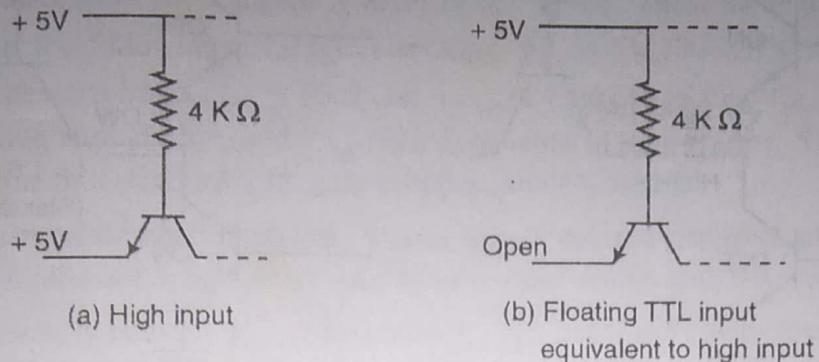


Fig. 4.12

Current sourcing and current sinking When the output of a gate is HIGH, thereby providing current to the input of the gate being driven, the output is said to act as a *current source*. For a TTL circuit, the maximum current drawn by an input from a high output is $40\mu A$.

When the output of a TTL gate goes LOW, it must be capable of sinking current drawn from gate inputs which are driven LOW. The driver then operates as a *current sink*. In a standard TTL gate, when one of its inputs is low, a current of 1.6mA flows out of the device. Thus,

$$I_{II}(\max) = -1.6\text{mA} \quad \text{and} \quad I_{IH}(\max) = +40\mu\text{A}.$$

Here, the negative sign indicates that the current flows out of the device. [Refer to Fig. 4.12(a) and (b).]

Standard loading A TTL device can source (high output) or sink current (low output). Specification sheets of standard TTL devices show that any 54/7400 series can sink upto 16 mA and is denoted by $I_{OL}(\text{max}) = 16\text{mA}$ and can source up to $400\mu\text{A}$, denoted by $I_{OH}(\text{max}) = -400\mu\text{A}$. The negative sign indicates that the conventional current is out of the device. Since the maximum output currents, i.e. $I_{OL}(\text{max})$ and $I_{OH}(\text{max})$, are 10 times larger than the input currents, i.e. $I_{IL}(\text{max})$ and $I_{IH}(\text{max})$, we can connect upto 10 TTL emitters to any TTL output.

Fan-out The maximum number of TTL loads that can be driven by a TTL driver is called fan-out. As discussed in the previous section, 10 TTL inputs can be connected to the output of a standard TTL. Thus, the fan-out of standard TTL is 10. When the totem-pole output of a TTL gate goes HIGH, it reverse-biases another gate input with the resulting current (40mA, maximum) as shown in Fig. 4.13(a). The TTL output going low must sink a current from the gate being driven, as shown in Fig. 4.13(b). The current from one standard TTL load is 1.6mA, while from an LS circuit the load current is only 0.36mA. Using the standard unit as reference, one unit load is then the same as a current of 1.6mA into a low output. Since a standard output drive is capable of sinking the current of 16mA, it can drive upto 10 loads.

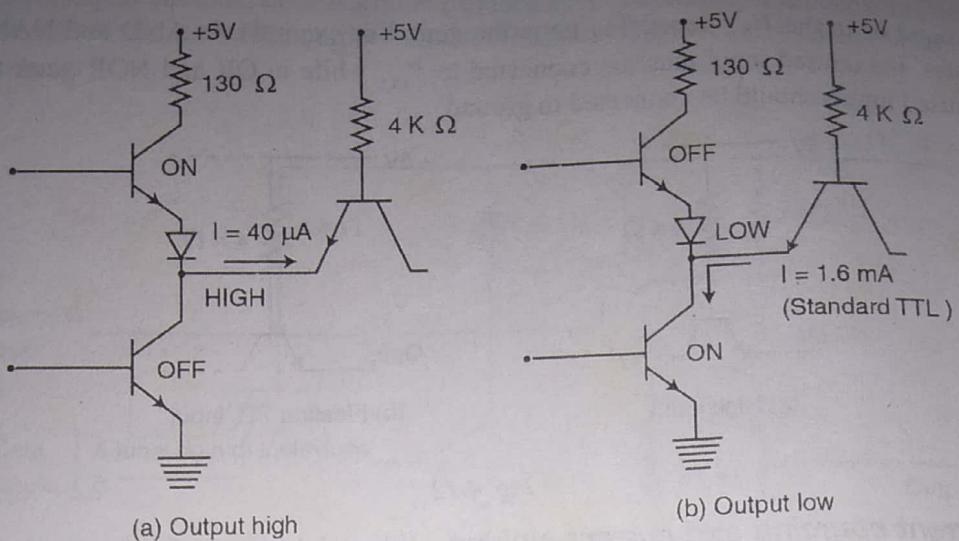


Fig. 4.13 Fan-out operation

For LOW power TTL,

$$I_{H\downarrow}(\text{max}) = -0.18 \text{ mA}; \quad I_{IH}(\text{max}) = 10 \text{ A}$$

$$I_{OL}(\text{max}) = 3.6 \text{ mA}; \quad I_{OH}(\text{max}) = -200 \text{ A}$$

Considering HIGH output state: $\frac{I_{OH\ max}}{I_{IH\ max}} = \frac{200\ mA}{10\ mA} = 20$

$$\text{Considering LOW output state : } \frac{I_{OL} \max}{I_{IL} \ max} = \frac{3.6 \text{ mA}}{0.18 \text{ mA}} = 20$$

Therefore, twenty LOW power TTL gate inputs can be connected to the output of another LOW power TTL gate.

For LOW power Schottky TTL,

$$I_{H\text{ (max)}} = -0.36 \text{ mA}; I_{IH\text{ (max)}} = 20 \text{ mA}$$

$$I_{OI}(\text{max}) = 8 \text{ mA}; I_{OH}(\text{max}) = -400 \text{ mA}$$

Therefore, for lowpower Schottky TTL,

$$\text{Fan-out} = \frac{8 \text{ mA}}{0.36 \text{ mA}} = 22 \text{ (or)} \quad \frac{400 : A}{20 : A} = 20, \text{ whichever is less.}$$

Also, a particular type of TTL gate can be connected with other types of TTL. For example, if a standard TTL is connected with a HTTL, the fan-out is 8; if it is connected with a LTTL, the fan-out is 40; if it is connected to a STTL, the fan-out is 8 and with a LS series, the fan-out is 20. The above data is summarised in Table 4.3.

Table 4.3 Fan-outs

TTL Driver	TTL load				
	74	74 H	74 L	74 S	74 LS
74	10	.8	40	8	20
74 H	12	10	50	10	25
74 L	2	1	20	1	10
74 S	12	10	100	10	50
74 LS	5	4	40	4	20

Switching speed The TTL circuit has the fastest switching speed of any saturated logic. Two switching parameters are tested on TI 54/74 TTL gates: propagation delay time t_{PHL} from a logical 1 to a logical 0 level at the output and propagation delay time t_{PLH} from a logical 0 to a logical 1 level at the output. These switching tests are performed at the following nominal conditions: $V_{CC} = 5V, T_A = 25^\circ C$ and $N = 10$. Acceptable devices have $t_{PHL} \leq 15\text{ns}$ and $t_{PLH} \leq 22\text{ns}$. Note that t_{PHL} decreases with increasing temperature, and t_{PLH} is independent of temperature. The propagation delay time of a standard TTL gate is approximately 10ns.

Supply current characteristics Power supply current requirements for all series 54/74 circuits are specified as maximum current drains with maximum permissible power-supply voltage, V_{CC} . Maximum $I_{CCL}[I_{CC}(0)]$ per gate is specified as 5.5 mA and maximum $I_{CCH}[I_{CC}(1)]$ per gate is specified as 2.0 mA. At the nominal supply voltage of 5V, typical I_{CCL} per gate is 3mA and typical I_{CCH} is 1 mA. Thus, I_{CCL} is about 3 times larger than I_{CCH} .

Worst case input and output voltages Theoretically, logic LOW state is 0V and a logic HIGH state is 5V. But, practically for TTL gates, there is a window or a range of low voltages which is still recognised as LOW state and a range of high voltages which is still recognised as HIGH state. Also, this range of LOW and HIGH state voltages is different at inputs and outputs of a TTL gate.

For a TTL gate, the worst case input voltages are:

$V_{IL, \text{max}} = 0.8\text{ V}$ (It means a voltage from 0 to 0.8V without changing the output is recognized as LOW state.)

$V_{IH, \text{min}} = 2\text{ V}$ (It means a voltage from 5V down to 2V without changing the output is recognized as HIGH state.)

A LOW voltage greater than 0.8V and a HIGH voltage lower than 2V lead to unpredictable input state. Similarly, the worst case output voltages are:

$V_{OL, \text{max}} = 0.4\text{ V}$ (It means a LOW state output having any value from 0 to 0.4V.)

$V_{OH, \text{min}} = 2.4\text{ V}$ (It means a HIGH state output having any value from 5 to 2.4V.)

Thus, as far as TTL output is concerned, a LOW voltage greater than 0.4V and a HIGH voltage less than 2.4V leads to unpredictable output state.

Noise immunity It is the maximum induced noise voltage a TTL device can withstand without a false change in the output state. The rating of the circuit depends upon the smallest noise voltage that will perturb it. TTL gate has less noise immunity. From the above section, the worst case LOW voltages are:

$$V_{OL}(\text{max}) = 0.4\text{ V}$$

$$V_{IL}(\text{max}) = 0.8\text{ V}$$

and the worst case HIGH voltages are :

$$V_{OH}(\text{min}) = 2.4\text{ V}$$

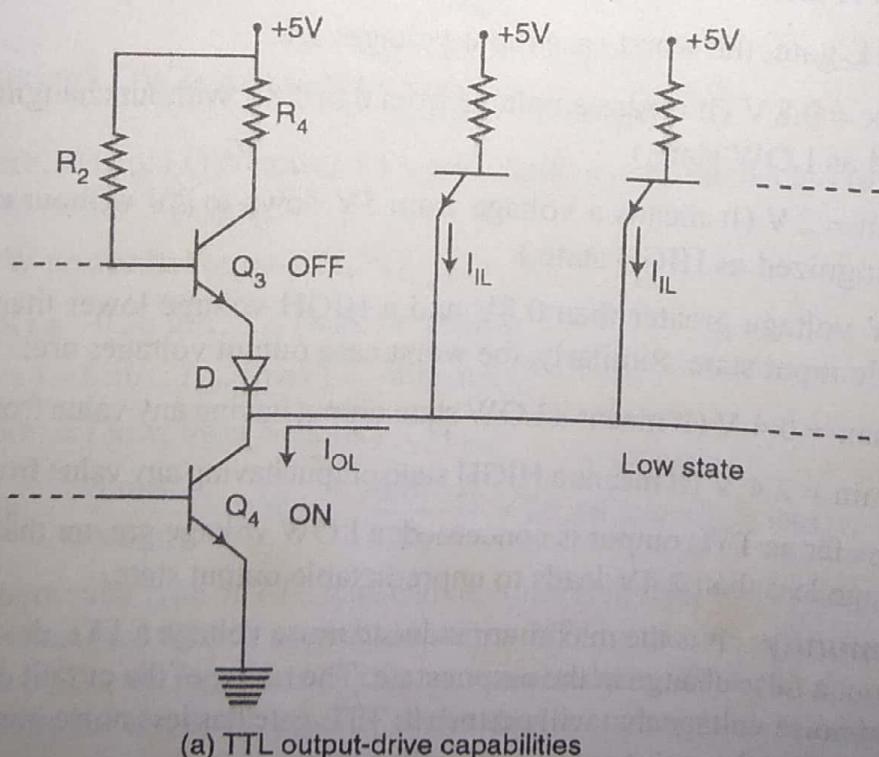
$$V_{IH}(\text{min}) = 2\text{ V}$$

One can observe that there is a difference of 0.4V in both cases. This difference between maximum input LOW voltage and maximum output LOW voltage is called noise *immunity*. The smallest magnitude of noise voltage that would perturb the input signal is 0.4V.

Power dissipation A standard TTL gate is operated with a power supply of 5 volts, which draws an average supply current of 2mA, resulting in a power dissipation of $2\text{mA} \times 5\text{V} = 10\text{mW}$.

Loading rules A single TTL output in the LOW state connected to several TTL inputs is shown in Fig. 4.14(a). Transistor Q_4 is ON and is acting as a current sink for all the currents (I_{IL}) coming back from each input. Although Q_4 is saturated, its ON state resistance is some value other than zero, so the current I_{OL} produces an output voltage drop V_{OL} . The value of V_{OL} must not exceed 0.4V for TTL, and this limits the value of I_{OL} and thus the number of loads that can be driven.

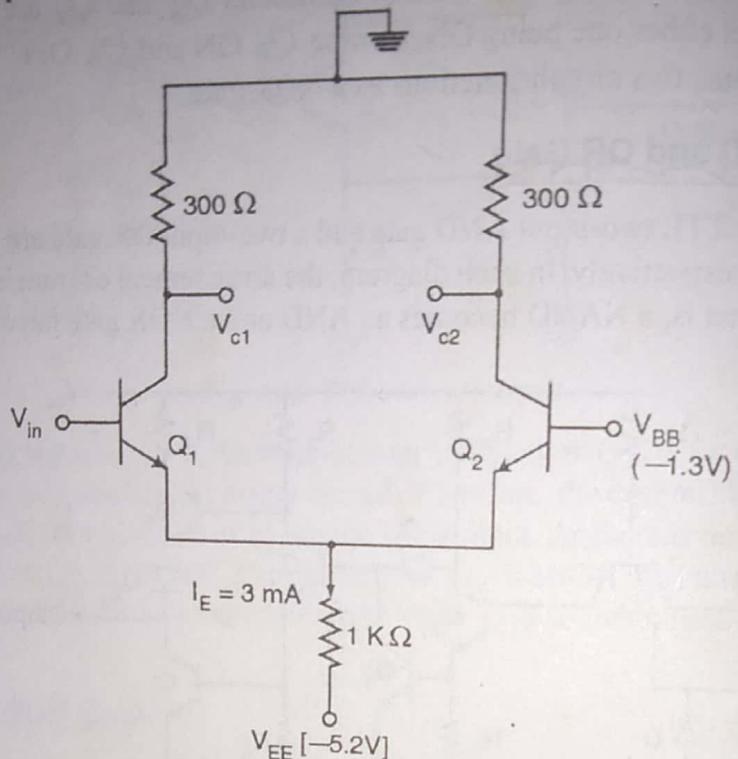
Fig. 4.14(b) shows the HIGH-state situation. The transistor Q_3 is acting as an emitter-follower and is sourcing current to each TTL input. If too many loads are driven, however, the total output current I_{OH} can become too large, causing larger drops across R_2 , Q_3 and D , thereby lowering V_{OH} below the minimum allowable voltage 2.4V.



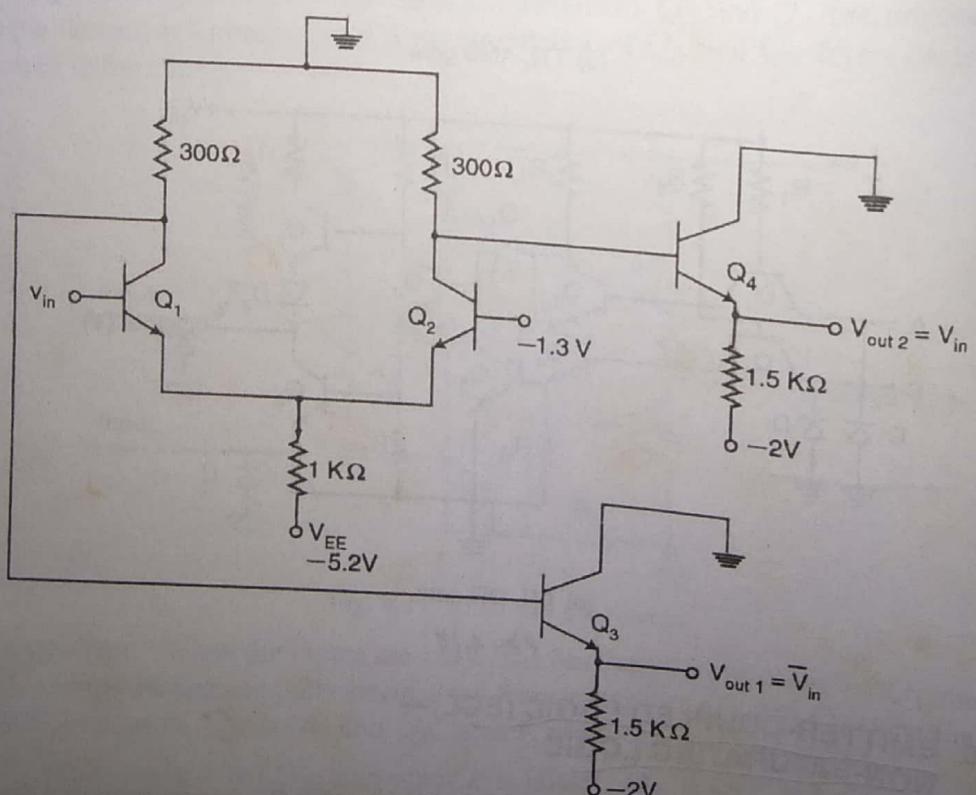
4.10 EMITTER-COUPLED LOGIC (ECL)— NON-SATURATING LOGIC

Emitter-coupled Logic (ECL) is a Current-Mode Logic (CML) or non-saturated digital logic family, which eliminates the turn-off delay of saturated transistors by operating in

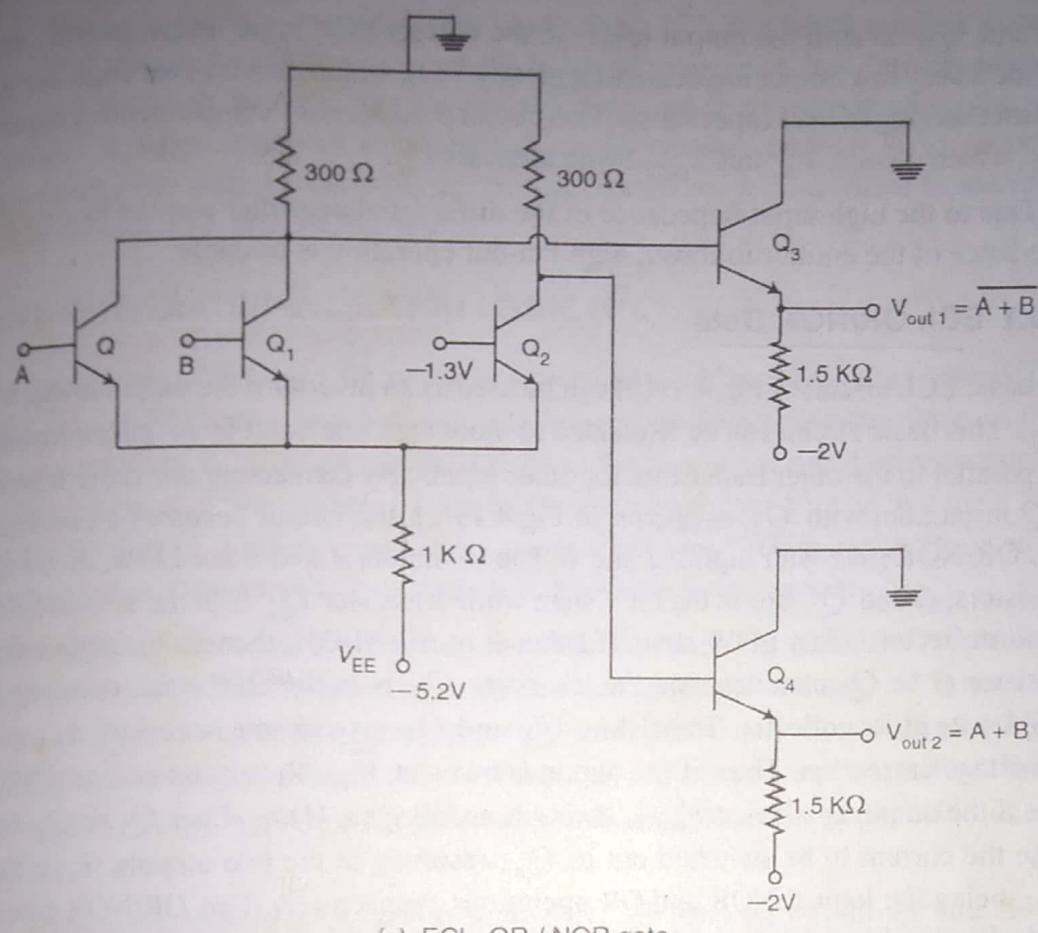
the active mode. At present, the ECL family has the fastest switching speed among the commercially available digital ICs. The propagation delay time of a typical ECL gate is 1ns. Also, it requires a relatively large silicon area and dissipates high power.



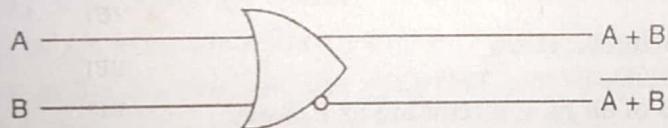
(a) Differential amplifier of ECL circuit



(b) Basic ECL circuit



(c) ECL OR / NOR gate



(d) Logic symbol of ECL OR / NOR gate

Fig. 4.19

The basic circuit of emitter-coupled logic is a differential amplifier as shown in Fig.4.19(a). As a constant current is drawn by the differential amplifier even during transition from one state to another, the power supply line can be free of noise and spikes. Because of the active mode of operation of the differential amplifier, there is no storage delay in switching between ON and OFF states of the transistors in the differential pair.

The V_{EE} supply produces a fixed current I_E , which remains around 3mA during normal operation. This current is allowed to flow through Q_1 or Q_2 , depending on the voltage level at V_m . In other words, this current switches between the collectors of Q_1 and Q_2 as V_m switches between its two logic levels of $-1.7V$ (logical 0 for ECL) and $-0.8V$ (logical 1 for ECL). V_{e1} and V_{e2} are the complements of each other, and the output voltage levels are not the same as the input logic levels.

The output voltage levels are made equal to the input logic level by connecting V_{e1} and V_{e2} to emitter-follower stages (Q_3 and Q_4), as shown in Fig.4.19 (b). The emitter followers perform two functions: (i) they subtract approximately 0.8V from

V_{C1} and V_{C2} to shift the output levels to the correct ECL logic levels, and (ii) they provide a very low output impedance (typically $7\ \Omega$), which provides for large fan-out and fast charging of load capacitance. This circuit produces low complementary outputs, V_{out1} , which equals, $\overline{V_m}$ and V_{out2} , which equals V_m .

Due to the high input impedance of the differential amplifier and the low output impedance of the emitter follower, high fan-out operation is possible.

4.10.1 ECL OR/NOR Gate

The basic ECL circuit of Fig.4.19(b) can be used as an inverter if the output is taken at V_{out1} . This basic circuit can be expanded to more than one input by making transistor Q_1 parallel to the other transistors for other inputs. By connecting one more transistor Q in parallel with Q_1 , as shown in Fig.4.19(c), the circuit becomes a two-input ECL OR/NOR gate with inputs A and B . If both inputs A and B are LOW, then both transistors, Q and Q_1 , are in the OFF state while transistor Q_2 is in the active region and its collector is in a LOW state. If either A or B is HIGH, then accordingly either transistor Q or Q_1 conducts and the transistor Q_2 is in the OFF state, resulting in HIGH state at its collector. Transistors Q_3 and Q_4 provide the necessary d.c. shift for voltage correction. Thus, if the output is taken at V_{out1} the circuit acts as a NOR gate; if the output is taken at V_{out2} , it acts as an OR gate. Here, either Q_1 or Q_2 can cause the current to be switched out of Q_2 , resulting in the two outputs, V_{out1} and V_{out2} being the logical NOR and OR operations, respectively. This OR/NOR gate is symbolized in Fig.4.19(d) and is the fundamental ECL gate.

4.10.2 ECL Characteristics

The characteristics of an ECL circuit are as follows:

- (i) The logic levels are nominally -0.8V (logic 1) and -1.70V (logic 0).
- (ii) The transistors never saturate, i.e. storage delay in ECL circuit is eliminated, and hence switching speed is very high. Typical propagation delay time is 1ns , which makes ECL faster than advanced Schottky TTL (74AS series).
- (iii) Because of the low noise margin, 250 milli-volt, ECL circuits are not reliable in heavy industrial environments.
- (iv) An ECL logic block usually produces an output and its complement. This eliminates the need for inverters.
- (v) Fan-outs are typically around 25, owing to the low-impedance emitter-follower outputs. Such a small fan-out is a limitation compared with the saturating logic families or the MOS logic families.
- (vi) Typical power dissipation for a basic ECL gate is 40 mW , somewhat higher than the 74AS series. This is true because all the transistors are in the active mode.
- (vii) The total current flow in an ECL circuit remains relatively constant regardless of its logic state. This helps to maintain an unvarying current drain on the circuit power supply even during switching transitions. Thus, no noise spikes will be internally generated like those produced by TTL totem-pole circuits.

The ECL family is not as widely used as the TTL and MOS families except in very high frequency applications, where its speed is superior. Its relatively low noise margins and high power drain are disadvantages when compared with other logic families. Another drawback is its negative supply voltage and logic levels, which are not compatible with the other logic families; this makes ECL difficult to use in conjunction with TTL and MOS circuits.

4.12.1 MOSFET

In MOSFET, the channel can be of *p* or *n* type, depending on whether the majority carriers are either holes or electrons. The mode of operation can be *enhancement* or *depletion*, depending on the state of the channel region at zero gate voltage. If the channel is initially doped lightly with *p*-type impurity, a conducting channel exists at zero gate voltage and the device is said to operate in the *depletion mode*. In this mode, current flows unless the channel is depleted by an applied gate field. If the region beneath the gate is left initially uncharged, a channel must be induced by the gate field before current can flow. Thus, the channel current is enhanced by the gate voltage and such a device is said to operate in the *enhancement mode*.

The schematic symbols for the *n*-channel and *p*-channel enhancement MOSFETs are shown in Fig. 4.22. The direction of the arrow indicates the type of channel *p* or *n*. The symbols show a broken line between the *source*, *substrate* and *drain* to indicate that there is *normally* no conducting channel among these electrodes. The symbol also shows a separation between the *gate* and the other terminals to indicate the very high resistance ($>10,000\text{ M}\Omega$) between the *gate* and *channel*.

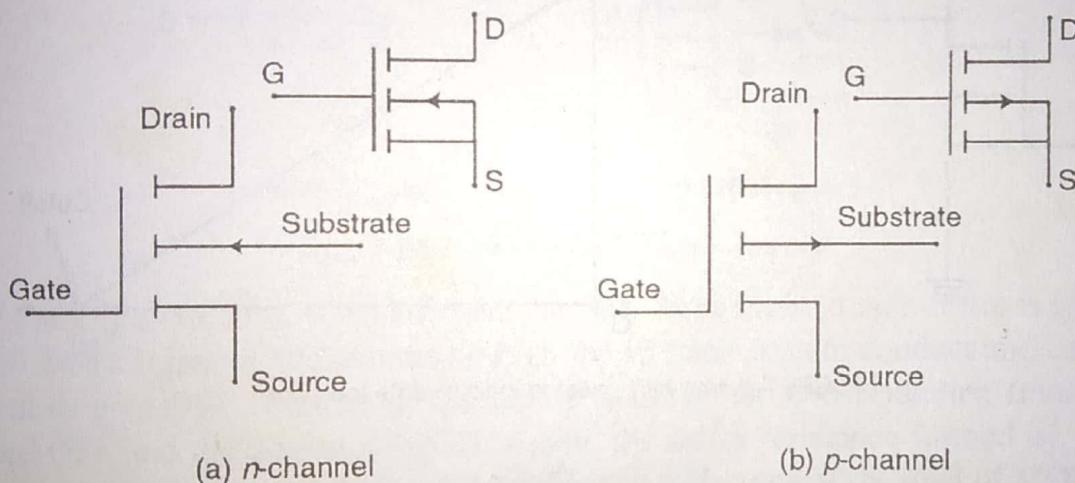


Fig. 4.22 Schematic symbols for the enhancement MOSFETs

PMOS It uses only *p*-channel enhancement MOSFET. A resistor at the output of a PMOS circuit could be used to drop the high level voltage to one suitable for CMOS circuit. *Holes* are the current carriers for PMOS.

NMOS It uses only *n*-channel enhancement MOSFET. NMOS has a greater packing density than PMOS. *Free electrons* are the current carriers in NMOS. These circuits require voltage typically ranging from 5V to 12V.

CMOS It uses both *p*-and *n*-channel devices. It has the greatest complexity and lowest packing density among the MOS families. It possesses the important advantages of much lower power dissipation, very high input impedance and high noise immunity. The CMOS logic gates are used in battery-operated portable equipment. Its main disadvantage is its low speed due to high input impedance.

PMOS and NMOS digital ICs have a greater packing density and are therefore more economical than CMOS. NMOS is also about twice as fast as PMOS. PMOS and NMOS find their widest applications in LSI (microprocessors, memories, ROMs, etc.) while CMOS is widely used in MSI applications.

the output voltage approaches the level V_{DD} . If all the inputs are LOW (at 0V), the transistors Q_4 , Q_5 and Q_6 turn OFF, and the voltage at point K comes close to V_{DD} . The transistor Q_3 then switches ON and the output drops to zero. Hence, this circuit performs the OR function.

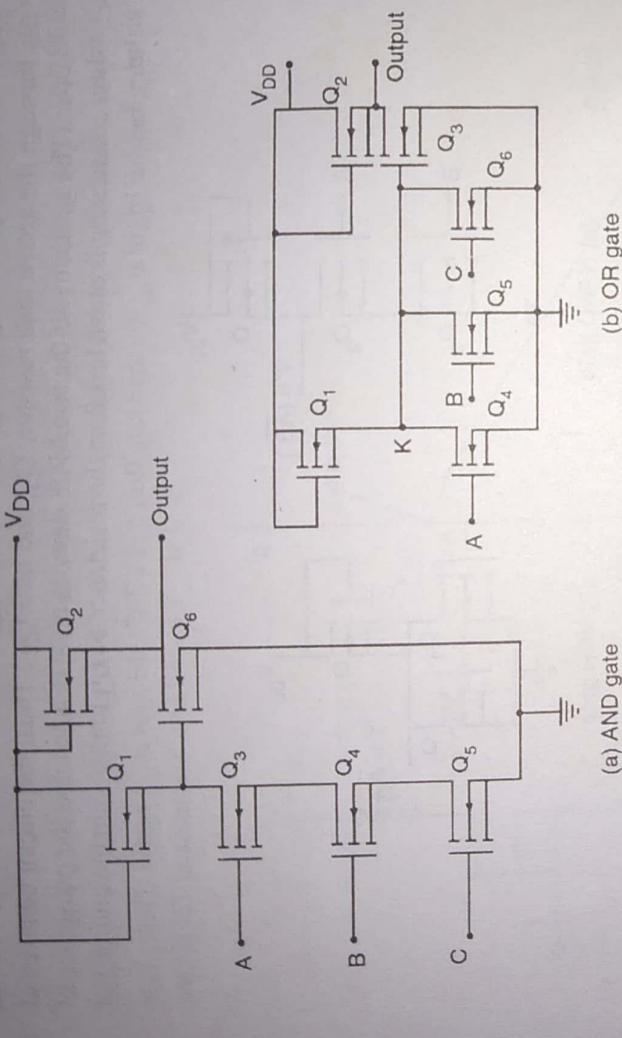


Fig. 4.25 n-channel MOS logic circuits

4.12.3 Characteristics of MOS Logic

MOS logic families are slower in operating speed, require much less power, have a better noise margin and a higher fan-out.

Operating speed A typical NMOS NAND gate has a propagation delay of 50ns. The combination of large R_{out} and large C_{load} serves to increase switching time.

Noise margin Typically NMOS noise margins are around 1V.

Fan-out The fan-out capabilities of MOS logic would be virtually unlimited because of the extremely high input resistance at each MOSFET input. MOS logic can easily operate at a fan-out value of 50.

Power drain MOS logic circuits draw small amount of power because of the relatively large resistance being used.

Process complexity MOS logic is the simplest logic family when it comes to fabrication since it uses only one basic element, an NMOS (or PMOS) transistor. It does not require resistors, diodes, etc. This characteristic together with its lower power dissipation (P_D) makes it ideally suited for LSI, and this is where MOS logic has made its greatest impact in the digital field.

4.13 COMPLEMENTARY MOS LOGIC

Complementary Symmetry Metal-oxide Semiconductors, COSMOS or CMOS, are logic gates made using both PMOS and NMOS transistors. The basic gates employ both *p*-and *n*-channels enhancement mode complementary symmetry MOSFETs. The power consumption of CMOS under static conditions is extremely low. CMOS logic circuits excel PMOS and NMOS logic elements in a number of features like extremely small d.c. power dissipation, enhanced noise immunity, high fan-out capability and ease of interfacing (compatibility with other logic circuits). CMOS circuits are used both in logic circuits and memory devices. The source terminal of the *p*-channel device is at V_{DD} , and the source terminal of the *n*-channel device is at ground. The systems employing CMOS transistors require only one power supply source of a wide range of voltages, from +3 to +15V. The CMOS fabrication process is simpler than TTL and has a greater packing density, therefore, permitting more circuitry in a given area and reducing the cost per function.

4.13.1 CMOS Inverter

Just as in the case of ordinary MOS gate, the inverter is basic to the CMOS gate. A basic inverter connection is shown in Fig. 4.26. The driver is transistor Q_2 which is the *n*-channel, and Q_1 (the *p*-channel device) acts as the load. Notice that drains are connected together to provide the output and that the source and substrate are connected together. The source of *p*-channel device is connected to $+V_{DD}$ and the source of *n*-channel is connected to ground. The gates of the two devices are connected together as a common input. It is important to note that the output voltage is equal to the supply voltage and the current flows through the circuit only during switching of the input voltage from one level to the other.

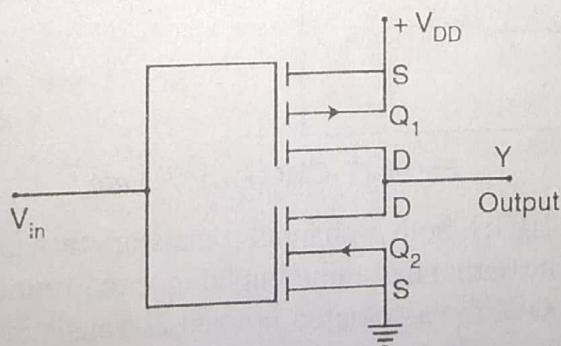


Fig. 4.26 CMOS inverter

Operation When V_{in} is LOW, Q_2 is OFF but Q_1 is ON. This means the output voltage is HIGH. On the other hand, when V_{in} is HIGH, Q_2 is ON and Q_1 is OFF. In this case, the output voltage is LOW. Since the output voltage is always opposite in phase to the input voltage, the circuit acts as an inverter.

The operation of CMOS transistors can be described by the following rules:

n-channel MOSFETs are turned ON by a positive gate voltage.

p-channel MOSFETs are turned ON by a negative gate voltage.

The CMOS inverter can be modified to build other CMOS logic circuits. A CMOS circuit is ideal in a number of ways. First, it needs extremely low power to operate the circuit. Since either one of the MOS devices is OFF when the input is in LOW or HIGH state, only the leakage current in the order of nanoamperes flows through the circuit and the power dissipation of the CMOS devices is typically in the range of nanowatts. This low power consumption is the reason for the popularity of CMOS devices in pocket calculators, digital wristwatches, and portable microcomputers.

Fan-out for CMOS circuits is ideally infinite since no loading occurs when it is connected to the gate of enhancement MOSFET. Practical values of fan-out greater than 50 are typical.

Propagation delay of a CMOS gate is typically about 25 to 100 ns, depending on the particular device. It increases with greater load capacitance.

4.13.2 CMOS NAND Gate (74C00)

A two-input NAND gate which consists of two *p*-type units in parallel and two *n*-type units in series is shown in Fig. 4.27. Notice that Q_1 and Q_2 form one complementary connection; Q_3 and Q_4 form another.

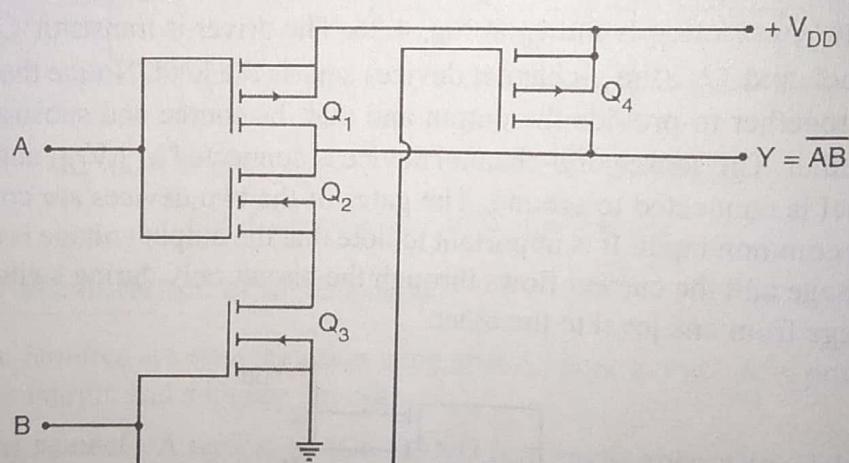


Fig. 4.27 CMOS NAND gate

If both inputs are HIGH, both *p*-channel transistors turn OFF and both *n*-channel transistors turn ON. The output has a low impedance to ground and produces a LOW state. If any input is LOW, the associated *n*-channel transistor is turned OFF and the associated *p*-channel transistor is turned ON. The output is coupled to V_{DD} and goes to the HIGH state. This functions as a logic NAND gate. The 74C00 is a quad 2-input NAND gate.

To produce the positive AND function, the output of the CMOS NAND gate can be connected to a CMOS inverter.

4.13.3 CMOS NOR Gate

A two-input CMOS NOR gate using a pair of PMOS transistors (Q_1 and Q_2) and NMOS transistors (Q_3 and Q_4) is shown in Fig. 4.28. Of the two inputs, A and B either of the inputs can turn ON the PMOS or NMOS device connected to it.

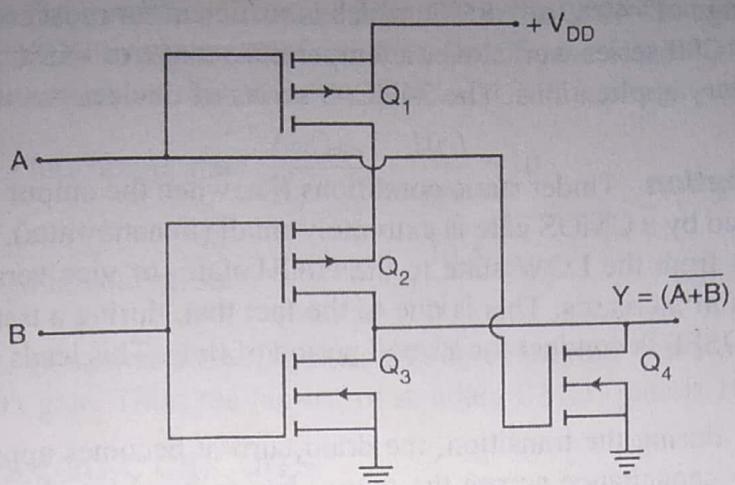


Fig. 4.28 CMOS NOR gate

When both inputs are LOW, both PMOS devices are driven ON and both NMOS devices OFF. The output is coupled to V_{DD} and goes to the HIGH state. If any input is HIGH, the associated p -channel transistor is turned OFF and the associated n -channel transistor turns ON. This connects the output to the ground causing a LOW output. Thus this circuit functions as a NOR gate. A CMOS OR gate can be formed by combining the output of the CMOS NOR gate with a CMOS inverter.

4.13.4 CMOS Series

There are several series of the CMOS digital logic family. The original design of CMOS ICs is recognised from the 4000 number designation. The 74C series are pin-and-function compatible with TTL devices having the same number. The performance characteristics of the 74C series are about the same as the 4000 series. CMOS IC type 74C04 has six inverters with the same pin configuration as TTL type 7404. The 74HC series operates at higher speeds than the 74C series. The 74HCT series is electrically compatible with TTL ICs. This means that the circuit in this series can be connected to the inputs and outputs of TTL ICs without the need of additional interfacing circuits. The commercially available CMOS series are listed in Table 4.5.

Table 4.5 Various series of the CMOS logic family

CMOS series	Prefix	Example
Original CMOS	40	4009
Pin compatible with TTL	74 C	74 C04
High-speed and pin compatible with TTL	74 HC	74 HC04
High-speed and electrically compatible with TTL	74 HCT	74 HCT04

4.14 CHARACTERISTICS OF CMOS

The first CMOS logic series was produced by RCA and is known as the 4000 series, which was later developed by other manufacturers. At present, several manufacturers have developed a CMOS series which is pin-for-pin compatible with TTL. This is the 74C00 series and it contains devices that have the same pin assignments and logic operations as their TTL counterparts. Any device in the 74C00 series works over a

temperature range of -40°C to $+85^{\circ}\text{C}$, which is sufficient for most commercial applications. The 54C00 series works over a temperature range of -55°C to 125°C and is useful for military applications. The 74HC00 series of devices has the advantage of higher speed.

Power dissipation Under static conditions (i.e. when the output is constant), the power consumed by a CMOS gate is extremely small (in nanowatts). When a CMOS output changes from the LOW state to the HIGH state (or vice versa), the average power dissipation increases. This is due to the fact that, during a transition between states, both MOSFETs conduct for a small period of time. This leads to a spike in the supply current.

Therefore, during the transition, the drain current becomes appreciable. Moreover, any stray capacitance across the output has to be charged before the output voltage can change. This capacitive charging draws additional current from the supply, thereby increasing the instantaneous power dissipation.

The average power dissipation of a CMOS device whose output is continuously changing is called the *active power dissipation*. This power dissipation per gate increases with frequency and supply voltage. The power consumption of a CMOS gate is around 10mW in the MHz region. Thus, CMOS loses its advantages at higher frequencies.

Propagation delay time The propagation delay of a standard CMOS gate ranges from 25 to 150ns, with the exact value depending on the power supply voltage and other factors. A CMOS NAND gate typically has a propagation delay time of about 25ns when $V_{DD} = 10\text{V}$, and 50ns when $V_{DD} = 5\text{V}$.

Voltage levels CMOS can be operated over a supply voltage range of 3 to 15V. A supply voltage of 9 to 12V can be used to obtain the overall best performance of a CMOS gate in respect of high speed and noise immunity. When CMOS is being used with TTL, the V_{DD} supply voltage is made 5V so that the voltage levels of the two families are the same.

Noise margin In CMOS series, the noise margin is typically about 45% of the supply voltage V_{DD} . They have the same noise margin in both HIGH and LOW states. A V_{DD} of 5V guarantees a 2.25V noise margin.

Floating inputs A floating TTL input is equivalent to a high input. If a CMOS input is floated, a possible noise problem is set up and there is excessive power dissipation. Therefore, it is necessary to connect all the input pins of the CMOS devices to some voltage level, preferably to ground or V_{DD} .

Sourcing and sinking When a standard CMOS driver output is LOW, the current from the CMOS load to the driver is only $1\ \mu\text{A}$. This indicates that the CMOS driver has to sink only $1\ \mu\text{A}$. Similarly, when the CMOS driver output is HIGH, the driver is sourcing $1\ \mu\text{A}$ to an input of the load gate. The worst case input currents for CMOS devices are:

$$\begin{aligned} I_{IL(\max)} &= -1\ \mu\text{A}; & I_{IH(\max)} &= 1\ \mu\text{A} \\ I_{OL(\max)} &= 10\ \mu\text{A}; & I_{OH(\max)} &= -10\ \mu\text{A} \end{aligned}$$

Fan-out The fan-out of CMOS gates depends on the type of load being connected. If a standard CMOS drives another standard CMOS, the fan-out can be calculated from the input and output currents of the standard CMOS gate given above.

$$\text{Considering low output state: } \frac{I_{OL,\max}}{I_{IL,\max}} = \frac{10\text{ A}}{1\text{ A}} = 10$$

$$\text{Considering high output state: } \frac{I_{OH,\max}}{I_{IH,\max}} = \frac{10\text{ A}}{1\text{ A}} = 10$$

Therefore, 10 standard CMOS gates can be connected to the output of another standard CMOS gate. Thus, the fan-out of standard CMOS gate is 10.