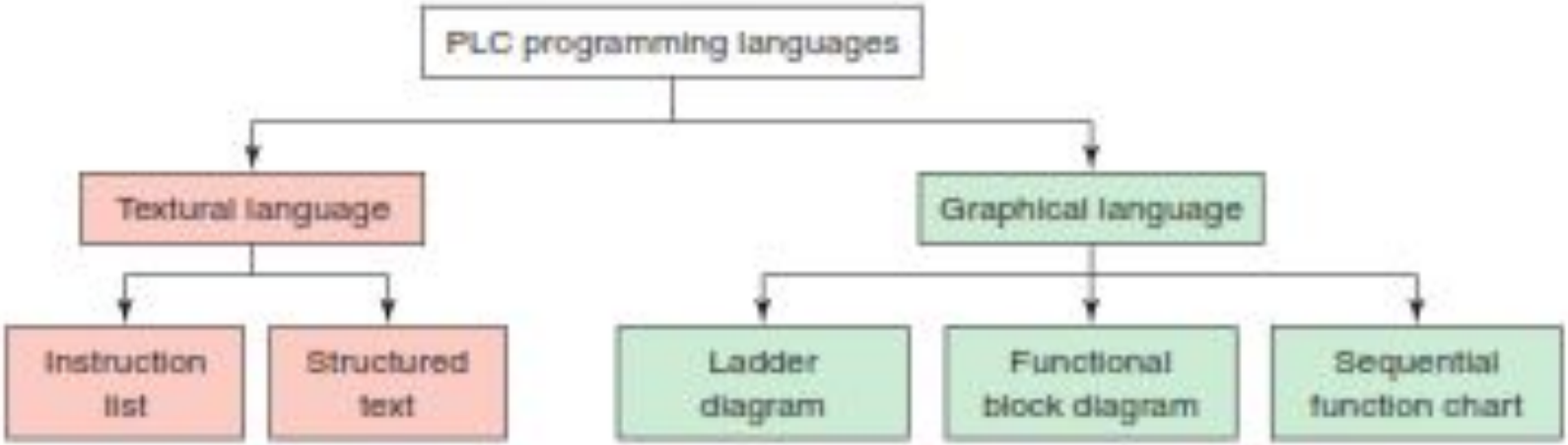
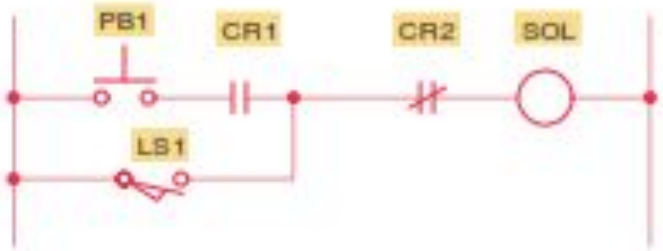
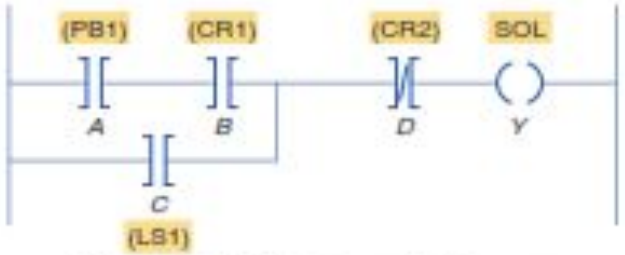


Figure 5-12 Standard IEC 61131 languages associated with PLC programming.



(*a*) Hardwired relay control circuit



(*b*) Equivalent ladder diagram (LD) program

START	PB1
AND	CR1
OR	LS1
AND NOT	CR2
OUT	SOL

(*c*) Equivalent instruction list (IL) program

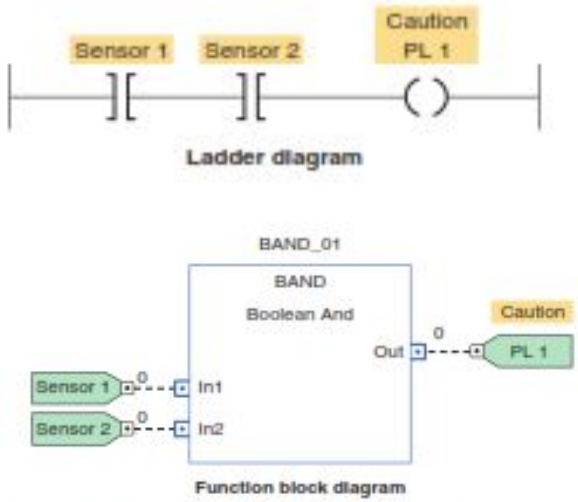
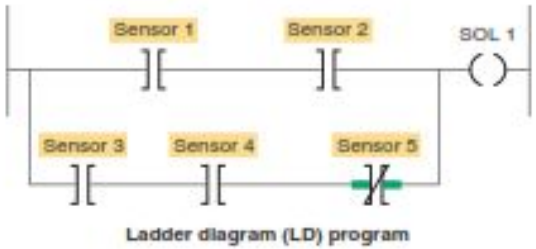


Figure 5-15 PLC ladder and equivalent function block diagram.




```
IF Sensor_1 AND Sensor_2 THEN
        SOL_1 := 1;
ELSEIF Sensor_3 AND Sensor_4 AND NOT Sensor_5 THEN
        SOL_1 := 1;
END_IF;
```

Structured text (ST) program

Figure 5-17 PLC ladder and equivalent structured text program.

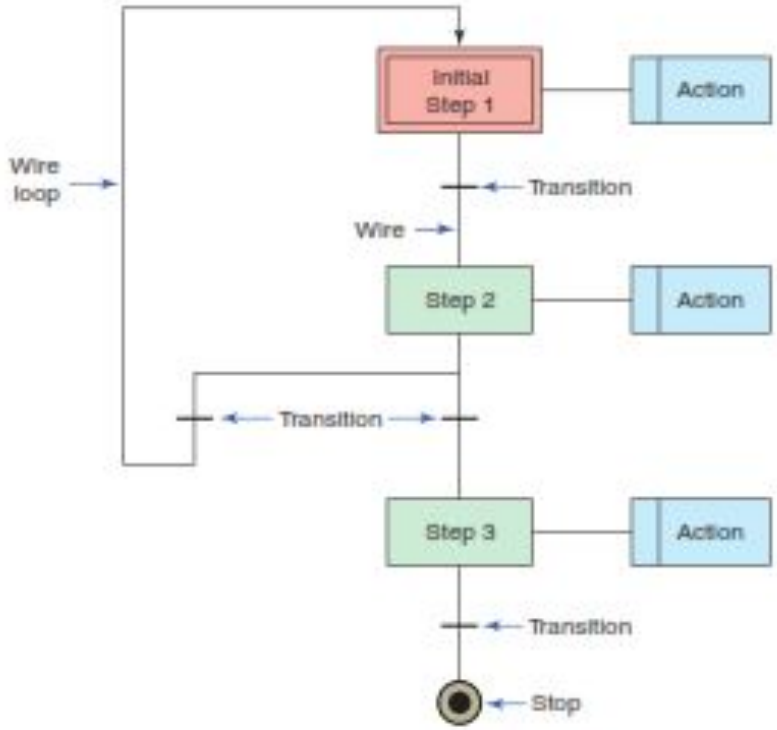


Figure 5-16 Major elements of a sequential function chart program.

Ladder Logic Programming

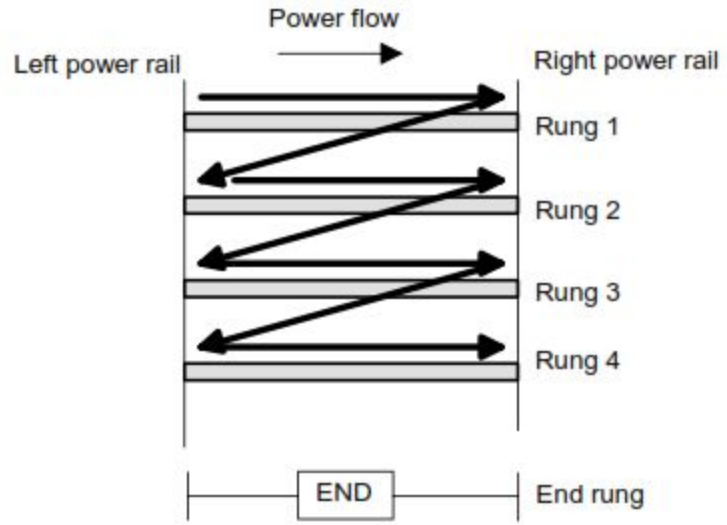
- Rules:

1. The vertical lines of the diagram represent the power rails between which circuits are connected. The power flow is taken to be from the left-hand vertical across a rung.
2. Each rung on the ladder defines one operation in the control process.
3. A ladder diagram is read from left to right and from top to bottom
4. The end rung might be indicated by a block with the word END or RET for return, since the program promptly returns to its beginning.
5. Each rung must start with an input or inputs and must end with at least one output.
6. Electrical devices are shown in their normal condition. Thus a switch which is normally open until some object closes it, is shown as open on the ladder diagram.

Ladder Logic Programming

- Rules:

7. A particular device can appear in more than one rung of a ladder.
8. The inputs and outputs are all identified by their addresses, the notation used depending on the PLC manufacturer



Ladder Logic Programming

- Standard IEC 1131-3 symbols that are used for input and output devices

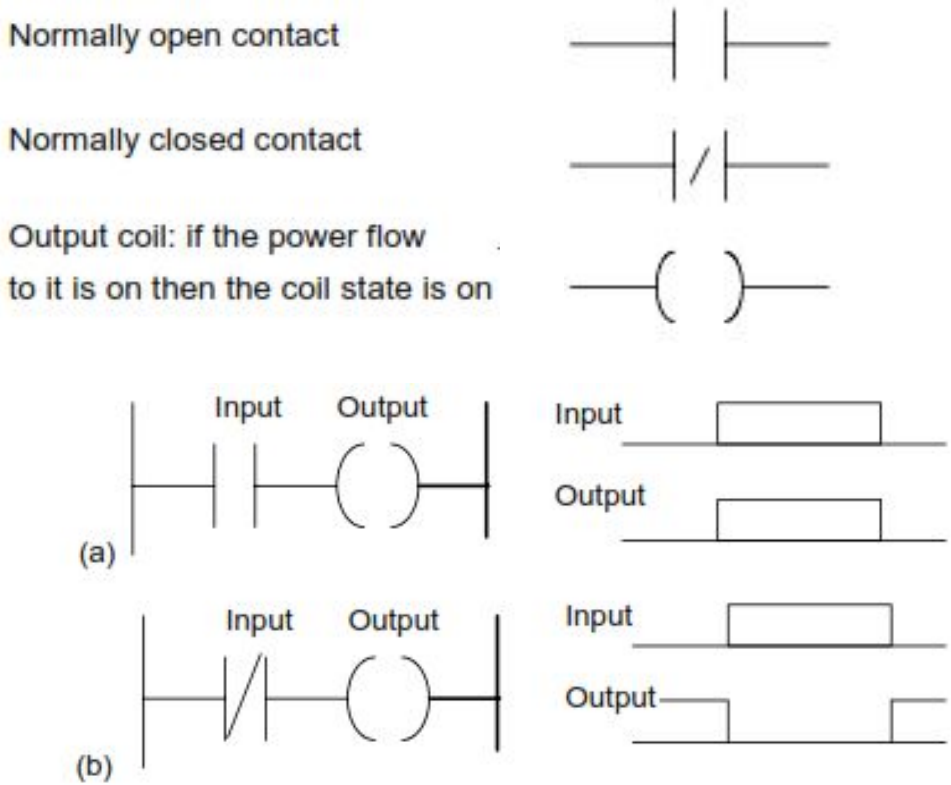


Figure 5.5 *A ladder rung*

Ladder Logic Programming

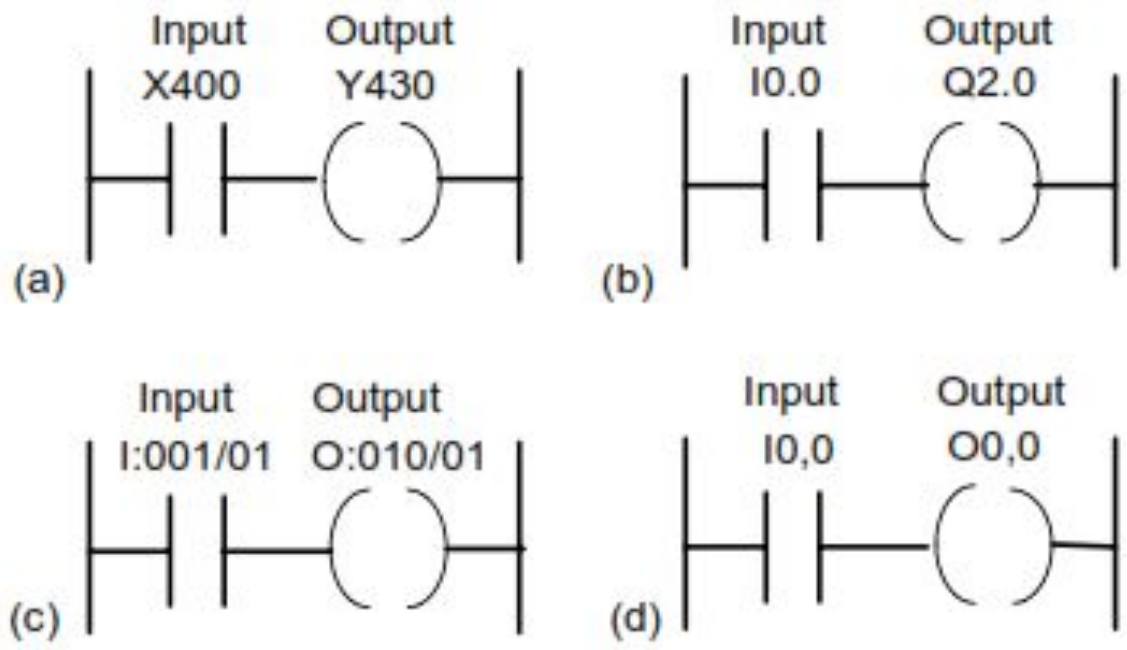


Figure 5.6 *Notation: (a) Mitsubishi, (b) Siemens, (c) Allen-Bradley, (d) Telemecanique*

Ladder Logic Programming

- Logical Functions:

1) AND Logic

Inputs		Output
A	B	
0	0	0
0	1	0
1	0	0
1	1	1

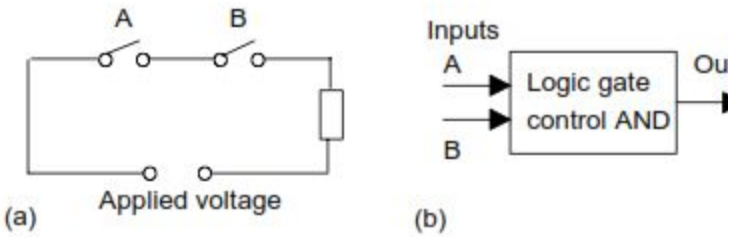


Figure 5.7 *(a) AND circuit, (b) AND logic gate*

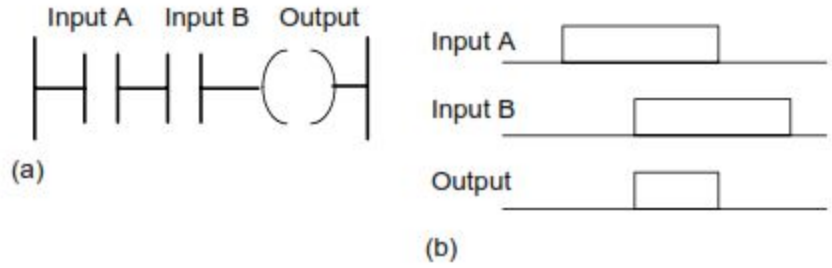


Figure 5.8 *AND gate with a ladder diagram rung*

Ladder Logic Programming

- Logical Functions:

2) OR Logic

Inputs		Output
A	B	
0	0	0
0	1	1
1	0	1
1	1	1

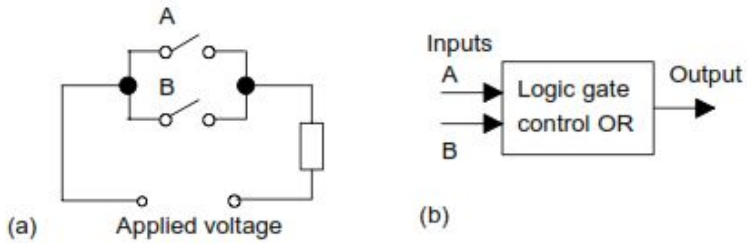


Figure 5.9 *(a) OR electrical circuit, (b) OR logic gate*

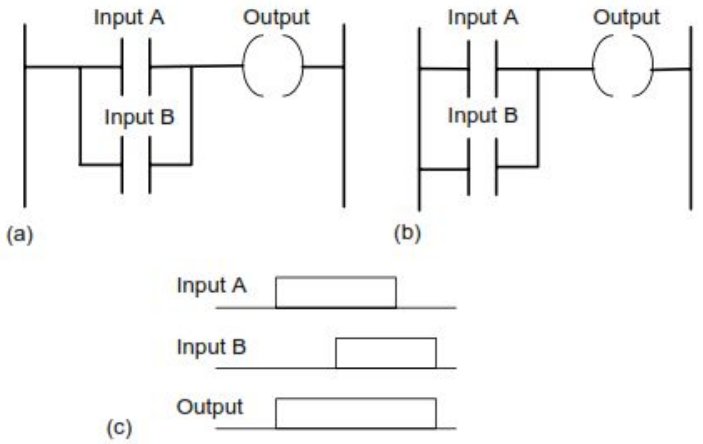


Figure 5.10 *OR gate*

Ladder Logic Programming

- Logical Functions:

3) NOT Logic

Input A	Output
0	1
1	0

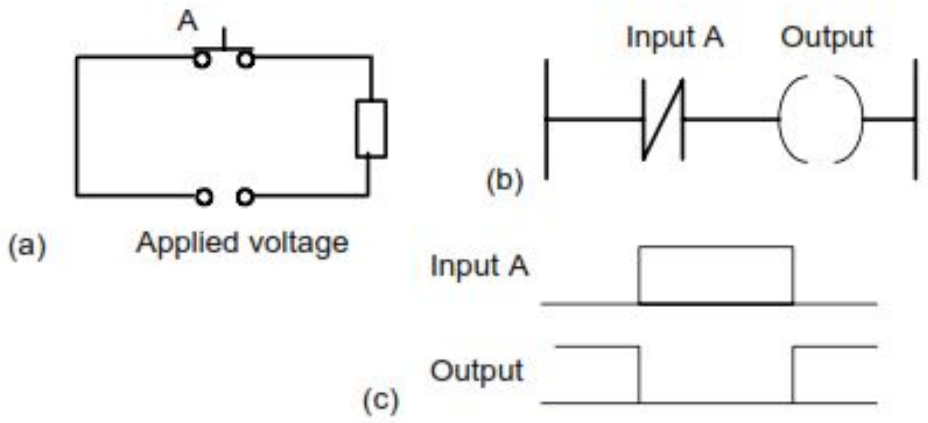


Figure 5.11 *(a) NOT circuit, (b) NOT logic with a ladder rung, (c) high output when no input to A*

Ladder Logic Programming

- Logical Functions:

4) NAND Logic

Inputs		Output
A	B	
0	0	1
0	1	1
1	0	1
1	1	0

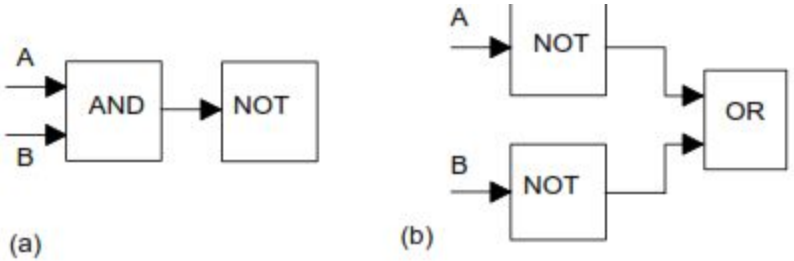


Figure 5.12 *NAND gate*

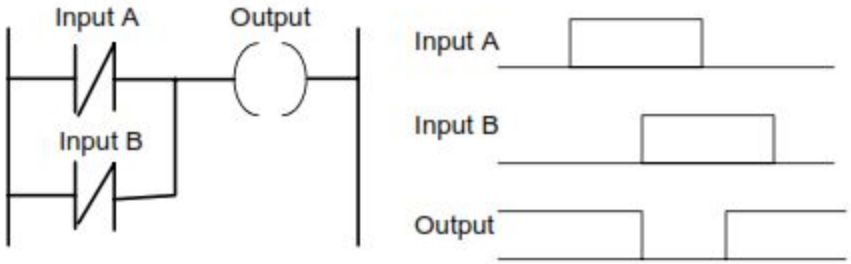


Figure 5.13 *A NAND gate*

Ladder Logic Programming

- Logical Functions:

5) NOR Logic

Inputs		Output
A	B	
0	0	1
0	1	0
1	0	0
1	1	0

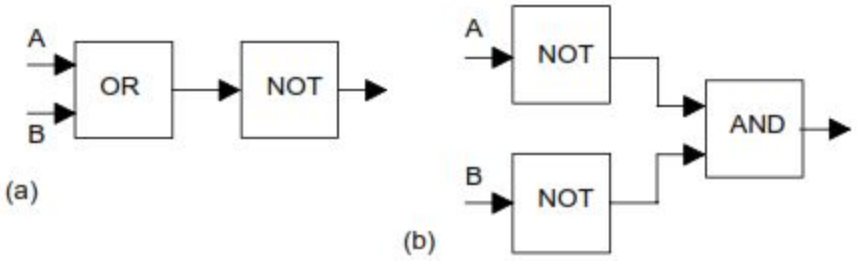


Figure 5.14 *NOR gate*

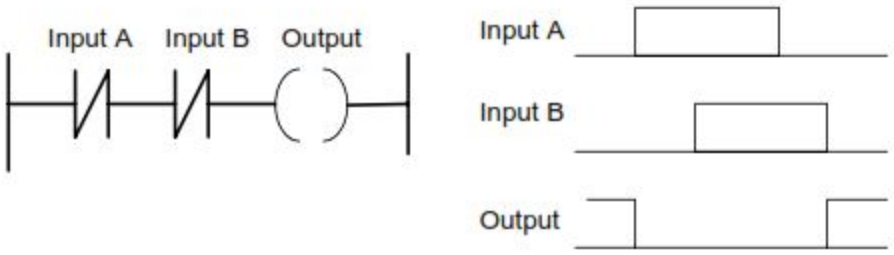


Figure 5.15 *NOR gate*

Ladder Logic Programming

- Logical Functions:

6) XOR Logic

Inputs		Output
A	B	
0	0	0
0	1	1
1	0	1
1	1	0

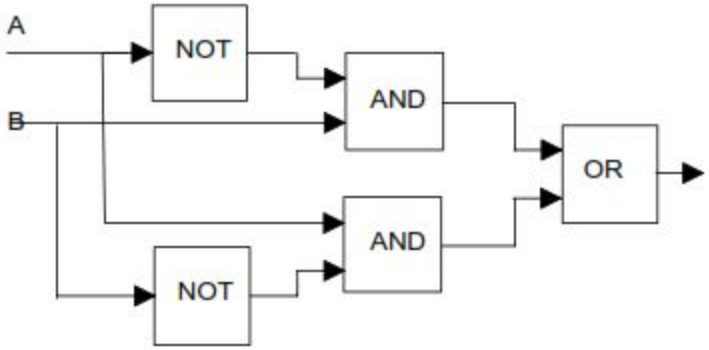


Figure 5.16 *XOR gate*

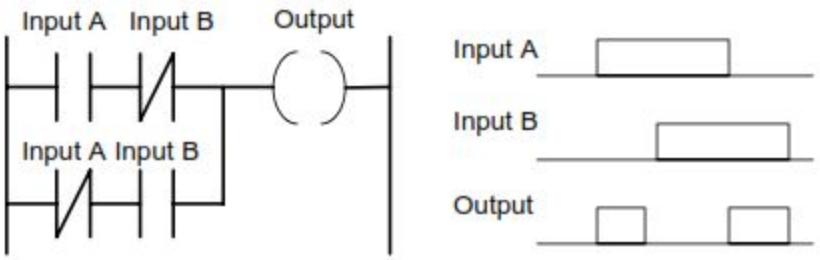


Figure 5.17 *XOR gate*