Q1)

```
abinav@Ubuntu:~/OpenSTA/Project$ ~/OpenSTA/build/sta
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This program comes with ABSOLUTELY NO WARRANTY; for details type `show_war
% read_liberty example_typ.lib
read_verilog top.v
link_design top
read_sdc top_mc_both.sdc
report_checks -path_delay min_max > reports_mc_both.txt
exit
```

```
abinav@Ubuntu:~/OpenSTA/Project$ ~/OpenSTA/build/sta
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This program comes with ABSOLUTELY NO WARRANTY; for details type `show_warra
% read_liberty example_typ.lib
read_verilog top.v
link_design top
read_sdc top_mc_setup.sdc
report_checks -path_delay min_max > reports_mc_setup.txt
exit
```

q2)

```
module top (
  input wire a,
  input wire b,
  input wire Clock,
  output wire out
);

  wire a_n, clk_c1, clk_c2;
  wire q1, q2, q2_n, and_y, out_q;

  INV_X1 N1 (.A(a), .ZN(a_n));
  INV_X1 C1 (.A(Clock), .ZN(clk_c1));
  INV_X1 C2 (.A(clk_c1), .ZN(clk_c2));


  DFF_X1 q1_reg (.D(a_n), .CK(Clock), .Q(q1), .QN());
```

```
  DFF_X1 q2_reg (.D(b), .CK(clk_c2), .Q(q2), .QN());
  DFF_X1 out_reg (.D(and_y), .CK(Clock), .Q(out_q), .QN());

  INV_X1 N2 (.A(q2), .ZN(q2_n));
  AND2_X1 A1 (.A1(q1), .A2(q2_n), .ZN(and_y));
  INV_X1 N3 (.A(out_q), .ZN(out));

endmodule
```

q3)

```
create_clock -name clk -period 10 [get_ports clk]

set_input_delay 2 -clock clk [get_ports {a b}]

set_output_delay 2 -clock clk [get_ports out]

set_drive 1 [get_ports {a b clk}]
set_load 0.1 [get_ports out]

set_clock_uncertainty 0.1 [get_clocks clk]
```

```
 Startpoint: q1_reg (rising edge-triggered flip-flop clocked by CLK)
 Endpoint: out_reg (rising edge-triggered flip-flop clocked by CLK)
 Path Group: CLK
 Path Type: min

   Delay Time Description
 ---------------------------------------------------------
    0.00 0.00 clock CLK (rise edge)
    0.00 0.00 clock network delay (ideal)
    0.00 0.00 ^ q1_reg/CK (DFF_X1)
    0.08 0.08 v q1_reg/Q (DFF_X1)
    0.03 0.10 v A1/ZN (AND2_X1)
    0.00 0.10 v out_reg/D (DFF_X1)
              0.10 data arrival time

    0.00 0.00 clock CLK (rise edge)
    0.00 0.00 clock network delay (ideal)
    0.10 0.10 clock uncertainty
    0.00 0.10 clock reconvergence pessimism
              0.10 ^ out_reg/CK (DFF_X1)
    0.00 0.10 library hold time
```

```
          0.10 data required time
-----------------------------------------------------------
          0.10 data required time
         -0.10 data arrival time
-----------------------------------------------------------
          0.00 slack (MET) (Set up)


Startpoint: out_reg (rising edge-triggered flip-flop clocked by CLK)
Endpoint: out (output port clocked by CLK)
Path Group: CLK
Path Type: max

  Delay Time Description
-----------------------------------------------------------
   0.00 0.00 clock CLK (rise edge)
   0.00 0.00 clock network delay (ideal)
   0.00 0.00 ^ out_reg/CK (DFF_X1)
   0.09 0.09 ^ out_reg/Q (DFF_X1)
   0.00 0.09 v N3/ZN (INV_X1)
   0.00 0.09 v out (out)
          0.09 data arrival time

  10.00 10.00 clock CLK (rise edge)
   0.00 10.00 clock network delay (ideal)
  -0.10 9.90 clock uncertainty
   0.00 9.90 clock reconvergence pessimism
  -2.00 7.90 output external delay
          7.90 data required time
-----------------------------------------------------------
          7.90 data required time
         -0.09 data arrival time
-----------------------------------------------------------
          7.81 slack (MET) (hold)
```

q4)

```
create_clock -name CLK -period 10 [get_ports Clock]


set_input_delay 2 -clock CLK [get_ports {a b}]
set_output_delay 2 -clock CLK [get_ports out]
```

```
set_clock_latency -source 0.5 [get_clocks CLK]
set_clock_uncertainty 0.1 [get_clocks CLK]
Startpoint: q1_reg (rising edge-triggered flip-flop clocked by CLK)
Endpoint: out_reg (rising edge-triggered flip-flop clocked by CLK)
Path Group: CLK
Path Type: min

  Delay Time Description
---------------------------------------------------------
   0.00 0.00 clock CLK (rise edge)
   0.50 0.50 clock network delay (ideal)
   0.00 0.50 ^ q1_reg/CK (DFF_X1)
   0.08 0.58 v q1_reg/Q (DFF_X1)
   0.03 0.60 v A1/ZN (AND2_X1)
   0.00 0.60 v out_reg/D (DFF_X1)
             0.60 data arrival time

   0.00 0.00 clock CLK (rise edge)
   0.50 0.50 clock network delay (ideal)
   0.10 0.60 clock uncertainty
   0.00 0.60 clock reconvergence pessimism
             0.60 ^ out_reg/CK (DFF_X1)
   0.00 0.60 library hold time
             0.60 data required time
---------------------------------------------------------
             0.60 data required time
            -0.60 data arrival time
---------------------------------------------------------
             0.00 slack (MET)


Startpoint: out_reg (rising edge-triggered flip-flop clocked by CLK)
Endpoint: out (output port clocked by CLK)
Path Group: CLK
Path Type: max

  Delay Time Description
---------------------------------------------------------
   0.00 0.00 clock CLK (rise edge)
   0.50 0.50 clock network delay (ideal)
```

```
  0.00  0.50 ^ out_reg/CK (DFF_X1)
  0.09  0.59 ^ out_reg/Q (DFF_X1)
  0.00  0.59 v N3/ZN (INV_X1)
  0.00  0.59 v out (out)
        0.59   data arrival time

 10.00 10.00 clock CLK (rise edge)
  0.50 10.50 clock network delay (ideal)
 -0.10 10.40 clock uncertainty
  0.00 10.40 clock reconvergence pessimism
 -2.00  8.40 output external delay
        8.40   data required time
---------------------------------------------------------
        8.40   data required time
       -0.59   data arrival time
---------------------------------------------------------
        7.81   slack (MET)
```

I only added source latency which which shifts both launch and capture edges causing not shift in the setup and hold worst case slack

q5)

```
create_clock -name CLK -period 5 [get_ports Clock]
set_input_delay 2 -clock CLK [get_ports {a b}]
set_output_delay 2 -clock CLK [get_ports out]
set_clock_uncertainty 0.1 [get_clocks CLK]
```

```
Startpoint: q1_reg (rising edge-triggered flip-flop clocked by CLK)
Endpoint: out_reg (rising edge-triggered flip-flop clocked by CLK)
Path Group: CLK
Path Type: min

  Delay Time Description
---------------------------------------------------------
  0.00 0.00 clock CLK (rise edge)
  0.00 0.00 clock network delay (ideal)
  0.00 0.00 ^ q1_reg/CK (DFF_X1)
  0.08 0.08 v q1_reg/Q (DFF_X1)
  0.03 0.10 v A1/ZN (AND2_X1)
  0.00 0.10 v out_reg/D (DFF_X1)
        0.10   data arrival time
```

```
   0.00 0.00 clock CLK (rise edge)
   0.00 0.00 clock network delay (ideal)
   0.10 0.10 clock uncertainty
   0.00 0.10 clock reconvergence pessimism
        0.10 ^ out_reg/CK (DFF_X1)
   0.00 0.10 library hold time
        0.10 data required time
-----------------------------------------------------------
        0.10 data required time
       -0.10 data arrival time
-----------------------------------------------------------
        0.00 slack (MET)


Startpoint: out_reg (rising edge-triggered flip-flop clocked by CLK)
Endpoint: out (output port clocked by CLK)
Path Group: CLK
Path Type: max

  Delay Time Description
-----------------------------------------------------------
   0.00 0.00 clock CLK (rise edge)
   0.00 0.00 clock network delay (ideal)
   0.00 0.00 ^ out_reg/CK (DFF_X1)
   0.09 0.09 ^ out_reg/Q (DFF_X1)
   0.00 0.09 v N3/ZN (INV_X1)
   0.00 0.09 v out (out)
        0.09 data arrival time

   5.00 5.00 clock CLK (rise edge)
   0.00 5.00 clock network delay (ideal)
  -0.10 4.90 clock uncertainty
   0.00 4.90 clock reconvergence pessimism
  -2.00 2.90 output external delay
        2.90 data required time
-----------------------------------------------------------
        2.90 data required time
       -0.09 data arrival time
-----------------------------------------------------------
        2.81 slack (MET)
```

When the clock frequency is doubled, the clock period is halved, giving the data less time to travel from one flip-flop to the next before the next active clock edge. As a result, the **setup slack decreases**, since the required arrival time for data is reduced. This makes setup timing more critical and can lead to setup violations if the design was already close to the timing limit. In contrast, the **hold slack remains almost unchanged**, because hold checks occur within the same clock edge and do not depend on the overall clock period. Therefore, doubling the clock frequency primarily affects setup timing while leaving hold timing largely unaffected. Q6)

```
#input delay was changed from 2 to 5
create_clock -name CLK -period 10 [get_ports Clock]
set_input_delay 5 -clock CLK [get_ports {a b}]
set_output_delay 2 -clock CLK [get_ports out]
set_clock_uncertainty 0.1 [get_clocks CLK]
```

```
Startpoint: q1_reg (rising edge-triggered flip-flop clocked by CLK)
Endpoint: out_reg (rising edge-triggered flip-flop clocked by CLK)
Path Group: CLK
Path Type: min

  Delay Time Description
---------------------------------------------------------
   0.00 0.00 clock CLK (rise edge)
   0.00 0.00 clock network delay (ideal)
   0.00 0.00 ^ q1_reg/CK (DFF_X1)
   0.08 0.08 v q1_reg/Q (DFF_X1)
   0.03 0.10 v A1/ZN (AND2_X1)
   0.00 0.10 v out_reg/D (DFF_X1)
             0.10 data arrival time

   0.00 0.00 clock CLK (rise edge)
   0.00 0.00 clock network delay (ideal)
   0.10 0.10 clock uncertainty
   0.00 0.10 clock reconvergence pessimism
             0.10 ^ out_reg/CK (DFF_X1)
   0.00 0.10 library hold time
             0.10 data required time
---------------------------------------------------------
             0.10 data required time
            -0.10 data arrival time
---------------------------------------------------------
             0.00 slack (MET)
```

```
Startpoint: a (input port clocked by CLK)
Endpoint: q1_reg (rising edge-triggered flip-flop clocked by CLK)
Path Group: CLK
Path Type: max

  Delay Time Description
---------------------------------------------------------
   0.00 0.00 clock CLK (rise edge)
   0.00 0.00 clock network delay (ideal)
   5.00 5.00 ^ input external delay
   0.00 5.00 ^ a (in)
   0.00 5.00 v N1/ZN (INV_X1)
   0.00 5.00 v q1_reg/D (DFF_X1)
             5.00 data arrival time

  10.00 10.00 clock CLK (rise edge)
   0.00 10.00 clock network delay (ideal)
  -0.10 9.90 clock uncertainty
   0.00 9.90 clock reconvergence pessimism
             9.90 ^ q1_reg/CK (DFF_X1)
  -0.04 9.86 library setup time
             9.86 data required time
---------------------------------------------------------
             9.86 data required time
            -5.00 data arrival time
---------------------------------------------------------
             4.86 slack (MET)
```

Q7)

```
#output delay delay was changed from 2 to 5
create_clock -name CLK -period 10 [get_ports Clock]
set_input_delay 2 -clock CLK [get_ports {a b}]
set_output_delay 5-clock CLK [get_ports out]
set_clock_uncertainty 0.1 [get_clocks CLK]

Startpoint: q1_reg (rising edge-triggered flip-flop clocked by CLK)
Endpoint: out_reg (rising edge-triggered flip-flop clocked by CLK)
Path Group: CLK
Path Type: min
```

```
  Delay Time Description
---------------------------------------------------------
   0.00 0.00 clock CLK (rise edge)
   0.00 0.00 clock network delay (ideal)
   0.00 0.00 ^ q1_reg/CK (DFF_X1)
   0.08 0.08 v q1_reg/Q (DFF_X1)
   0.03 0.10 v A1/ZN (AND2_X1)
   0.00 0.10 v out_reg/D (DFF_X1)
         0.10 data arrival time

   0.00 0.00 clock CLK (rise edge)
   0.00 0.00 clock network delay (ideal)
   0.10 0.10 clock uncertainty
   0.00 0.10 clock reconvergence pessimism
         0.10 ^ out_reg/CK (DFF_X1)
   0.00 0.10 library hold time
         0.10 data required time
---------------------------------------------------------
         0.10 data required time
        -0.10 data arrival time
---------------------------------------------------------
         0.00 slack (MET)


Startpoint: out_reg (rising edge-triggered flip-flop clocked by CLK)
Endpoint: out (output port clocked by CLK)
Path Group: CLK
Path Type: max

  Delay Time Description
---------------------------------------------------------
   0.00 0.00 clock CLK (rise edge)
   0.00 0.00 clock network delay (ideal)
   0.00 0.00 ^ out_reg/CK (DFF_X1)
   0.09 0.09 ^ out_reg/Q (DFF_X1)
   0.00 0.09 v N3/ZN (INV_X1)
   0.00 0.09 v out (out)
         0.09 data arrival time

  10.00 10.00 clock CLK (rise edge)
   0.00 10.00 clock network delay (ideal)
```

-0.10 9.90 clock uncertainty
0.00 9.90 clock reconvergence pessimism
-5.00 4.90 output external delay
4.90 data required time
---
4.90 data required time
-0.09 data arrival time
---
4.81 slack (MET)

Q8)

```
create_clock -name CLK -period 10 [get_ports Clock]
set_input_delay 2 -clock CLK [get_ports {a b}]
set_output_delay 2 -clock CLK [get_ports out]
set_clock_uncertainty 0.1 [get_clocks CLK]
set_multicycle_path 4 -setup -from [get_cells q1_reg] -to [get_cells out_reg]
```

Startpoint: q1_reg (rising edge-triggered flip-flop clocked by CLK)
Endpoint: out_reg (rising edge-triggered flip-flop clocked by CLK)
Path Group: CLK
Path Type: min

Delay Time Description
---
0.00 0.00 clock CLK (rise edge)
0.00 0.00 clock network delay (ideal)
0.00 0.00 ^ q1_reg/CK (DFF_X1)
0.08 0.08 v q1_reg/Q (DFF_X1)
0.03 0.10 v A1/ZN (AND2_X1)
0.00 0.10 v out_reg/D (DFF_X1)
0.10 data arrival time

30.00 30.00 clock CLK (rise edge)
0.00 30.00 clock network delay (ideal)
0.10 30.10 clock uncertainty
0.00 30.10 clock reconvergence pessimism
30.10 ^ out_reg/CK (DFF_X1)
0.00 30.10 library hold time
30.10 data required time
---
30.10 data required time

```
          -0.10 data arrival time
-----------------------------------------------------------
         -30.00 slack (VIOLATED)


Startpoint: out_reg (rising edge-triggered flip-flop clocked by CLK)
Endpoint: out (output port clocked by CLK)
Path Group: CLK
Path Type: max

  Delay Time Description
---------------------------------------------------------
   0.00 0.00 clock CLK (rise edge)
   0.00 0.00 clock network delay (ideal)
   0.00 0.00 ^ out_reg/CK (DFF_X1)
   0.09 0.09 ^ out_reg/Q (DFF_X1)
   0.00 0.09 v N3/ZN (INV_X1)
   0.00 0.09 v out (out)
             0.09 data arrival time

  10.00 10.00 clock CLK (rise edge)
   0.00 10.00 clock network delay (ideal)
  -0.10 9.90 clock uncertainty
   0.00 9.90 clock reconvergence pessimism
  -2.00 7.90 output external delay
             7.90 data required time
---------------------------------------------------------
             7.90 data required time
            -0.09 data arrival time
---------------------------------------------------------
             7.81 slack (MET)


create_clock -name CLK -period 10 [get_ports Clock]
set_input_delay 2 -clock CLK [get_ports {a b}]
set_output_delay 2 -clock CLK [get_ports out]
set_clock_uncertainty 0.1 [get_clocks CLK]

set_multicycle_path 4 -setup -from [get_cells q1_reg] -to [get_cells out_reg]
set_multicycle_path 3 -hold -from [get_cells q1_reg] -to [get_cells out_reg]

Startpoint: q1_reg (rising edge-triggered flip-flop clocked by CLK)
```

Endpoint: out_reg (rising edge-triggered flip-flop clocked by CLK)
Path Group: CLK
Path Type: min

```
  Delay Time Description
---------------------------------------------------------
   0.00 0.00 clock CLK (rise edge)
   0.00 0.00 clock network delay (ideal)
   0.00 0.00 ^ q1_reg/CK (DFF_X1)
   0.08 0.08 v q1_reg/Q (DFF_X1)
   0.03 0.10 v A1/ZN (AND2_X1)
   0.00 0.10 v out_reg/D (DFF_X1)
             0.10 data arrival time

   0.00 0.00 clock CLK (rise edge)
   0.00 0.00 clock network delay (ideal)
   0.10 0.10 clock uncertainty
   0.00 0.10 clock reconvergence pessimism
             0.10 ^ out_reg/CK (DFF_X1)
   0.00 0.10 library hold time
             0.10 data required time
---------------------------------------------------------
             0.10 data required time
            -0.10 data arrival time
---------------------------------------------------------
             0.00 slack (MET)
```

Startpoint: out_reg (rising edge-triggered flip-flop clocked by CLK)
Endpoint: out (output port clocked by CLK)
Path Group: CLK
Path Type: max

```
  Delay Time Description
---------------------------------------------------------
   0.00 0.00 clock CLK (rise edge)
   0.00 0.00 clock network delay (ideal)
   0.00 0.00 ^ out_reg/CK (DFF_X1)
   0.09 0.09 ^ out_reg/Q (DFF_X1)
   0.00 0.09 v N3/ZN (INV_X1)
   0.00 0.09 v out (out)
             0.09 data arrival time
```

```
  10.00 10.00 clock CLK (rise edge)
   0.00 10.00 clock network delay (ideal)
  -0.10  9.90 clock uncertainty
   0.00  9.90 clock reconvergence pessimism
  -2.00  7.90 output external delay
         7.90 data required time
-----------------------------------------------------------
         7.90 data required time
        -0.09 data arrival time
-----------------------------------------------------------
         7.81 slack (MET)
```