8086 MICROPROCESSOR



Author: Bharat Acharya Sem IV – Electronics Mumbai 2018

SHIFT INSTRUCTIONS

 SAL/SHL destination, count LEFT-Shifts the bits of destination. MSB shifted into the CARRY. LSB gets a 0.

Bits are shifted 'count' number of times.

If count = 1, it is directly specified in the instruction.

If count > 1, it has to be given using CL Register.

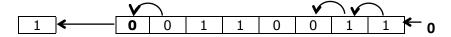
Destination: Register, Memory Location. #Please refer Bharat Sir's Lecture Notes for this ...

Eg: **SAL BL, 1** ; Left-Shift BL bits, once.

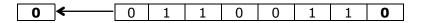
Assume:

Before Operation: BL = 0011 0011 and CF = 1

Carry Destination



After Operation: BL = 0110 0110 and CF = 0



More examples:

MOV CL, 05H ; Load number of shifts in CL register.
SAL BL, CL ; Left-Shift BL bits CL (5) number of times.

2) SHR destination, count

RIGHT-Shifts the bits of destination.

MSB gets a **0** (∴ Sign is lost). **LSB** shifted **into** the **CARRY**.

Bits are shifted 'count' number of times.

If count is 1, it is directly specified in the instruction.

If count > 1, it has to be given using CL register.

Eq: **SHR BL, 1** ; Right-Shift BL bits, once.



BHARAT ACHARYA EDUCATION

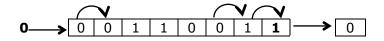
Videos | Books | Classroom Coaching E: bharatsir@hotmail.com M: 9820408217

Assume:

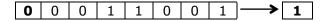
Before Operation: BL = 0011 0011 and CF = 0

Destination

Carry



After Operation: BL = 00011 1001 and CF = 1



3) SAR destination, count

RIGHT-Shifts the bits of destination.

MSB placed **in MSB itself** (∴ Sign is preserved).

LSB shifted into the CARRY.

Bits are shifted 'count' number of times.

If count is 1, it is directly specified in the instruction.

If count > 1 it has to be given using CL register. \odot For doubts contact Bharat Sir on 98204 08217

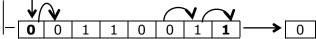
Destination: Register, Memory Location

Eg: **SAR BL, 1** ; Right-Shift BL bits, once.

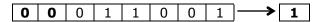
Assume:

Before Operation: BL = 0011 0011 and CF = 0





After Operation: BL = 0001 1001 and CF = 1





Author: Bharat Acharya Sem IV – Electronics Mumbai 2018

ROTATE INSTRUCTIONS

1) ROL destination, count

LEFT-Shifts the bits of destination.

MSB shifted into the CARRY.

MSB also goes to LSB.

Bits are shifted 'count' number of times.

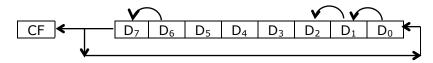
If count = 1, it is directly specified in the instruction.

If count > 1, it has to be loaded in the CL register, and CL gives the count in the instruction.

Destination: Register, Memory Location

Eg: **ROL BL, 1** ; Left-Shift BL bits once.

Carry Destination



More examples:

MOV CL, 05H ROL BL, CL ; Load number of shifts in CL register.

; Left-Shift BL bits CL (5) number of times.

2) ROR destination, count

RIGHT-Shifts the bits of destination.

LSB shifted into the CARRY.

LSB also goes to MSB.

Bits are shifted 'count' number of times.

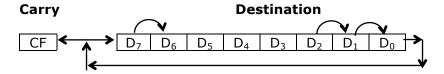
If count = 1, it is directly specified in the instruction.

If count > 1, it has to be loaded in the CL register, and CL gives the count in the instruction.

Eg:

ROR BL, 1

; Right-Shift BL bits once.





BHARAT ACHARYA EDUCATION

Videos | Books | Classroom Coaching E: bharatsir@hotmail.com M: 9820408217

3) RCL destination, count

LEFT-Shifts the bits of destination.

MSB shifted into the Carry Flag (CF).

CF goes to LSB.

Bits are shifted 'count' number of times.

If count = 1, it is directly specified in the instruction.

If count > 1, it has to be loaded in the CL register, and CL is specified as the count in the instruction.

Destination: Register, Memory Location

Eg: **RCL BL, 1** ; Left-Shift BL bits once.

4) RCR destination, count

RIGHT-Shifts the bits of destination.

LSB shifted into the CF.

CF goes to MSB.

Bits are shifted 'count' number of times.

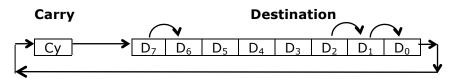
If count = 1, it is directly specified in the instruction.

If count > 1, it has to be loaded in the CL register, and CL is specified as the count in the instruction.

Destination: Register, Memory Location

Eq:

RCR BL, 1 ; Right-Shift BL bits once.



More examples:

MOV CL, 05H

; Load number of shifts in CL register.

RCR BL, CL

; Right-Shift BL bits CL (5) number of times.