`ifndef CONFIG\_SV

`define CONFIG\_SV

`define RISCV

// always define ASIC when we do a synthesis run

`ifndef PULP\_FPGA\_EMUL

`ifdef SYNTHESIS

`define ASIC

`endif

`endif

// data and instruction RAM address and word width

`define ROM\_ADDR\_WIDTH 12

`define ROM\_START\_ADDR 32'h8000

// Simulation only stuff

`ifndef SYNTHESIS

//`define DATA\_STALL\_RANDOM

//`define INSTR\_STALL\_RANDOM

`endif

`endif