module axi\_spi\_slave\_wrap

#(

parameter AXI\_ADDRESS\_WIDTH = 32,

parameter AXI\_DATA\_WIDTH = 64,

parameter AXI\_ID\_WIDTH = 16,

parameter AXI\_USER\_WIDTH = 10

)

(

input logic clk\_i,

input logic rst\_ni,

input logic test\_mode,

AXI\_BUS.Master axi\_master,

input logic spi\_clk,

input logic spi\_cs,

output logic [1:0] spi\_mode,

output logic spi\_sdo0,

output logic spi\_sdo1,

output logic spi\_sdo2,

output logic spi\_sdo3,

input logic spi\_sdi0,

input logic spi\_sdi1,

input logic spi\_sdi2,

input logic spi\_sdi3

);

axi\_spi\_slave

#(

.AXI\_ADDR\_WIDTH ( AXI\_ADDRESS\_WIDTH ),

.AXI\_DATA\_WIDTH ( AXI\_DATA\_WIDTH ),

.AXI\_ID\_WIDTH ( AXI\_ID\_WIDTH ),

.AXI\_USER\_WIDTH ( AXI\_USER\_WIDTH )

)

axi\_spi\_slave\_i

(

.axi\_aclk ( clk\_i ),

.axi\_aresetn ( rst\_ni ),

.axi\_master\_aw\_valid ( axi\_master.aw\_valid ),

.axi\_master\_aw\_id ( axi\_master.aw\_id ),

.axi\_master\_aw\_prot ( axi\_master.aw\_prot ),

.axi\_master\_aw\_region ( axi\_master.aw\_region ),

.axi\_master\_aw\_qos ( axi\_master.aw\_qos ),

.axi\_master\_aw\_cache ( axi\_master.aw\_cache ),

.axi\_master\_aw\_lock ( axi\_master.aw\_lock ),

.axi\_master\_aw\_burst ( axi\_master.aw\_burst ),

.axi\_master\_aw\_size ( axi\_master.aw\_size ),

.axi\_master\_aw\_len ( axi\_master.aw\_len ),

.axi\_master\_aw\_addr ( axi\_master.aw\_addr ),

.axi\_master\_aw\_user ( axi\_master.aw\_user ),

.axi\_master\_aw\_ready ( axi\_master.aw\_ready ),

.axi\_master\_w\_valid ( axi\_master.w\_valid ),

.axi\_master\_w\_data ( axi\_master.w\_data ),

.axi\_master\_w\_strb ( axi\_master.w\_strb ),

.axi\_master\_w\_last ( axi\_master.w\_last ),

.axi\_master\_w\_user ( axi\_master.w\_user ),

.axi\_master\_w\_ready ( axi\_master.w\_ready ),

.axi\_master\_b\_valid ( axi\_master.b\_valid ),

.axi\_master\_b\_id ( axi\_master.b\_id ),

.axi\_master\_b\_resp ( axi\_master.b\_resp ),

.axi\_master\_b\_user ( axi\_master.b\_user ),

.axi\_master\_b\_ready ( axi\_master.b\_ready ),

.axi\_master\_ar\_valid ( axi\_master.ar\_valid ),

.axi\_master\_ar\_id ( axi\_master.ar\_id ),

.axi\_master\_ar\_prot ( axi\_master.ar\_prot ),

.axi\_master\_ar\_region ( axi\_master.ar\_region ),

.axi\_master\_ar\_qos ( axi\_master.ar\_qos ),

.axi\_master\_ar\_cache ( axi\_master.ar\_cache ),

.axi\_master\_ar\_lock ( axi\_master.ar\_lock ),

.axi\_master\_ar\_burst ( axi\_master.ar\_burst ),

.axi\_master\_ar\_size ( axi\_master.ar\_size ),

.axi\_master\_ar\_len ( axi\_master.ar\_len ),

.axi\_master\_ar\_addr ( axi\_master.ar\_addr ),

.axi\_master\_ar\_user ( axi\_master.ar\_user ),

.axi\_master\_ar\_ready ( axi\_master.ar\_ready ),

.axi\_master\_r\_valid ( axi\_master.r\_valid ),

.axi\_master\_r\_id ( axi\_master.r\_id ),

.axi\_master\_r\_data ( axi\_master.r\_data ),

.axi\_master\_r\_resp ( axi\_master.r\_resp ),

.axi\_master\_r\_last ( axi\_master.r\_last ),

.axi\_master\_r\_user ( axi\_master.r\_user ),

.axi\_master\_r\_ready ( axi\_master.r\_ready ),

.test\_mode ( test\_mode ),

.spi\_sclk ( spi\_clk ),

.spi\_cs ( spi\_cs ),

.spi\_mode ( spi\_mode ),

.spi\_sdo0 ( spi\_sdo0 ),

.spi\_sdo1 ( spi\_sdo1 ),

.spi\_sdo2 ( spi\_sdo2 ),

.spi\_sdo3 ( spi\_sdo3 ),

.spi\_sdi0 ( spi\_sdi0 ),

.spi\_sdi1 ( spi\_sdi1 ),

.spi\_sdi2 ( spi\_sdi2 ),

.spi\_sdi3 ( spi\_sdi3 )

);

endmodule